FTP30N20R

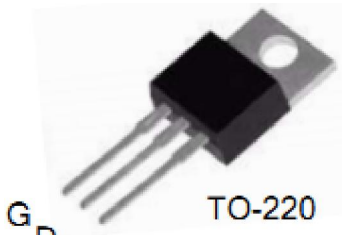
N-Channel MOSFET

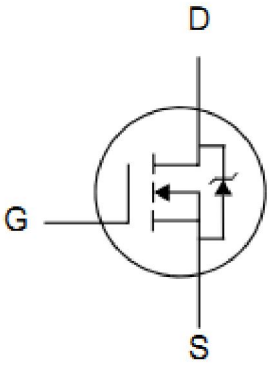
Lead Free Package and Finish

Applications:
- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$(Typ.)	I_D
200V	70mΩ	30A

Features:
- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves





Ordering Information

PART NUMBER	PACKAGE	BRAND
FTP30N20R	TO-220	***IPS***

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	FTP30N20R	Units
V_{DSS}	Drain-to-Source Voltage	200	V
I_D	Continuous Drain Current	30	A
	Continuous Drain Current T_C =100℃	18.9	A
I_{DM}	Pulsed Drain Current (NOTE *1)	120	A
P_D	Power Dissipation	200	W
	Derating Factor above 25℃	1.2	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	1050	mJ
dv/dt	Peak Diode Recovery dv/dt(NOTE *3)	5	V/ns
T_L	Maximum Temperature for Soldering	300	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150，-55 to150	

Thermal Resistance

Symbol	Parameter	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	0.62	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	--	--	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=200V, V_{GS}=0V T_J=25℃
		--	--	100		V_{DS}=160V, V_{GS}=0V T_J=125℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+30V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -30V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance	--	70	80	mΩ	V_{GS}=10V, I_D=15A
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	V_{DS}=V_{GS},I_D=250μA
g_{fs}	Forward Transconductance	--	14.5	--	S	V_{DS}=15V, I_D=15A
Pulse width ≤300μs; duty cycle≤ 2%						

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1945	--	pF	V_{GS}= 0V,V_{DS} = 25V f =1.0MHz
C_{oss}	Output Capacitance	--	300	--		
C_{rss}	Reverse Transfer Capacitance	--	24	--		
Q_g	Total Gate Charge	--	38	--	nC	I_D=30A,V_{DD}=100V V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	--	12	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	13	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	13	--	ns	V_{DD}=100V, I_D=30A, V_G=10V R_G=3.9Ω
t_{rise}	Rise Time	--	24	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	32	--		
t_{fall}	Fall Time	--	6	--		

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	30	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	120	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_{SD}=30A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	230	--	ns	I_F= I_S di/dt=100A/us
Q_{rr}	Reverse Recovery Charge	--	1037	--	nC	
Pulse width ≤300μs; duty cycle ≤ 2%						

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. L=10mH, I_D=14.5A, Start T_J=25℃

*3. I_{SD} =30A,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve：

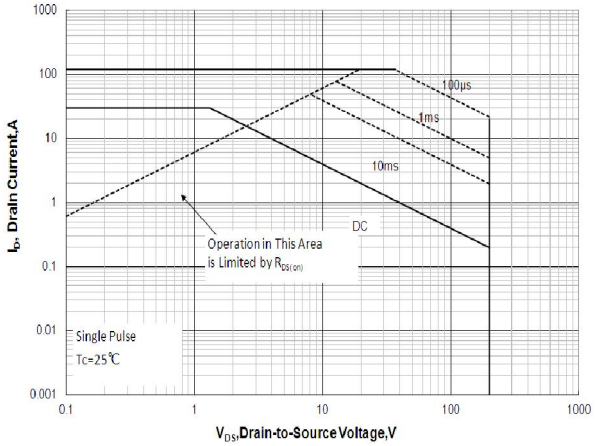


Figure 1 Maximum Forward Bias Safe Operating Area

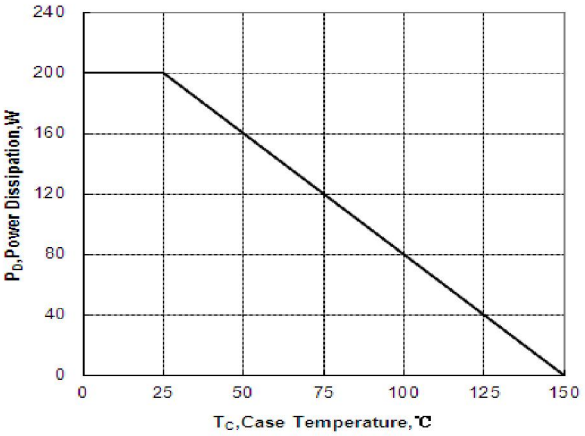


Figure 2 Maximum Power dissipation vs Case Temperature

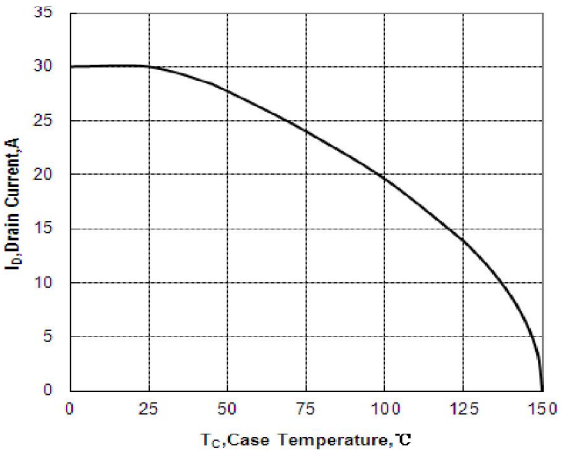


Figure 3 Maximum Continuous Drain Current vs Case Temperature

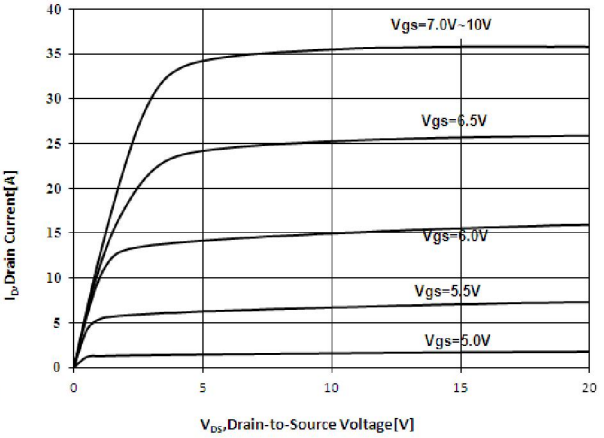


Figure 4 Typical Output Characteristics

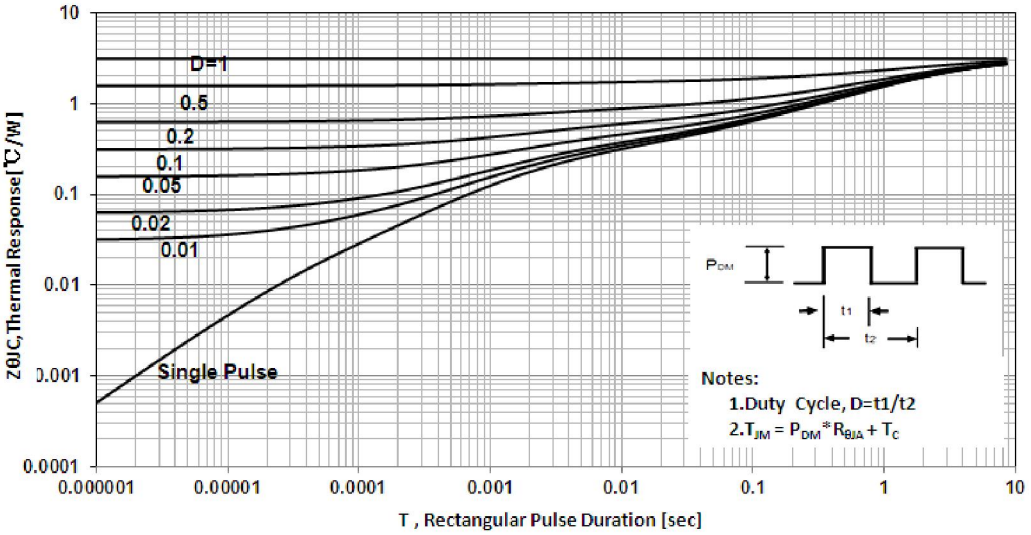


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

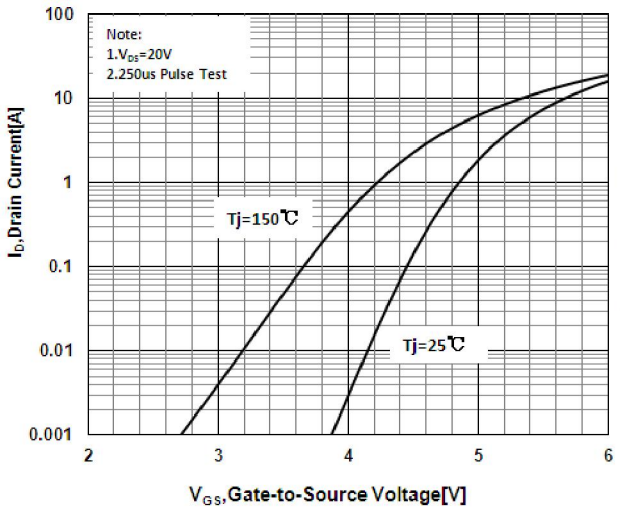


Figure 6 Typical Transfer Characteristics

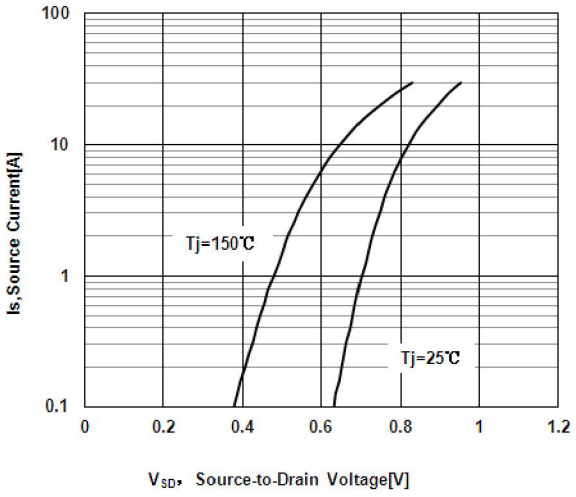


Figure 7 Typical Body Diode Transfer Characteristics

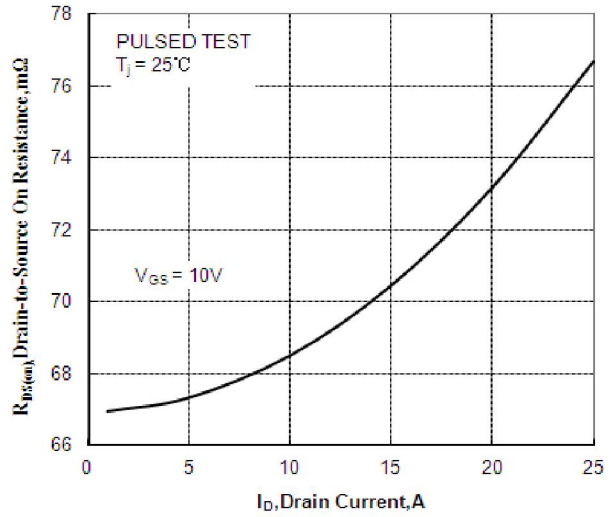


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

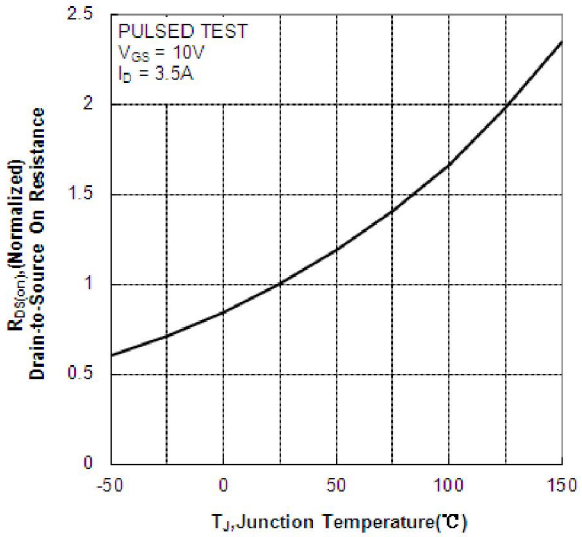


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

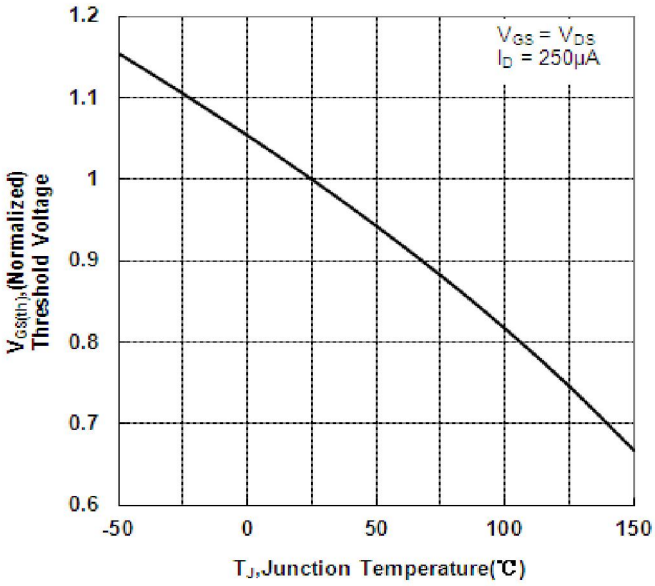


Figure 10 Typical Theshold Voltage vs Junction Temperature

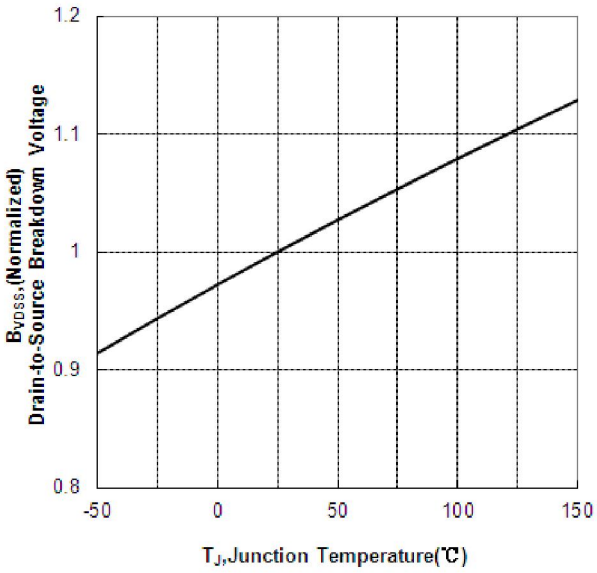


Figure 11 Typical Breakdown Voltage vs Junction Temperature

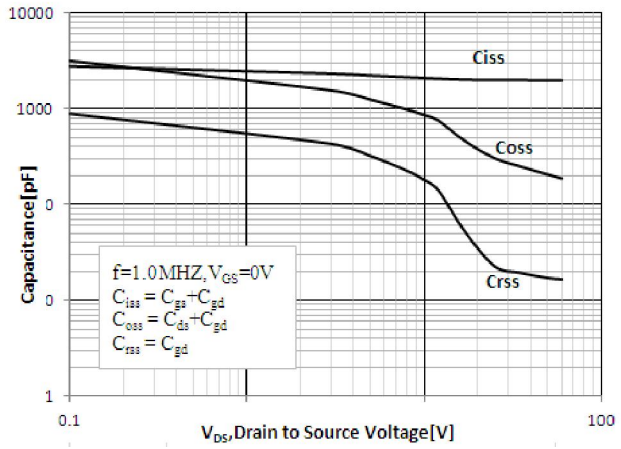


Figure 12 Typical Capacitance vs Drain to Source Voltage

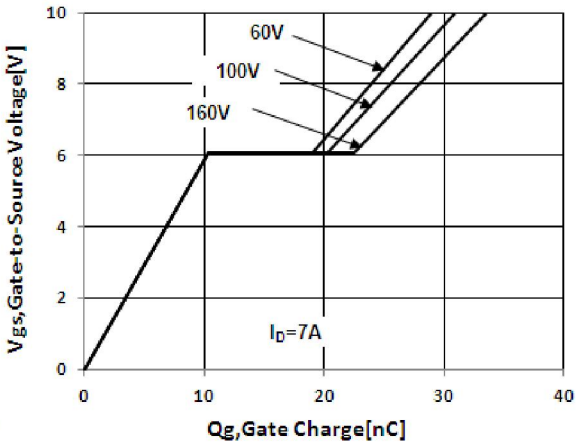


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuits and Waveforms

Figure 14. Gate Charge Test Circuit

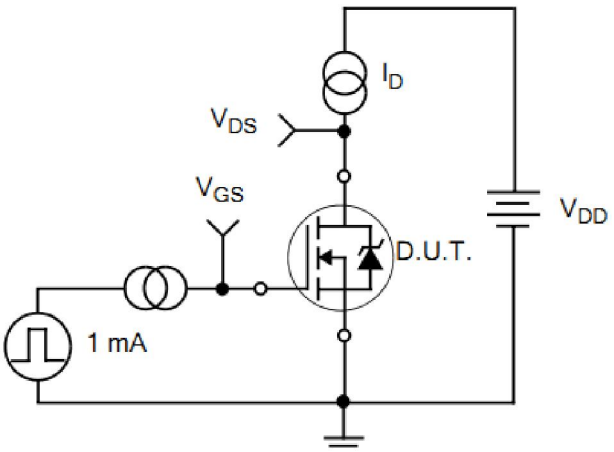


Figure 15. Gate Charge Waveforms

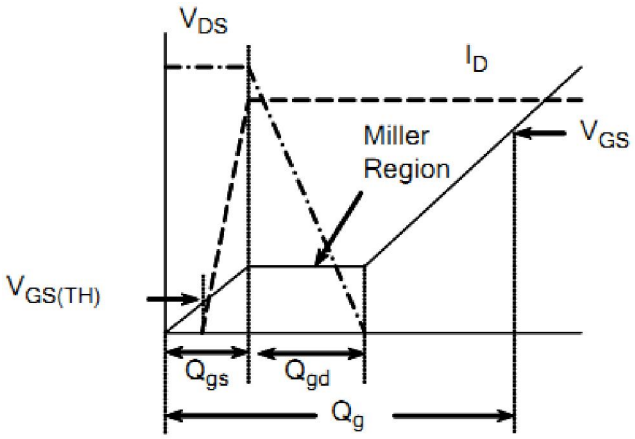


Figure 16. Resistive Switching Test Circuit

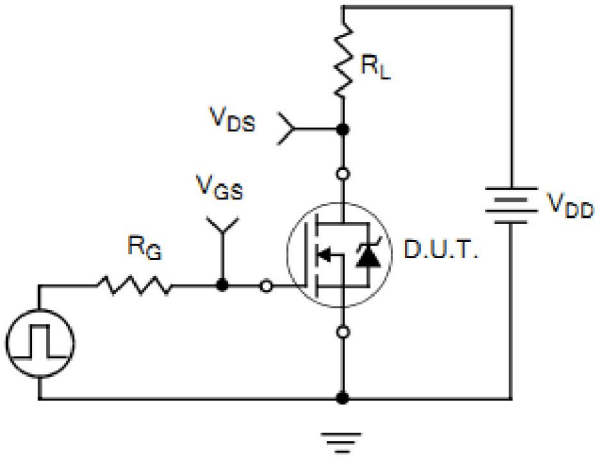


Figure 17. Resistive Switching Waveforms

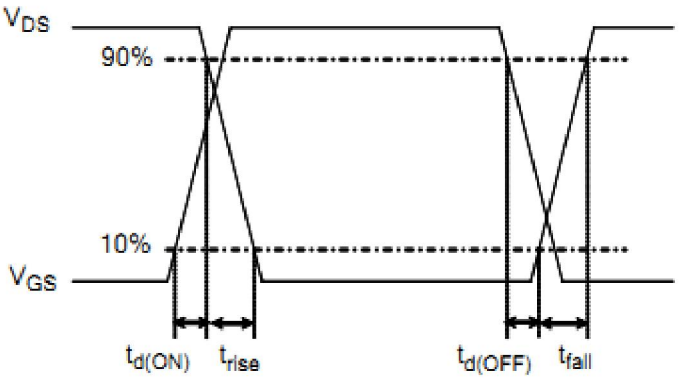


Figure 18. Diode Reverse Recovery Test Circuit

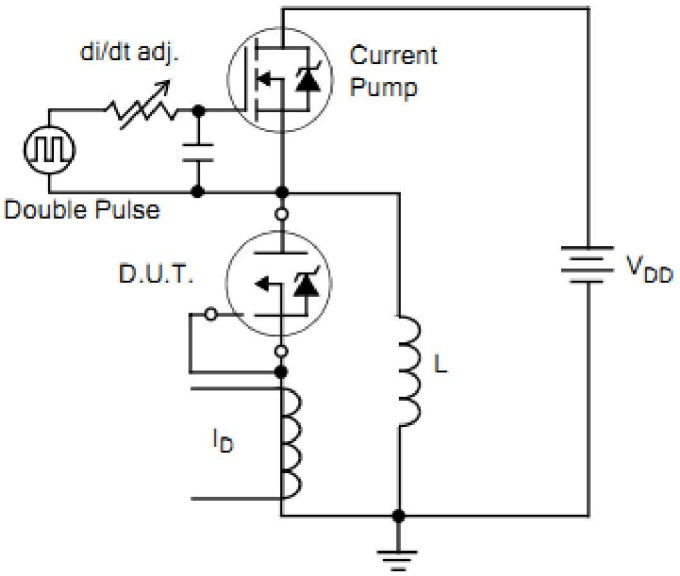


Figure 19. Diode Reverse Recovery Waveform

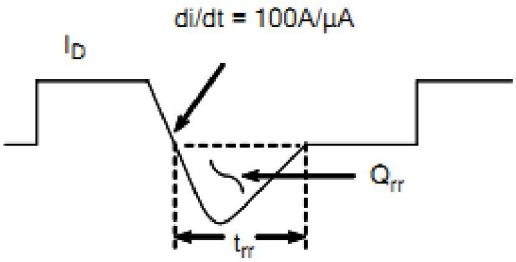


Figure20.Unclamped Inductive Switching Test Circuit

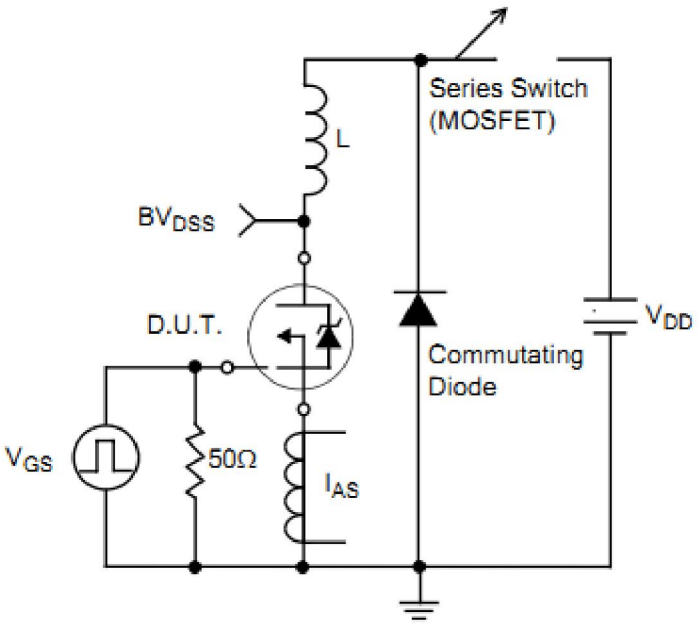
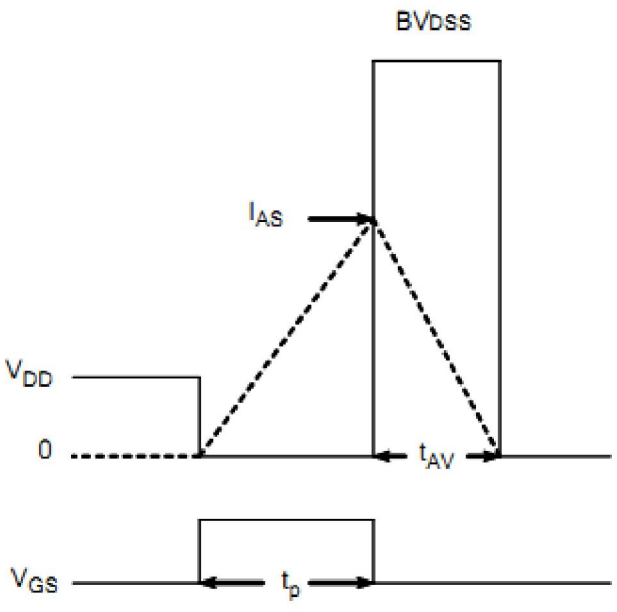


Figure21.Unclamped Inductive Switching Waveform



$$E_{AS} \quad \frac{I_{AS}^{2} L}{2}$$

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