FTW50N20R

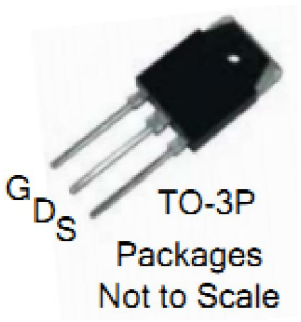
N-Channel MOSFET

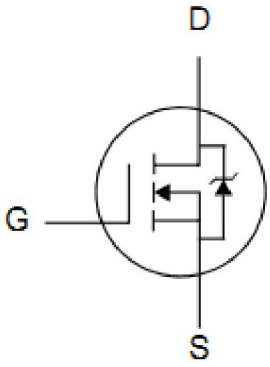
Lead Free Package and Finish

Applications:
- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$(Typ.)	I_D
200V	42mΩ	50A

Features:
- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves





Ordering Information

PART NUMBER	PACKAGE	BRAND
FTW50N20R	TO-3P	***IPS***

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	FTW50N20R	Units
V_{DSS}	Drain-to-Source Voltage	200	V
I_D	Continuous Drain Current	50	A
	Continuous Drain Current T_C =100℃	38.5	A
I_{DM}	Pulsed Drain Current (NOTE *1)	200	A
P_D	Power Dissipation	300	W
	Derating Factor above 25℃	2.4	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	1700	mJ
dv/dt	Peak Diode Recovery dv/dt(NOTE *3)	5	V/ns
T_L	Maximum Temperature for Soldering	300	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150，-55 to150	

Thermal Resistance

Symbol	Parameter	Max.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	0.42	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	40		1 cubic foot chamber, free air.

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	--	--	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=200V, V_{GS}=0V T_J=25℃
		--	--	100		V_{DS}=160V, V_{GS}=0V T_J=125℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+30V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -30V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance	--	42	51	mΩ	V_{GS}=10V, I_D=20A
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	V_{DS}=V_{GS},I_D=250μA
g_{fs}	Forward Transconductance	--	65	--	S	V_{DS}=15V, I_D=20A
Pulse width ≤300μs; duty cycle≤ 2%						

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	2819	--	pF	V_{GS}= 0V,V_{DS} = 25V f =1.0MHz
C_{oss}	Output Capacitance	--	394	--		
C_{rss}	Reverse Transfer Capacitance	--	34	--		
Q_g	Total Gate Charge	--	49.4	--	nC	I_D=20A,V_{DD}=160V V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	--	13	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	18	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	35.7	--	ns	V_{DD}=100V, I_D=20A, V_{GS}=10V R_G=10Ω
t_{rise}	Rise Time	--	38.9	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	74.7	--		
t_{fall}	Fall Time	--	21.9	--		

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	50	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	200	A	
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_{SD}=40A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	261	--	ns	I_F= I_S di/dt=100A/us
Q_{rr}	Reverse Recovery Charge	--	2770	--	nC	
Pulse width ≤300μs; duty cycle ≤ 2%						

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. L=10mH, I_D=18.5A, Start T_J=25℃

*3. I_{SD} =20A,di/dt ≤100A/us,V_{DD}≤BV_{DS}, Start T_J=25℃

Characteristics Curve：

Figure 1.Maximum Effective Thermal Impedance，Junction-to-Case

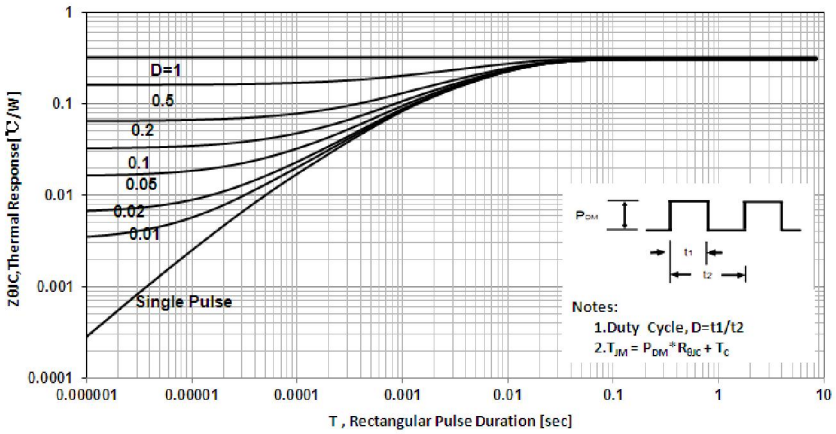


Figure2.Max. Power Dissipation vs Case Temperature

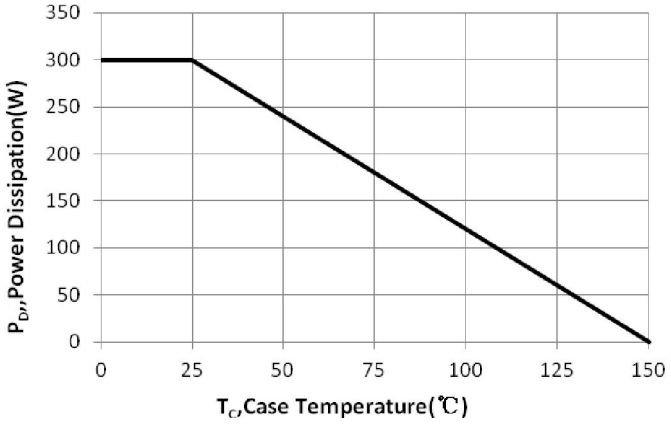


Figure3.Max. Drain Current vs Case Temperature

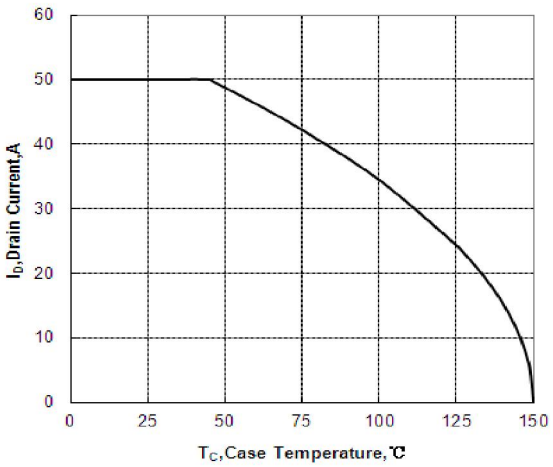


Figure 4.Typical Output Characteristics

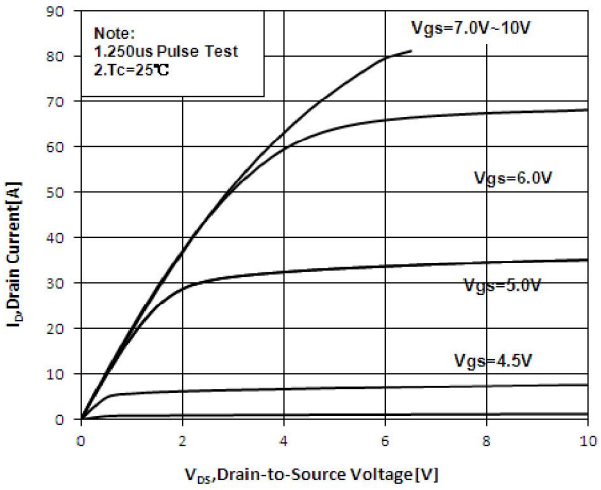


Figure 5. Typical Transfer Characteristics

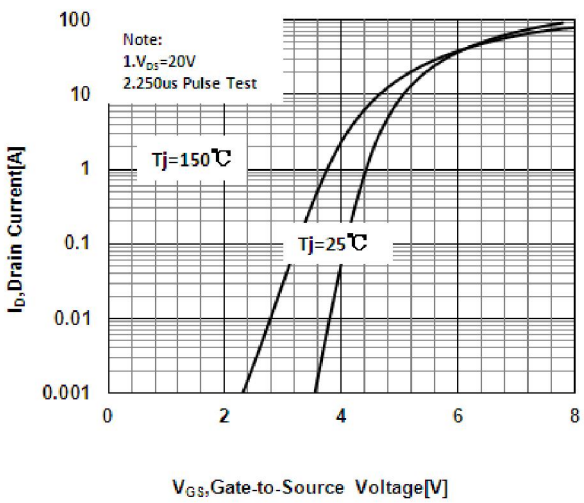


Figure 6. Typical Body Diode Transfer Characteristics

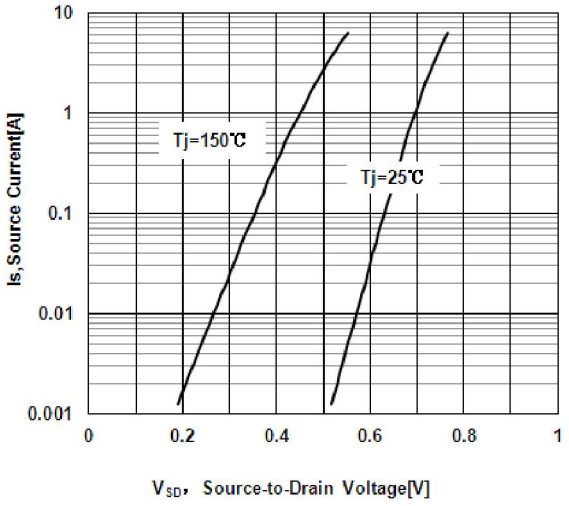


Figure 7. Typical on Resistance VS Drain Current

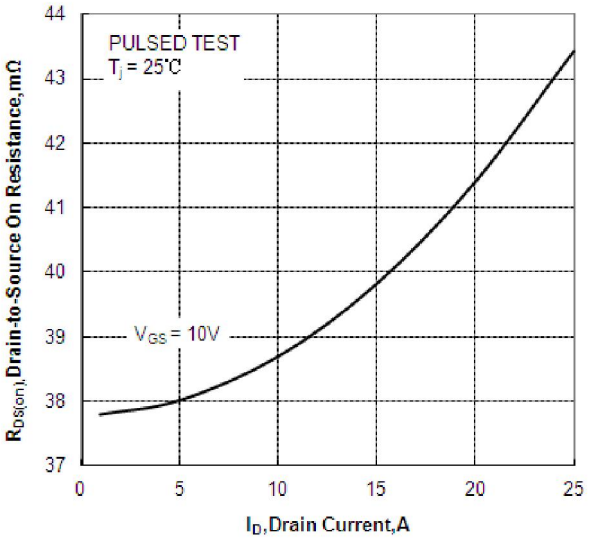


Figure 8. Capacitance VS Drain-to-Source Voltage

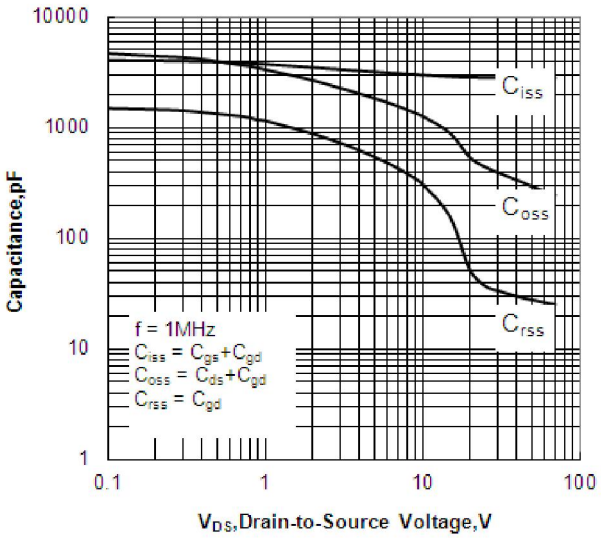


Figure 9. Gate Charge VS Gate-to-Source Voltage

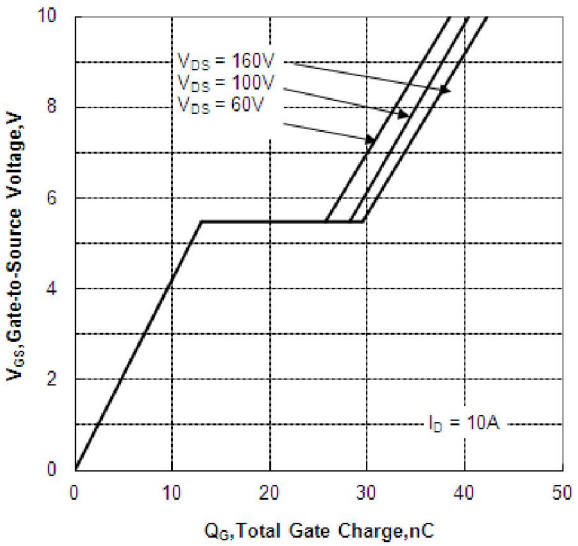


Figure 10. Breakdown Voltage VS Temperature

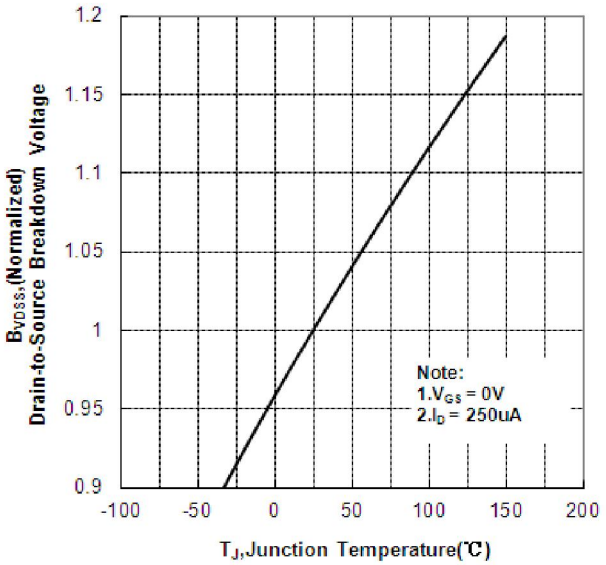


Figure 11. on-Resistance VS Temperature

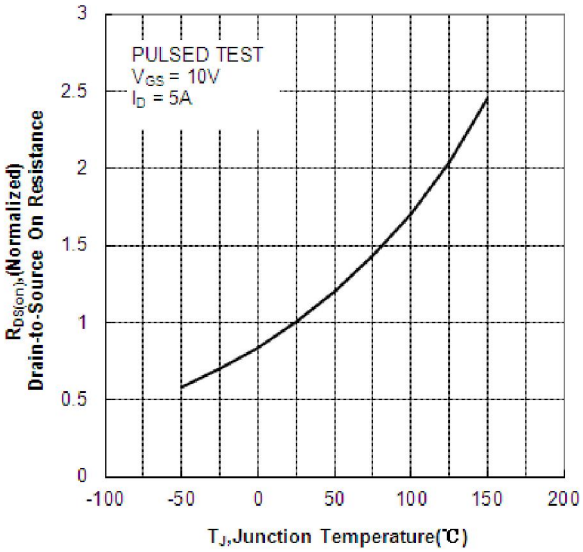


Figure 12 Theshold Voltage vs Junction Temperature

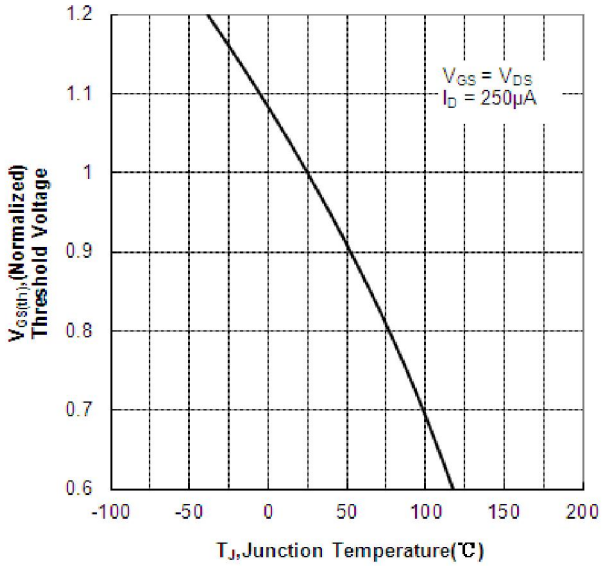
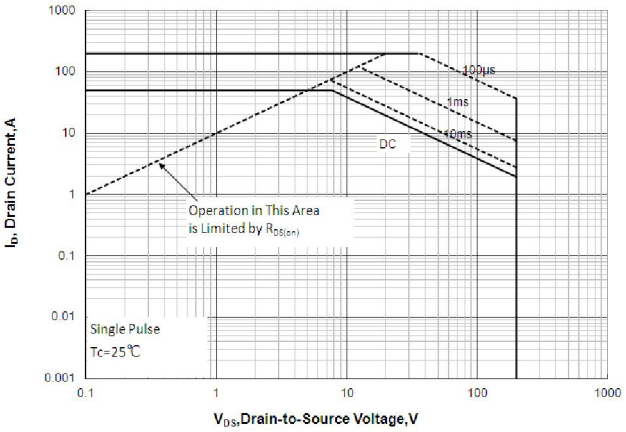


Figure 13. Safe Operating Area



Test Circuits and Waveforms

Figure 14. Gate Charge Test Circuit

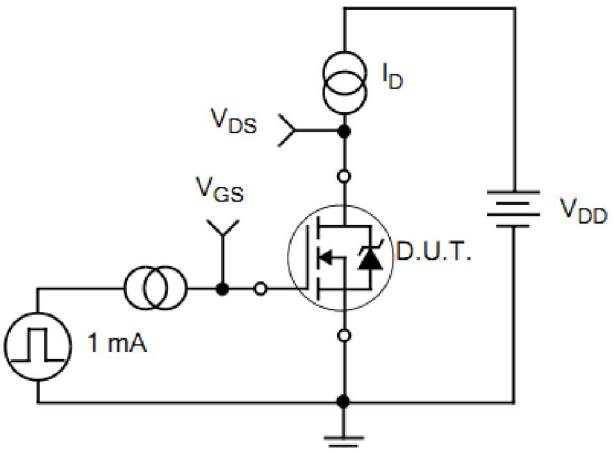


Figure 15. Gate Charge Waveforms

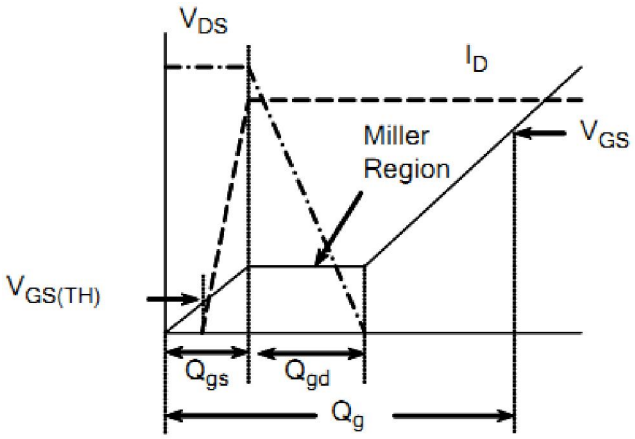


Figure 16. Resistive Switching Test Circuit

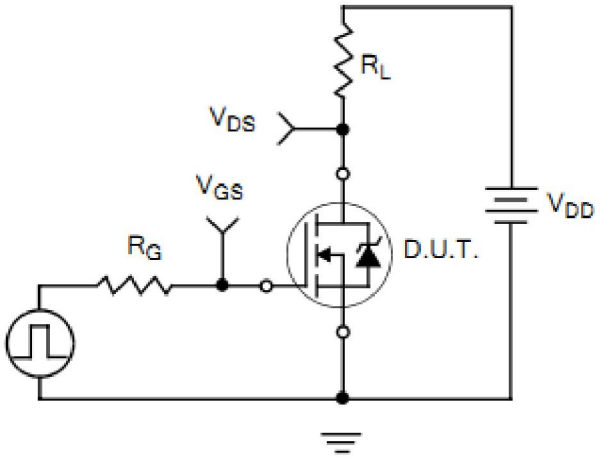


Figure 17. Resistive Switching Waveforms

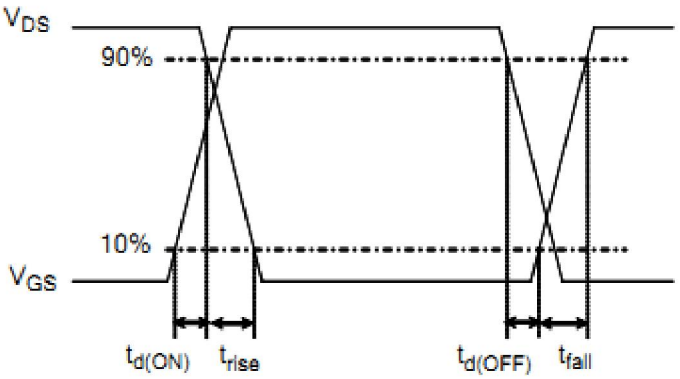


Figure 18. Diode Reverse Recovery Test Circuit

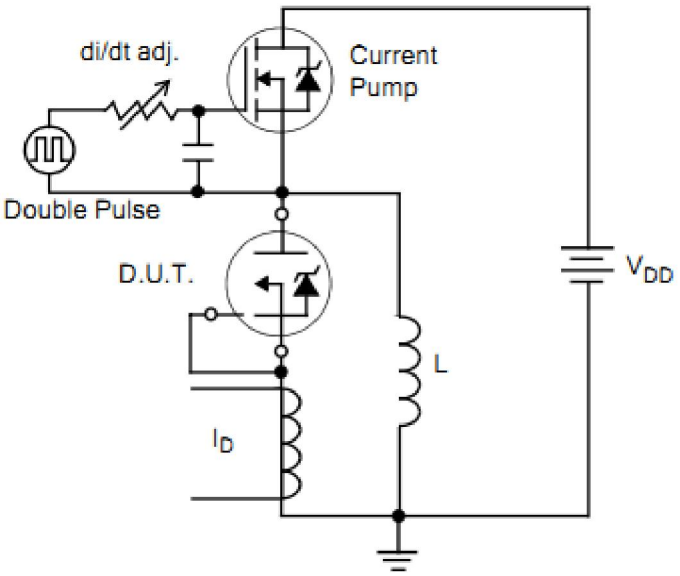


Figure 19. Diode Reverse Recovery Waveform

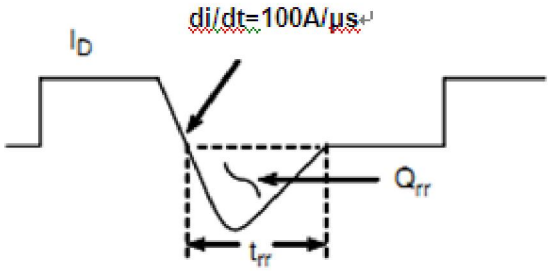


Figure20.Unclamped Inductive Switching Test Circuit

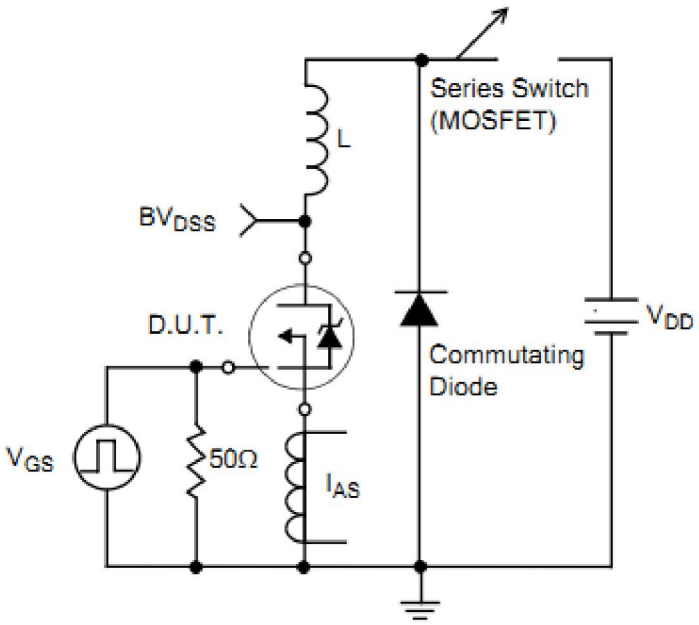
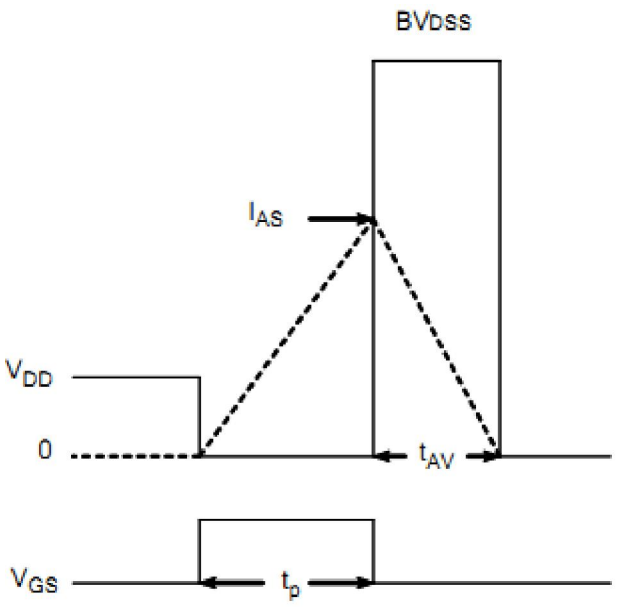


Figure21.Unclamped Inductive Switching Waveform



$$E_{AS} \quad \frac{I_{AS}^{2} L}{2}$$

Disclaimers:

InPower Semiconductor Co., Ltd (IPS) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to IPS's terms and conditions supplied at the time of order acknowledgement.

InPower Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing reliability and quality control are used to the extent IPS deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

InPower Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using IPS's components. To minimize risk, customers must provide adequate design and operating safeguards.

InPower Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in IPS's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of IPS's products with statements different from or beyond the parameters stated by InPower Semiconductor Co., Ltd for that product or service voids all express or implied warrantees for the associated IPS's product or service and is unfair and deceptive business practice. InPower Semiconductor Co., Ltd is not responsible or liable for any such statements.

Life Support Policy:

InPower Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of InPower Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
   a. are intended for surgical implant into the human body,
   b. support or sustain life,
   c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.