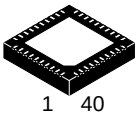
Dual Port USB Type-C & PD Controller for Sink and DRP Applications

FUSB15200



QFN40 5x5, 0.4P
CASE 485CR

The FUSB15200 is a highly integrated dual port USB Type−C and Power Delivery Controller optimized for Sink and DRP applications. The FUSB15200 enables a complete solution through optimized hardware peripherals and complete open−source embedded firmware all in a compact solution. Maximizing total system power budgets is enabled through both hardware and firmware of the FUSB15200.

onsemi offers a complete open−source embedded firmware solution. System designers can easily tailor this firmware to meet the specific needs of their end application through an easy to use API for the embedded firmware. The FUSB15200 also provides a completely USB PD3.1 compliant solution with interoperability with leading mobile and computing devices in the market.

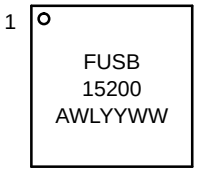
Features

- Small Footprint Dual−port USB PD Controller Supporting the Most Popular Peripherals
  - USB PD 3.1 & USB Type−C 2.1
  - 4x I^2C Host/Device
  - Dual USB BC1.2 Consumer/Provider
  - USB2.0 Isolation Switches
- Fully Programmable and Upgradable Open−Source Firmware Providing API for Customer Specific Device Policy Manager Development
- Integrated LDOs from VBUS Allows Dead−Battery Functionality
- High Voltage Protection on CC and VBUS Pins (28 V DC)
- Up to 20 GPIOs
- 10−bit ADC for High Performance System Measurements
- External Temperature Monitoring via NTC Resistors
- DisplayPort® HPD Signal Conversion
- FastRole Swap Support
- 40−pin QFN Package (5 mm x 5 mm, 0.4 mm Pitch)
- These are Pb−free Devices

Typical Applications

- Sinks and DRP Devices
- Laptops
- Docks

MARKING DIAGRAM



FUSB15200	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week

ORDERING INFORMATION

Device	Package	Shipping†
FUSB15200MNTWG	QFN40	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FEATURES

- *Arm® Cortex®−M0+:* A 32−bit core with flexible clocking up to 24 MHz.
- *Memories:* A total of 132 KB of flash is available to store program code. 6 KB of SRAM program memory.
- *USB Type−C and PD:* Integrated hardware USB PD PHY and Type−C termination/comparators supporting latest USB−IF specification.
- *Integrated VCONN Switch:* Provides the full 1.5 W power to interrogate cable eMarkers and power active cables.
- *BC1.2 Support:* Fully programmable and capable of presenting and detecting SDP, CDP or DCP.
- *High Voltage Protection:* Robust USB−C connector interface with 28 V DC tolerant VBUS, and CC pins.
- *ADC:* Multi−channel 10−bit ADC for accurate monitoring of VBUS, external temperature and voltages.
- *I^2C:* Four serial communication ports capable of acting as a host or device allowing control of external system peripherals by FUSB15200.
- *GPIOs:* Fully programmable I/Os with internal terminations. Configurable as input or output (CMOS or open−drain).
- *Programmable VBUS discharge:* Internal programmable resistors capable of discharging up to 100 μF.
- *Multiple Timers:* Four independent 32−bit timers are available: 2 General Purpose, 1 Watchdog, and 1 Wake−up/General Purpose
- *External NTC:* Integrated current sources are used in conjunction with the ADC to monitor a variety of NTC resistors.
- *Low Power Operation Modes:* Programmable sleep modes allowing device to minimize power usage as needed. Automatic USB−C detection and wake−up functionality from sleep modes.
- *DisplayPort Support:* Configurable I/Os to support hot−plug detect in either display sinks or display source modes.
- *Integrated LDO:* Device can be powered from VBUS input of either port allowing complete USB PD capabilities and contract negotiation under dead battery or no battery conditions.

FUSB15200 INTERNAL BLOCK DIAGRAM

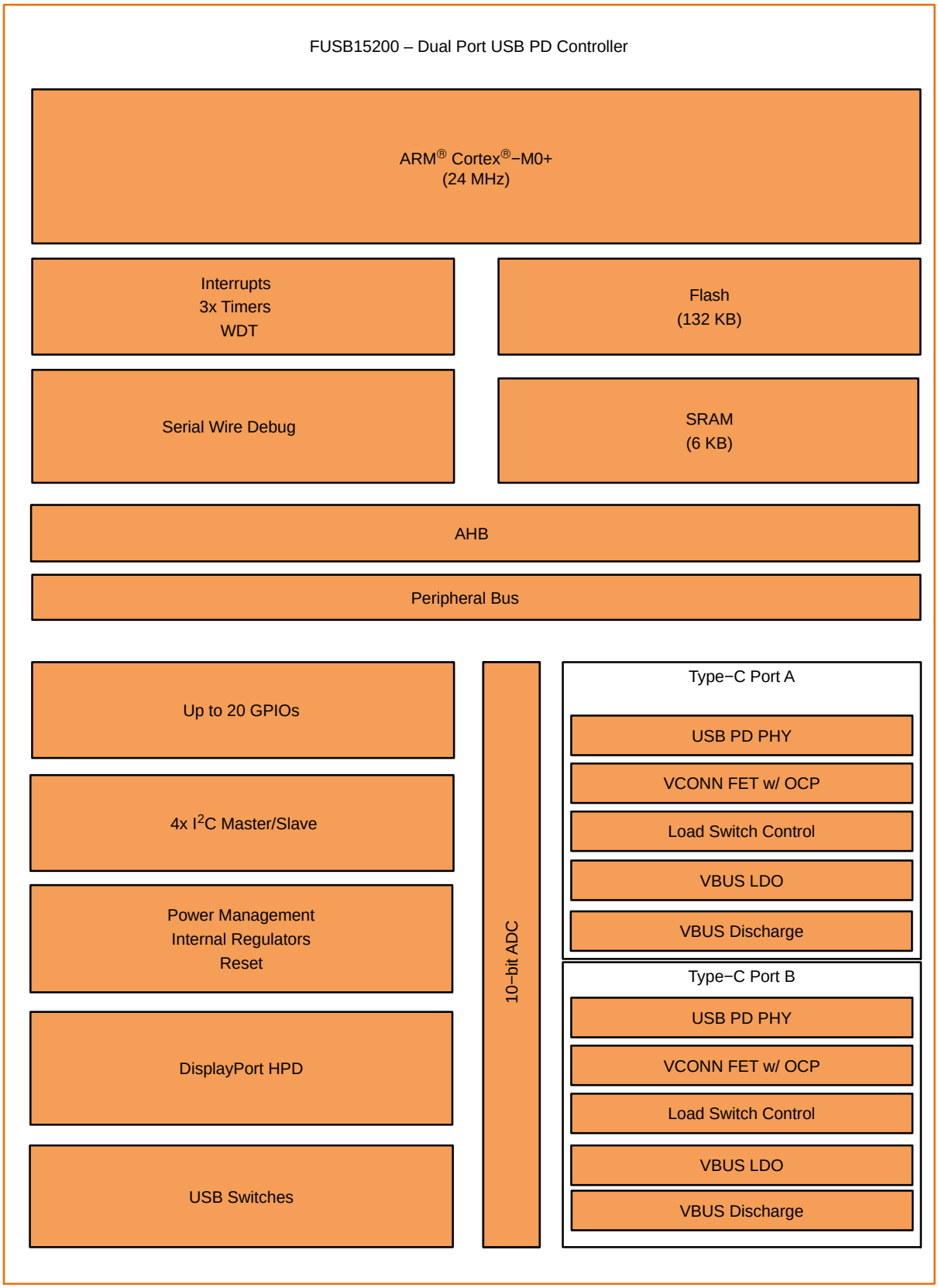


Figure 1. FUSB15200 Block Diagram

PIN DIAGRAM

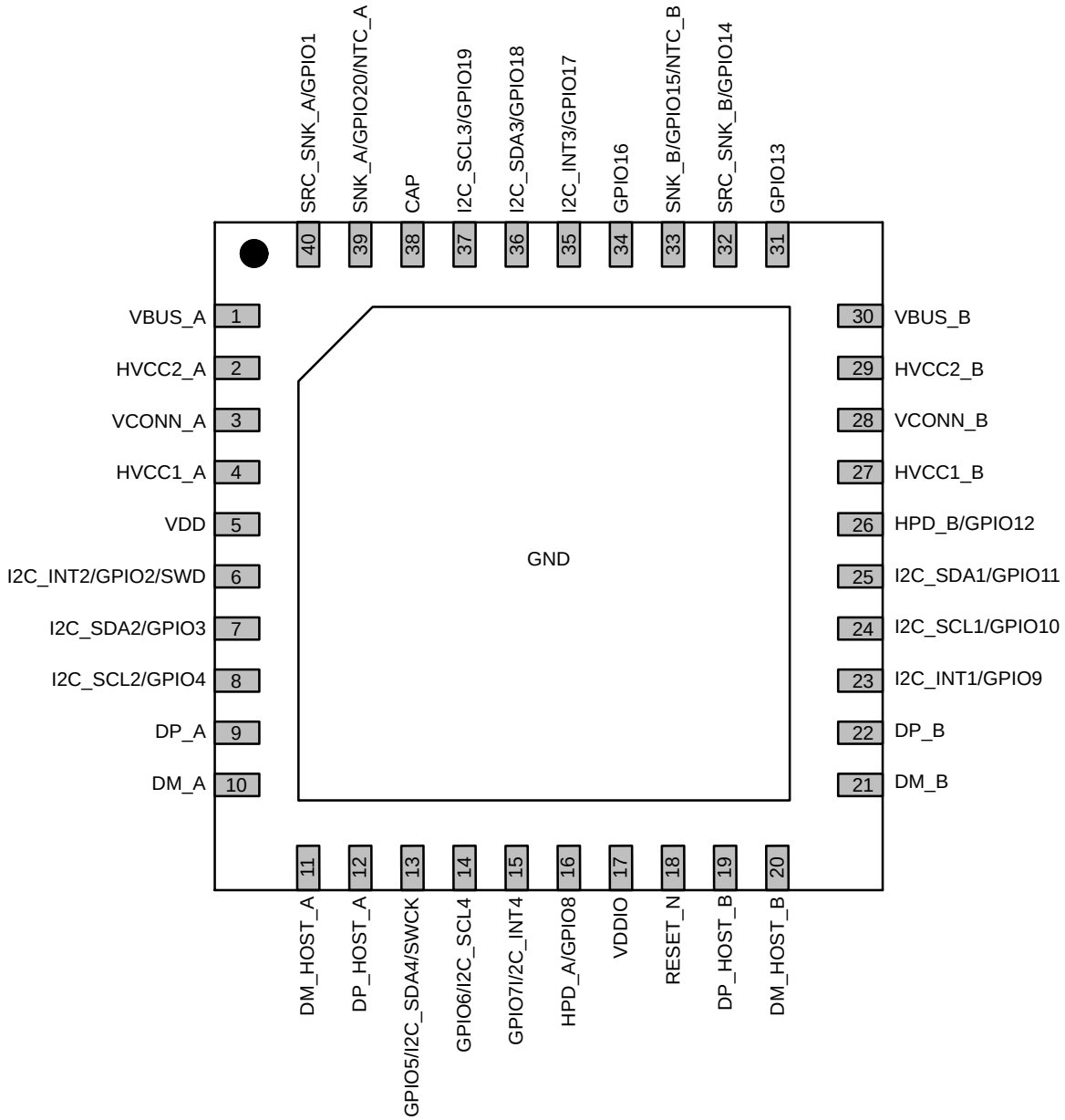


Figure 2. Pin Diagram

PIN DESCRIPTION

Pin #	Name	Port	Description
1	VBUS_A	Power	Port A VBUS. Monitoring Discharge (28 V)
2	HVCC2_A	Analog	Port A High Voltage Configuration Channel 2 (28 V)
3	VCONN_A	Power	Port−A VCONN Supply
4	HVCC1_A	Analog	Port A High Voltage Configuration Channel 1 (28 V)
5	VDD	Power	Power Supply
6	I2C_INT2/GPIO2/SWD	PA2	I^2C Port 2 Interrupt/ General Purpose I/O /Serial Wire Debug Data
7	I2C_SDA2/GPIO3	PA3	I^2C Port 2 Data/ General Purpose I/O (Open Drain)
8	I2C_SCL2/GPIO4	PA4	I^2C Port 2 Clock/ General Purpose I/O
9	DP_A	Analog	Port A USB 2.0 D+ (Connector side)
10	DM_A	Analog	Port A USB 2.0 D− (Connector side)
11	DM_HOST_A	Analog	Port A USB 2.0 D− (Host side)
12	DP_HOST_A	Analog	Port A USB 2.0 D+ (Host side)
13	GPIO5/I2C_SDA4/SWCK	PA5	General Purpose I/O/ I^2C Port 4 Data/ Serial Wire Debug Port Clock
14	GPIO6/I2C_SCL4	PA6	General Purpose I/O I^2C Port 4 Clock
15	GPIO7/I2C_INT4	PA7	General Purpose I/O/ I^2C Port 4 Interrupt
16	HPD_A/GPIO8	PA8	Hot Plug Detect/ General Purpose I/O
17	VDDIO	Power	I/O Voltage Supply
18	RESET_N	Input	Active Low chip reset
19	DP_HOST_B	Analog	Port B USB 2.0 D+ (Host side)
20	DM_HOST_B	Analog	Port B USB 2.0 D− (Host side)
21	DM_B	Analog	Port B USB 2.0 D− (Connector side)
22	DP_B	Analog	Port B USB 2.0 D+ (Connector side)
23	I2C_INT1/GPIO9	PA9	I^2C Port 1 Interrupt/ General Purpose I/O
24	I2C_SCL1/GPIO10	PA10	I^2C Port 1 Clock/ General Purpose I/O (Open Drain)
25	I2C_SDA1/GPIO11	PA11	I^2C Port 1 Data/ General Purpose I/O
26	HPD_B/GPIO12	PA12	Hot Plug Detect/ General Purpose I/O
27	HVCC1_B	Analog	Port B High Voltage Configuration Channel 1 (28 V)
28	VCONN_B	Power	Port−B VCONN Supply
29	HVCC2_B	Analog	Port B High Voltage Configuration Channel 2 (28 V)
30	VBUS_B	Power	Port B VBUS. Monitoring Discharge (28 V)
31	GPIO13	PA13	General Purpose I/O
32	SRC_SNK_B/GPIO14	PA14	Port B Source/Sink load switch control/ General Purpose I/O
33	SNK_B/GPIO15	PA15	Port B Sink Control/ General Purpose I/O
34	GPIO16	PA16	General Purpose I/O
35	I2C_INT3/GPIO17	PA17	I^2C Port 3 Interrupt/ General Purpose I/O
36	I2C_SDA3/GPIO18	PA18	I^2C Port 3 Data/ General Purpose I/O
37	I2C_SCL3/GPIO19	PA19	I^2C Port 3 Clock/ General Purpose I/O
38	CAP	Analog	1.5 V capacitor
39	SNK_A/GPIO20	PA20	Port A Sink Control/ General Purpose I/O
40	SRC_SNK_A/GPIO1	PA1	Port A Source/Sink load switch control/ General Purpose I/O
DAP	GND	GND	Ground

APPLICATIONS DIAGRAM

The figure below shows a typical dual port DRP application.

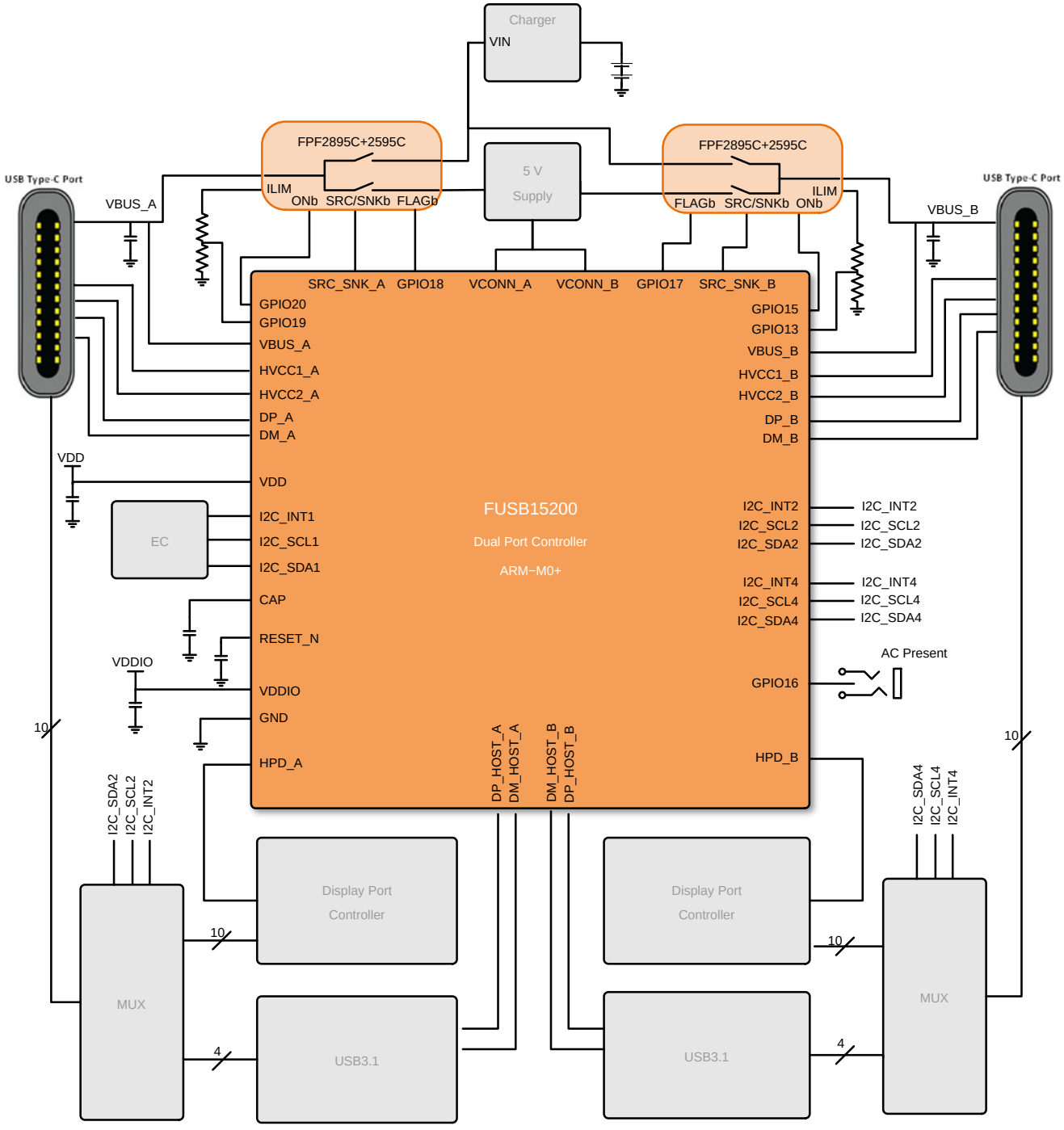


Figure 3. Application Diagram

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Symbol	Parameter	Min	Max	Unit
VBUS	VBUS Pin Voltage	−0.3	28	V
$V_{CONNECTOR-HV}$	HVCC1, HVCC2 Connector Pins	−0.3	28	V
$V_{CONNECTOR-LV}$	DP, DM Connector Pins	−0.5	6.0	V
VIO	I/O Voltage	−0.5	6.0	V
VDD	Supply Voltage	−0.5	6.0	V
VCONN	Supply Voltage	−0.5	6.0	V
VDDIO	VDDIO Supply	−0.3	6.0	V
VCAP	CAP Pin	−0.5	2.0	V
T_J	Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature	−40	150	°C
TL	Lead Temperature, (Soldering, 10 Seconds)	−	260	°C
ESD_{HBM}	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 (Note 3)	2	−	kV
ESD_{CDM}	Charged Device Model, JESD22−C101 (Note 3)	1	−	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

RECOMMENDED ESD DEVICES

Function	Manufacturer	Part Number
Type−C Connector Pins ESD	**onsemi**	TBD

OPERATING RATINGS

Symbol	Parameter	Min	Typ	Max	Unit
V_{CONN}	Supply Voltage Range	3.0	3.3	5.5	V
V_{DD}	Supply Voltage Range	3.0	3.3	5.5	V
V_{BUS}	V_{BUS} Voltage	3.1	−	22.05	V
V_{DDIO}	I/O Supply Voltage	1.7	−	5.5	V
V_{HVCCx}	Communication Channel Pins	0	−	5.5	V
V_{USB}	DM, DP Pins	0	−	3.6	V
V_{IO}	GPIO, I2C, RESET, HPD	0	−	5.5	V
T_A	Operating Ambient Temperature	−40	−	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TYPE−C AND PD SECTION						
USB PD PHY						
TRANSMITTER						
UI	Unit Interval		3.03	3.33	3.7	μs
pBitRate	Maximum Difference between the bit−rate During the Payload and Last 32 Bits of Preamble		−	−	0.25	%
tEndDriveBMC	Time to Cease Driving the Line after the End of the Last Bit of the Frame		−	−	23	μs
tHoldLowBMC	Time to Cease Driving the Line after the Final High−to−low Transition		1	−	−	μs
tInterFrameGap	Any PD Transmission Cannot be Sent Out before a Dead Time of at Least tInterFrameGap from Receiving or Sending a Packet		25	−	−	μs
tFall	Fall Time		300	−	−	ns
tRise	Rise Time		300	−	−	ns
tStartDrive	Time before the Start of the First Bit of the Preamble when the Transmitter Shall Start Driving the Line		−1	−	1	μs
vSwing	BMC Voltage Swing		1.05	1.125	1.2	V
zDriver	TX Output Impedance at 750 kHz with an External 220 pF or Equivalent Load		33	−	75	Ω
rFRSwapTx	Fast Role Swap Request Transmit Driver Resistance	VDD = 3.0 V to 5.5 V	−	−	5	Ω
RECEIVER						
cReceiver	Receiver Capacitance when Driver isn't Turned On	Vrms = 0.371; Vdc = 0.5 V; Freq. = 1 MHz	−	75	−	pF
tRxFilter	Rx Bandwidth Limiting Filter		100	−	−	ns
tTransitionWindow	Time Window for Detecting Non−idle		12	−	20	μs
vFRSwapCableTx	The Fast Role Swap Request Has to be Below this Voltage Threshold to be Detected		490	520	550	mV
tFRSwapRx	Fast Role Swap Request Detection Time (Note 4)		30	−	50	μs
zBmcRx	Receiver Input Impedance (Cannot be Tested but Can be Simulated and Guaranteed by Design)		1	−	−	MΩ
TYPE−C FRONT END						
I_{80_CCX}	SRC 80 μA CC Current (Default)		64	80	96	μA
I_{180_CCX}	SRC 180 μA CC Current (1.5 A)		166	180	194	μA
I_{330_CCX}	SRC 330 μA CC Current (3 A)		304	330	356	μA
R_{DEVICE}	Device Pull−down Resistance		4.6	5.1	5.6	kΩ
R_A	Powered Cable Termination		800	−	1200	Ω
zOPEN	CC Resistance for Disabled State, when Vdd is Valid		126	−	−	kΩ
I_{SW_CCX}	Over Current Protection (OCP) Limit at which VCONN Switch Shuts Off over the Entire VCONN Voltage Range	VCONN_OCP = 800 mA	600	800	1000	mA
V_{CCx_OVP}	CC1/2 Over−Voltage Protection		5.6	−	6.0	V

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TYPE−C FRONT END						
R_{SW_CCx}	Rdson for VDD to CC1 or VDD to CC2	I_{SW_CCX} = 0 to 600 mA, VCONN_OCP > 80 mA	−	0.85	1.8	Ω
$R_{SW\_CCx\_LOW\_OCP}$	Low OCP Setting Rdson for VDD to CC1 or VDD to CC2	I_{SW_CCX} = 0 to 80 mA, VCONN_OCP ≤ 80 mA	−	2.7	5	Ω
vRdSRCUSB	Source Attach Threshold for CC Pin at Default Current		1.5	1.6	1.65	V
vRdSRC1.5	Source Attach Threshold for CC Pin at 1.5 A Current		1.5	1.6	1.65	V
vRdSRC3.0	Source Attach Threshold for CC Pin at 3 A Current		2.45	2.6	2.75	V
vRaSRCUSB	Source Ra Threshold for CC Pin at Default Current		0.15	0.2	0.25	V
vRaSRC1.5	Source Ra Threshold for CC Pin at 1.5 A Current		0.35	0.4	0.45	V
vRaSRC3.0	Source Ra Threshold for CC Pin at 3 A Current		0.75	0.8	0.85	V
vRdSNKUSB	Attach Threshold for CC Pin SNK (Default Current)		0.61	0.66	0.7	V
vRdSNK1.5	Attach Threshold for CC Pin SNK (1.5 A Current)		1.16	1.23	1.31	V
vRdSNK3.0	Attach Threshold for CC Pin SNK (3 A Current)		2.04	2.11	2.18	V
vRaSNK	Attach Threshold for CC Pin SRC or SNK		0.15	0.2	0.25	V
vSafe0V	Safe Operating Voltage at 0 V		0.6	−	0.8	V
VBUS DISCHARGE						
$R_{VBUS\_DISCH\_0}$	Pull−down Resistance Applied to VBUS when Selected	VBUS = 0.8 V to 21.5 V	315	450	585	Ω
$R_{VBUS\_DISCH\_1}$		VBUS = 0.8 V to 21.5 V	420	600	780	
$R_{VBUS\_DISCH\_2}$		VBUS = 0.8 V to 21.5 V	525	750	975	
$R_{VBUS\_DISCH\_3}$		VBUS = 0.8 V to 21.5 V	700	1000	1300	
$R_{VBUS\_DISCH\_4}$		VBUS = 0.8 V to 21.5 V	1400	2000	2600	
$R_{VBUS\_DISCH\_5}$		VBUS = 0.8 V to 21.5 V	4.20	6.00	7.80	kΩ
CURRENT CONSUMPTION						
$I_{SLEEP−UNATTACHED}$	Current Consumption when in Deep Sleep	VDD = VDDIO = 3.0 to 5.5 V VBUS = 0 V; Not Type−C attached, DRP Toggling; LSOSC enabled; BC1.2 disabled	−	−	75	μA
I_{SLEEP}	Sleep Current	VDD = VDDIO = 3.0 to 5.5 V VBUS = 0; No I^2C traffic, LSOSC and HSOSC running; PD Peripheral and ADC enabled. No PD traffic.	−	700	−	μA
$I_{PD−ACTIVE}$	Port with PD Traffic	Active and communicating via USB PD transmitting and receiving packets on both ports	−	4.0	−	mA
PMU						
V_{VDD_POR}	POR Trip point	VDD Rising	1.0	−	2.4	V
V_{VDD_GOOD}	Minimum VDD Level for Enabling Device	VDD Rising	3.0	−	−	
V_{VDDIO_GOOD}	VDDIO Detection Threshold Used in Asserting PMU_STS when VDDIO is above it	VDDIO Rising	−	−	1.0	V
V_{VDD_BRWN}	VDD Brown Out Threshold	VDD Falling	2.6	−	3.0	V

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PMU						
V_{VDD_DBAT}	VDD Voltage where the Device is Powered from VDD Instead of VBUS	VDD Rising	2.6	−	3.0	V
CLOCKS						
F_{LS_CLK}	Low Speed Clock for Idle, Type−C Attach		114	120	126	kHz
F_{HS_CLK}	Internal Clock for Active Core and Full Function		22.8	24	25.2	MHz
EXTERNAL TEMPERATURE PROTECTION						
I_{NTCA}	Current Source on NTCA		55	60	65	μA
I_{NTCB}	Current Source on NTCB		55	60	65	μA
INTERNAL TEMPERATURE MEASUREMENT						
T_{SHUT}	Temperature for Internal Temperature Protection	VDD = 3.0 to 5.5	−	145	−	°C
T_{HYS}	Temp Hysteresis for Internal Temperature Protection	VDD = 3.0 to 5.5	−	10	−	°C
BC1.2 DETECTION						
R_{DCP}	DCP Emulation Resistance	VD+/D− = 0 V, 1.0 V, ION = 2 mA	−	80	180	Ω
R_{Dx_DWN}	DP/DM Pull Down Resistance	VD+/− = 0 V − 3.6 V	16	19.5	23	kΩ
I_{DP_SRC}	DCD Source Current	VDD = 3.0 V to 5.5 V	7	10	13	μA
I_{Dx_SNK}	Sink Current to Dx	VDD = 3.0 V to 5.5 V	25	75	175	μA
V_{DIV}	Divider Mode Output Voltage	VDD = 3.0 V to 5.5 V	2.65	2.75	2.85	V
R_{DIVP}	Divider Mode Resistance on DP	5 μA pulled out of DP	24	30	36	kΩ
R_{DIVM}	Divider Mode Resistance on DM	5 μA pulled out of DM	24	30	36	kΩ
R_{DAT_LKG}	Resistor Weak Pull−down on D+ and D−	V(sw) = 0 to 3.6 V	300	700	1100	kΩ
V_{Dx_SRC}	Source Voltage	VDD = 3.0 V to 5.5 V	0.5	0.6	0.7	V
R_{PU_MOS}	Pull−Up Moisture Detection Resistor		288	320	352	kΩ
V_{SRC_MOS}	Voltage Source for Moisutre Detection		0.9	1.0	1.1	V
SWITCH PATHS						
I_{OFFUSB}	Power−Off Leakage Current	All data ports, vsw = 3.6, vdd = 0	−	−	18	μA
R_{ONUSB}	USB Switch On Resistance	Vsw− =0 V, 0.4 V, ION = 8 mA, VDD = 3.0 to 5.0 V	−	5	−	Ω
C_{ONUSB}	DP_x, DM_x On Capacitance	Vsw = 400 mVpk−pk, f = 240 MHz, VDD = 3.8	−	7.5	−	pF
C_{OFFUSB}	DP/DM OFF Capacitance	f = 240 MHz, VDD = wc	−	3.3	−	pF
BW_{USB}	Differential −3 db Bandwidth	Vsw = 400 mVpk−pk, RL = 50 Ω, CL = 0 pF, VDD = 3.0 to 5.0 V	−	650	−	MHz
HPD						
HPD_Rx						
V_{IL-HPD}	Low−Level Input Voltage	VDD = 2.8 V to 5.5 V, VBUS = 3.1 V to 22.5 V, or VDD = 0 V and VBUS = 3.1 V to 22.5 V	−	−	0.8	V
V_{IH-HPD}	High−Level Input Voltage	VDD = 2.8 V to 5.5 V, VBUS = 3.1 V to 22.5 V, or VDD = 0 V and VBUS = 3.1 V to 22.5 V	2.0	−	−	V
$V_{HYS-HPD}$	Input Hysteresis	VDD = 2.8 V to 5.5 V, VBUS = 3.1 V to 22.5 V, or VDD = 0 V and VBUS = 3.1 V to 22.5 V. Typ VDD = 3.0 V	−	280	−	mV

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HPD_Rx						
I_{IN-HPD}	Input Leakage	VDD = 2.8 V to 5.5 V, VBUS = 3.1 V to 22.5 V, or VDD = 0 V and VBUS = 3.1 V to 22.5 V, Input Voltage 0 V to 3.6 V	−5	−	5	μA
$I_{OFF-HPD}$	Off Input Leakage	VDD = 0 V, VBUS = 0 V, Input Voltage 0 V to 5.5 V	−5	−	5	μA
C_{IN-HPD}	Pin Capacitance		−	5	−	pF
HPD_Tx						
V_{OL-HPD}	Ouptut Low Voltage	VDD = 2.8 V to 5.5 V, VBUS = 3.1 V to 22.5 V, or VDD = 0 V and VBUS = 3.1 V to 22.5 V, Iout = +4 mA	−	−	0.4 V	V
V_{OH-HPD}	Output High Voltage for HPD Output	VDD = 2.8 V to 5.5 V, VBUS = 3.1 V to 22.5 V, or VDD = 0 V and VBUS = 3.1 V to 22.5 V, Iout = −2 mA	2.25	−	3.6	
R_{PD-HPD}	Pull Down resistance on HPD Pin when Enabled	PORT's pull−down resistance is enabled and HPD peripheral is enabled	100	−	−	kΩ
SERIAL WIRE DEBUG INTERFACE						
F_{SWDCLK}	Serial Wire Debug Input Clock Frequency	Core frequency = 24 MHz	−	−	10	MHz
T_{SWDI_SET}	Serial Wire Debug Data Setup Timing		0.25 * (1 / SWCLK)	−	−	ns
T_{SWDI_HOLD}	Serial Wire Debug Data Hold Timing		0.25 * (1 / SWCLK)	−	−	ns
V_{IH-SWD}	Serial Wire Debug Input Voltage Threshold	VDDIO = 1.7 V to 5.5 V	0.7 x VDDIO	−	−	V
V_{IL-SWD}		VDDIO = 1.7 V to 5.5 V	−	−	0.3 x VDDIO	
$V_{HYS-SWD}$	Serial Wire Debug Input Voltage Hysteresis	VDDIO = 1.7 V to 5.5 V	−	300	−	mV
$I_{LKG-SWD}$	Serial Wire Debug Input Leakage	VDDIO = 1.7 V to 5.5 V, Input Voltage 0 V to 5.5 V	−10	−	+10	μA
V_{OH-SWD}	Serial Wire Debug Output Voltage High	VDDIO = 1.7 V to 5.5 V, Iout = −2 mA	VDDIO − 0.5 V	−	−	V
V_{OL-SWD}	Serial Wire Debug Output Voltage Low	VDDIO = 1.7 V to 5.5 V, Iout = +4 mA	−	−	0.4 V	V
RESET						
RESET_N_VIL1	Low Level Input Voltage	VDD = 2.8 V to 5.5 V	−	−	0.3 x VDD	V
RESET_N_VIH1	High Level Input Voltage	VDD = 2.8 V to 5.5 V	0.7 x VDD	−	−	V
RESET_N_RPU	Internal Pull−Up Resistor to VDD		−	100	−	kΩ
RESET_N_ILKG	Input Leakage		−120	−	−	μA
GPIO						
VI_{H-GPIO}	High Level Input Voltage	VDDIO = 1.7 V to 5.5 V	0.7 x VDDIO	−	−	V
$V_{IL-GPIO}$	Low level Input Voltage	VDDIO = 1.7 V to 5.5 V	−	−	0.3 x VDDIO	V
$V_{OH-GPIO}$	Output High Voltage (Not Applicable to Open−Drain GPIO3 and GPIO10)	VDDIO = 1.7 V to 5.5 V, Iout = −2 mA	VDDIO − 0.5	−	−	V

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VDD = 2.8 V to 5.5 V, TA = −40°C to +85°C unless otherwise noted. Typical values are at TA = 25°C, VDD = 3.3 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GPIO						
$V_{OL-GPIO}$	Output Low Voltage	VDDIO = 1.7 V to 5.5 V, Iout = +4 mA	−	−	0.4	V
V_{OH-SNK}	SNKx Pin Output High Voltage		2.5	−	−	V
V_{OL-SNK}	SNKx Pin Output Low Voltage		−	−	0.4	V
V_{OH-NTC}	Output High Voltage for PA4 and PA8	VDD = 2.8 V to 5.5 V, Iout = −2mA	VDD – 0.5	−	−	V
V_{OL-NTC}	Output Low Voltage for PA4 and PA8	VDD = 2.8 V to 5.5 V, Iout = +4mA	−	−	0.4	V
$V_{HYS-GPIO}$	Input Hysteresis	VDDIO = 1.7 V to 5.5 V, 3.6 V Typ	−	300	−	mV
$I_{IN-GPIO}$	Input Leakage	VDDIO = 1.7 V to 5.5 V, Input Voltage 0 V to 5.5 V	−5	−	5	μA
$I_{OFF-GPIO}$	Off Input Leakage	VDDIO = 0 V, VDD = 0 V to 5.5 V, Input Voltage 0 V to 5.5 V	−5	−	5	μA
$R_{PD-GPIO}$	Pull−Down Resistance	PORT_PDx = 1	−	100	−	kΩ
$R_{PU-GPIO}$	Pull−Up Resistance (Not Applicable to Open−Drain GPIO3 and GPIO10)	PORT_PUx = 1	−	100	−	kΩ
C_{GPIO}	Pin Capacitance		−	5	−	pF
I^2C I/O						
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH	VDD = 2.8 to 5.5, VIN = 1.8 V	−10	−	10	μA
I_{i2C}	Input Current of SDA and SCL Pins	VDD = 2.8 to 5.5, VIN = 0 to 5.5 V	−10	−	10	μA
V_{IH-I2C}	High−Level Input Voltage	VDD = 2.8 to 5.5	1.2	−	−	V
V_{IL-I2C}	Low−Level Input Voltage	VDD = 2.8 to 5.5	−	−	0.4	V
$V_{OL1-I2C}$	Low−Level Output Voltage at 3 mA Sink Current (Open−Drain)	VDD = 2.8 to 5.5	0	−	0.3	V
$V_{OL2-I2C}$	Low−Level Output Voltage at 2 mA Sink Current (Open−Drain)	VDD = 2.8 V − 5.5 V	0	−	0.3	V
$V_{HYS-I2C}$	Hysteresis of Schmitt Trigger Inputs	VDD = 2.8 to 5.5	0.1	0.2	−	V
I_{OLSDA}	Low−Level Output Current (Open−Drain)	VDD = 2.8 to 5.5, VOL = 0.4 V	20	−	−	mA
V_{OL_INT}	INT_N Output Low Voltage	VDD = 2.8 to 5.5, IOL = 4 mA	−	−	0.4	V
C_{I-I2C}	Capacitance for Each I/O Pin	VDD = 2.8 to 5.5	−	5	−	pF
t_{SP}	Pulse Width of Spikes that Must be Suppressed by the Input Filter		0	−	50	ns
V_{IH_INT}	High−Level Input Voltage	VDD = 2.8 to 5.5	1.2	−	−	V
V_{IL_INT}	Low−Level Input Voltage	VDD = 2.8 to 5.5	−	−	0.4	V
FLASH						
NEND	Sector Endurance		20,000	−	−	Erase/ write cycles
T_{DR}	Data Retention	T = 25°C	100	−	−	years
		T = 105°C	20	−	−	Years
		T = 125°C	10	−	−	Years

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. (SRC/SNK I/Os will switch to its new configuration based on USB_IO_CONFIG setting within tFRSwapRx(max))

Arm Cortex−M0+ Processor

The FUSB15200 integrates an ARM Cortex−M0+ processor with Nested Vector Interrupt Controller (NVIC), Wake−up Interrupt Controller (WIC), and Debug Access Port (DAP). The processor uses the Thumb instruction set and is optimized for high performance with reduced code size and low power operation. The ARM Cortex−M0+ efficiently handles multiple parallel peripherals and has integrated sleep modes. Test and debug capability is enhanced with the ARM Serial Wire Debug Port.

The ARM implementation in the FUSB15200 includes a 132KB Flash RAM and 6KB of SRAM.

The MCU, Memory and DAP are interconnected using the AMBA (Advanced Microcontroller Bus Architecture) AHB−Lite interface and peripherals are connected to the AHB via APB interface (Advanced Peripheral Bus).

In addition to the base Arm Cortex−M0+ processor interrupts, the FUSB15200 implements multiple external source interrupts for peripheral devices. A powerful nested, pre−emptive and priority based interrupt handling system assures timely and flexible response to external events.

Low power features on FUSB15200 include the WIC, adjustable clock rates, and different software controlled power modes to maximize opportunities to save power in the final application.

Power Management Unit

The Power Management Unit (PMU) provides appropriate power to all the blocks in the FUSB15200.

The FUSB15200 is able to power from either VBUS pin when VDD is not present (dead battery condition). When VDD > VDD_DBAT becomes available, PMU will automatically switch the internal power to VDD.

When device is powered from VBUS alone, the SNK pins can be controlled without VDDIO.

The FUSB15200 power management unit prevents system brown−outs in case VDD voltage dips below the specified minimum voltage required for reliable operation. Firmware may monitor the power supply and safely shutting down the system if needed.

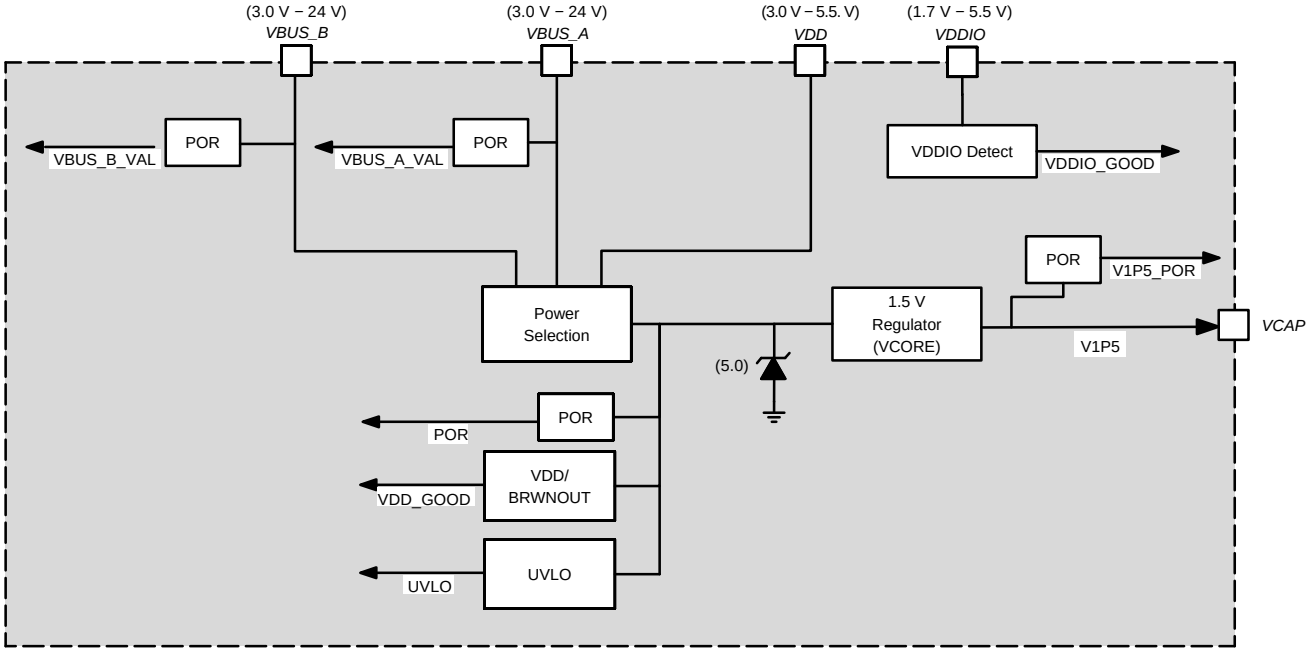


Figure 4. FUSB15200 PMU

Reset Sources

The FUSB15200 has various sources of reset including:

- *Internal Power−On Reset (VDD_POR)* – The VDD_POR reset asserts when the regulated supply is below threshold levels for proper operation. The VDD_POR resets the entire chip including core, debug port, peripherals, wakeup timer, and watchdog.
- *Software Issued Reset* – The software reset can be called by writing to a given register in the Cortex address space. It is typically called on exit from a processor exception. Software reset resets the entire chip including core, peripherals, wakeup timer, and watchdog.
- *Watchdog Timer Reset* – The watchdog timer reset is caused by the watchdog timeout and is used to prevent errant software from locking up the device. The watchdog reset resets the entire chip including core, debug port, peripherals, and watchdog. The watchdog timer is disabled upon power up and must be enabled by software. The watchdog is paused when the debugger halts the processor.

- *External Pin Reset* – The external reset is under user control with the external RESET_N pin. External pin reset resets the entire chip including core, debug port, peripherals, wakeup timer, and watchdog

Power and Sleep Behavior

The FUSB15200 has been optimized to conserve power by utilizing peripheral interrupts and hardware autonomy. The device can be configured via firmware to enter low power states, disable unneeded peripherals and scale clock frequencies based on different application needs.

The Type−C block is designed to function at the lowest power states and will automatically wake when a Type−C attach is detected. This minimizes total power consumption when no device is attached.

Clock Sources

FUSB15200's implements a dual oscillator architecture to minimize power consumption.

- A 24 MHz internal RC oscillator to enable full functionality.
- A 120 kHz internal RC oscillator that can be used for very low power sleep modes.

Timers

32−bit General Purpose Timers (TIM0/1)

There are two 32−bit down−counters that can generate an interrupt request signal, status, when the counter reaches 0.

The timing resolution depends on the programmable clock source and pre−scale ratios.

32−bit Wake−up Timer (WUT)

The main purpose of the wakeup timer is to facilitate scheduled exit from low power modes. It can also be used for general purpose event timing.

32−bit Watchdog Timer (WDT)

The watchdog timer applies a reset to the system in the event of a software failure, providing a way to recover from software crashes. The watchdog timer is disabled by default and must be enabled through software.

The watchdog is protected with a lock mechanism to prevent rogue software from disabling the watchdog functionality. A special value has to be written to the lock register to access watchdog control.

Serial Wire Debug Interface (SWD)

The ARM M0+ implementation includes a Debug Access Port (DAP).

The debug mode implementation includes 4 hardware breakpoints and 2 hardware watch points.

The Debug Access Port interface implementation is the ARM Serial Wire Debug Port (SW−DAP) connected to pins SWCLK and SWDIO. The Serial Wire Debug Port Interface uses a single bi−directional data connection. Each operation consists of three phases: Packet request, Acknowledge response, and Data transfer phase. Use any Serial Wire Debug (SWD) compliant hardware debugger interface to interact with the internals of the FUSB15200.

USB Type−C & PD Peripheral Overview

The USB Type−C and PD peripheral provides the building blocks to enable a fully compliant USB Type−C and PD solution.

This peripheral consists of an analog front end and a digital state machine. Firmware implements higher level protocol and policy layers whereas the analog and digital components can perform lower level PD protocol and PHY layer functions.

The Type−C block includes all terminations and comparators required for Source/Sink/DRP operation: plug orientation detection, power capability advertisement and power role detection.

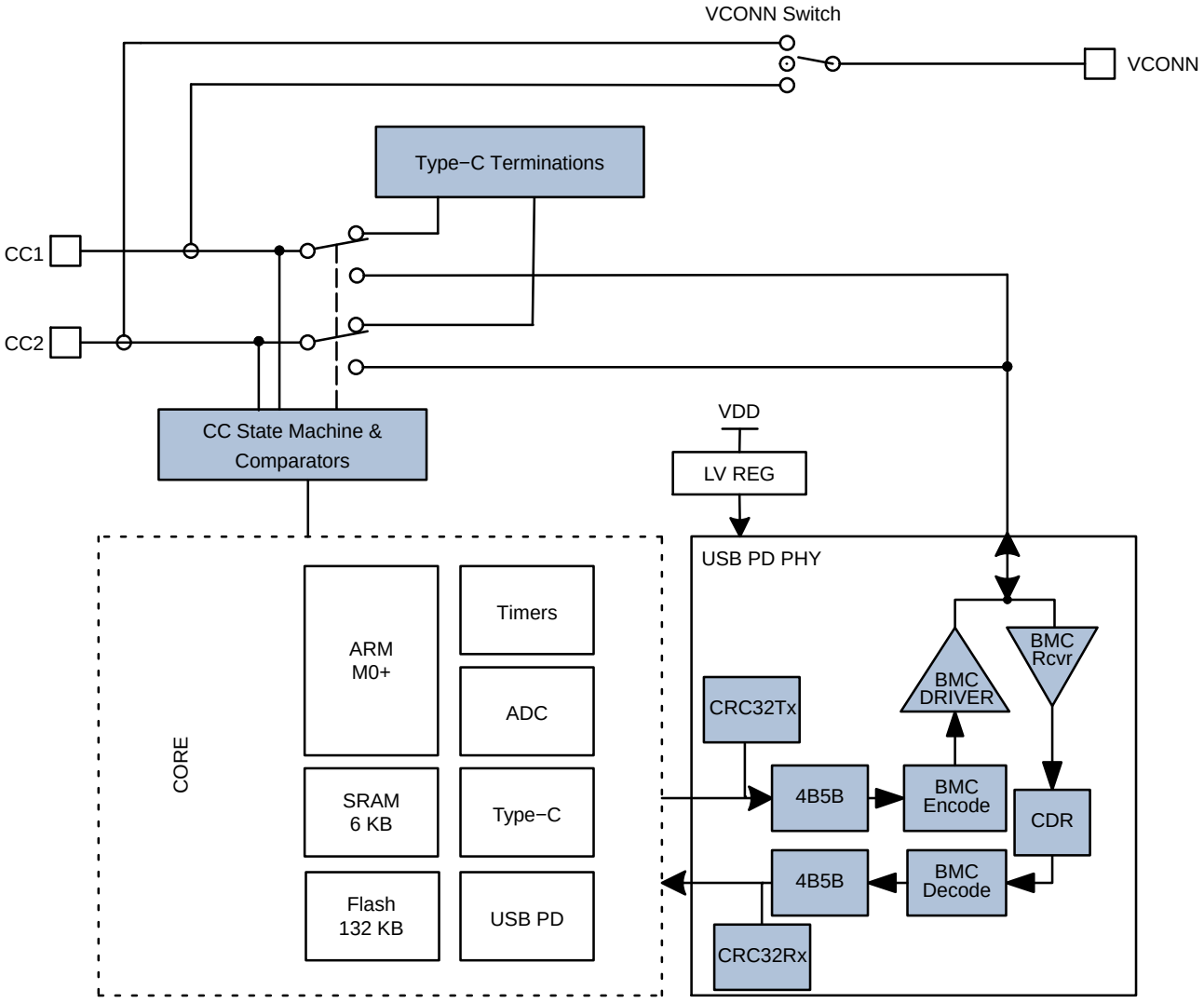


Figure 5. USB Type−C and PD

VCONN Switch

Some applications require that a VCONN voltage be sourced in order to provide additional capabilities, such as greater than 3 A VBUS sourcing or support for full−featured Type−C cables.

The FUSB15200 can provide 1.5 W or more depending on VCONN level.

USB PD PHY State Machine Logic

The FUSB15200 PD module includes the following digital functions to enable USB PD messaging:

- Serialization and de−serialization
- Clock and data recovery (CDR)
- 4B5B coding
- BMC coding
- Packet CRC generation and checking
- Coding and detection of Power Delivery K−Codes
- Automatic GoodCRC packet response

VBUS Discharge

The FUSB15200 is able to discharge VBUS via selectable pull−down resistors.

Typical source applications will rely on the DC−DC converter to transition between VBUS voltages.

If the application requires the FUSB15200 to discharge VBUS, the firmware may select the proper resistance of the discharge. Selection of discharge resistance needs to take into account any capacitive load on VBUS as not to violate VsrcSlewNeg in the USB PD spec (30 mV/μs).

Source applications, where the FUSB15200 internal discharge is utilized, will have to isolate any large bulk capacitances in order to prevent extreme internal temperature rises. Typical isolated source capacitances are around 4.7 μF.

The FUSB15200 is capable of discharging up to 100 μF from VBUS in the entire operating range.

Fast Role Swap

Fast Role Swap is the process of exchanging the Source and Sink roles between Port Partners rapidly due to the disconnection of an external power supply.

The Fast Role Swap process is intended for use by a capable USB device that presently has an external power supply, and is providing power both through its downstream Ports to USB Devices and upstream to a USB Host such as a laptop. On removal of the external power supply Fast Role Swap enables a VBUS supply to be maintained by allowing the USB Host to apply vSafe5V after having detected Fast Role Swap signaling. The initial Source will signal a Fast Role Swap request by driving CC to ground with a resistance of less than rFRSwapTx for tFRSwapTx. The initial Source will only signal a Fast Role Swap when it has an Explicit Contract.

The FUSB15200 has dedicated I/Os (SRC_SNK_x and SNK) that can autonomously toggle when programmed to detect or transmit a fast role swap signal.

Internal Protection

The FUSB15200 integrates multiple system level protections to enable robust designs.

VCONN Over−Current Protection

Each port's VCONN Switch provides over−current detection and protection for the switch that is enabled based on the Type−C orientation and can be software configured based on application needs. The level of OCP can be controlled via a register setting.

In case of an over−current event the switch will be opened.

CC Over−Voltage Protection

Over−voltage protection on CC pins protects the internal circuitry damage from high voltages.

Interrupts can be used to inform the software that an OVP event has occurred and take appropriate actions.

Internal Over Temperature Protection

Internal over temperature protection is always on. Two potential sources of elevated internal temperature are:

- High Current through VCONN Switch
- High current through VBUS discharge

In either case, if the over temperature is triggered (T > Tshut), both ports' VCONN switches and VBUS discharge circuitry will be disabled.

Connector Moisture Detection

If moisture or pollutants are present in the connector and the device provides VBUS, there could be a resistive short between VBUS and other connector pins.

The FUSB15200 provides a method to detect if there is moisture or other pollutants in the connector.

Moisture detection can be turned on or off as not to conflict with cable attach detection.

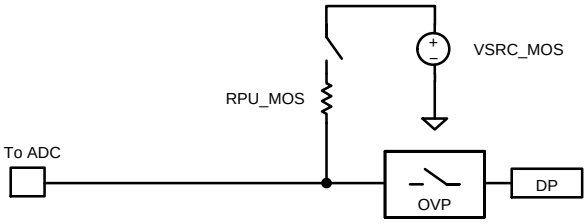


Figure 6. Moisture Detection

Port Control and GPIOs

The FUSB15200 includes a number of pins that can be configured to be used as standard GPIO or for use with a dedicated peripheral such as I^2C. A subset of these pins can also be connected as an input to the ADC. Internal pull−up/down resistors are programmable. Pull−up resistors are always connected to VDDIO.

When the PORT is configured as GPIOs it will have the following capabilities:

- Bi−directional capability
- Push pull or open drain configuration
- Individually configurable interrupt lines
- Rising or Falling edge interrupt
- High or Low level interrupt

NOTE:

5. PA14 and PA20's output supply is derived from an internal 3.0 V regulator to guarantee operation of sink path load switch in dead battery condition.
6. GPIO3 and GPIO10 are Open−Drain and do not have pull−up resistance.

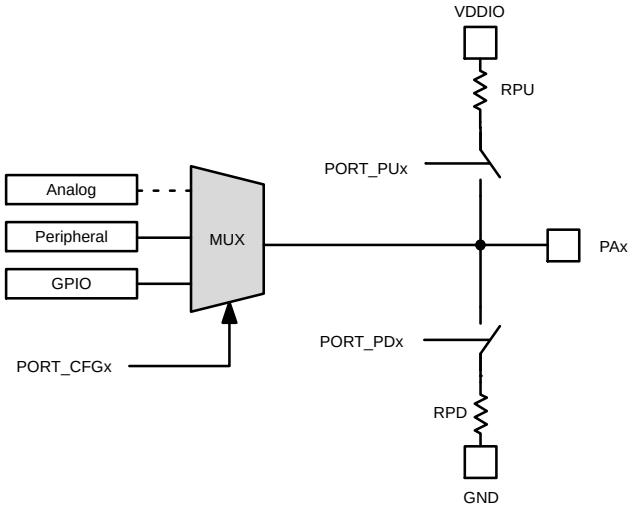


Figure 7. Typical Port Configuration

Table 1. PIN − PORT CONFIGURATION AND POWER DOMAIN

Pin #	Name	Port	Power Supply
40	SRC_SNK_N_A	PA1	VDDIO
	GPIO1		VDDIO
6	I2C_INT2	PA2	VDD
	GPIO2		VDDIO
	SWD		VDDIO
7	I2C_SDA2	PA3	VDD
	GPIO3 (OD)		VDDIO
8	I2C_SCL2	PA4	VDD
	GPIO4		VDDIO
13	I2C_SDA4	PA5	VDD
	GPIO5		VDDIO
	SWCK		VDDIO
14	I2C_SCL4	PA6	VDD
	GPIO6		VDDIO
15	I2C_INT4	PA7	VDD
	GPIO7		VDDIO
16	HPD_A	PA8	Internal 3.0 V Regulator
	GPIO8		VDDIO
18	RESET_N	Input	VDD
23	I2C_INT1	PA9	VDD
	GPIO9		VDDIO

Table 1. PIN − PORT CONFIGURATION AND POWER DOMAIN (continued)

Pin #	Name	Port	Power Supply
24	I2C_SCL1	PA10	VDD
	GPIO10 (OD)		VDDIO
25	I2C_SDA1	PA11	VDD
	GPIO11		VDDIO
26	HPD_B	PA12	Internal 3.0 V Regulator
	GPIO12		VDDIO
31	GPIO13	PA13	VDDIO
32	SRC_SNK_N_B	PA14	Output = Internal 3.0 V Regulator Input = VDDIO
	GPIO14		
33	SNK_B	PA15	VDDIO
	GPIO15		VDDIO
34	GPIO16	PA16	VDDIO
35	I2C_INT3	PA17	VDD
	GPIO17		VDDIO
36	I2C_SDA3	PA18	VDD
	GPIO18		VDDIO
37	I2C_SCL3	PA19	VDD
	GPIO19		VDDIO
39	SNK_A	PA20	Output = Internal 3.0 V Regulator Input = VDDIO
	GPIO20		

Table 2. PORT DEFAULT CONFIGURATION

Pin #	FUSB15200 Pin Name	Port	Default Configuration on Power Up	I/O State	NMI	Analog Function
40	SRC_SNK_N_A/GPIO1	PA1	GPIO1	Input Float		
6	I2C_INT2/GPIO2/SWD	PA2	SWD	Input		
7	I2C_SDA2/GPIO3	PA3	GPIO3 (OD)	Input Float		
8	I2C_SCL2/GPIO4	PA4	GPIO4	Input Float		
13	GPIO5/I2C_SDA4/SWCK	PA5	SWCK	Input		
14	GPIO6/I2C_SCL4	PA6	GPIO6	Input Float		
15	GPIO7/I2C_INT4	PA7	GPIO7	Input Float	Yes	
16	HPD_A/GPIO8	PA8	GPIO8	Input Float		
23	I2C_INT1/GPIO9	PA9	GPIO9	Input Float		
24	I2C_SCL1/GPIO10	PA10	GPIO10 (OD)	Input Float		
25	I2C_SDA1/GPIO11	PA11	GPIO11	Input Float		
26	HPD_B/GPIO12	PA12	GPIO12	Input Float		
31	GPIO13	PA13	GPIO13	Input	Yes	
32	SRC_SNK_N_B/GPIO14	PA14	GPIO14	Input Float		
33	SNK_B/GPIO15/NTC_B	PA15	GPIO15	Input Float	Yes	Yes
34	GPIO16	PA16	GPIO16	Input		
35	I2C_INT3/GPIO17	PA17	GPIO17	Input Float	Yes	
36	I2C_SDA3/GPIO18	PA18	I2C_SDA	Input		
37	I2C_SCL3/GPIO19	PA19	I2C_SCL	Input		
39	SNK_A/GPIO20/NTC_A	PA20	GPIO20	Input Float		Yes

Non−Maskable Interrupts (NMI)

The FUSB15200 provides a method of selecting one of four GPIOs that can be used as a source of an external non−maskable interrupt. (See table 2)

If a non−maskable external interrupt is not required, all GPIOs provide a method to interrupt the processor. In this case, the Brown−Out detector can be assigned to the NMI slot of the interrupt controller.

The port mapping, power domain and default configuration are shown in the Table 2.

HPD I/Os

HPD I/Os are used in DisplayPort (DP) applications to signal events between the DP Source and DP Receiver.

The FUSB15200 HPD I/Os can be configured as an input (DP receiver) or Output (DP Source).

The HPD I/Os supply is derived from an internal 3.0 V regulator to guarantee levels in all conditions.

DP Receiver Behavior

When the FUSB15200 is implemented in a DP Receiver, the HPD I/O is setup as an input. Debounce timers implemented in HW facilitates HPD IRQ and Level detection. Please see t_{HPD_Rx} in Electrical Specifications.

DP Source Behavior

When the FUSB15200 is implemented in a DP Source, the HPD I/O is setup as an Output.

The HPD output will be driven by the firmware. HPD IRQ pulsewidth timer is implemented in hardware, see t_{HPD_Tx} in Electrical Specifications.

If the application does not have external pull−down resistors as required by the VESA spec, internal pull downs can be enabled via the PORT interface. When the HPD peripheral is enabled, an additional resistance is added to the PORT's pull−down to achieve the minimum 100 kOhm required (See figure 8 below).

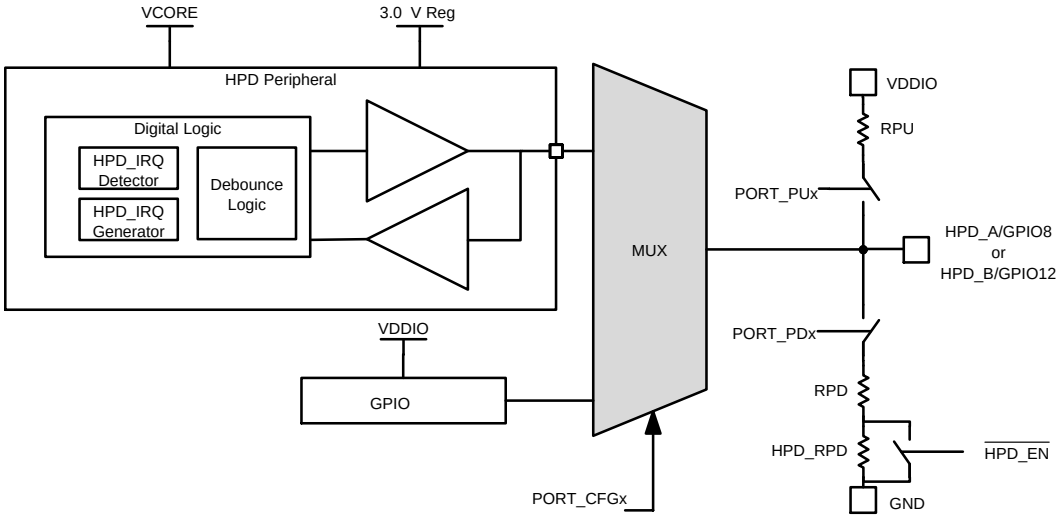


Figure 8. HPD I/O Configuration

External Temperature Measurements

There are two pins that can be configured to monitor external NTC resistors that can be located near where high temperature devices are located. A parallel resistor is recommended for measurement linearity.

These NTC measurements are useful for monitoring temperatures for protection due to excessive thermals.

Firmware implementation of the external temperature measurements make NTC selection flexible.

The pull−up current sources INTCA and INTCB provide a bias to the external NTC resistor networks. If desired, this current source may be turned−off.

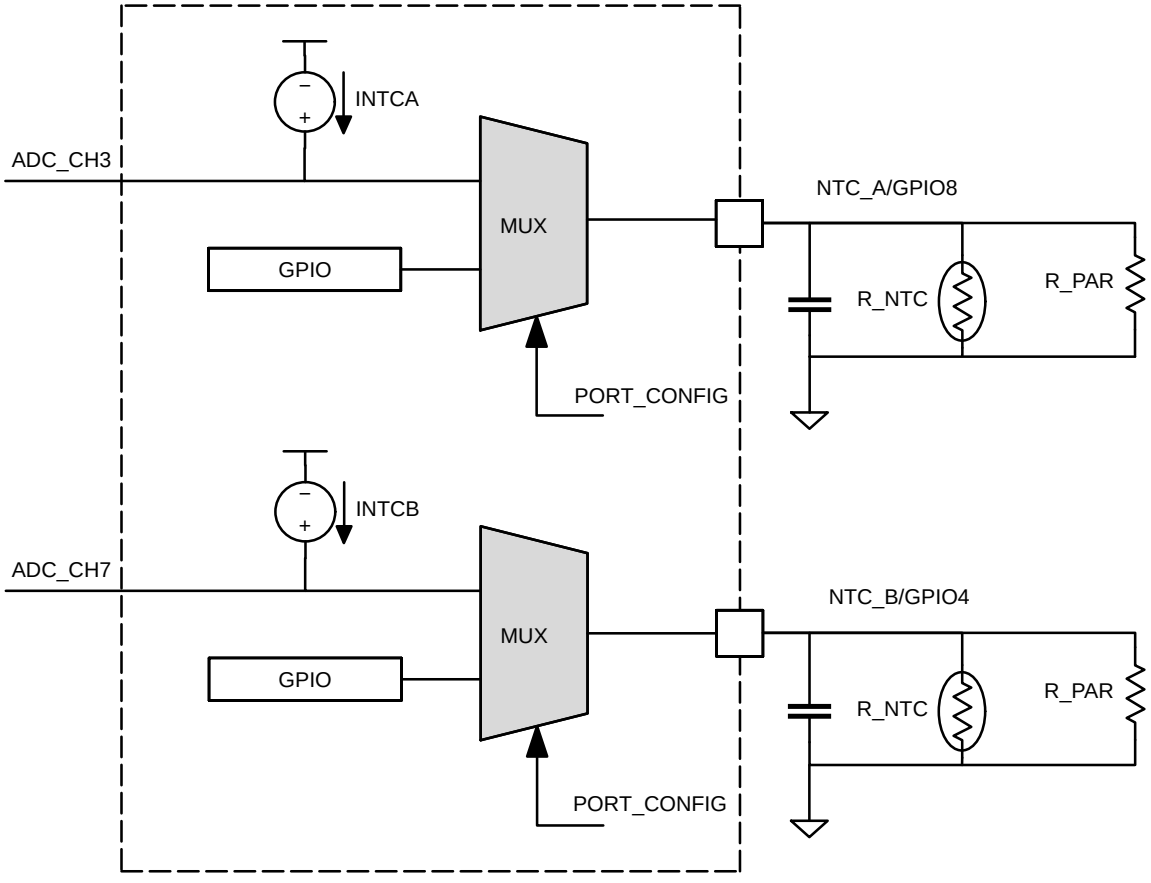


Figure 9. External NTC Diagram

BC1.2 Support

The FUSB15200 is capable of emulating and detecting BC1.2 and Divider Mode.

The following modes are supported:

- SDP
- CDP
- DCP
- 2.4 A Divider Mode (Provider only)

The analog circuitry is firmware configurable for the function required by the application and follows the final BC1.2 specification.

I²C

The FUSB15200's four I²C serial interfaces are compatible with Standard, Fast, and Fast Mode Plus I2C bus specifications. The I²C peripheral can be configured for either host or device modes.

Bus Timing

As shown in figure below, for data bits, SDA must be stable while SCL is HIGH. SDA may only transition when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

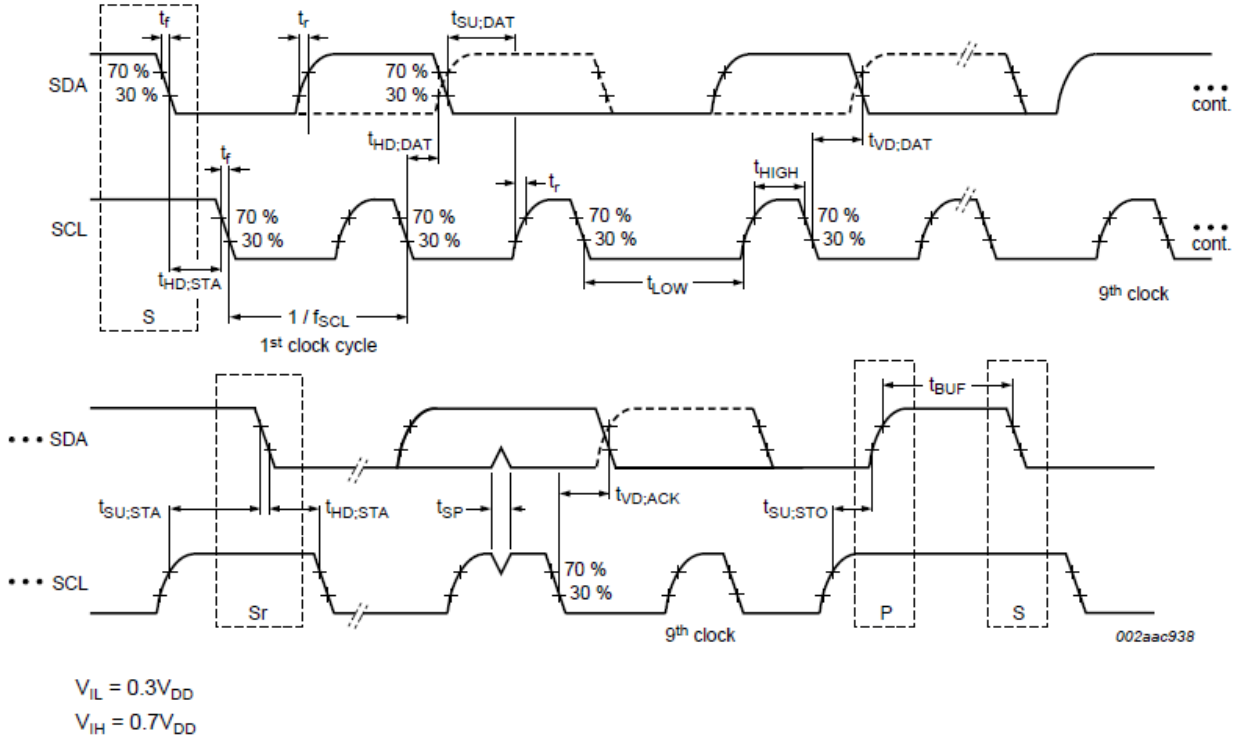


Figure 10. I²C Bus Timing Definition

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH.

A transaction ends with a STOP condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH.

During a read from the FUSB15200, the host issues a Repeated Start after sending a data command and before resending the device address. The Repeated Start is a 1−to−0 transition on SDA while SCL is HIGH.

7. Bus timing referenced from I²C−bus specification Rev. 6 – 4 April 2014

ADC

The FUSB15200 allows for up to 12 signals to be measured and converted using the internal 10−bit ADC. For most applications, this will consist of two VBUS voltages, two NTC temperature channels, two D+/D− BC1.2 and, optionally, two CC1/2 ports. The table below shows the typical FUSB15200 configuration along with the expected settings for the ADC module.

Table 3. ADC CONFIGURATION ADC CHANNEL

ADC Channel	Pin Measurement	Resolution	Range	Full Scale Voltage
0	VBUS_A	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
1	DP_A	4 mV	0 V to 4.096 V	4.096 V
2	DM_A	4 mV	0 V to 4.096 V	4.096 V
3	NTC1 Temperature	1°C	0°C to 160°C	1.28 V
4	HVCC1_A	4 mV	0 V to 4.096 V	4.096 V
5	HVCC2_A	4 mV	0 V to 4.096 V	4.096 V
6	VBUS_B	10 mV	0 V to 10.23 V	1.024 V
		20 mV	0 V to 20.46 V	2.048 V
		40 mV	0 V to 40.92 V	4.096 V
7	DP_B	4 mV	0 V to 4.096 V	4.096 V
8	DM_B	4 mV	0 V to 4.096 V	4.096 V
9	NTC2 Temperature	1°C	0°C to 160°C	1.28 V
10	HVCC1_B	4 mV	0 V to 4.096 V	4.096 V
11	HVCC2_B	4 mV	0 V to 4.096 V	4.096 V

Development Tools

FUSB15200 is supported by a full suite of comprehensive tools including:

- An easy−to−use development board
- Software Development Kit (SDK) including:
  USB PD protocol stacks, shared capacity algorithms, sample code, libraries, and documentation

Specifications References

- Universal Serial Bus Power Delivery specification revision 3.1 Version 1.3, dated January 2022
- Universal Serial Bus Type C Cable and Connection Specification release 2.1, dated May 2021
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- I2C−bus specification Rev. 6 – 4 April 2014

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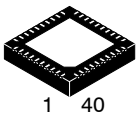

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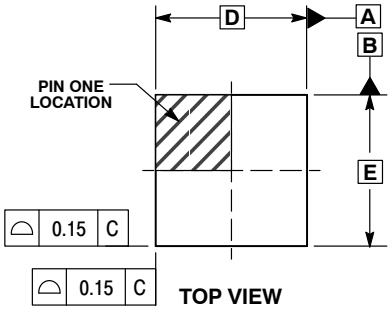
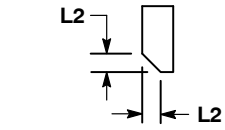
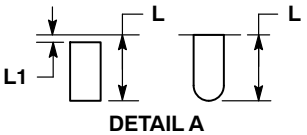
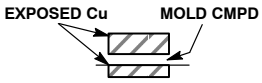
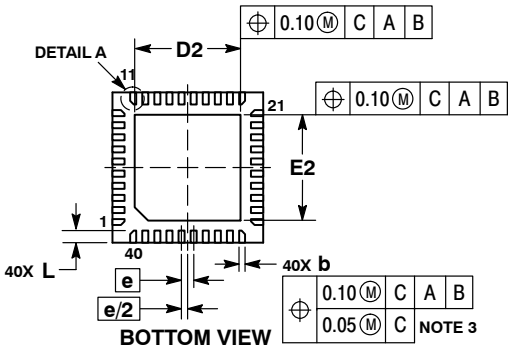


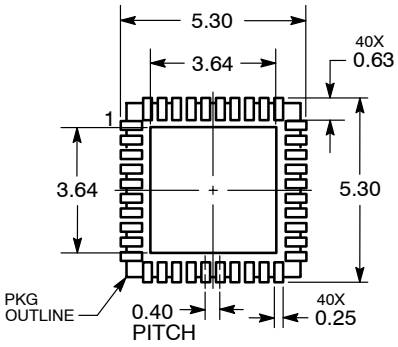








RECOMMENDED SOLDERING FOOTPRINT

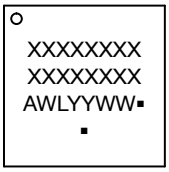


DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.15	0.25
D	5.00 BSC	
D2	3.40	3.60
E	5.00 BSC	
E2	3.40	3.60
e	0.40 BSC	
L	0.30	0.50
L1	---	0.15
L2	0.12 REF	

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**QFN40, 5x5, 0.4P**		**PAGE 1 OF 1**

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