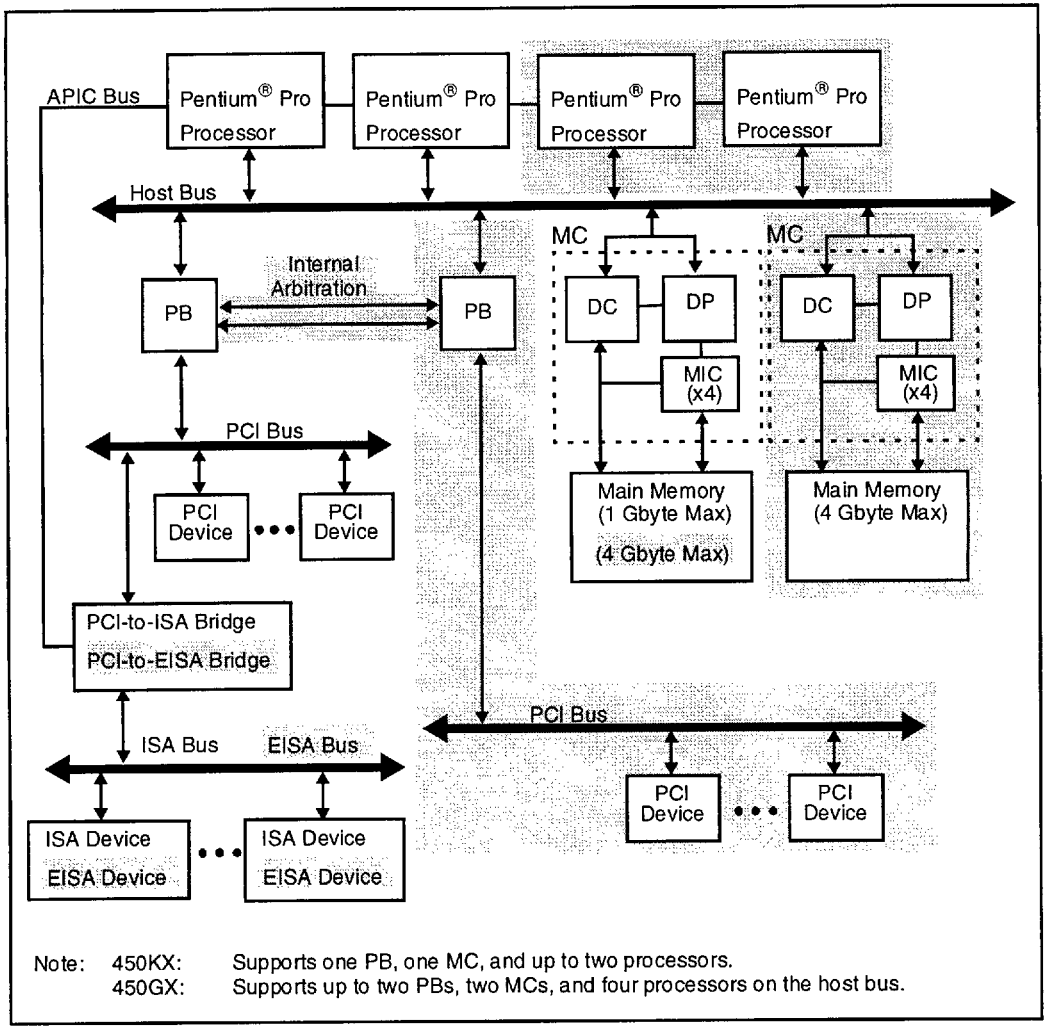
PCIset Product Overview

- PCIset Host Bus Support
  - Supports Pentium® Pro Processor at 60 MHz, and 66 MHz Bus Speeds
  - 64-Bit Data and 36-Bit Address Bus
  - Parity Protection on Control Signals
  - ECC Protection on Host Data Bus (450GX)
  - Dual-Processor Support (450KX)
  - Quad-Processor Support (450GX)
  - Up to Eight Deep In-Order Queue
  - Four Deep Outbound Request Queue
  - Four Cache Line Read and Write Buffers
  - GTL+ Bus Driver Technology
- Host-to-PCI Bridge (PB)
  - Combines Both the Control and Data Path in a Single Chip
  - Internal Bridge Arbiter For Two PBs in a system (450GX)
  - Synchronous PCI Interface
  - 32-bit Address/Data PCI Bus (64-bit Dual Cycle Address Support)
  - Parity Protection on All PCI Bus Signals
  - Four Deep Inbound Request Queue
  - Data Collection/Write Assembly of Line Bursts.
  - Support for 3.3V & 5V PCI Devices
  - Available in 304 Pin QFP or 352 pin BGA
- Memory Controller (MC)
  - 1 GB Maximum Memory (450KX)
  - 4 GBs Maximum Main Memory (per 82453GX)
  - 2-Way interleaved and Non-Interleaved Memory Organizations
  - 4-Way and 2-Way Interleaved, and Non-Interleaved Memory Organizations (450GX)
  - Up to Two MCs in a System (450GX)
  - Supports 3.3V and 5V SIMMs
  - Supports Standard 32- or 36-bit SIMMs or 72-bit DIMMs
  - Supports 4 Mbit, 16 Mbit, and 64 Mbit DRAM Technology
  - Single Bit Error Correction, Double Bit and Nibble Error Detection
  - Memory Array Power Management
  - Recovers DRAM Memory Behind Programmable Memory Gaps
  - Read Page Hit 8-1-1-1 (at 66 MHz, 60 ns DRAM)
  - Read Page Miss 11-1-1-1 (66 MHz, 60 ns DRAM)
  - Read Page Miss + Precharge 14-1-1-1 (66 MHz, 60 ns DRAM)
  - Available in 208-Pin QFP for the DC; 240-Pin QFP or 256-Pin BGA for the DP; 144-Pin QFP for the MIC
- On-Chip Digital PLL (Both PB and MC)
- Test Support (JTAG) (Both PB and MC)

The Intel 450KX/GX PCIsets provide a high-performance system solution for Pentium® Pro processor-based PCI systems by combining high integration, high performance technology with a scalable architecture that is capable of high throughput for up to four Pentium Pro processors. Scalability provides a wide range of system solutions from cost-effective uniprocessor systems to high-end multiprocessor systems without sacrificing performance. For systems requiring extensive I/O (e.g., file servers), a second PB can be easily added providing two high-performance PCI bus structures. The flexibility of the memory controller permits easy expansion from a simple non-interleaved organization to a 2-way or 4-way interleaved organization to increase performance. Extended error checking and logging, ECC, and the ability to build in redundancy (e.g, multiple processors and dual PCI bridges) provides a comprehensive solution for systems requiring high reliability.

The PCIset may contain design defects or errors known as errata. Current characterized errata are available upon request.

This document describes both the Intel 450KX and 450GX PCIsets. Unshaded areas apply to both the PCIsets. Shaded areas, like this one, describe the 450GX operations that differ from the 450KX.



Note: 450KX: Supports one PB, one MC, and up to two processors.
450GX: Supports up to two PBs, two MCs, and four processors on the host bus.

Figure 1. 450KX/GX Simplified System Block Diagram

1.0 INTEL 450KX PCISET

The 450KX desktop PCIset consists of the 82454KX PCI Bridge (PB) and the Memory Controller (MC). The MC consists of the 82453KX DRAM Controller (DC), the 82452KX Data Path (DP), and four 82451KX Memory Interface Components (MIC). The system configuration using the Intel 450KX PCIset supports one PB, one MC and up to two Pentium Pro processors (Figure 1). An ISA subsystem is also located below the PB. For Pentium Pro processor bus error detection, the 450KX generates and checks parity over the address and request/response signal lines. This feature can be enabled/disabled during system configuration.

KX PCI Bridge (PB)

The PB is a single-chip host-to-PCI Bridge. A rich set of CPU-to-PCI and PCI-to-CPU bus transaction translations optimize bus bandwidth and improve system performance. All ISA and EISA regions are supported. Three programmable memory gaps can be created—a PCI Frame Buffer Region with specialized frame buffer attributes and two general-purpose memory gaps (called the Memory Gap Region and the High Memory Gap Region).

The PB takes advantage of the Pentium Pro processor ratio clocking scheme to assure modularity now and upgradability in the future. The PB has a synchronous interface to the Pentium Pro processor bus and supports a derived clock for the synchronous PCI interface. The PB derives either a 30 or 33 MHz PCI clock output from the Pentium Pro processor bus clock. The PB PCI signals are 5 volt tolerant and can be used with either 5 volt or 3.3 volt PCI devices.

KX Memory Controller (MC)

The combined MC (DC, DP, and four MICs) act as one physical load on the Pentium Pro processor bus. The DC provides control for the DRAM memory subsystem, the DP provides the data path, and the four MICs are used to interface the MC datapath with the DRAM memory subsystem.

The memory configuration can be either 2-way interleaved or non-interleaved. Both single-sided and double-sided SIMMs are supported. DRAM technologies up to 64 Mbits at speeds of 50ns, 60ns, and 70ns can be used. Asymmetric DRAM is supported up to two bits of asymmetry (e.g., 12 row address lines and 10 column address lines). The maximum memory size is 1 Gbyte for the 2-way interleaved configuration and 512 Mbytes for the non-interleaved configuration using 16 Mbit technology. In addition to these memory configurations, the MC provides data integrity features including ECC in the memory array. These features, as well as a set of error reporting mechanisms, can be selected via configuration of the MC. Each interleave provides a 64-bit data path to main memory (72-bits including ECC).

The MC is PC compatible. All ISA and EISA regions are decoded and shadowed based on programmable configurations. Regions above 1 Mbyte with size 1 Mbyte or larger that are not mapped to memory may be reclaimed by setting the appropriate configuration in the MC. Three programmable memory gaps can be created and are called the *Low Memory Gap Region*, the *Memory Gap Region* and the *High Memory Gap Region*.

2.0 INTEL 450GX PCISET

The Intel 450GX PCIset includes the features discussed for the Intel 450KX PCIset and provides the additional capabilities described in this section. This PCIset consists of the 82454GX PCI Bridge (PB) and the Memory Controller (MC). The MC for the 450GX consists of the 82453GX DRAM Controller (DC), the 82452GX Data Path (DP), and four 82451GX Memory Interface Controllers (MIC). The 450GX permits two PBs and two MCs in a system. In addition to parity support on the host bus described for the 450KX, the 450GX generates and checks ECC over the host data lines. This feature can be enabled/disabled during configuration.

One aspect of the 450GX is that it can be used as a drop-in replacement for an 450KX design. Additional pins are added in such a way that proper wiring of 450KX test pins (GTLHI, TESTLO, and TESTHI) will allow an 450GX to operate in the same system while functioning exactly as an 450KX.

GX PCI Bridge (PB)

Two 82454GX PBs can be used in a system. Dual PBs provide a modular approach to I/O performance improvements. Compatibility versus speed are addressed with an optional compatibility operating mode to guarantee standard bus compatible operation when needed, and allow bus concurrency when possible.

In a dual PB system, one PB is configured by strapping options at power-up to be the *Compatibility PB*. This PB provides the PC compatible path to Boot ROM and the ISA/EISA bus. The second PB is configured by the strapping options to be the *Auxiliary PB*. The Compatibility PB is the highest priority bridge to ensure a proper response time for ISA bus masters. When two PBs are on the host bus, the Compatibility PB handles arbitration with an internal arbiter.

GX Memory Controller (MC)

The memory configuration can be either 4-way interleaved, 2-way interleaved, or non-interleaved. Both single-sided and double-sided SIMMs are supported. DRAM technologies up to 64Mbit at speeds of 50ns, 60ns, and 70ns can be used. Asymmetric DRAM is supported up to two bits of asymmetry (e.g., 12 row address lines and 10 column address lines). The maximum memory size is 4 Gbytes for the 4-way interleaved configuration, 2 Gbytes for the 2-way interleaved configuration, and 1 Gbyte for the non-interleaved configuration using 64 Mbit technology. The MC provides a 64-bit data path to main memory (72-bits including ECC) for each interleave (288 bits for a 4-way interleave design).

3.0 HOST BUS EFFICIENCY

The Pentium Pro processor bus achieves high bus efficiency by providing support for multiple, pipelined transactions. A single Pentium Pro processor may have up to four transactions outstanding at the same time, and can be configured to support up to eight transactions active on the Pentium Pro processor bus at any one time. The PB and MC support a choice of one or eight active transactions on the Pentium Pro processor system bus at one time (In-Order Queue depth).

The number of transactions that can target a particular bus client is configured separately from the total number of transactions allowed on the bus. Each PB can accept up to four transactions into its Outbound Request Queue that target its associated PCI bus. The PB also contains a four deep Inbound Queue that holds PCI initiated requests directed to the Pentium Pro processor bus. Each MC can accept up to four transactions that target its associated memory space.

Both the PB and MC provide four 32-byte buffers for outbound data and four 32-byte buffers for inbound data. For the PB, the outbound data refers to CPU-to-PCI writes or PCI reads from the CPU bus and inbound data refers to PCI-to-CPU writes or CPU reads from PCI. For the MC outbound data refers to CPU writes to main memory and inbound data refers to CPU reads of main memory.

The maximum data transfer that is supported by the Pentium Pro processor bus is four 64-bit wide transfers. This transfer satisfies the 32-byte cache line size of the Pentium Pro processor interface. The Pentium Pro processor supports operations that are not completed in the order in which they were requested. This 'deferred response' capability allows the Pentium Pro processor bus to be freed to execute other requests while waiting for the response from a request to a device with relatively long latency. Note that the 450 PCIset does not defer requests to itself, nor does it (the PB) allow its transactions to be deferred.

4.0 SYSTEM MEMORY MAP

A Pentium Pro processor system can have up to 64 Gbytes of addressable memory. The lower 1 Mbyte of this memory address space is divided into regions that can be individually controlled with programmable attributes such as disable, read/write, write only, or read only.

At the highest level, the address space is divided into four conceptual regions as shown in Figure 2. These are the 0–1 Mbyte Compatibility Area, the 1 Mbyte to 16 Mbyte Extended Memory region used by ISA, the 16 Mbyte to 4 Gbyte Extended Memory region used by EISA, and the 4 Gbyte to 64 Gbyte Extended Memory introduced by 36 bit addressing. Each of the regions are divided into subregions, as described in the following sections.

For the 450GX, up to two MCs can be placed in the address space spanned by these regions. In a PC architecture, the only restrictions on memory placement are that there be memory starting at address 0 and that there be enough memory to operate a system. The MCs in a system need not have contiguous address spaces. Each MC also supports two memory ranges for the memory connected to the MC, by providing a high memory gap range register that defines the space between the two ranges of memory. This range effectively defines the top address for the lower memory range and the base address for the upper memory range.

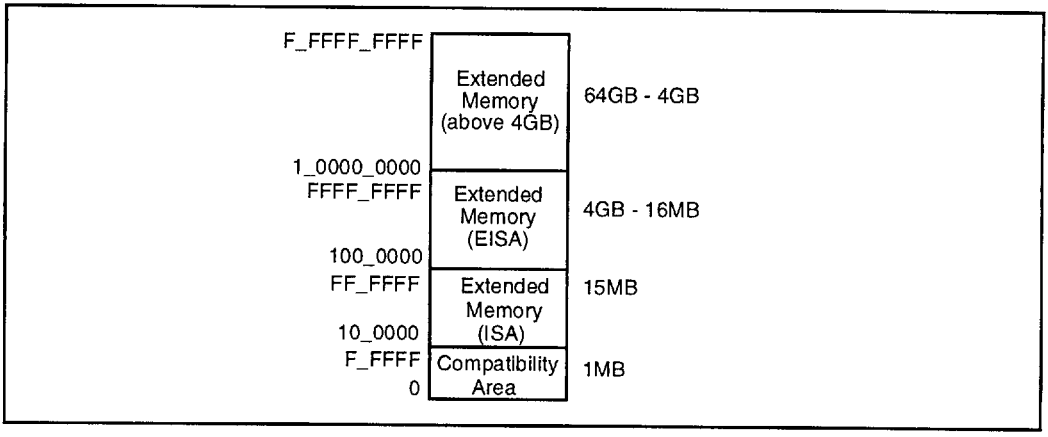


Figure 2. Pentium Pro Processor Memory Address Space.

4.1 Compatibility Area

The first region of memory is called the Compatibility Area because it was defined for early PCs. This region is divided into 5 subregions, as shown in Figure 3.

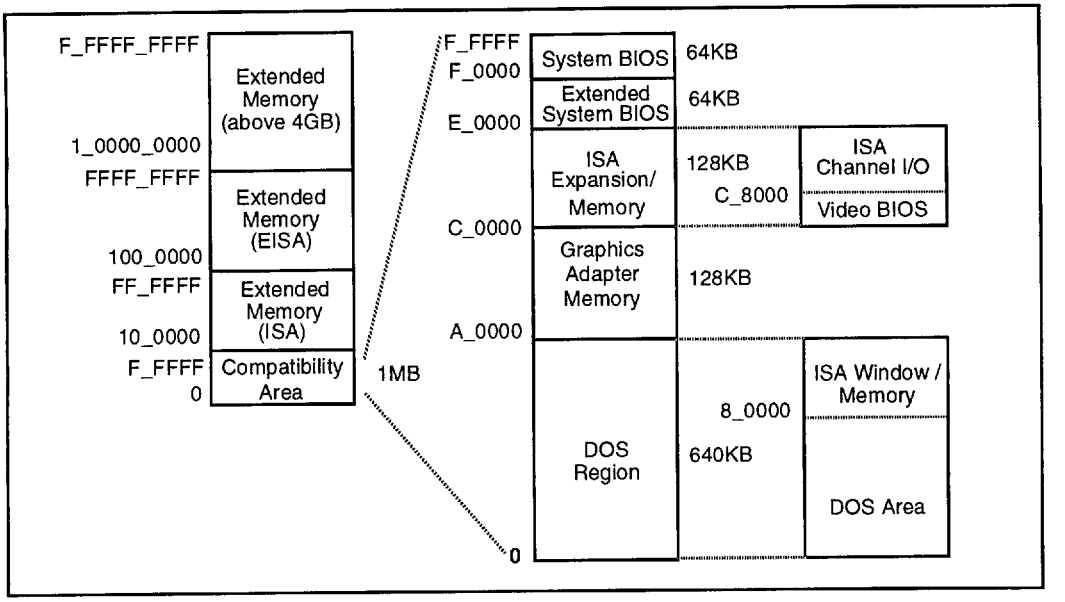


Figure 3. Expanded View of Compatibility Area.

DOS Region

The DOS Region is 640 Kbytes in the address range 00000h–9FFFFh. DOS applications execute here. This region is further divided into two parts. The 512 Kbyte area at 00000h–7FFFFh is always mapped to memory on the Pentium Pro processor bus (enabled in the MC), while the 128 Kbyte area from 80000h–9FFFFh can be mapped to memory on the Pentium Pro processor bus or PCI memory (enabled in the PB). This region can be programmed as disabled, read/write, write only, or read only.

Graphics Adapter Memory

The 128 Kbyte Graphics Adapter Memory region at A0000h–BFFFFh is normally mapped to a video device on the PCI bus. Typically, this is a VGA controller. If there are no graphics compatible devices, this region can be used as system memory. The range A0000h–AFFFFh (64 Kbytes) is also the default region for SMM space. The SMM region can be re-mapped by programming the SMM Range Register in the PB and MC.

ISA Expansion

The 128 Kbyte ISA expansion region is divided into eight 16 Kbyte blocks that can be independently programmed as disabled, read/write, write only, or read only providing the capability to "shadow" these regions in main memory. Typically, these blocks are mapped through the PB to ISA space.

Historically, the 32 Kbyte region from C0000h–C7FFFh has contained the video BIOS located on a video card in the ISA Expansion Area. However, in the high integration portable and desktop market video BIOS is more likely to be located in the Extended System BIOS or System BIOS regions that start at E0000h.

The 96 Kbyte area from C8000h–DFFFFh has usually been made available to expand memory windows in 16 Kbyte blocks, depending on the requirements of other channel devices in the corresponding ISA space. More recently, PCMCIA devices for the portable market have been assigned within this region.

This region could also be used as System Management Mode (SMM) memory.

Extended System BIOS

This 64 Kbyte region from E0000h–EFFFFh is divided into four 16 Kbyte blocks and may be mapped either to the memory controller or the PCI bridge. This region can be programmed as disabled, read/write, write only, or read only, providing the capability to shadow these regions in main memory. Typically, this area is used for RAM or ROM.

System BIOS

The 64 Kbyte region from F0000h–FFFFFh is treated as a single block. After power-on reset, the PB (Compatibility PB in an 450GX dual PB system) has this area R/W enabled to respond to fetches during system initialization. The MC(s) and Auxiliary PBs (450GX PCIset) have this area R/W disabled. This region can be programmed as disabled, read/write, write only, or read only, providing the capability to shadow these regions in main memory.

4.2 Extended Memory (ISA)

The ISA Extended Memory region in Figure 4 covers 15 Mbytes ranging from 100000h–FFFFFFh. There are three programmable ranges that may be mapped to the ISA Extended Memory region of the MC—the Low Memory Gap range, the Memory Gap Range, and the High memory Gap Range. Memory in these ranges, that would normally be "lost", is recovered by the MC by extending the effective top of system memory, if reclaiming is enabled. The Memory Gap Range and High Memory Gap range are also programmable ranges in the PB. The PB also has a programmable PCI Frame Buffer Range.

Low Memory Gap Range (MC Only)

The Low Memory Gap range can start on any 1 Mbyte boundary in the ISA or EISA Extended Memory region, and can be 1, 2, 4, 8, 16, or 32 Mbytes. This region defines a "hole" in system DRAM space where accesses can be directed to the PCI bus. The Low Memory Gap Range is used by ISA devices such as LAN or linear frame buffers which are mapped into the ISA Extended region, or by any EISA or PCI device. The Low Memory Gap Range must reside at the lowest address of the three memory gaps, if it is enabled.

PCI Frame Buffer Range (PB Only)

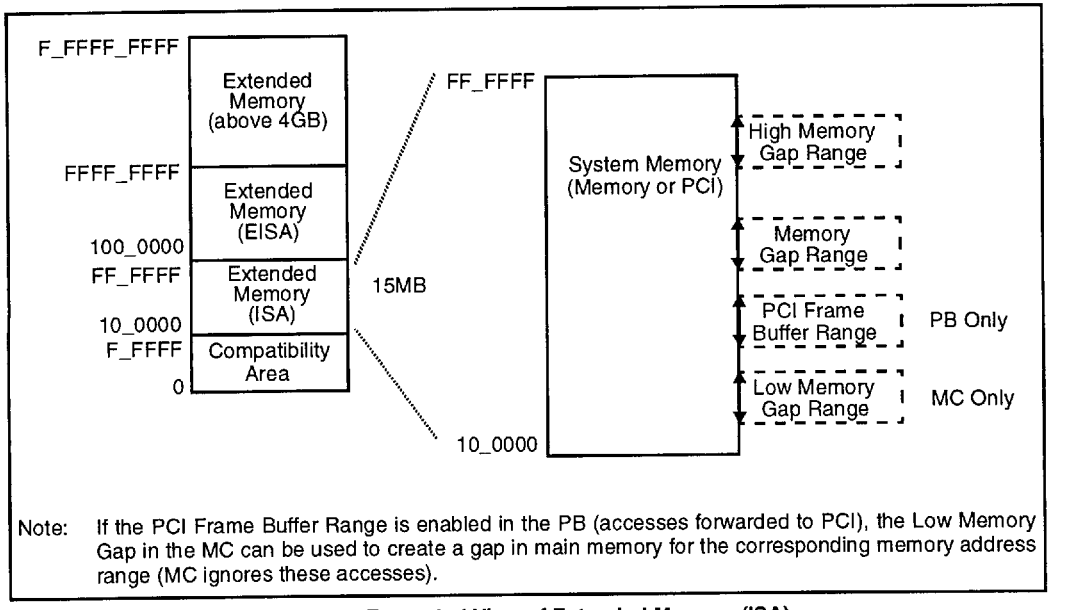
The PCI Frame Buffer range can start on any 1 Mbyte boundary in either the ISA Extended Memory region or the EISA Extended Memory Region, and can be 1, 2, 4, 8, 16,or 32 Mbytes.

Memory Gap Range (MC and PB)

The Memory Gap Range can start on any 1 Mbyte boundary, above 1 Mbyte, and can 1, 2, 4, 8, 16, or 32 Mbytes. This region defines a "hole" in system DRAM space where accesses can be directed to the PCI bus. The Memory Gap Range is used by ISA devices such as LAN or linear frame buffers which are mapped into the ISA Extended region, or by any EISA or PCI device. The Memory Gap Range must reside above the Low Memory Gap Range and below the High Memory Gap Range, if it is enabled.

High Memory Gap Range (MC and PB)

The High Memory Space Gap can start on any 1 Mbyte boundary in either the ISA Extended Memory region, EISA Extended Memory Region, or the Extended Memory Region above 4Gbyte, and can extend up to 64 Gigabytes. It is defined by specifying a start and end address, both on 1 Mbyte boundaries. The High Memory Gap Range is provided as additional support for memory mapped I/O. The High Memory Gap Range must reside at the highest address of the three memory gap range registers, if it is enabled.

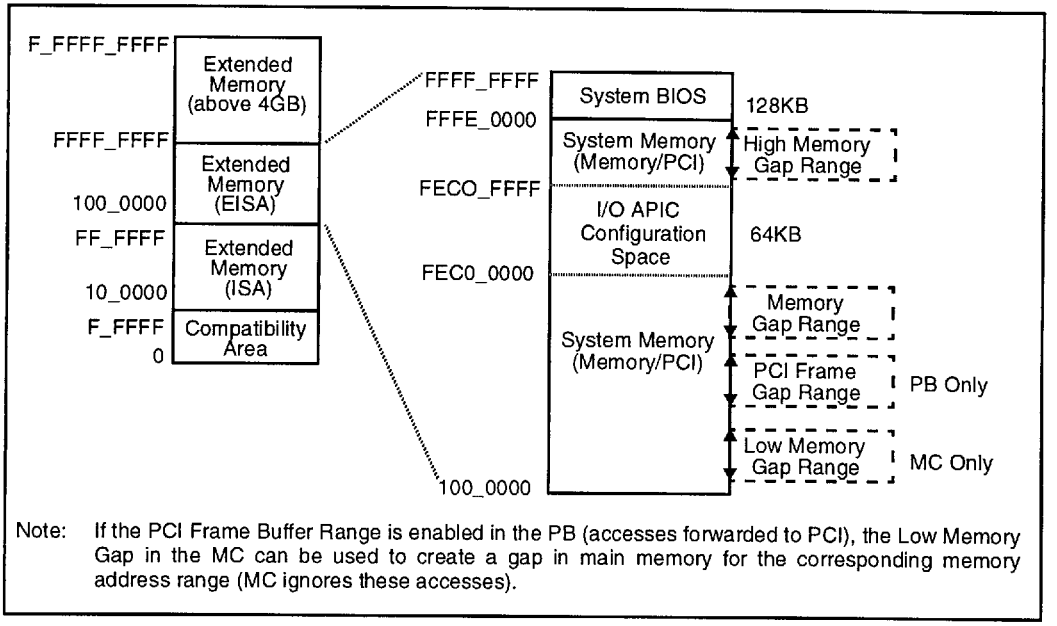


Note: If the PCI Frame Buffer Range is enabled in the PB (accesses forwarded to PCI), the Low Memory Gap in the MC can be used to create a gap in main memory for the corresponding memory address range (MC ignores these accesses).

Figure 4. Expanded View of Extended Memory (ISA)

4.3 Extended Memory (EISA)

The EISA Extended Memory region covers the 16 Mbyte to 4 Gbyte range (1000000h–FFFFFFFFh). This region is divided into three sections—System BIOS, APIC configuration space, and system memory. The APIC configuration space is contained within the system memory region (Figure 5). The Low Memory Gap, Memory Gap, and High Memory Gap ranges can also be enabled in this region.



Note: If the PCI Frame Buffer Range is enabled in the PB (accesses forwarded to PCI), the Low Memory Gap in the MC can be used to create a gap in main memory for the corresponding memory address range (MC ignores these accesses).

Figure 5. Expanded View of Extended Memory (EISA).

System BIOS

The top 2 Mbytes of the EISA Extended Memory region is used for System BIOS (High BIOS). This is where the Pentium Pro processor begins execution after reset. If the PCI bus is bridged to an ISA bus, this region is aliased to the top 128 Kbyte of the ISA Extended Memory range.

The actual address space required for system BIOS is less than 2 Mbytes. However, the minimum Pentium Pro processor MTTR range for this region is 2 Mbytes. This establishes the minimum size for this gap. The MC supports enabling or disabling this region for access to the MC memory via the HBIOSR Register.

I/O APIC Configuration Space

The FEC00000h (4GB minus 20 MB) to FEC0FFFFh range is reserved for APIC configuration space which includes the default I/O APIC configuration space. Note that there is no I/O APIC unit in either the MC or PB. The default Local APIC configuration space is FEE00000h–FEE00FFFh.

Pentium Pro processor accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the Pentium Pro processor. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each Pentium Pro processor should be relocated to the FEC00000h (4GB minus 20 MB) to FEC0FFFFh range so that one MTRR can be programmed to 64 Kbyte for the Local and I/O APICs.

I/O APIC units (there should be at least one for each I/O subsystem) are located beginning at the default base address FEC00000h. The first I/O APIC (unit #0) is at FEC00000h. Each I/O APIC unit is located at FEC0x000h where x is I/O APIC unit 0 through F.

The address range between the APIC Configuration space and the High BIOS (FED00000h–FFDFFFFFh) is always mapped to local memory unless the range is above top of physical memory or The High BIOS and APIC Range are disabled in the PB and the range falls within a memory gap range. The MC supports enabling or disabling this region for access to the MC memory via the I/O APIC Range Register.

4.4 Extended Memory (above 4 Gbytes)

The Extended Memory region is from 4 Gbyte to 64 Gbyte (100000000h–FFFFFFFFFh). The PB and MC can be mapped into this range. The Memory Gap Range and High Memory Gap Range are both available for use within the Extended memory region (above 4 Gbyte).

4.5 System Management Mode (SMM)

A Pentium Pro processor asserts SMMEM# in its Request Phase if it is operating in System Management Mode. SM code resides in SM memory space. SM memory can overlap with memory residing on the Pentium Pro processor bus or memory normally residing on the PCI bus. The MC and PB determine where SM memory space is located through the value programmed in their respective SMM Range Registers.

5.0 I/O SPACE (PB ONLY)

The PB optionally supports ISA expansion aliasing (Figure 6). When ISA expansion aliasing is enabled, the ranges designated as I/O Expansion are internally aliased to the 100–3FFh range before the I/O Space Range registers are checked. Note that all devices on the Pentium Pro processor bus that are mapped into I/O space must have I/O aliasing consistently enabled/disabled.

For the Intel 450GX PCIset, the PB allows I/O addresses to be mapped to the Pentium Pro processor bus or through designated bridges in a multi bridge system. Two I/O Space Range registers allow the PB to decode two I/O address ranges. If the address range is enabled, transactions targeting that range are forwarded to the PCI bus. If the address range is disabled, the transaction is ignored.

6.0 MEMORY MAPPED I/O

The PB allows memory addresses to be mapped to the host bus, or for the 450GX PCIset, through the other bridge in a dual PB system. Memory mapped I/O devices can be located anywhere in the 64 Gbyte address space. The Frame Buffer Range allows the PB to decode memory mapped I/O space extending up to 4 Gbyte. The Memory Space Gap and High Memory Gap registers allow the PB to decode two address ranges extending up to 64 Gbytes.

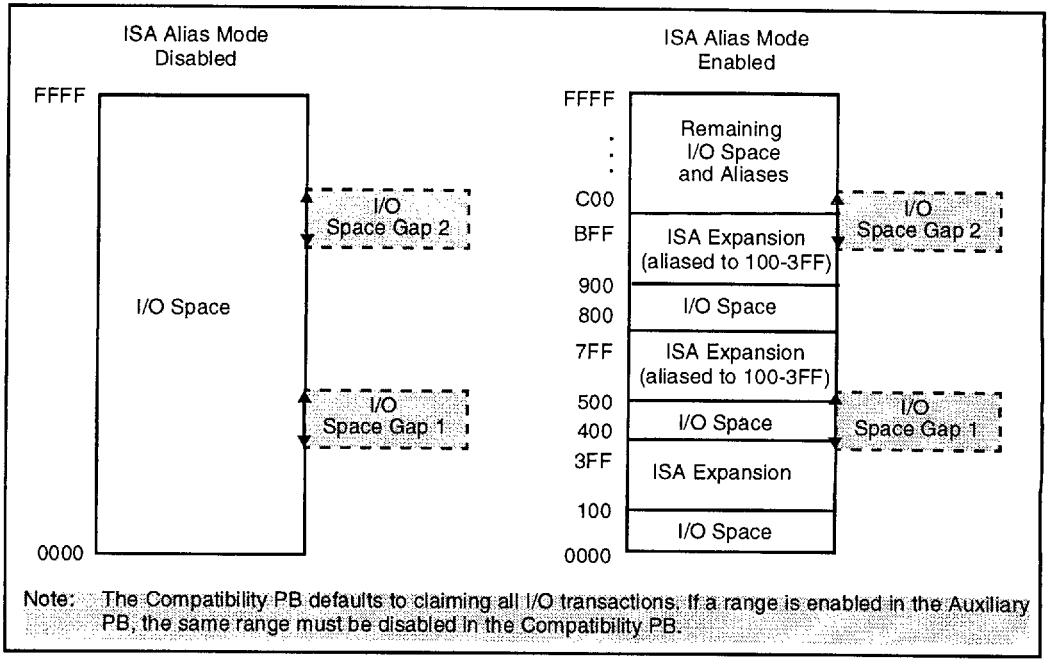


Figure 6. View of I/O Space