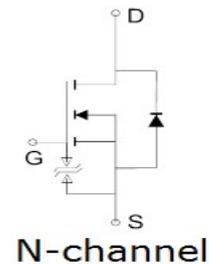
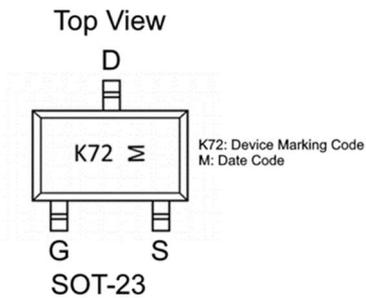


General Description

The FX2N7002KMFH-06S3G is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits and low in-line power loss are needed in a very small outline surface mount package.

PIN Configuration



Features

- $R_{DS(ON)} \leq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 4\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 4.5\Omega @ V_{GS}=3V$
- ESD Protection HBM >2KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

Applications

- Power Management in Note book
- Portable Equipment
- Load Switch
- Battery Powered System
- DSC

Absolute Maximum Ratings(TA=25oC Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain	$T_A=25^\circ C$	I_D	A
	$T_A=70^\circ C$	I_D	
Pulsed Drain Current	I_{DM}	1.1	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	W
	$T_A=70^\circ C$	P_D	
Operating Junction Temperature	T_J	-55 to 150	$^\circ C$
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	350	$^\circ C/W$

* The device mounted on 1in² FR4 board with 2 oz copper

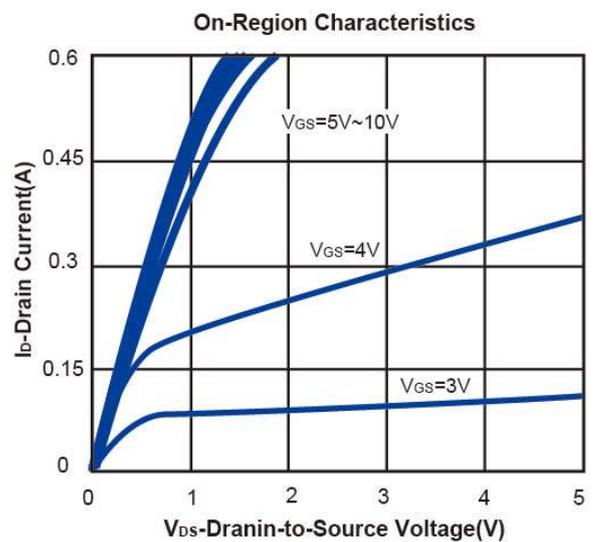
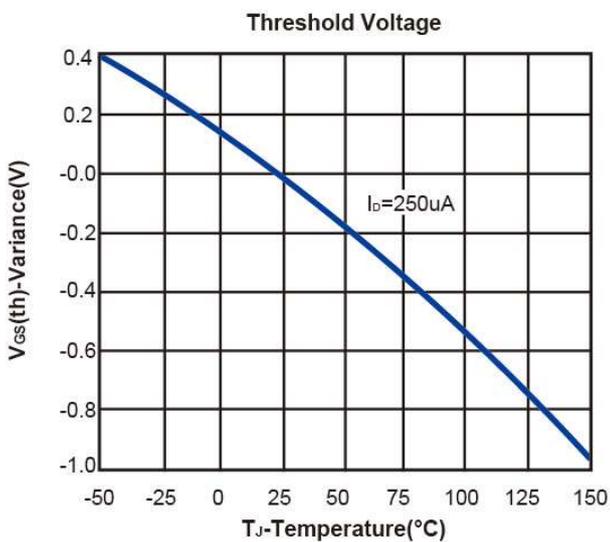
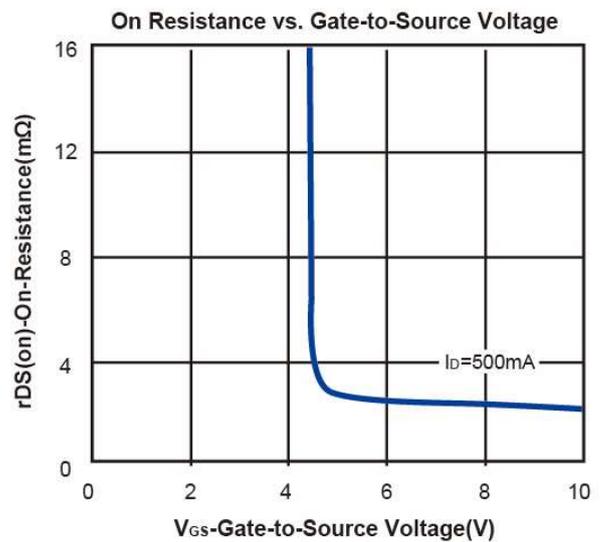
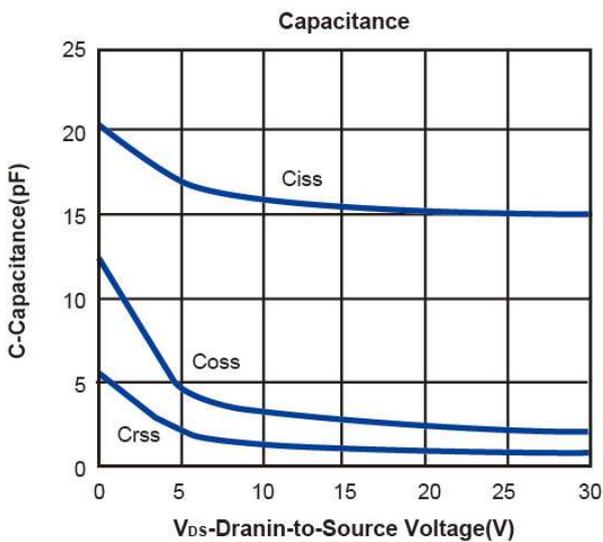
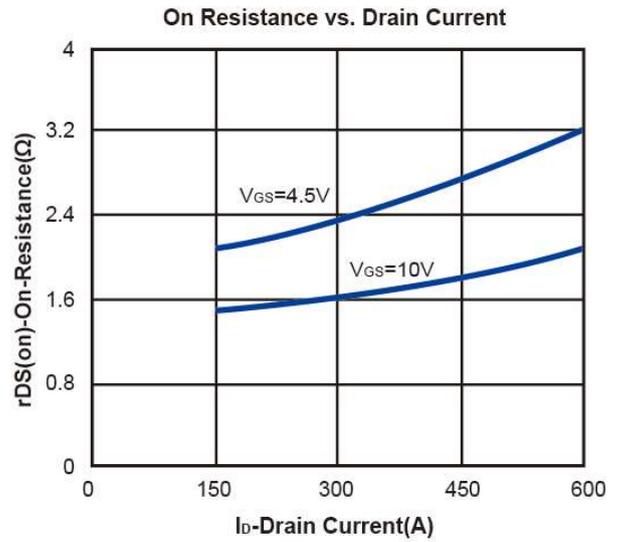
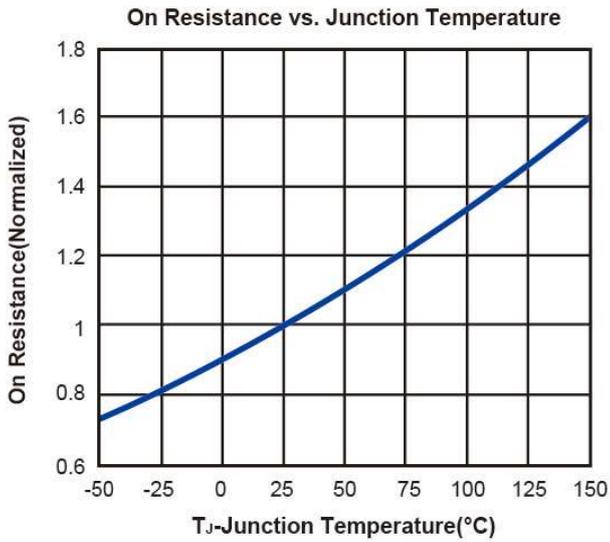
Electrical Characteristics (TA =25 °C Unless Otherwise Specified)

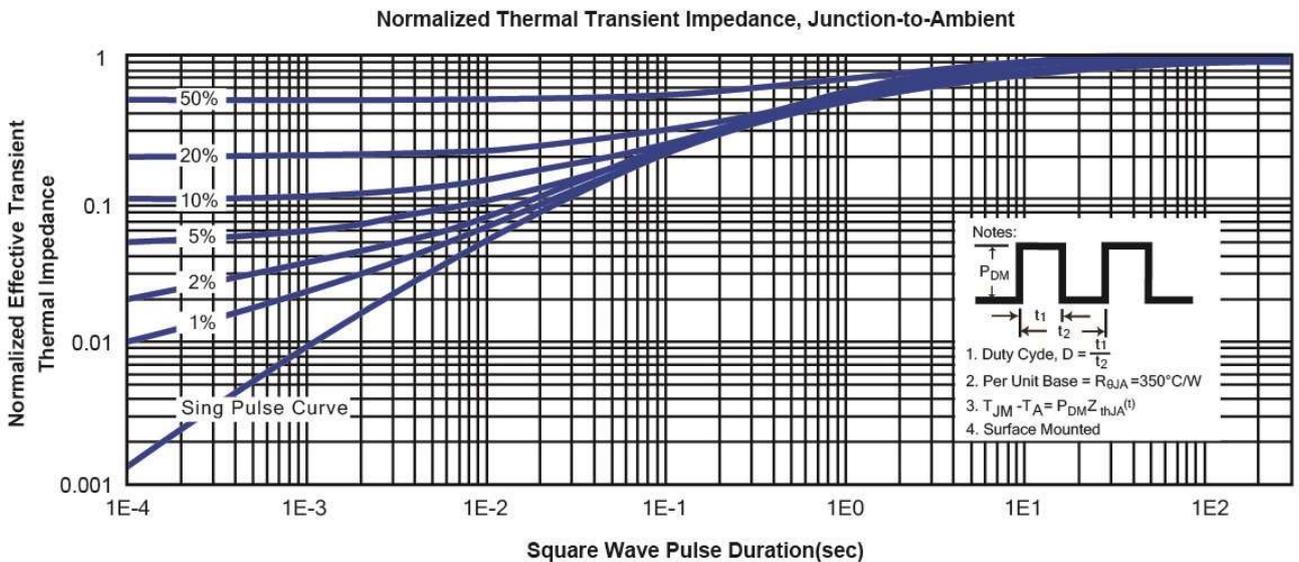
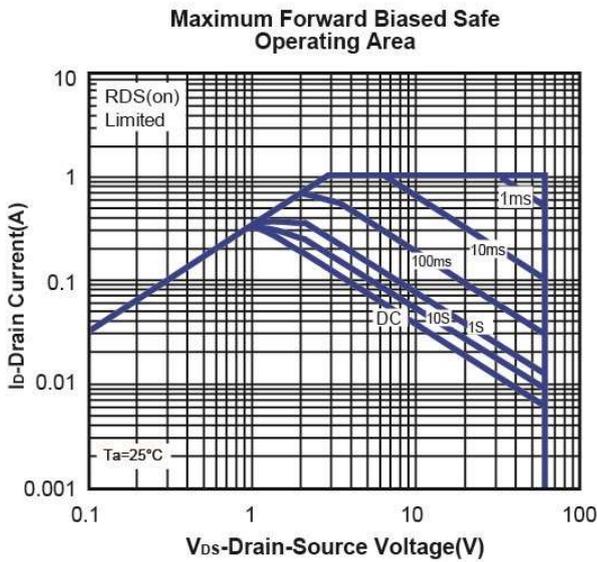
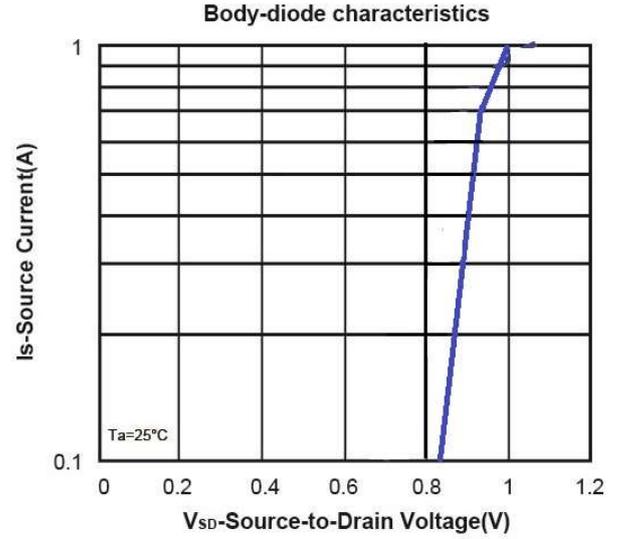
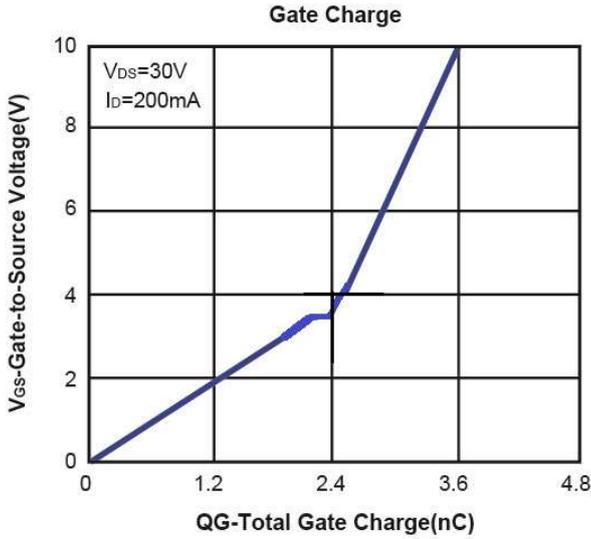
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0, I _D =10uA	60			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1		2.5	V
I _{GSS}	Gate Body Leakage	V _{GS} = ±20V, V _{DS} =0V			±10	uA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V			1	uA
R _{DS(on)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =500mA		1.8	3	Ω
		V _{GS} =4.5V, I _D =200mA		2.3	4	
		V _{GS} =3V, I _D =10mA		3.8	4.5	
V _{SD}	Diode Forward Voltage	I _S =200mA, V _{GS} =0V		0.82	1.3	V
Dynamic						
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =10V, I _D =200mA		3.7		nC
Q _g	Total Gate Charge	V _{DS} =30V, V _{GS} =4.5V, I _D =200mA		1.4		
Q _{gs}	Gate-Source Charge			2		
Q _{gd}	Gate-Drain Charge			0.2		
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz		15		pF
C _{oss}	Output Capacitance			2		
C _{rss}	Reverse Transfer Capacitance			1		
t _{d(on)}	Turn-On Delay Time	V _{DS} =30V, R _L =150Ω V _{GS} =10V, R _{GS} =10Ω I _D =200mA		3.7		Ns
t _r	Turn-On Rise Time			21.7		
t _{d(off)}	Turn-Off Delay Time			5.9		
t _f	Turn-Off Fall Time			21.4		

Notes : a. Pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

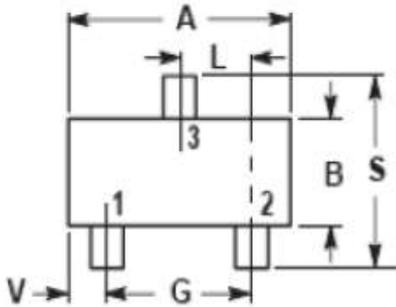
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

Typical Characteristics (T_J = 25 °C Noted)



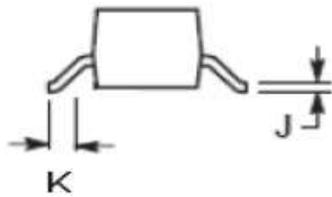
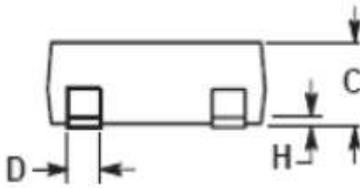


Package Outline Dimensions



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.5
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.007	—	0.018	—
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

Small SOT-23 Package

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