Ordering number:EN4888

FX605

P-Channel Silicon MOSFET

Ultrahigh-Speed Switching Applications

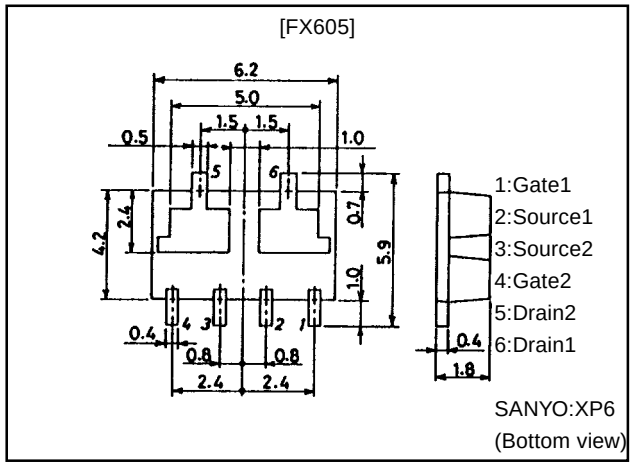
Features

- Composite type composed of two low ON-resistance P-channel MOSFET chips for ultrahigh-speed switching and low-voltage drive.
- Facilitates high-density mounting.
- The FX605 is formed with two chips, each being equivalent to the 2SJ190, placed in one package.
- Matched pair characteristics.

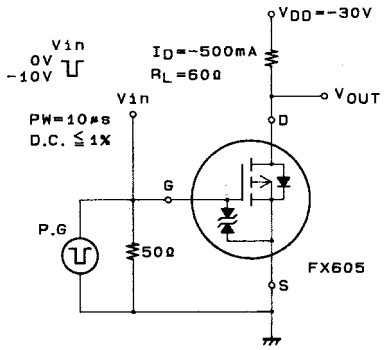
Package Dimensions

unit:mm

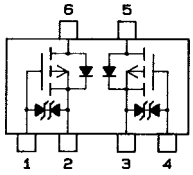
2120



Switching Time Test CIrcuit



Electrical Connection



1:Gate1
2:Source1
3:Source2
4:Gate2
5:Drain2
6:Drain1

(Top view)

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		–60	V
Gate-to-Source Voltage	V_{GSS}		±15	V
Drain Current (DC)	I_D		–1	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	–4	A
Allowable Power Dissipation	P_D	Tc=25˚C, 1unit	6	W
	P_D	Mounted on ceramic board (750mm²×0.8mm) 1unit	1.5	W
Total Dissipation	P_T	Mounted on ceramic board (750mm²×0.8mm)	2	W
Channel Temperature	Tch		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

- Marking:605

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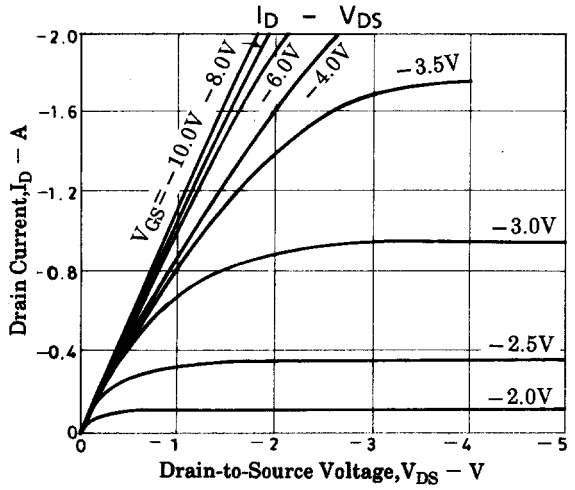
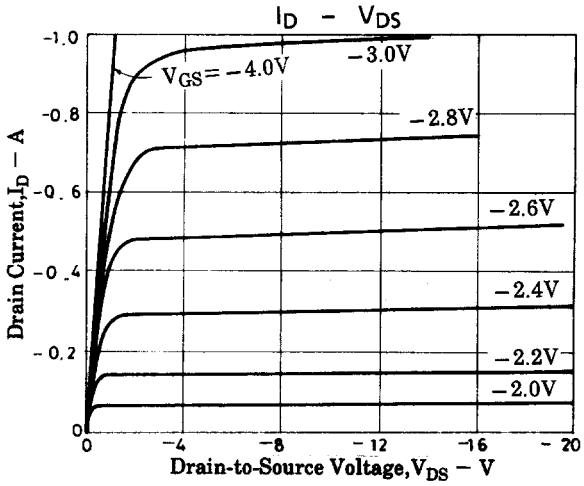
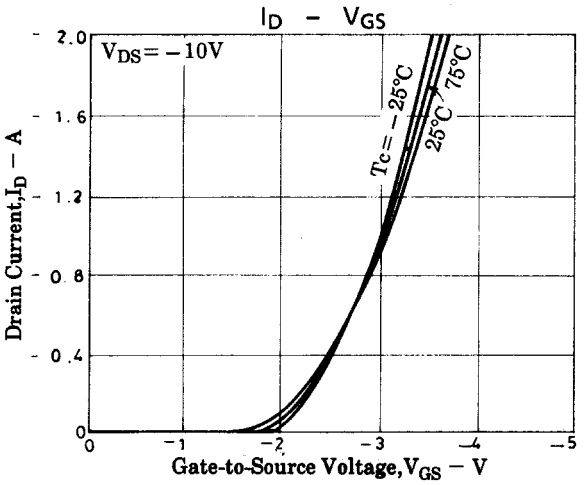
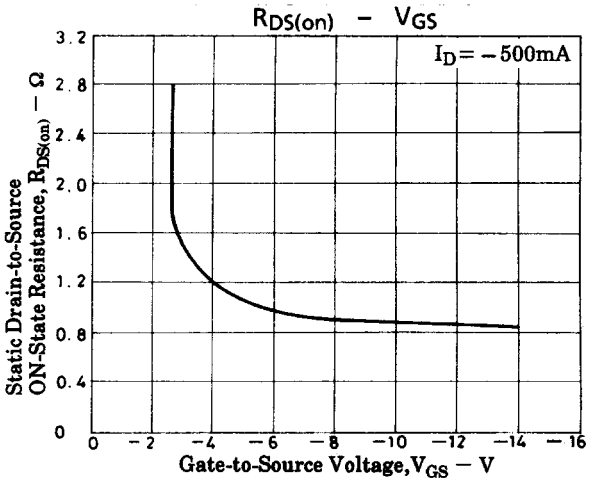
Electrical Characteristics at Ta = 25˚C

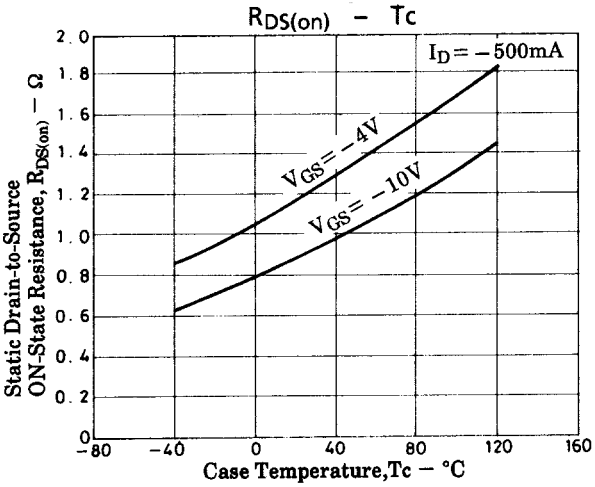
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
D-S Breakdown Voltage	$V_{(BR)DSS}$	I_D=–1mA, V_{GS}=0	–60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=–60V, V_{GS}=0			–100	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±12, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=–10V, I_D=–1mA	–1.0		–2.0	V
Forward Transfer Admittance	$\|Y_{fs}\|$	V_{DS}=–10V, I_D=–500mA	0.6	1.0		S
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	I_D=–500mA, V_{GS}=–10V		0.9	1.2	Ω
	$R_{DS(on)}$	I_D=–500mA, V_{GS}=–4V		1.2	1.6	Ω
Input Capacitance	Ciss	V_{DS}=–20V, f=1MHz		160		pF
Output Capacitance	Coss	V_{DS}=–20V, f=1MHz		60		pF
Reverse Transfer Capacitance	Crss	V_{DS}=–20V, f=1MHz		10		pF
Turn-ON Delay Time	$t_{d(on)}$	See Specified Test Circuit		10		ns
Rise Time	t_r	See Specified Test Circuit		13		ns
Turn-OFF Delay Time	$t_{d(off)}$	See Specified Test Circuit		70		ns
Fall Time	t_f	See Specified Test Circuit		30		ns
Diode Forward Voltage	V_{SD}	I_S=–1A, V_{GS}=0		–0.9		V

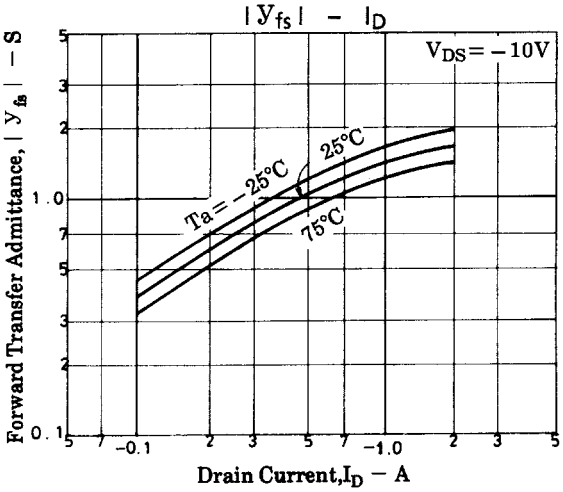

I_D – V_{DS}
Drain Current, I_D – A
Drain-to-Source Voltage, V_{DS} – V
V_{GS} = –10.0V
–8.0V
–6.0V
–4.0V
–3.5V
–3.0V
–2.5V
–2.0V

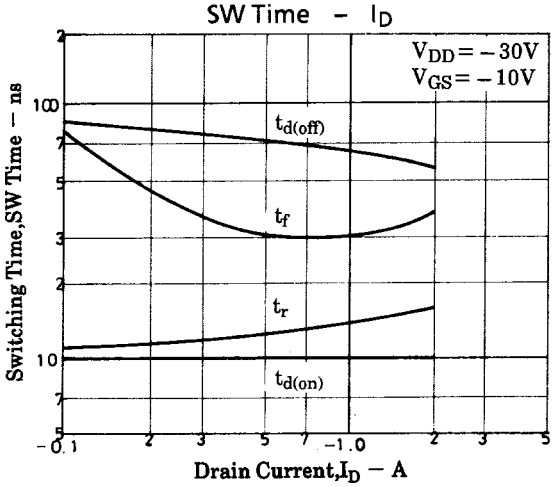

I_D – V_{DS}
Drain Current, I_D – A
Drain-to-Source Voltage, V_{DS} – V
V_{GS} = –4.0V
–3.0V
–2.8V
–2.6V
–2.4V
–2.2V
–2.0V

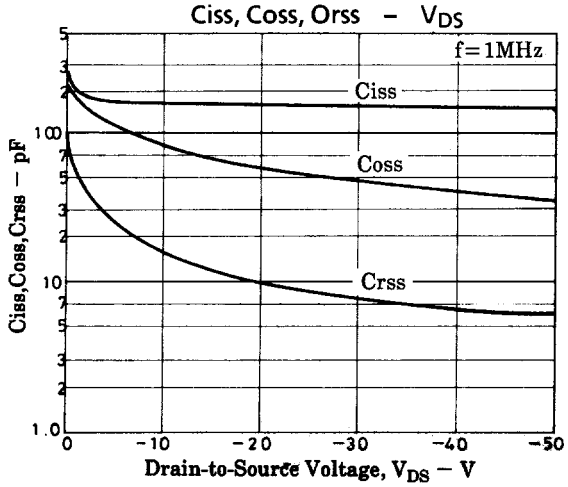

I_D – V_{GS}
V_{DS} = –10V
Drain Current, I_D – A
Gate-to-Source Voltage, V_{GS} – V
Tc = –25°C
25°C
75°C


$R_{DS(on)}$ – V_{GS}
I_D = –500mA
Static Drain-to-Source ON-State Resistance, $R_{DS(on)}$ – Ω
Gate-to-Source Voltage, V_{GS} – V


$R_{DS(on)}$ – Tc
I_D = –500mA
V_{GS} = –4V
V_{GS} = –10V
Static Drain-to-Source ON-State Resistance, $R_{DS(on)}$ – Ω
Case Temperature, Tc – °C


$|y_{fs}|$ – I_D
V_{DS} = –10V
Ta = –25°C
25°C
75°C
Forward Transfer Admittance, $|y_{fs}|$ – S
Drain Current, I_D – A


SW Time – I_D
V_{DD} = –30V
V_{GS} = –10V
$t_{d(off)}$
t_f
t_r
$t_{d(on)}$
Switching Time, SW Time – ns
Drain Current, I_D – A


Ciss, Coss, Orss – V_{DS}
f = 1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, V_{DS} – V