

# FXL2SD106

## Low Voltage Dual Supply 6-Bit SD Interface Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing

### Features

- Bi-directional interface between two levels from 1.1V to 3.6V
- Fully configurable: Inputs and outputs track  $V_{CC}$  level
- Non-preferential power-up; either VCC may be powered-up first
- Outputs remain in 3-state until active  $V_{CC}$  level is reached
- Outputs switch to 3-state if either  $V_{CC}$  is at GND.
- Power off protection
- Bushold on data inputs eliminates the need for SDIO pull-up resistors
- Control input (OE and CLK IN) are referenced to  $V_{CCA}$  voltage
- Packaged in 16-terminal DQFN (2.5mm x 3.5mm)
- Direction control not needed
- 80 Mbps throughput when translating between 1.8V and 2.5V
- ESD protection exceeds:
  - 12kV HBM (B port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 8kV HBM (A port I/O to GND) (per JESD22-A114 & Mil Std 883e 3015.7)
  - 1kV CDM (per ESD STM 5.3)

### General Description

The FXL2SD106 is a configurable dual-voltage-supply translator designed for both uni-directional and bi-directional voltage translation between two logic levels. The device allows translation between voltages as high as 3.6V to as low as 1.1V. The A port tracks the  $V_{CCA}$  level, and the B port tracks the  $V_{CCB}$  level. This allows for bi-directional voltage translation over a variety of voltage levels: 1.2V, 1.5V, 1.8V, 2.5V and 3.3V.

The FXL2SD106 is specifically designed as a translator to interface with the SDIO standard. I/O capacitance is managed to meet the SD maximum capacitance specification. The B side ESD performance allows interface as an external card and the part can handle 80 Mbps throughput when translating between 1.8V and 2.5V.

The device remains in 3-state until both  $V_{CCS}$  reach active levels allowing either  $V_{CC}$  to be powered-up first. Internal power down control circuits place the device in 3-state if either VCC is removed.

The OE input, when low, disables both the A and B ports by placing them in a 3-state condition. The FXL2SD106 is designed so that both control pins (OE and CLK IN) are supplied by  $V_{CCA}$ .

The device senses an input signal on A or B port automatically. The input signal is transferred to the other port.

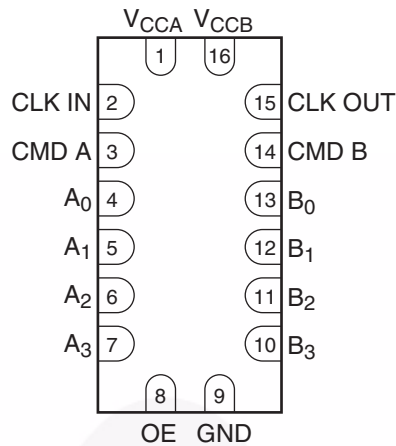
### Ordering Information

Order Number	Package Number	Package Description
FXL2SD106BQX	MLP16E	16-Terminal Depopulated Quad Very-Thin Flat Pack, No Leads (DQFN), JEDEC MO-241, 2.5mm x 3.5mm



All packages are lead free per JEDEC: J-STD-020B standard.

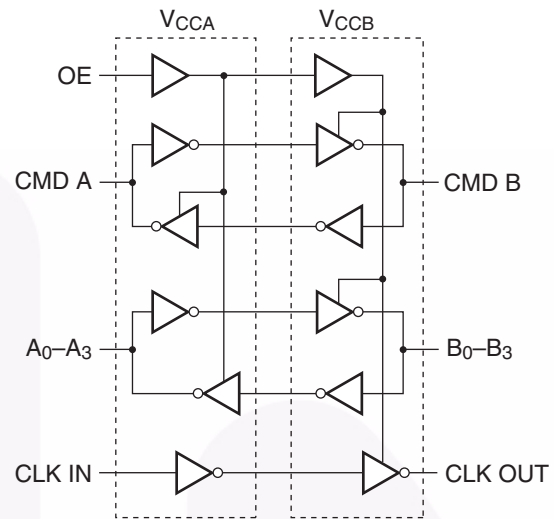
## Connection Diagram



## Pin Description

Number	Name	Description	
1	V <sub>CCA</sub>	A Side Power Supply	
2	CLK IN	A Side Input	
3	CMD A	A Side Inputs or 3-State Outputs	
4-7	A <sub>0</sub> -A <sub>3</sub>		
8	OE		Output Enable Input
9	GND		
10-13	B <sub>3</sub> -B <sub>0</sub>	B Side Inputs or 3-State Outputs	
14	CMD B		
15	CLK OUT	3-State Output	
16	V <sub>CCB</sub>	B Side Power Supply	

## Functional Diagram



## Function Table

Control	Outputs
OE	
L	3-State
H	Normal Operation

H = HIGH Logic Level

L = LOW Logic Level

## Power-Up/Power-Down Sequencing

FXL translators offer an advantage in that either V<sub>cc</sub> may be powered up first. This benefit derives from the chip design. When either V<sub>CC</sub> is at 0 volts, outputs are in a high-impedance state. The control input (OE) is designed to track the V<sub>ccA</sub> supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/power-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is the following:

1. Apply power to the first V<sub>CC</sub>.
2. Apply power to the second V<sub>CC</sub>.
3. Drive the OE input high to enable the device.

The recommended power-down sequence is the following:

1. Drive OE input low to disable the device.
2. Remove power from either V<sub>CC</sub>.
3. Remove power from other V<sub>CC</sub>.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CCA}, V_{CCB}$	Supply Voltage	-0.5V to +4.6V
$V_I$	DC Input Voltage I/O Port A I/O Port B Control Inputs (OE, CLK IN)	-0.5V to +4.6V -0.5V to +4.6V -0.5V to +4.6V
$V_O$	Output Voltage <sup>(1)</sup> Outputs 3-STATE Outputs Active ( $A_n$ , CMD A) Outputs Active ( $B_n$ , CMD B, CLK OUT)	-0.5V to +4.6V -0.5V to $V_{CCA} + 0.5V$ -0.5V to $V_{CCB} + 0.5V$
$I_{IK}$	DC Input Diode Current @ $V_I < 0V$	-50mA
$I_{OK}$	DC Output Diode Current @ $V_O < 0V$ $V_O > V_{CC}$	-50mA +50mA
$I_{OH}/I_{OL}$	DC Output Source/Sink Current	-50mA / +50mA
$I_{CC}$	DC $V_{CC}$ or Ground Current per Supply Pin	±100mA
$T_{STG}$	Storage Temperature Range	-65°C to +150°C

### Note:

1.  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions<sup>(2)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CCA}$ or $V_{CCB}$	Power Supply Operating	1.1V to 3.6V
	Input Voltage Port A Port B Control Inputs (OE, CLK IN)	0.0V to 3.6V 0.0V to 3.6V 0.0V to $V_{CCA}$
	Dynamic Output Current in $I_{OH}/I_{OL}$ with $V_{CC}$ @ 3.0V to 3.6V 2.3V to 2.7V 1.65V to 1.95V 1.4V to 1.65V 1.1V to 1.4V	±18.0mA ±11.8mA ±7.4mA ±5.0mA ±2.6mA
	Static Output Current $I_{OH}/I_{OL}$ with $V_{CC}$ @ 1.1V to 3.6V	±20.0µA
$T_A$	Free Air Operating Temperature	-40°C to +85°C
$\Delta t/\Delta V$	Maximum Input Edge Rate $V_{CCA/B} = 1.1V$ to 3.6V	10ns/V

### Note:

2. All unused inputs and I/O pins must be held at  $V_{CCI}$  or GND.

### DC Electrical Characteristics ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )

Symbol	Parameter	$V_{CCA}$ (V)	$V_{CCB}$ (V)	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	High Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs An, CMD A, Control inputs CLK IN, OE	$0.6 \times V_{CCA}$			V
		1.1–1.4	1.1–3.6		$0.9 \times V_{CCA}$			
		1.1–3.6	1.4–3.6	Data inputs Bn, CMD B	$0.6 \times V_{CCB}$			
		1.1–3.6	1.1–1.4		$0.9 \times V_{CCB}$			
$V_{IL}$	Low Level Input Voltage	1.4–3.6	1.1–3.6	Data inputs An, CMD A, Control inputs CLK IN, OE			$0.35 \times V_{CCA}$	V
		1.1–1.4	1.1–3.6				$0.1 \times V_{CCA}$	
		1.1–3.6	1.4–3.6	Data inputs Bn, CMD B			$0.35 \times V_{CCB}$	
		1.1–3.6	1.1–1.4				$0.1 \times V_{CCB}$	
$V_{OH}^{(3)}$	High Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs An, CMD A, $I_{HOLD} = -20\mu\text{A}$	$0.75 \times V_{CCA}$			V
		1.1–1.4	1.1–3.6			0.8		
		1.1–3.6	1.65–3.6	Data outputs Bn, CMD B, $I_{HOLD} = -20\mu\text{A}$	$0.75 \times V_{CCB}$			
		1.1–3.6	1.1–1.4			0.8		
$V_{OL}^{(3)}$	Low Level Output Voltage	1.65–3.6	1.1–3.6	Data outputs An, CMD A, $I_{HOLD} = 20\mu\text{A}$			$0.2 \times V_{CCA}$	V
		1.1–1.4	1.1–3.6			0.3		
		1.1–3.6	1.65–3.6	Data outputs Bn, CMD B, $I_{HOLD} = 20\mu\text{A}$			$0.2 \times V_{CCB}$	
		1.1–3.6	1.1–1.4			0.3		
$I_{I(ODH)}^{(4)}$	Bushold Input Overdrive High Current	3.6	3.6	Data inputs An, CMD A, Bn, CMD B	450			$\mu\text{A}$
		2.7	2.7		300			
		1.95	1.95		200			
		1.6	1.6		120			
		1.4	1.4		80			
$I_{I(ODL)}^{(5)}$	Bushold Input Overdrive Low Current	3.6	3.6	Data inputs An, CMD A, Bn, CMD B	-450			$\mu\text{A}$
		2.7	2.7		-300			
		1.95	1.95		-200			
		1.6	1.6		-120			
		1.4	1.4		-80			
$I_I$	Input Leakage Current	1.1–3.6	3.6	Control inputs OE, CLK IN, $V_I = V_{CCA}$ or GND			$\pm 1.0$	$\mu\text{A}$
$I_{OFF}$	Power Off Leakage Current	0	3.6	An, CMD A, $V_O = 0\text{V}$ to 3.6V			$\pm 2.0$	$\mu\text{A}$
		3.6	0	Bn, CMD B, CLK OUT, $V_O = 0\text{V}$ to 3.6V			$\pm 2.0$	
$I_{OZ}^{(6)}$	3-State Output Leakage	3.6	3.6	An, CMD A, Bn, CMD B, CLK OUT, $V_O = 0\text{V}$ or 3.6V, OE = $V_{IL}$			$\pm 2.0$	$\mu\text{A}$
		3.6	0	An, CMD A, $V_O = 0\text{V}$ or 3.6V, OE = Don't Care			$\pm 2.0$	
		0	3.6	Bn, CMD B, CLK OUT, $V_O = 0\text{V}$ or 3.6V, OE = Don't Care			$\pm 2.0$	
$I_{CCA/B}^{(7)(8)}$	Quiescent Supply Current	1.1–3.6	1.1–3.6	$V_I = V_{CCI}$ or GND, $I_O = 0$			5.0	$\mu\text{A}$
$I_{CCZ}^{(7)}$	Quiescent Supply Current	1.1–3.6	1.1–3.6	$V_I = V_{CCI}$ or GND, $I_O = 0$ , OE = $V_{IL}$			5.0	$\mu\text{A}$

**FXL2SD106 — Low Voltage Dual Supply 6-Bit SD Interface Voltage Translator with Configurable Voltage Supplies and Signal Levels, 3-State Outputs, and Auto Direction Sensing**

**DC Electrical Characteristics** ( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) (Continued)

Symbol	Parameter	$V_{CCA}$ (V)	$V_{CCB}$ (V)	Conditions	Min.	Typ.	Max.	Units
$I_{CCA}^{(7)}$	Quiescent Supply Current	0	1.1–3.6	$V_I = V_{CCB}$ or GND; $I_O = 0$			-2.0	$\mu\text{A}$
		1.1–3.6	0	$V_I = V_{CCA}$ or GND; $I_O = 0$			2.0	
$I_{CCB}^{(7)}$	Quiescent Supply Current	1.1–3.6	0	$V_I = V_{CCB}$ or GND; $I_O = 0$			-2.0	$\mu\text{A}$
		0	1.1–3.6	$V_I = V_{CCA}$ or GND; $I_O = 0$			2.0	

**Notes:**

- This is the output voltage for static conditions. Dynamic drive specifications are given in “Dynamic Output Electrical Characteristics.”
- An external driver must source at least the specified current to switch LOW-to-HIGH.
- An external driver must source at least the specified current to switch HIGH-to-LOW.
- “Don’t Care” indicates any valid logic level.
- $V_{CCI}$  is the  $V_{CC}$  associated with the input side.
- Reflects current per supply,  $V_{CCA}$  or  $V_{CCB}$ .

**Dynamic Output Electrical Characteristics<sup>(9)</sup>****A Port (An, CMD A)**Output Load:  $C_L = 15\text{pF}$ ,  $R_L \geq 1\text{M}\Omega$  ( $C_{I/O} = 5\text{pF}$ )

Symbol	Parameter	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{CCA} =$									Units
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	
$t_{\text{rise}}^{(10)}$	Output Rise Time A port		3.0		3.5		4.0		5.0	7.5	ns
$t_{\text{fall}}^{(11)}$	Output Fall Time A port		3.0		3.5		4.0		5.0	7.5	ns
$I_{\text{OHD}}^{(10)}$	Dynamic Output Current High	-18.0		-11.8		-7.4		-5.0		-2.6	mA
$I_{\text{OLD}}^{(11)}$	Dynamic Output Current Low	+18.0		+11.8		+7.4		+5.0		+2.6	mA

**B Port (Bn, CMD B, CLK OUT)**Output Load:  $C_L = 15\text{pF}$ ,  $R_L \geq 1\text{M}\Omega$  ( $C_{I/O} = 15\text{pF}$ )

Symbol	Parameter	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{CCB} =$									Units
		3.0V to 3.6V		2.3V to 2.7V		1.65V to 1.95V		1.4V to 1.6V		1.1V to 1.3V	
		Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	
$t_{\text{rise}}^{(10)}$	Output Rise Time A port		3.0		3.5		4.0		5.0	7.5	ns
$t_{\text{fall}}^{(11)}$	Output Fall Time A port		3.0		3.5		4.0		5.0	7.5	ns
$I_{\text{OHD}}^{(10)}$	Dynamic Output Current High	-18.0		-11.8		-7.4		-5.0		-2.6	mA
$I_{\text{OLD}}^{(11)}$	Dynamic Output Current Low	+18.0		+11.8		+7.4		+5.0		+2.6	mA

**Notes:**

- Dynamic Output Characteristics are guaranteed but not tested.
- See Figure 5.
- See Figure 6.

## AC Characteristics

$V_{CCA} = 3.0V$  to  $3.6V$

Symbol	Parameter	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CCB} =$									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}$ , $t_{PHL}$	A to B	0.2	3.5	0.3	3.9	0.5	5.4	0.6	6.8	22.0	ns
	B to A	0.2	3.5	0.2	3.8	0.3	5.0	0.5	6.0	15.0	ns
$t_{PLH}$ , $t_{PHL}$	CLK IN to CLK OUT		3.0		3.5		4.5		6.0	15.0	ns
$t_{PZL}$ , $t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{skew}^{(12)}$	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

$V_{CCA} = 2.3V$  to  $2.7V$

Symbol	Parameter	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CCB} =$									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}$ , $t_{PHL}$	A to B	0.2	3.8	0.4	4.2	0.5	5.6	0.8	6.9	22.0	ns
	B to A	0.3	3.9	0.4	4.2	0.5	5.5	0.5	6.5	15.0	ns
$t_{PLH}$ , $t_{PHL}$	CLK IN to CLK OUT		3.5		4.0		4.5		6.5	15.0	ns
$t_{PZL}$ , $t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{skew}^{(12)}$	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

$V_{CCA} = 1.65V$  to  $1.95V$

Symbol	Parameter	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CCB} =$									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}$ , $t_{PHL}$	A to B	0.3	5.0	0.5	5.5	0.8	6.7	0.9	7.5	22.0	ns
	B to A	0.5	5.4	0.5	5.6	0.8	6.7	1.0	7.0	15.0	ns
$t_{PLH}$ , $t_{PHL}$	CLK IN to CLK OUT		4.5		4.5		6.3		6.7	15.0	ns
$t_{PZL}$ , $t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{skew}^{(12)}$	A Port, B Port		0.5		0.5		0.5		1.0	1.0	ns

$V_{CCA} = 1.4V$  to  $1.6V$

Symbol	Parameter	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{CCB} =$									Units
		3.0V–3.6V		2.3V–2.7V		1.65V–1.95V		1.4V–1.6V		1.1V–1.3V	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Typ.	
$t_{PLH}$ , $t_{PHL}$	A to B	0.5	6.0	0.5	6.5	1.0	7.0	1.0	8.5	22.0	ns
	B to A	0.6	6.8	0.8	6.9	0.9	7.5	1.0	8.5	15.0	ns
$t_{PLH}$ , $t_{PHL}$	CLK IN to CLK OUT		6.0		6.5		6.7		8.5	15.0	ns
$t_{PZL}$ , $t_{PZH}$	OE to A, OE to B		1.7		1.7		1.7		1.7	1.7	$\mu s$
$t_{skew}^{(12)}$	A Port, B Port		1.0		1.0		1.0		1.0	1.0	ns

### Note:

12. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (An, CMD A or Bn, CMD B) and switching with the same polarity (Low-to-High or High-to-Low). See Figure 8.

**Max Data Rate<sup>(13)(14)</sup>**

$V_{CCA}$	$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CCB} =$					Units
	3.0V to 3.6V	2.3V to 2.7V	1.65V to 1.95V	1.4V to 1.6V	1.1V to 1.3V	
	Min.	Min.	Min.	Min.	Typ.	
$V_{CCA} = 3.0\text{V to } 3.6\text{V}$	100	100	80	60	20	Mbps
$V_{CCA} = 2.3\text{V to } 2.7\text{V}$	100	100	80	60	20	Mbps
$V_{CCA} = 1.65\text{V to } 1.95\text{V}$	80	80	60	40	20	Mbps
$V_{CCA} = 1.4\text{V to } 1.6\text{V}$	60	60	40	40	20	Mbps
	Typ.	Typ.	Typ.	Typ.	Typ.	
$V_{CCA} = 1.1\text{V to } 1.3\text{V}$	20	20	20	20	20	Mbps

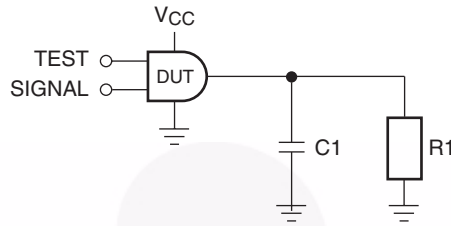
**Note:**

13. Max Data Rate is guaranteed but not tested.

14. Max Data Rate is specified in megabits per second. See Figure 7. It is equivalent to two times the F-toggle frequency, specified in megahertz. For example, 100 Mbps is equivalent to 50 MHz.

**Capacitance**

Symbol	Parameter	Conditions	$T_A = +25^{\circ}\text{C}$	Units
			Typical	
Cin	Input Capacitance, Control pin (OE, CLK IN)	$V_{CC}A = V_{CC}B = \text{GND}$	4	pF
Ci/o	Input/Output Capacitance	An, CMD A	5	pF
		Bn, CMD B, CLK OUT		
Cpd	Power Dissipation Capacitance	$V_{CC}A = V_{CC}B = 3.3\text{V},$ $V_i = 0\text{V or } V_{CC}, f = 10\text{MHz}$	25	pF



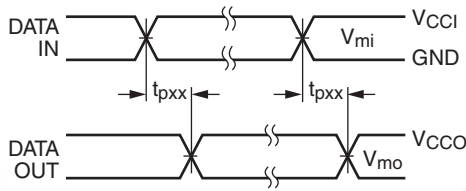
Test	Input Signal	Output Enable Control
$t_{PLH}$ , $t_{PHL}$	Data Pulses	$V_{CCA}$
$t_{PZL}$	0V	Low to High Switch
$t_{PZH}$	$V_{CCI}$	Low to High Switch

Figure 1. AC Test Circuit

**AC Load Table**

$V_{CCO}$	CI	RI
$1.2V \pm 0.1V$	15pF	1M $\Omega$
$1.5V \pm 0.1V$	15pF	1M $\Omega$
$1.8V \pm 0.15V$	15pF	1M $\Omega$
$2.5V \pm 0.2V$	15pF	1M $\Omega$
$3.3 \pm 0.3V$	15pF	1M $\Omega$

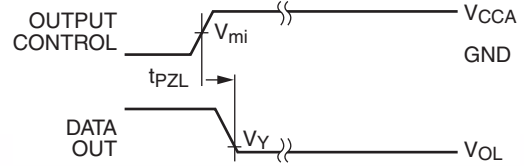




Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90%

Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_i = 3.0\text{V}$  to  $3.6\text{V}$  only

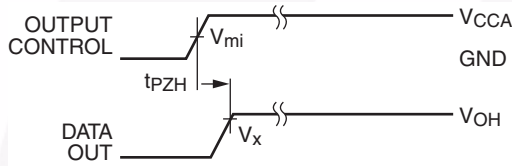
**Figure 2. Waveform for Inverting and Non-inverting Functions**



Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90%

Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_i = 3.0\text{V}$  to  $3.6\text{V}$  only

**Figure 3. 3-STATE Output Low Enable Time for Low Voltage Logic**



Input  $t_R = t_F = 2.0\text{ns}$ , 10% to 90%

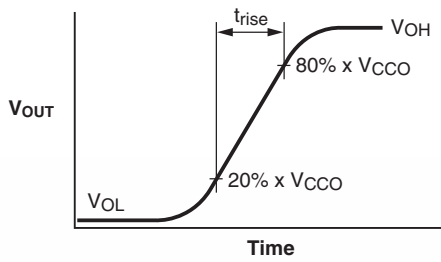
Input  $t_R = t_F = 2.5\text{ns}$ , 10% to 90%, @  $V_i = 3.0\text{V}$  to  $3.6\text{V}$  only

**Figure 4. 3-STATE Output High Enable Time for Low Voltage Logic**

Symbol	Vcc
$V_{mi}^{(15)}$	$V_{CCI} / 2$
$V_{mo}$	$V_{CCO} / 2$
$V_X$	$0.9 \times V_{CCO}$
$V_Y$	$0.1 \times V_{CCO}$

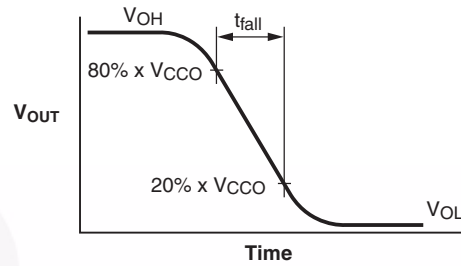
**Note:**

15.  $V_{CCI} = V_{CCA}$  for control pin OE or  $V_{mi} = (V_{CCA} / 2)$ .



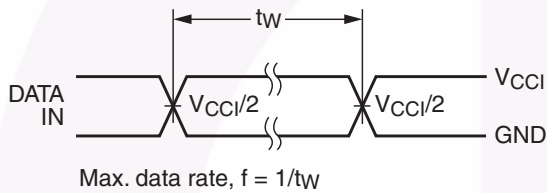
$$I_{OHD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(20\% - 80\%) \times V_{CCO}}{t_{RISE}}$$

**Figure 5. Active Output Rise Time and Dynamic Output Current High**

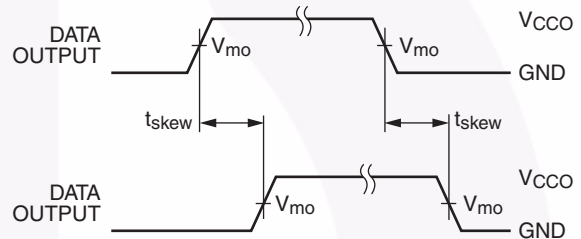


$$I_{OLD} \approx (C_L + C_{I/O}) \times \frac{\Delta V_{OUT}}{\Delta t} = (C_L + C_{I/O}) \times \frac{(80\% - 20\%) \times V_{CCO}}{t_{FALL}}$$

**Figure 6. Active Output Fall Time and Dynamic Output Current Low**



**Figure 7. Maximum Data Rate**



$$t_{skew} = (t_{pHLmax} - t_{pHLmin}) \text{ or } (t_{pLHmax} - t_{pLHmin})$$

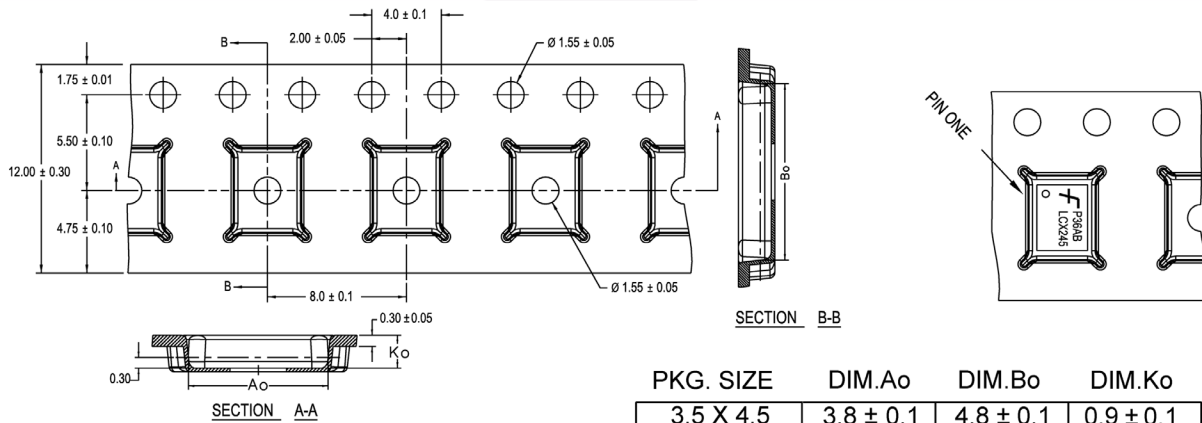
**Figure 8. Output Skew Time**

## Tape and Reel Specification

### Tape Format for DQFN 10

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

### Tape Dimensions millimeters



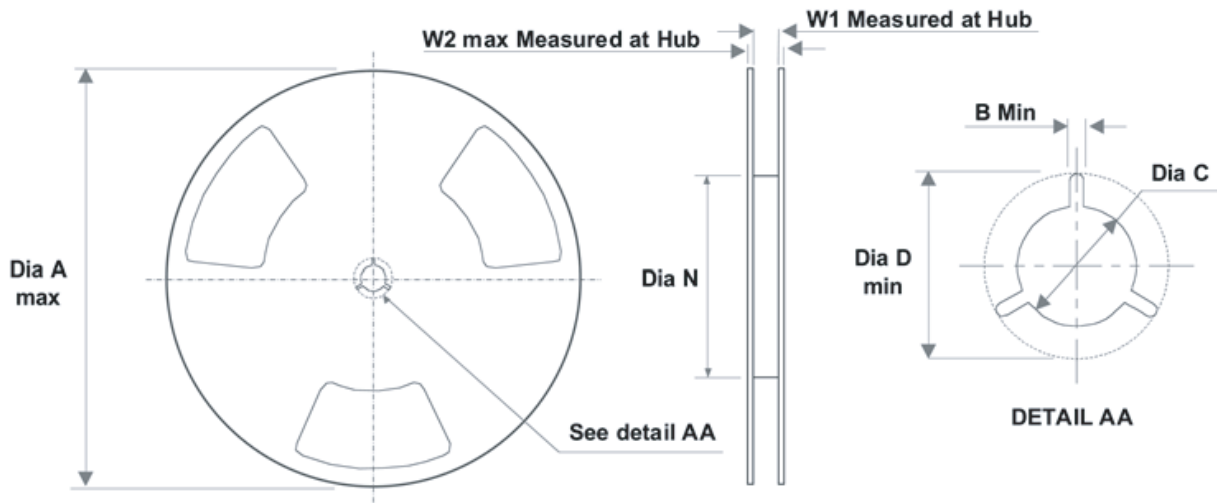
PKG. SIZE	DIM.Ao	DIM.Bo	DIM.Ko
3.5 X 4.5	3.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
3.0 X 3.0	3.3 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 4.5	2.8 ± 0.1	4.8 ± 0.1	0.9 ± 0.1
2.5 X 3.5	2.8 ± 0.1	3.8 ± 0.1	0.9 ± 0.1
2.5 X 3.0	2.8 ± 0.1	3.3 ± 0.1	0.9 ± 0.1
2.5 X 2.5	2.8 ± 0.1	2.8 ± 0.1	0.9 ± 0.1

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

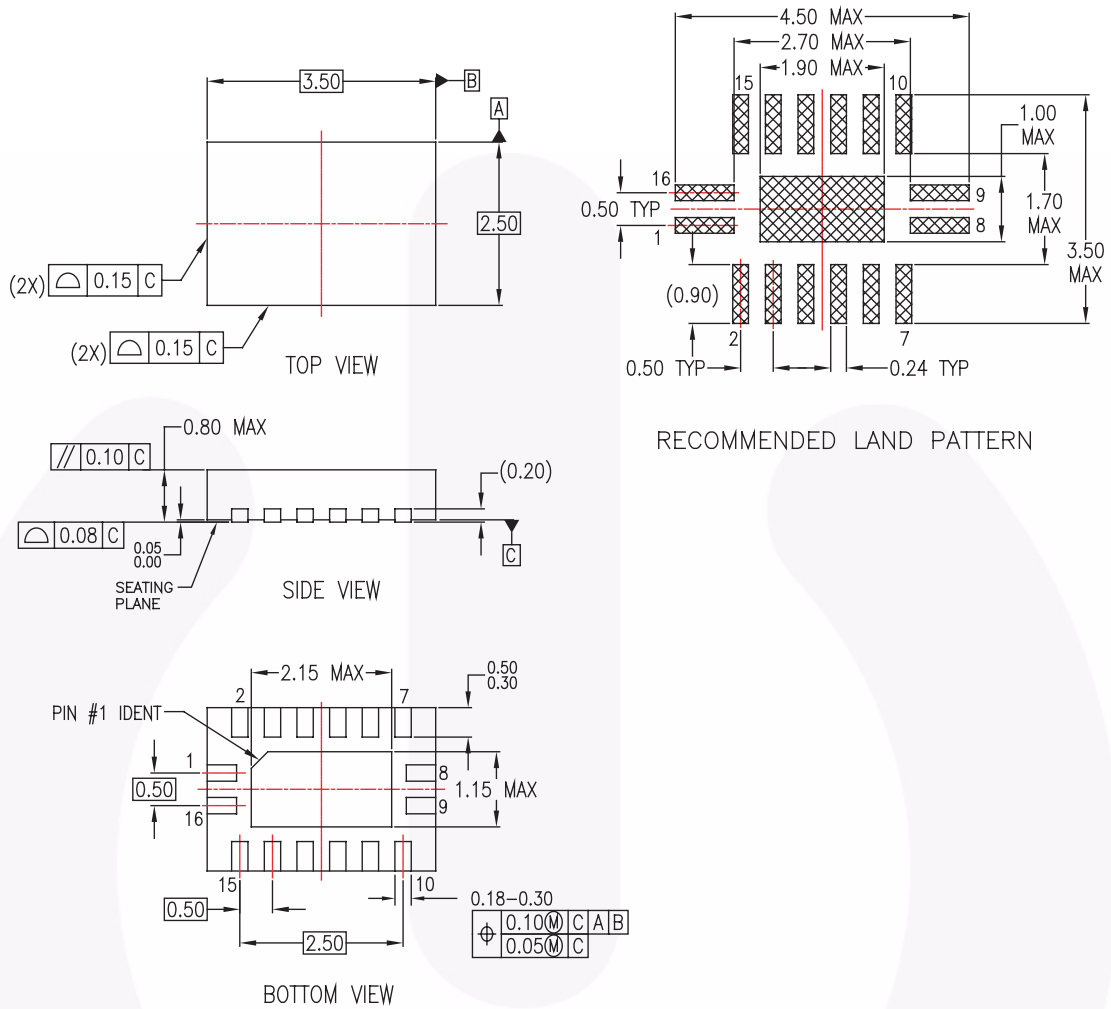
1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

**Reel Dimensions** inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2
12mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

### Physical Dimensions



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AB
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP16ErevA

**Figure 9. 6-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241 2.5mm x 3.5mm**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.






Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:

<http://www.fairchildsemi.com/packaging/>



## TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACEx <sup>®</sup>	FPS <sup>™</sup>	PDP SPM <sup>™</sup>	The Power Franchise <sup>®</sup>
Build it Now <sup>™</sup>	F-PFS <sup>™</sup>	Power-SPM <sup>™</sup>	the <b>power</b> franchise
CorePLUS <sup>™</sup>	FRFET <sup>®</sup>	PowerTrench <sup>®</sup>	TinyBoost <sup>™</sup>
CorePOWER <sup>™</sup>	Global Power Resource <sup>SM</sup>	Programmable Active Droop <sup>™</sup>	TinyBuck <sup>™</sup>
CROSSVOLT <sup>™</sup>	Green FPS <sup>™</sup>	QFET <sup>®</sup>	TinyLogic <sup>™</sup>
CTL <sup>™</sup>	Green FPS <sup>™</sup> e-Series <sup>™</sup>	QS <sup>™</sup>	TINYOPTO <sup>™</sup>
Current Transfer Logic <sup>™</sup>	GTO <sup>™</sup>	Quiet Series <sup>™</sup>	TinyPower <sup>™</sup>
EcoSPARK <sup>®</sup>	IntelliMAX <sup>™</sup>	RapidConfigure <sup>™</sup>	TinyPWM <sup>™</sup>
EfficientMax <sup>™</sup>	ISOPLANAR <sup>™</sup>	Saving our world, 1mW at a time <sup>™</sup>	TinyWire <sup>™</sup>
EZSWITCH <sup>™</sup> *	MegaBuck <sup>™</sup>	SmartMax <sup>™</sup>	μSerDes <sup>™</sup>
 <sup>™</sup>	MICROCOUPLER <sup>™</sup>	SMART START <sup>™</sup>	 <sup>™</sup>
 <sup>®</sup>	MicroFET <sup>™</sup>	SPM <sup>®</sup>	UHC <sup>®</sup>
Fairchild <sup>®</sup>	MicroPak <sup>™</sup>	STEALTH <sup>™</sup>	Ultra FRFET <sup>™</sup>
Fairchild Semiconductor <sup>®</sup>	MillerDrive <sup>™</sup>	SuperFET <sup>™</sup>	UniFET <sup>™</sup>
FACT Quiet Series <sup>™</sup>	MotionMax <sup>™</sup>	SuperSOT <sup>™</sup> -3	VCX <sup>™</sup>
FACT <sup>®</sup>	Motion-SPM <sup>™</sup>	SuperSOT <sup>™</sup> -6	VisualMax <sup>™</sup>
FAST <sup>®</sup>	OPTOLOGIC <sup>®</sup>	SuperSOT <sup>™</sup> -8	
FAST <sup>®</sup>	OPTOPLANAR <sup>®</sup>	SupreMOS <sup>™</sup>	
FastvCore <sup>™</sup>	 <sup>®</sup>	SyncFET <sup>™</sup>	
FlashWriter <sup>®</sup>		 <sup>®</sup>	

\* EZSWITCH<sup>™</sup> and FlashWriter<sup>®</sup> are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

## DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

## LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I34