FXS50LD1-03 Databook

High-Drive Line Driver (LD)

for the

Fx100100S-5 Multi-Mode (VDSL2, VDSL, ADSL2+, ADSL2, ADSL) SLE Chipset

Application: FTTx Subscriber Located Equipment (SLE)

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Preliminary Information (Subject to Change)

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Document Status

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Advance—Information on a product in early development.
Preliminary—Current information on a product under development.
Final—Complete information on a developed product.

Revision History

Version	Date	Changes
1.0	June 06, 2006	First release.
1.1	June 16, 2006	Updated Package Type in part number.
1.2	August 1, 2006	Updated the following: • "Thermal Resistance" on page 10. • Chapter 6, "Ordering Information" to include "Marking Data".

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Chapter 1 Overview

1.1 About the Fx100100S-5 Chipset

The Fx100100S-5 chipset is a single-port, standards-compliant solution that enables equipment vendors to develop high-performance Subscriber Located Equipment (SLE) such as modems, bridges, routers, VoIP gateways, and residential gateways. Since this chipset is highly programmable with superior integration features, it can be easily customized for worldwide applications. SLE vendors can therefore build fewer products, reduce time to market, and dramatically lower development, manufacturing, and inventory costs.

The Fx100100S-5 chipset consist of the following components:

- *Burst Mode Engine (BME)—FXS50BM1-00,* which is a single-port Digital Signal Processing (DSP) engine.
- *Integrated Front End (IFE)—FXS50IF1-03,* which includes ADC, DAC, filters, and amplifiers.
- *High-Drive Line Driver (LD)—FXS50LD1-03,* which is a single port 14.5dBm line driver across 30 MHz bandwidth.

1.1.1 Features of the Fx100100S-5 Chipset

The Fx100100S-5 chipset ships with the following features:

- Industry Leading Performance
  - One port of asymmetric line data rates up to 100 Mbps downstream and up to 100 Mbps upstream
  - One port of symmetric line data rates up to 100 Mbps
- Universal SLE
  - VDSL2, VDSL, ADSL2+, ADSL
- Lower BOM and board space
  - One design worldwide 100/100 + VLR
  - Simplified VLR filter
- IP or ATM with a single design
  - Integrated AAL5 SAR

- Compliant with the following worldwide standards:
  - ITU-T G.993.2 (VDSL2)
  - ITU-T G.993.1-2004 (VDSL)
  - ANSI T1.424-2004
  - ETSI TS 101 270-1 and TS 101 270-2
  - G.992.x (ADSL2+, ADSL2, ADSL)
- Flexibility to be deployed for a variety of markets:
  - Fiber to the Exchange (FTTx)— FTTP, FTTH, FTTB, and FTTC
  - Multi-tenant and Multi-dwelling Unit (MxU)
- Exceptional programmability:
  - Real time optimization of dedicated data and voice bandwidth.
  - Programmable throughput in increments of 64 Kbps that enables service levels in tiers.
  - Drive level up to 14.5dBm.
- Faster deployment and easier integration with any other equipment using Ikanos Programmable Operating System (iPOS):
  - iPOS consists of optimized firmware and OS/µP independent API commands.
  - iPOS lets vendors configure the chipset for FTTx/ MxU asymmetric/ symmetric applications and ATM/Ethernet protocols with scalable speeds.
- Standards-compliant DMT modulation and Frequency Division Multiplexing (FDM).
- Spectrally compatible with POTS and ISDN for voice services.
- Support for Hostless Ethernet Bridge Modem and any Hostful application.
- Backward compatible with SL8100, SL8800, SL94xx, Fx7030, Fx10050, Fx100100, and Fx100100-4 chipsets.
- Industrial operating temperature of –40° to +85° C.

1.2 About FXS50LD1-03

The FXS50LD1-03 is a single-port 100100 differential line driver that extends the reach and transmission reliability of SLE equipment. The FXS50LD1-03 is a part of the Fx100100S-5 multi-mode SLE chipset and integrates all the features required to deploy a line interface for FTTx Subscriber Located Equipment (SLE).

A transformer connects the FXS50LD1-03 to the line. On the network side, the FXS50LD1-03 is connected to the FXS50IF1-03.

1.2.1 FXS50LD1-03 Features

The FXS50LD1-03 contains the following features:

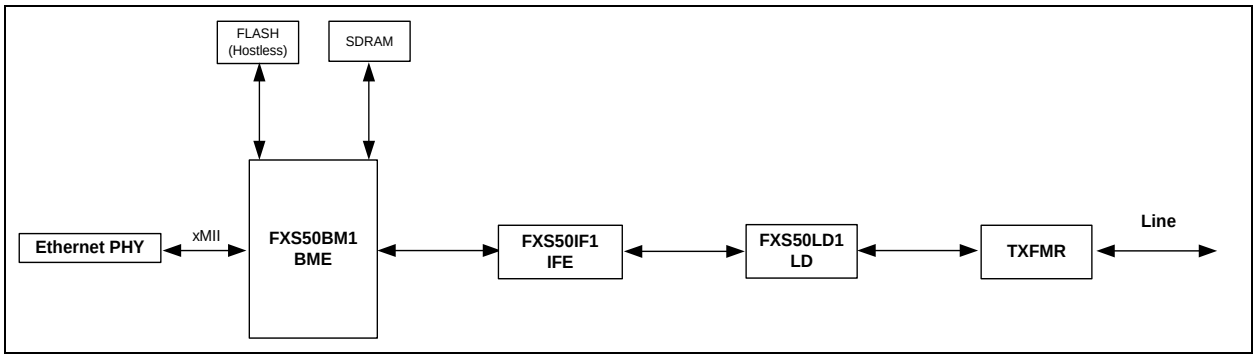
- Compact single-port line driver that delivers 14.5dBm transmit power.
- Complies with the following worldwide standards:
  - ITU-T G.993.2 VDSL2 standard
  - ITU-T G.993.1-2004 VDSL standard
  - ANSI T1.424-2004
  - ETSI TS 101 270-1 and TS 101 270-2
  - ITU-T G.992.x (ADSL2+, ADSL2, ADSL) standards
- Targeted at Subscriber Located Equipment (SLE) such as:
  - Hostless Bridge Modem
  - Hostful Residential Gateway
- Low operating power:
  - Dynamically reduces power when using less bandwidth
- Low power operation: +12V and +2.5V power supply.
- Integrated 2-bit Low Noise Amplifier (LNA) with gain and bias control.
- Integrates all negative and positive feedback components excluding sense resistors.
- Analog echo cancellation system to cancel transmit signals in the receive path.
- Integrated programmable hybrid.
- Integrated serial interface.
- Integrated bandgap reference generator.
- Integrated tertiary lightning protection.
- Packaged in 7x7 mm 32-pin LQFP.
- Industrial operating temperature of –40° to +85° C.
- 30 MHz bandwidth.

1.3 Sample Target Applications

1.3.1 Single Port Hostless SLE

Figure 1–1 shows an example of a Hostless single port SLE that can be built using the Fx100100S-5 chipset. The external program memory (SDRAM) and Boot Flash memory store the firmware and power up the system respectively.

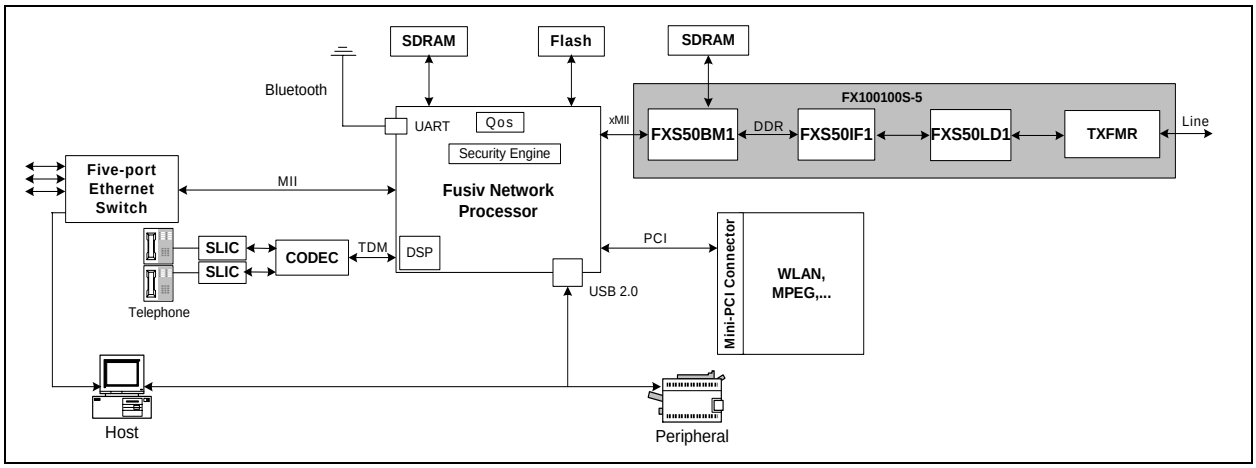
Figure 1–1 *Sample Single Port Hostless (VDSL2/VDSL/ADSL2+/ADSL) SLE*



1.3.2 Residential Gateway With Internal VoIP DSP

Figure 1–2 shows an example of a Residential Gateway Hostful SLE that can be built using the Fx100100S-5 chipset. FXS50BM1-00 interfaces with the Fusiv Network Processor through the Utopia or xMII interface. The Fusiv Network Processor provides the processing power required for the Residential Gateway networking function.

Figure 1–2 *Sample Residential Gateway With Internal VoIP DSP*



Chapter 2 Pin Definition

2.1 FXS50LD1-03 Signals

Figure 2–1 *FXS50LD1-03 Pinout Diagram*

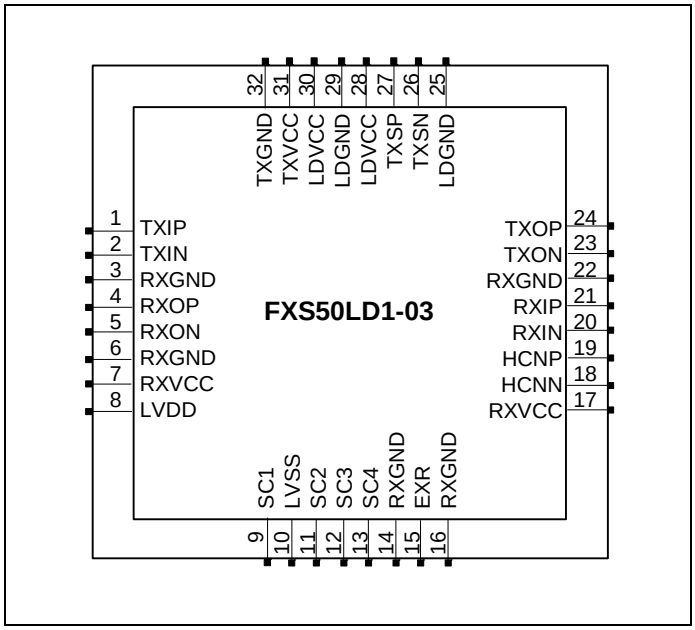


Table 2–1 *FXS50LD1-03 Signals*

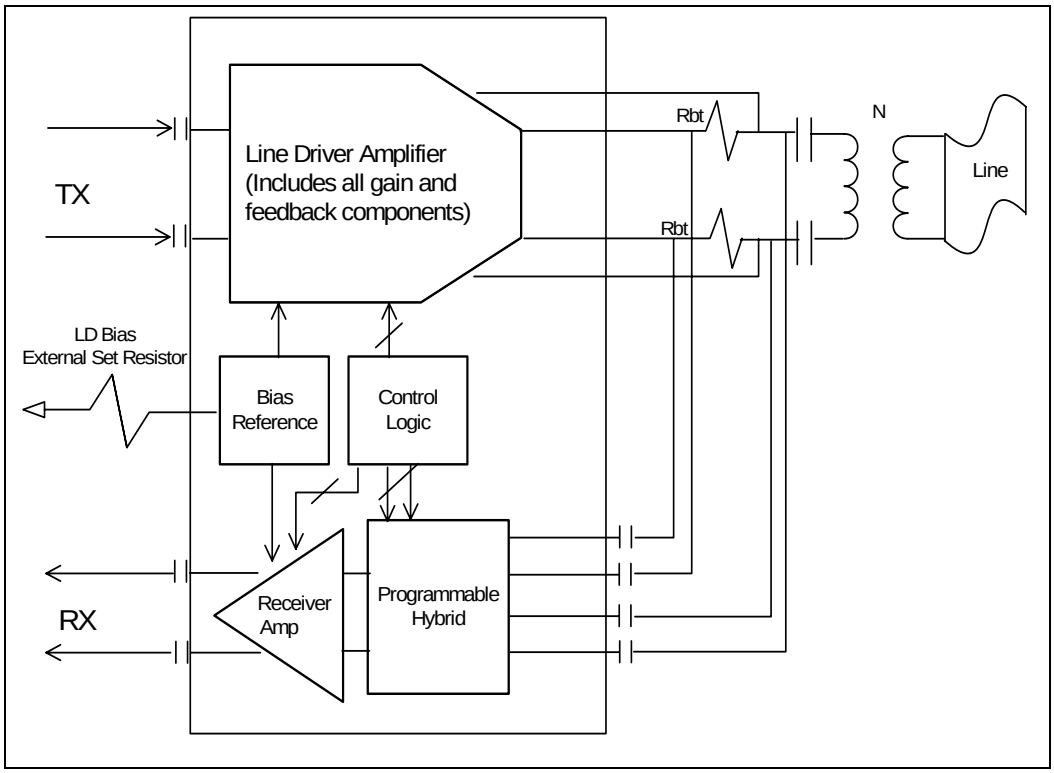
Pin #	Signal Name	Signal Type	Description
1	TXIP	Input	TX Positive Input
2	TXIN	Input	TX Negative Input
3	RXGND	Input	RX Ground
4	RXOP	Output	RX Positive Output
5	RXON	Output	RX Negative Output
6	RXGND	Input	RX Ground
7	RXVCC	Input	RX Power Supply
8	LVDD	Input	Logic Power Supply
9	SC1	Input	Serial Interface Clk1
10	LVSS	Input	Logic Ground
11	SC2	Input	Serial Interface Clk2
12	SC3	Input	Serial Interface Data
13	SC4	Input	Test Pin (Normally LVSS)
14	RXGND	Input	RX Ground
15	EXR	Output	Bias External Pin
16	RXGND	Input	RX Ground
17	RXVCC	Input	RX Power Supply
18	HCNN	Input	Hybrid Negative Input
19	HCNP	Input	Hybrid Positive Input
20	RXIN	Input	RX Negative Input
21	RXIP	Input	RX Positive Input
22	RXGND	Input	RX Ground
23	TXON	Output	TX Negative Output
24	TXOP	Output	TX Positive Output
25	LDGND	Input	LD Ground
26	TXSN	Input	Positive Feedback Negative Input
27	TXSP	Input	Positive Feedback Positive Input
28	LDVCC	Input	LD Power Supply
29	LDGND	Input	LD Ground
30	LDVCC	Input	LD Power Supply
31	TXVCC	Input	TX Power Supply
32	TXGND	Input	TX Ground

Chapter 3 Functional Description

3.1 Block Diagram of the FXS50LD1-03

Figure 3–1 shows the function block diagram of the single-port FXS50LD1-03. The various function blocks on the FXS50LD1-03 are described in the sections below.

Figure 3–1 *Block Diagram of the FXS50LD1-03*



3.2 Functional Summary

The FXS50LD1-03 consists of a Line Driver, a Low-Noise Receive Amplifier, and Programmable Hybrid Circuits.

The FXS50LD1-03 transmit path includes the Line Driver, which combines high speed and high power delivery capability (up to 14dBm) with low power dissipation. The Line Driver provides external bias setting resistor that configures the internal bandgap biasing with accurate quiescent current setting and with power flexibility

The FXS50LD1-03 receive path includes the Low Noise Amplifier (LNA), and the Programmable Hybrid Network.

Chapter 4 Electrical Data

Voltages should be applied to the Fx100100S-5 multi-mode SLE chipset in the following order:

1. 12V to the LD I/O circuitry
2. 2.5V to the serial interface

NOTE: Make sure the FXS50LD1-03 conforms to the following power-up requirement: The 12V powers up first and the 2.5V powers up next.

4.1 Operating Conditions

Operating conditions refer to the limits that guarantee the functioning of the device. Functioning of the device is guaranteed using the following methods:

- Production testing between 0°C and 70°C
- Characterization and periodic sampling of production units between –40°C and +85°C

Table 4–1 *Operating Conditions*

Parameter	Typical Value	Unit
Number of channels (ports)	1	
Power supply voltage **Note**: The power supply voltage can be between ±5% of the typical values.	+12	V
Power dissipation : • 14.5dBm output power on the line • LNA • Serial Interface and Hybrid	<1W	 mW/port mW/port mW/port
Operating temperature range	–40 to +85	°C
Transformer turns ratio	1:1.5	

4.2 Thermal Resistance

Table 4–2 *Themal Resistance*

Package	Conditions	Θ_{JA} (Junction to Ambient)	Θ_{JB} (Junction to Ball)	Θ_{JC} (Junction to Case)	Unit
7 × 7mm 32-Pin LQFP	Still Air (0m/s air flow)	52.0	NA	15.74	°C/W

4.3 Electrical Specifications

4.3.1 Line Driver

Table 4–3 *Electrical Specifications – Line Driver*

Parameter	Typical Value	Unit
Gain (excluding transformer)	20/17	dB
HD3 (F=2 MHz, RL=44.4 ohm, Vout=1/2 peak swing voltage) **Note:** Only the differential HD3 of the FXS50LD1-03 is tested.	60	dBc
Input referred noise	12	nV/√Hz

4.3.2 Low Noise Amplifier (LNA)

Table 4–4 *Electrical Specifications–LNA*

Parameter	Typical Values	Unit
HD3 (Vout=1/2 peak swing voltage) at 2 MHz	60	dBc
Maximum output swing	3	Vppd
Output current drive	TBD	mA
Power dissipation	TBD	mW

4.4 Bandgap Bias

Table 4–5 *Bandgap Bias Specifications*

Parameter	Typical Value	Unit
Vbg voltage	1.22	V
Temperature variation **Note:** The temperature varies between –40°C to +85°C.	±3	%
External Resistor **Note:** The external resistor is added to ensure high-power performance	TBD	

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Chapter 5 Mechanical Data

All dimensions in Figure 5–1 are in millimeters.

Figure 5–1 *Top View of 7 x 7 x 1.4 mm 32-Pin LQFP*

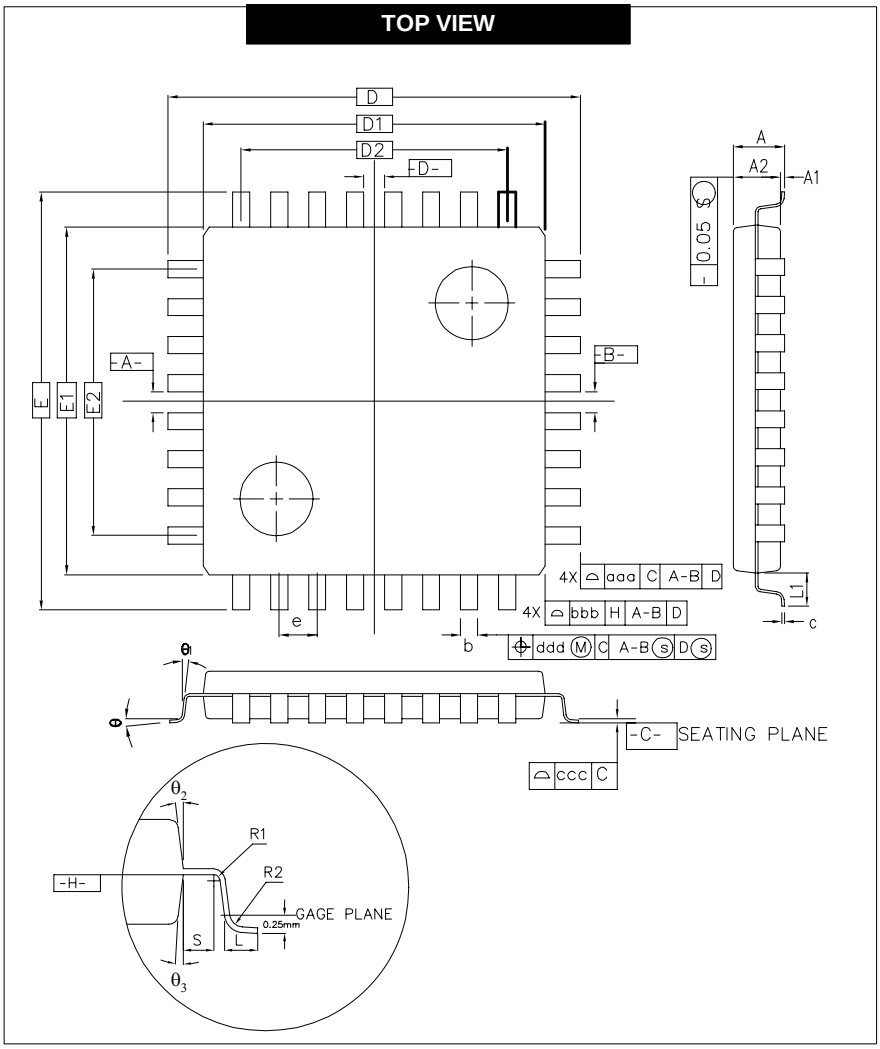


Figure 5–2 *Dimensions of 7 x 7 x 1.4 mm 32-Pin LQFP*

COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D_1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E_1	7.00 BSC.			0.276 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

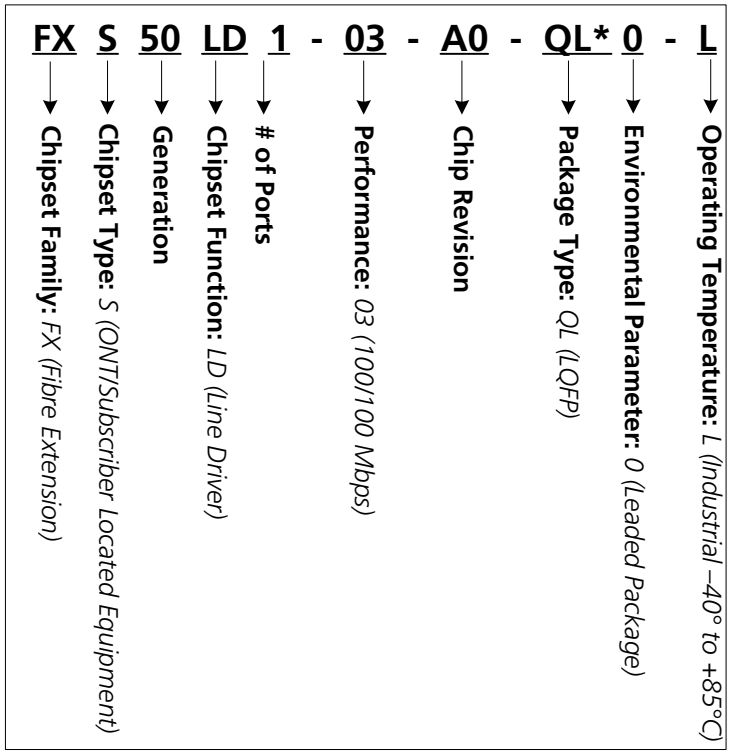
SYMBOL	32L						44L						48L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.17	0.20	0.27	0.007	0.008	0.011	0.17	0.20	0.27	0.007	0.008	0.011
e	0.80 BSC.			0.031 BSC.			0.50 BSC.			0.020 BSC.			0.50 BSC.			0.020 BSC.		
D2	5.60			0.220			5.00			0.197			5.50			0.217		
E2	5.60			0.220			5.00			0.197			5.50			0.217		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.003			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.08			0.003			0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
   ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE
   MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE
   LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY
   MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS
   OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION
   AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and
   0.5mm PITCH PACKAGES.
3. ALL DIMENSION OF 44L WERE BASE ON THOSE OF 48L SINCE
   THEY ARE NOT MENTIONED IN JEDEC SPEC MS-026.

Chapter 6 Ordering Information

Figure 6–1 *FXS50LD1-03 Part Number*

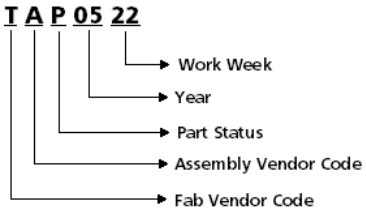


In Figure 6–1:

- **FXS50LD1-03-A0-QL0-L** is part of the Fx100100S-5 chipset that supports VDSL2 Profiles 8a/8b/8c/8d, 12a/12b, 17a, and 30a.
- ***** refers to the environmental parameter, where:
  - 0 corresponds to Standard package
  - 1 corresponds to Lead Free package
  - 2 corresponds to Green package

6.1 Marking Data

Table 6–1 *Marking Specification*

Line #	Marking Specification	Example(s)
1	Logo	
2	Part number	• FXO51BM8- • IKF6836-A0-
3	Package	• A0-HB0 • PB1-C
4	Datacode	TAP0522:  See Table 6–2, Table 6–3, and Table 6–4 for legends on fab vendor code, assembly vendor code, and part status respectively.
5	Fab lot number	Fab lot number

6.1.1 Fab Vendor Code

Table 6–2 *Fab Vendor Code*

Foundry	Code Designator
TSMC	T
UMC	U
IBM	B
CHARTERED	C
TOWER	W
AMS	A

Table 6–2 *Fab Vendor Code (Continued)*

Foundry	Code Designator
SAMSUNG	S
IMP	M

6.1.2 Assembly Vendor Code

Table 6–3 *Assembly Vendor Code*

Assembly Vendor	Code Designator
ASEK	A
SPIL	L
STATSChipPac-Singapore	S
OSE	O
STATSChipPac-China	H
STATSChipPac-Korea	R
UTAC	U
AMKOR—Philippines	P
AMKOR—Singapore	G
ASEM	M
ASECL	C

6.1.3 Part Status

Table 6–4 *Part Status*

Part Status	Code Designator
Production	P
Engineering	E
Marketing Sample	M

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