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样 品 规 格 承 认 书

公司料号：FY07024DI26A30-D

客户名称：

客户料号：

日　　期：2014-04-30

CUSTOMER（客户承认签字）		TECHNOLOGY UNION（厂商确认签字）		
CHECKED（核准）	APPROVED（审批）	PREPARED（制作）	CHECKED（检查）	APPROVED（审核）

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1.REVISION RECORD

DATE	VERSION	REVISION ITEMS	PAGE	DESING BY
2014-05-20	1.0	Preliminary	----	CZH
2014-06-10	2.0	Modify display mode	5	CZH

ote : The Product and specifications are subject to change without any notice.
Please ask for the latest Product Standards to guarantee the satisfaction of our product requirements.

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Contents

3. PRODUCT INFORMATION

3.1. Description

FY07024DI26A30-D is a color active matrix LCD module incorporating amorphous silicon TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs FPC and a backlight unit. The 7.0′ display area contains 1024 (RGB) x 600 pixels

3.2. Applications

☐**UMPC**

☐**Portable DVD**

☐**GPS**

☐MID

3.3. Features

☐**High Resolution:1024(RGB) x 600 Dots**

☐**adopting a high aperture ratio**

☐**24 chip LED backlight**

☐**Dot-Inversion**

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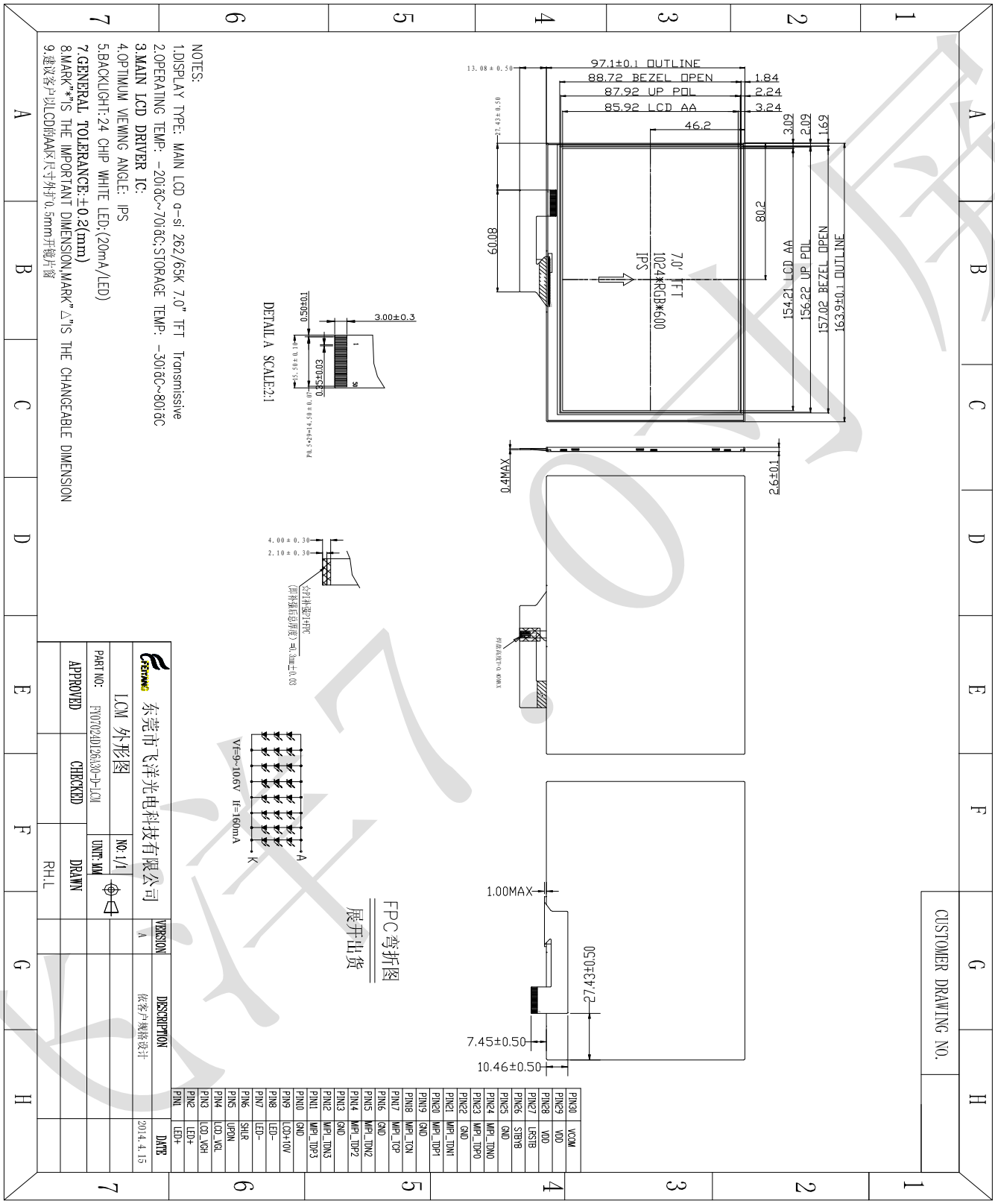
4. General Specifications

NO.	ITEM	SPECIFICATION	UNIT	REMAR
1	LCD size	7.0 (Diagonal)	inch	
2	Driver Method	a-si TFT active matrix	-	
3	Resolution	1024 × 3(RGB) × 600	dots	
4	Display mode	FFS Normally black	-	
5	Dot pitch	0.1506(H) × 0.1432(V)	mm	
6	Active area	154.21(H) × 85.92(V)	mm	
7	Panel size	163.9 (H) ×97.1(V) ×2.6(T)	mm	
8	Color Pixel	RGB vertical stripe	-	
9	Surface treatment	Glare type	-	
10	View Direction	ALL	o'clock	
11	Interface	MIPI	-	

5. Mechanical drawing



6. ABSOLUTE MAXIMUM RATINGS

The following are maximun values which, if exceeded, may cause faulty operation or damage to the unit.

Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	DVDD	-0.3	3.96	V	-
Analog Supply Voltage	AVDD	-0.5	14.85	V	-
Gate On Voltage	VGH	-0.3	40	V	-
Gate Off Voltage	VGL	-20	0.3	V	-
Gate On-Gate Off Voltage	VGH-VGL	12	40	V	-
Operating Temperature	Topa	-20	70	℃	Note1
Storage Temperature	Tstg	-30	80	℃	Note1

Note1：If users use the product out off the environmemtal operation range（temperature and humidity,it will have visual quality concerns.

7.ELECTRICAL CHARACTERISTICS

7.1 Typical operation conditions

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Digital supply voltage	DVDD	1.79	1.8	1.89	V	
Analog supply voltage	AVDD	9.4	9.6	9.8	V	
Gate on voltage	VGH	17	18	19	V	
Gate off voltage	VGL	-6.6	-6	-5.4	V	
Common voltage	VCOM	2.85	--	3.45	V	
Logic input voltage	VIH	0.7*DVDD	-	DVDD	V	NOTE1
	VIL	GND	-	0.3*DVDD	V	

[note1] please adjust VCOM to make the flicker lever be minimum

7.2 Current consumption

Current consumption

TEM	SYMBOL	CONDITION	MIN	TYPE	MAX	UNIT	NOTE
Gate on Power Current	IVGH	VGH =18V	--	0.7	1.5	mA	Note1
Gate off Power Current	IVGL	VGL= -6V	--	0.7	1.5	mA	Note1
Digital Power Current	IDVDD	DVDD =1.8V	--	65	70	mA	Note1
Analog Power Current	IAVDD	AVDD = 9.6V		40	50	mA	Note1
Total Power Consumption	PC		--	674	822	mW	Note1

Note1: Typ. specification：Gray-level test Pattern

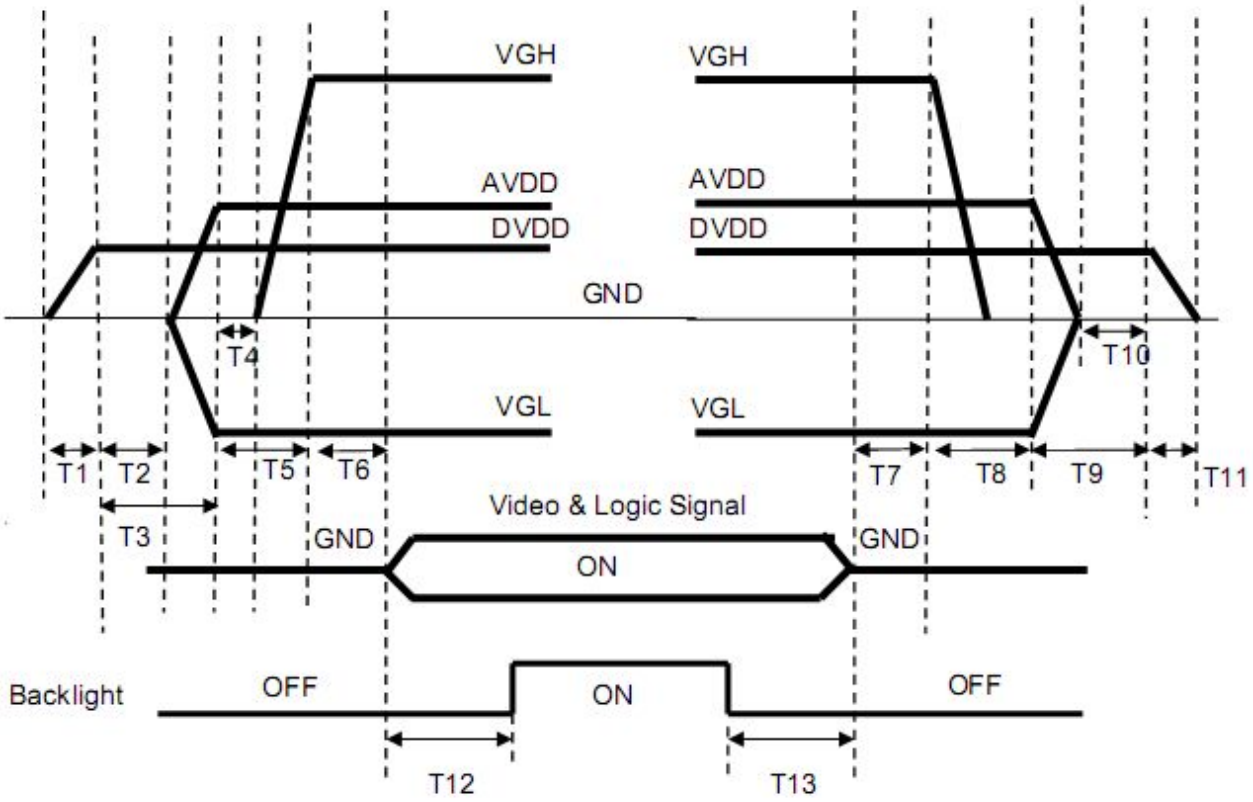
Max. specification：Black test Pattern

(a)Gray-level Pattern

(b)Black Pattern

7.3 Power、Signal sequence

Power On：DVDD→AVDD/VGL →VGH →Video &Logic Signal→Backlight
Power Off：Backlight→Video &Logic Signal→ VGH→AVDD/VGL→DVDD



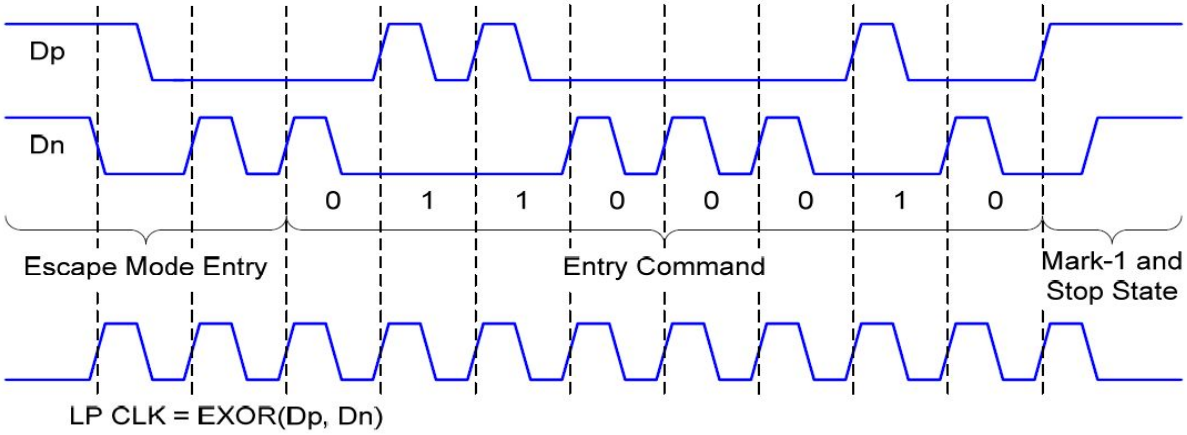
0<T1≦10ms
T2>0ms
T3>20ms
T4>0ms
T5>10ms
0<T6≦10ms
T12≧200ms

T7>0ms
T8>0ms
T9>0ms
T10>0ms
0<T11≦10ms
T13≧200ms

.4 MIPI AC Characteristic

7.1.1. LP Transmitter AC Specification

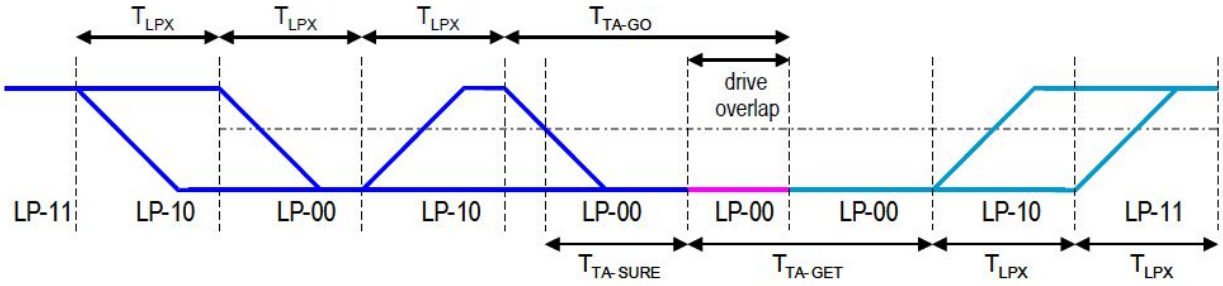
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR clock	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	-
	All other pulses		20	-	-	ns	-
Period of the LP EXOR clock		$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @C_{LOAD} =0pF		$\delta V/\delta t_{SR}$	30	-	500	mV/ns	-
Slew Rate @C_{LOAD} =5pF			30	-	200	mV/ns	-
Slew Rate @C_{LOAD} =20pF			30	-	150	mV/ns	-
Slew Rate @C_{LOAD} =70pF			30	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-



7.1.2. Turnaround Procedure

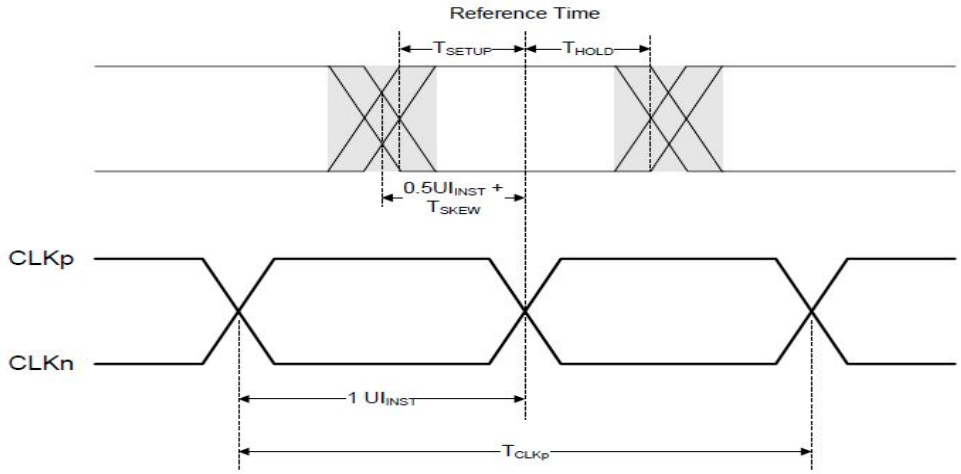
Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period: Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period: Slave side	T_{LPX}	50	55.56	58.34	ns
Ratio of T_{LPX}(Master)/ T_{LPX} (Slave) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}		2T_{LPX}	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	5T_{LPX}	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	4T_{LPX}	-	ns



7.1.3. High speed transmission

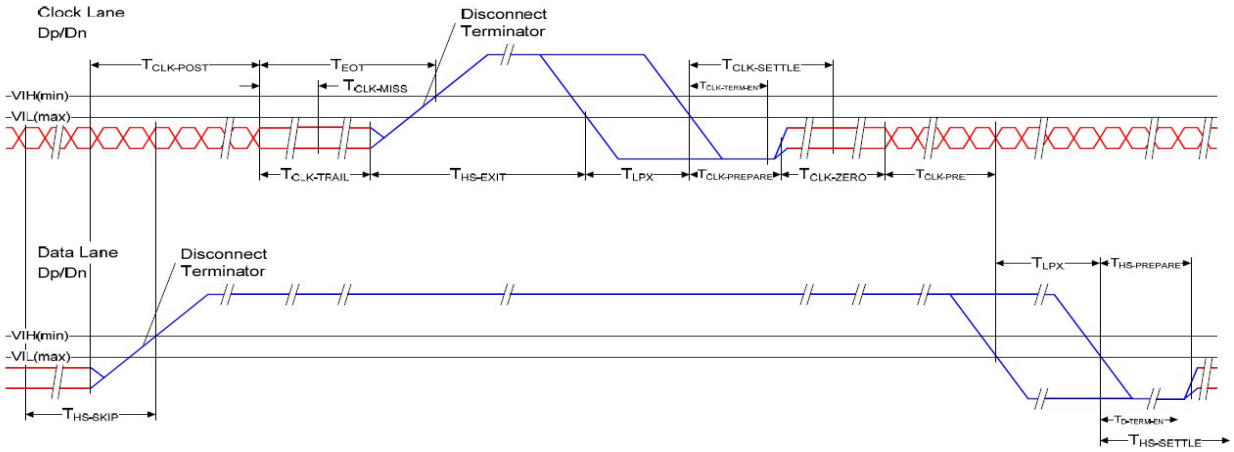
Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter	$T_{SKEW(TX)}$	-0.15	-	0.15	UI_{INST}
Data to Clock Setup time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to Clock Hold time(measured at receiver)	$T_{HOLD(RX)}$	0.15		-	UI_{INST}
20%~80% rise time and fall time	T_R, T_F	150	-	-	ps
		-	-	0.3	UI_{INST}



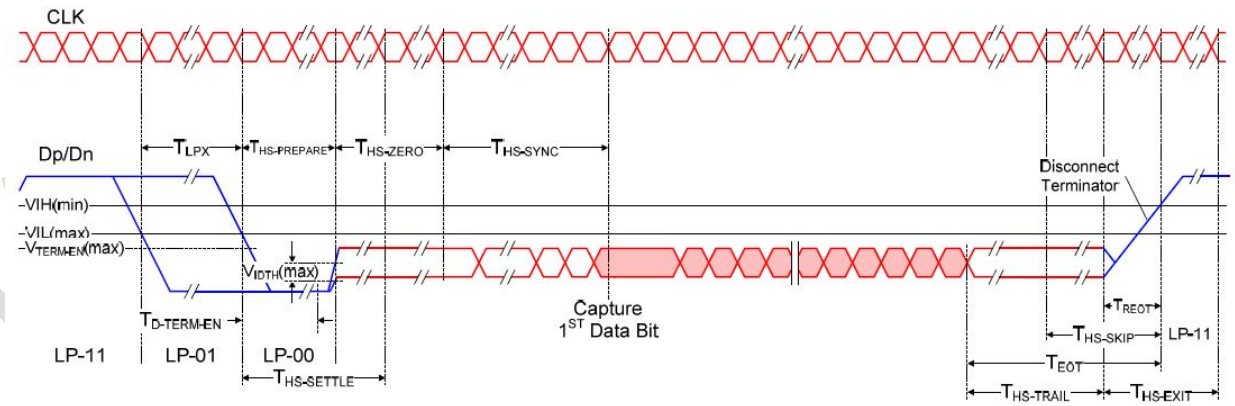
7.1.4. High Speed Clock Transmi

Parameter	Symbol	Min	Typ	Max	Unit s
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52 UI	-	--	ns
Detection time that the clock has stopped toggling	TCLK-MISS	—	—	60	ns
Time to drive LP-00 to prepare for HS clock	TCLK-PREPA	38	-	95	

transmission	RE				
Minimum lead HS-0 drive period before starting clock	TCLK-PREPARE + TCLK-ZERO	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn crossVIL,MAX	THS-TERM-EN	-	-	38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	TCLK-PRE	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns



7.1.5. High Speed Data Transmission in Bursts



When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low powe ode. If Date lane of TX chip

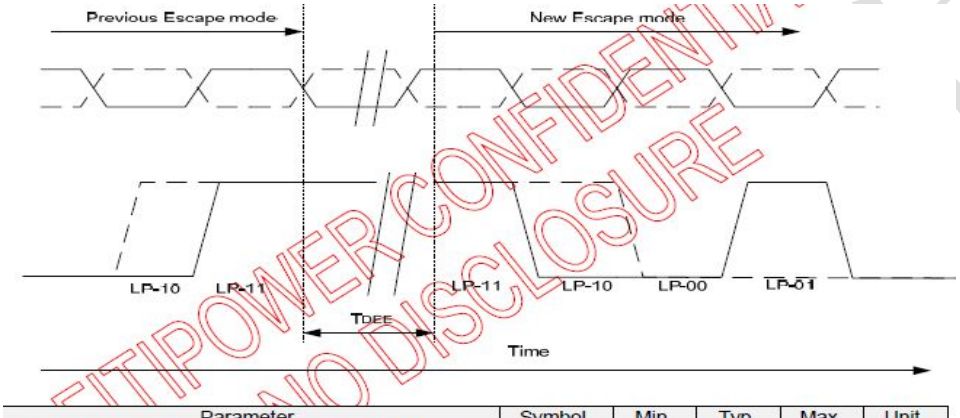
needs to transmit the next new data transmission or sequence,after the end of Low power mode or High speed moc
BTA. Then TX chip needs

to keep LP-11 stop statebefore the next new data transmission, no matter in Low power mode or High speed moc
BTA. TheLP-11

minimum timing is required for RX chip in the following 9 conditions, include of LP—LP, LP—HS, HS—LP, HS—H
TA— BTA, LP— BTA,

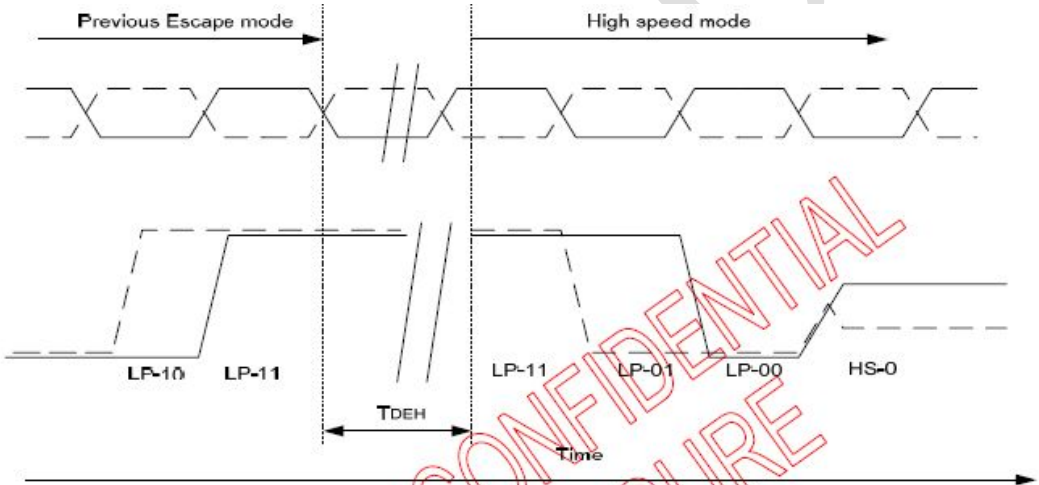
BTA— LP, HS— BTA, and BTA— HS.This rule is suitable for short or long packet between TX and RX data transmissio

(1) Timing between LP-LP command



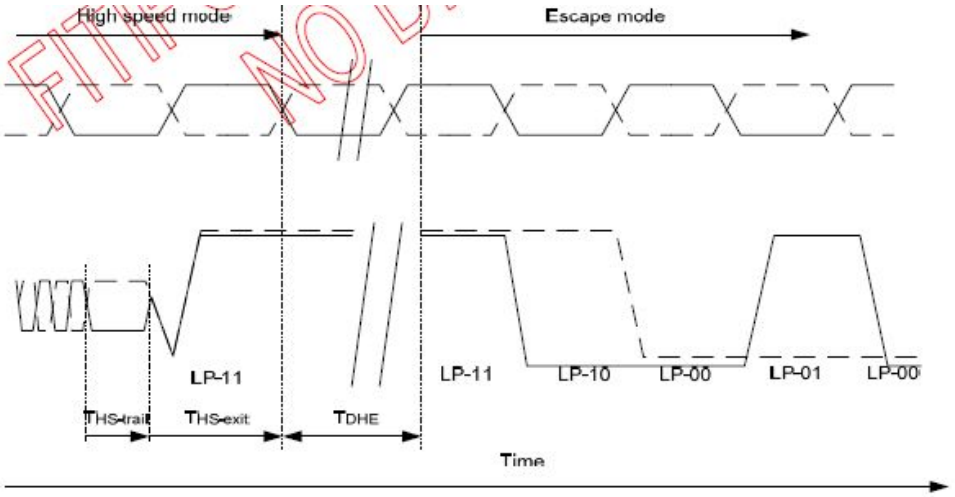
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new Escape Mode Entry	TDEE	150	-	-	ns

(2) Timing between LP-HS command



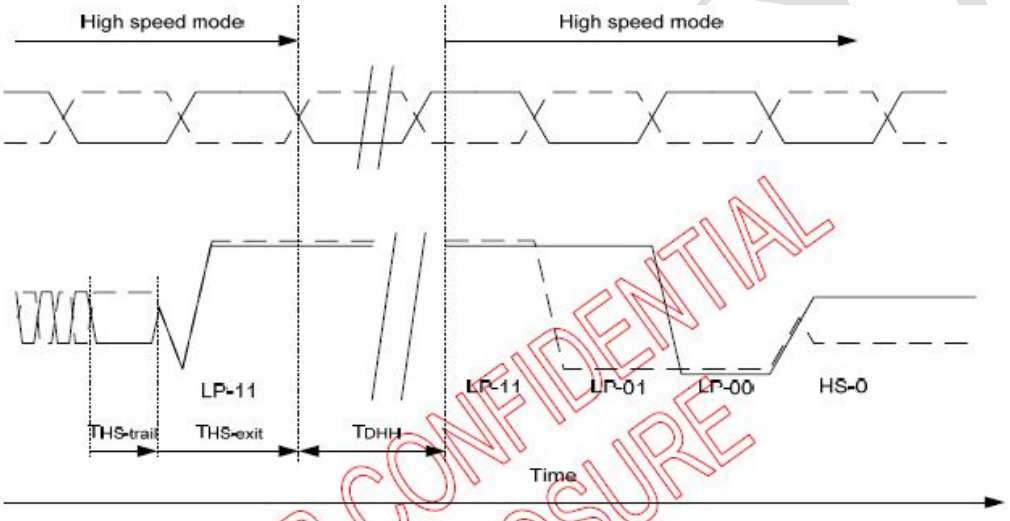
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDEH	Max(150,32UI)	-	-	ns

(3) Timing between HS-LP command



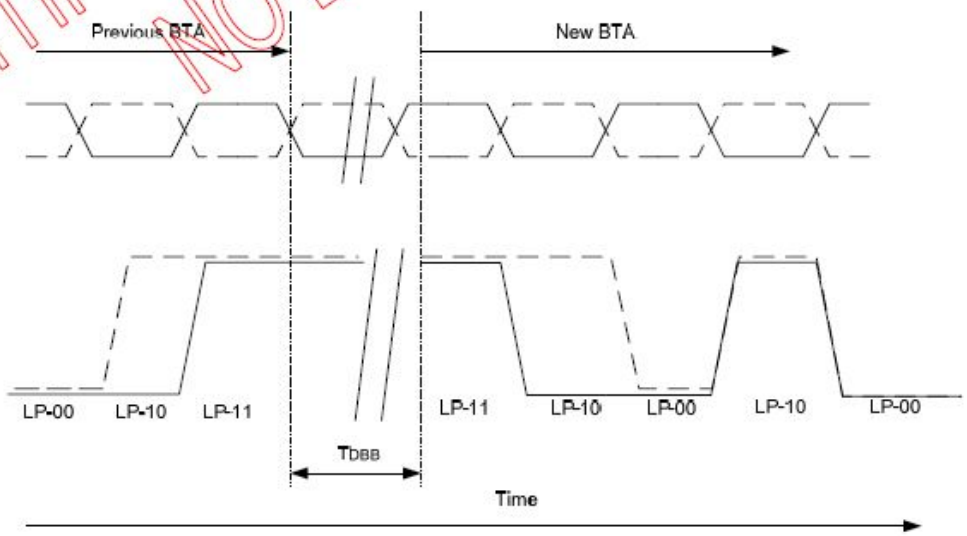
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDHE	Max(150,32UI)	-	-	ns

(4) Timing between HS-HS command



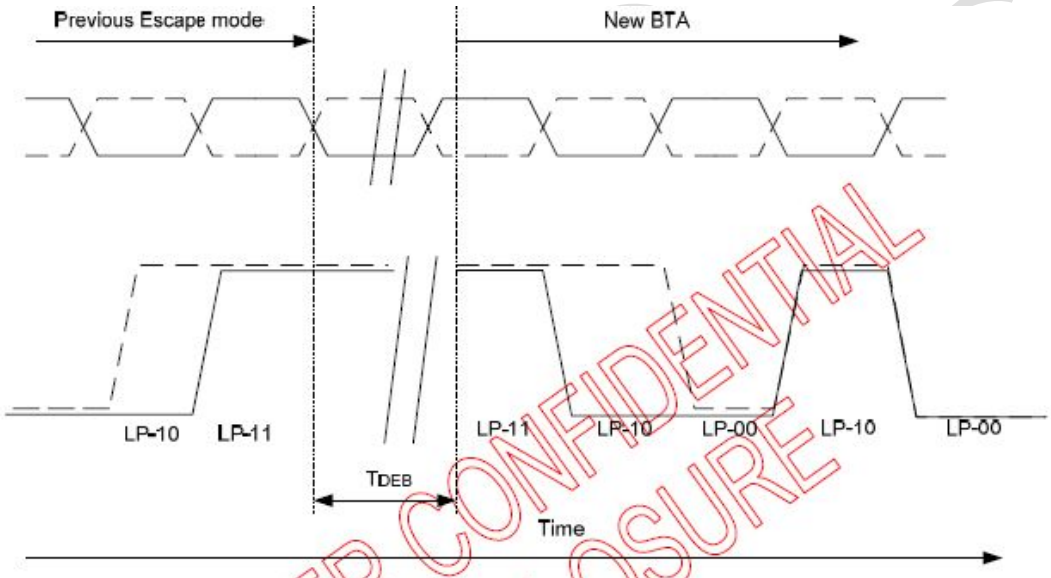
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDHH	Max(150,32UI)	-	-	ns

(5) Timing between BTA-BTA command



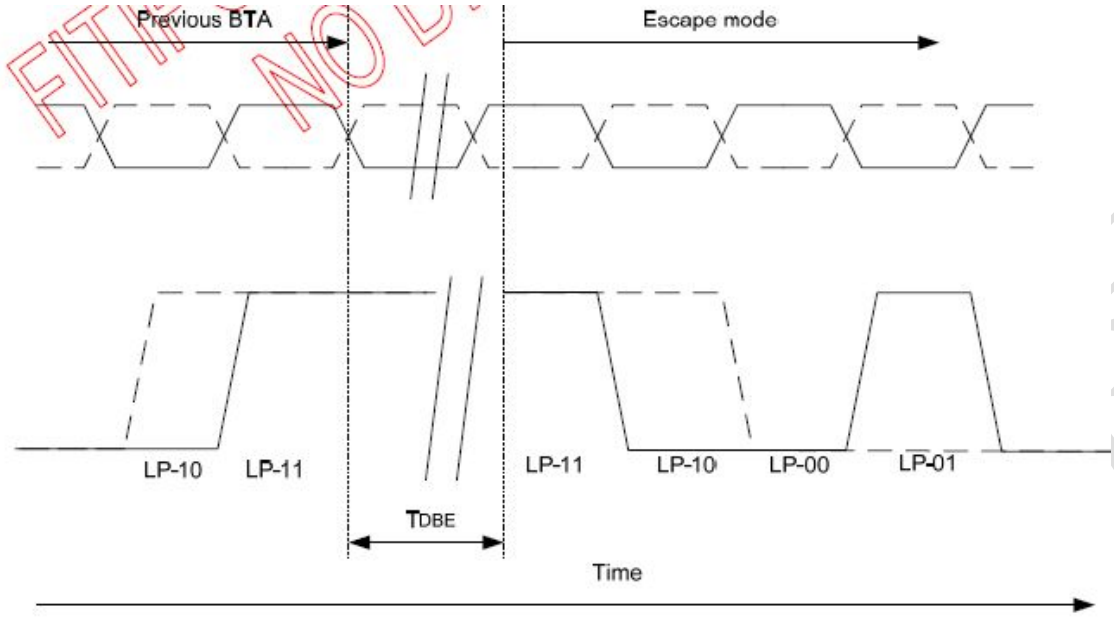
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	TDBB	150	-	-	ns

(6) Timing between LP-BTA command



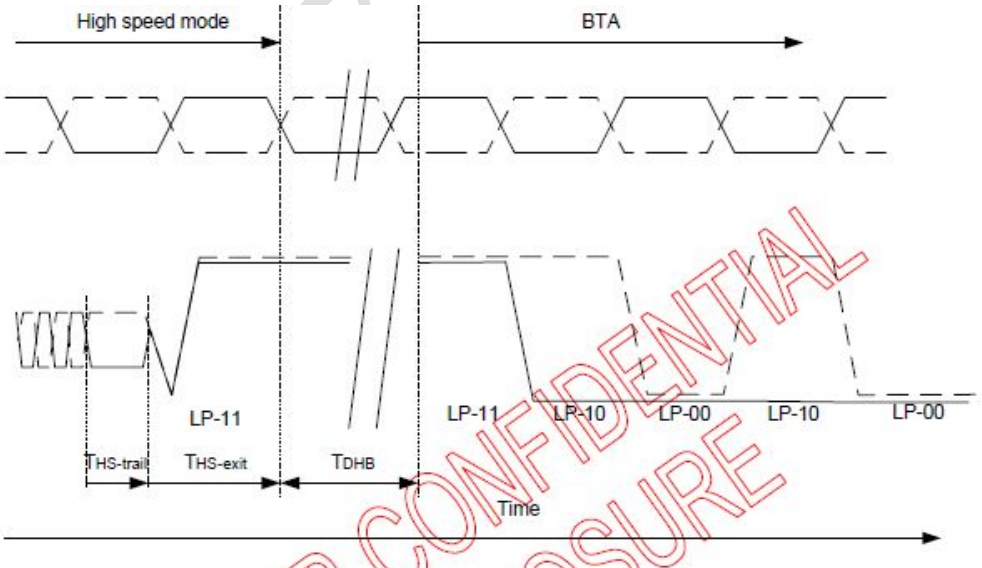
Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the new BTA	TDEB	150	-	-	ns

(7) Timing between BTA-LP command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Escape Mode Entry	TDBE	150	-	-	ns

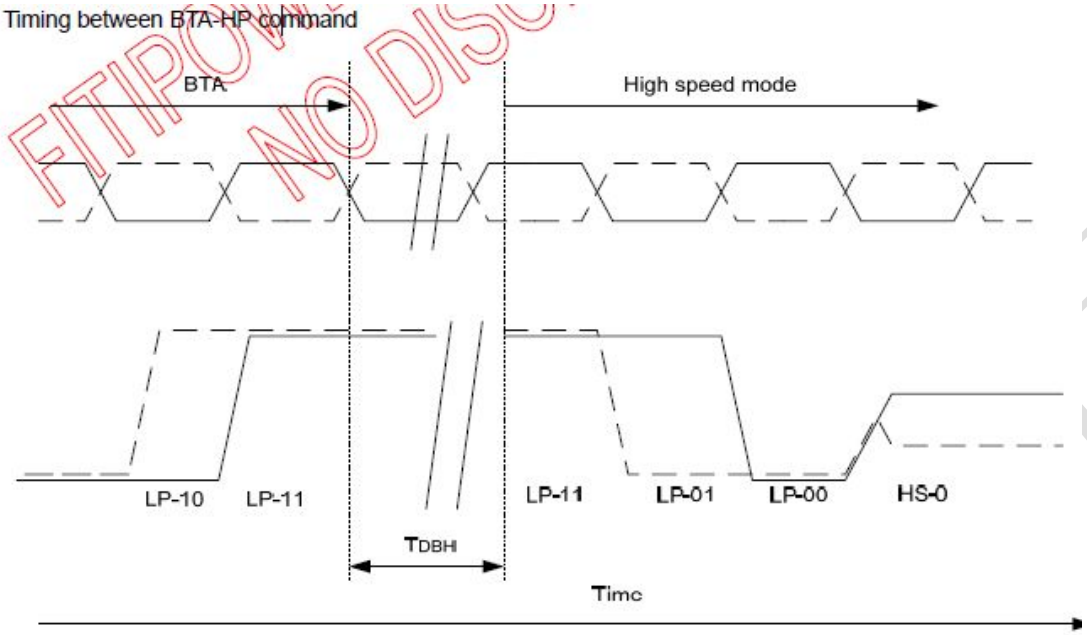
(8) Timing between HS-BTA command



Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the BTA	TDHB	Max(150,32UI)	-	-	ns

(9) Timing between BTA-HP command

(9) Timing between BTA-HP command

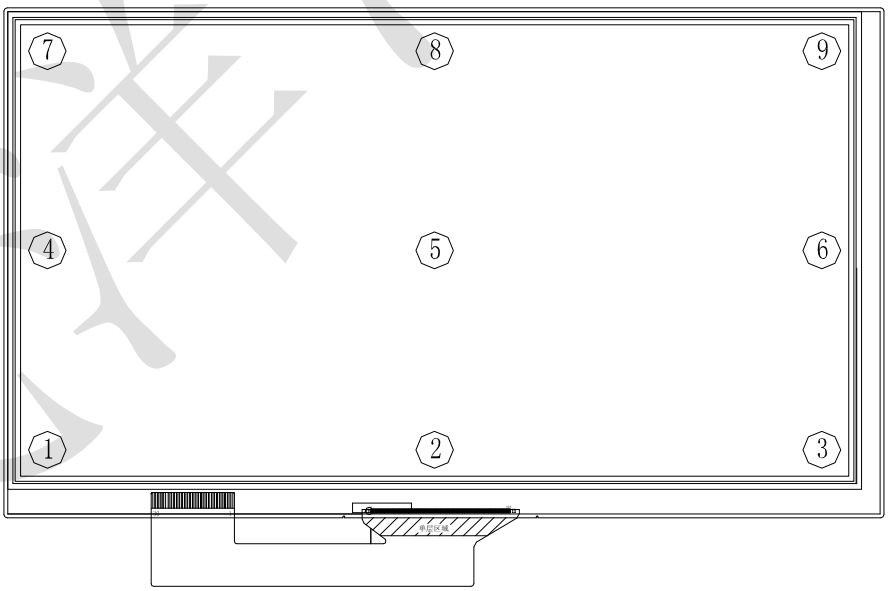


Parameter	Symbol	Min	Typ	Max	Unit
LP-11 delay to start of the Entering High Speed Mode	TDBH	Max(150,32UI)	-	-	ns

. OPTICAL CHARACTERISTICS

ITEM		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
Transmittance		T		3.8	4.1		%	
Contrast Ratio		CR	*1)	600	800	--	--	Note 3
Response Time		Tr+ Tf	*3)	-	25	40	ms	Note 4
NTSC				45%	50%	--		
Viewing Angle	Left	ϕ	CR≧10	80	85			
	Right	ϕ		80	85			Note 5
	Upper	θ		80	85			
	Lower	θ		80	85			
Color Filter Chromacicity with C light	White	x	θ=ϕ= 0°	0.27	0.290	0.31		Note 6
		y		0.311	0.331	0.351		
	Red	x	θ=ϕ= 0°	0.612	0.632	0.652		
		y		0.291	0.311	0.331		
	Green	x	θ=ϕ= 0°	0.277	0.297	0.317		
		y		0.516	0.536	0.556		
	Blue	x	θ=ϕ= 0°	0.12	0.140	0.16		
		y		0.134	0.154	0.174		

Note2: Definition of contrast ratio :
Contrast Ratio (CR)= (White) Luminance of ON ÷ (Black) Luminance of OFF



Note 3: Definition of Response Time.(White-Black)
The response time is defined as the time interval between the 10% and 90% amplitudes.

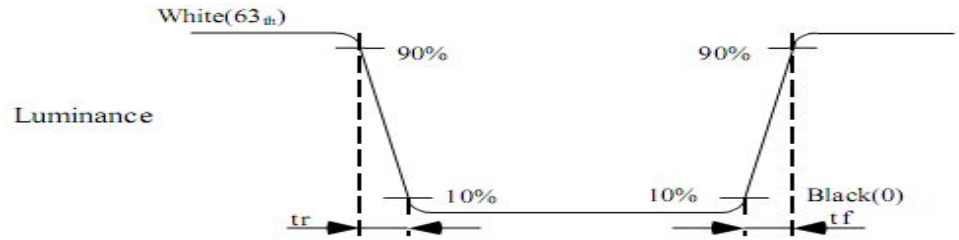


Fig. 6-2 Measuring point

Note 4: Definition of Viewing Angle(θ,ψ),refer to Fig.6 as below :

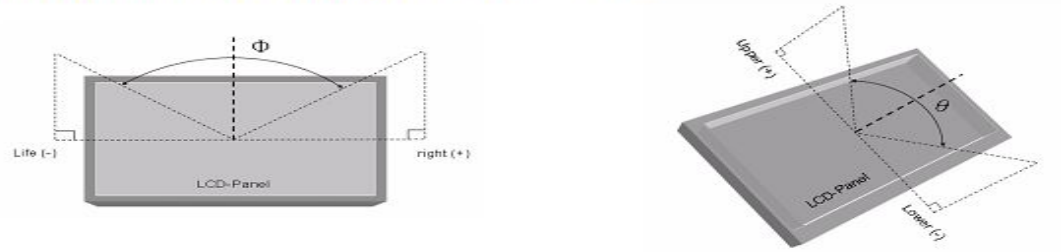


Fig.6-3 Definition of Viewing Angle

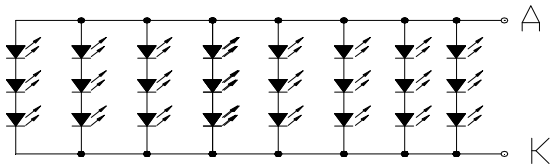
). Backlight Driving Section

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Voltage	VF	9	9.8	10.6	V	Note1
LED Current	IF	-	160	-	mA	
Life Time	-	-	(25,000)	-	hr	Note2;3
Number of LED	--	24			--	

Note 1: There are 1 Groups LED

Note 2: Ta = 25_

Note 3: Brightness to be decreased to 50% of the initial value



Vf=9~10.6V If=160mA

BLU CIRCUIT DIAGRAM

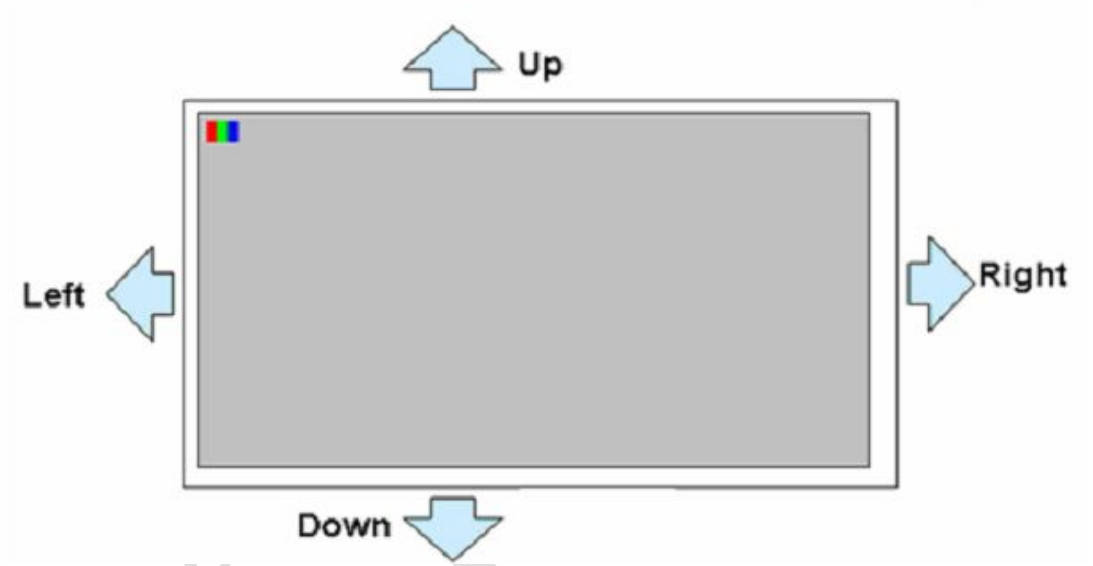
0. MIPI Interface Pin Function

Pin No. 序号	Symbol 符号	I/O	Description 描述	When not in use 不用时
30	VCOM	I	Common voltage	-
29	DVDD	I	Digital power	-
28	DVDD	I	Digital power	-
27	RESET	I	Global reset pin. Active low to enter reset state. Suggest to connecting with an RC reset circuit for stability Normally pull high. (R=10KΩ ， C=1μF) Standby mode, normally pull high STBYB=”1”, normal operation	-
26	STBYB	I	Standby mode, normally pull high STBYB=”1”, normal operation STBYB=”0”,timing control, source driver will turn off, all output are high-Z	DVDD
25	GND	P	Ground	-
24	MIPI_D0N	I	Negative MIPI differential data input	-
23	MIPI_D0P	I	Positive MIPI differential data input	-
22	GND	P	Ground	-
21	MIPI_D1N	I	Negative MIPI differential data input	-
20	MIPI_D1P	I	Positive MIPI differential data input	-
19	GND	P	Ground	
18	MIPI_CLKN	I	Negative MIPI differential clock input	
17	MIPI_CLKP	I	Positive MIPI differential clock input	
16	GND	P	Ground	-
15	MIPI_D2N	I	Negative MIPI differential data input	-
14	MIPI_D2P	I	Positive MIPI differential data input	-
13	GND	P	Ground	-
12	MIPI_D3N	I	Negative MIPI differential data input	-
11	MIPI_D3P	I	Positive MIPI differential data input	-
10	GND	P	Ground	-
9	AVDD	P	Power for Analog Circuit	--
8	LED-	LEDP	LED Cathode	-
7				
6	SHLR	I	Left or Right Display Control	-

5	UPDN	I	Up / Down Display Control	-
4	VGL	P	Negative power for TFT	-
3	VGH	P	Positive power for TFT	-
2	LED+		LED Anode	-
1				

【Note1】SHLR：left or right setting
UPDN：up or down setting

UPDN	SHLR	FUNCTION
0	1	Normal Display
0	0	Inverse Left and Right
1	1	Inverse Up and Down
1	0	Inverse Left and Right Inverse Up and Down



11. Caution

11.1 Handling of LCM

. Be sure to ground the body when handling the LCM.

. Don't give external shock

. Don't apply excessive force on the surface.

. Liquid in LCD is hazardous substance. Must not lick and swallow. When the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.

. Don't operate it above the absolute maximum rating.

. Don't disassemble the LCM

11.2 Storage

.Store in an ambient temperature of 5℃ to 45℃,and in a relative humidity of 40% to 60%. Don't expose to sunlight or intensive ultraviolet rays

. Storage in a clean environment, free from dust, active gas, and solvent.

. Store in anti-static electricity container.

. Store without any physical load.