( ) Preliminary Specifications
(V) Final Specifications

Module	5.5” Inch Color TFT-LCD
Model Name	G055HAN01.0

Customer	**Date**	**Approved by**	**Date**
		Grace Hung	2020/03/05
Checked & Approved by		**Prepared by**	
		Jon Tseng	2020/03/05
		General Display Business Unit / AU Optronics corporation	

2. General Description

This specification applies to the Color Active Matrix Liquid Crystal Display G055HAN01.0 composed of a TFT-LCD display, and a LED backlight system. The screen format is intended to support FHD (1080(H) x 1920(V)) screen and 16.7M (8-bits). All input signals are MIPI interface.

G055HAN01.0 designed with wide viewing angle; wide temperature and long life LED backlight is well suited for industial applications.

G055HAN01.0 is a RoHS product.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ºC condition:

Items	Unit	Specifications
Screen Diagonal	[inch]	5.46”
Active Area	[mm]	68.04 x 120.96
Pixels H x V		1080 x RGB x 1920
Pixel Pitch	[mm]	0.063 X 0.063
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
Nominal Input Voltage VDD	[Volt]	AVDD= 5, AVEE= -5,IOVCC= 1.8
Power Consumption	[Watt]	0.15W (max.)(w/o LED driver)
Weight	[Grams]	20g (max.)
Physical Size (type.)	[mm]	70.5(H) ×128.7(V) ×1.25 (T)
Electrical Interface		MIPI
Surface Treatment		HC
Support Color		16.7M colors
Temperature Range Operating Storage (Non-Operating)	 [ºC] [ºC]	 -20 to +70 -30 to +80
RoHS Compliance		RoHS Compliance

2.2 Display Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m2]	I_{LED}= 20 mA (*2 parallels) (center point)	400	500		1
Uniformity	%	9 points	80			2,3
Contrast Ratio				1000		4
Response Time	[msec]	Rising + Falling		25	30	
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	80 80	89 89		6
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	80 80	89 89		
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.598	0.648	0.698	
		Red y	0.287	0.337	0.387	
		Green x	0.254	0.304	0.354	
		Green y	0.564	0.614	0.664	
		Blue x	0.102	0.152	0.202	
		Blue y	0.014	0.064	0.114	
		White x	0.27	0.30	0.33	
		White y	0.30	0.33	0.36	
Color Gamut	%			70		

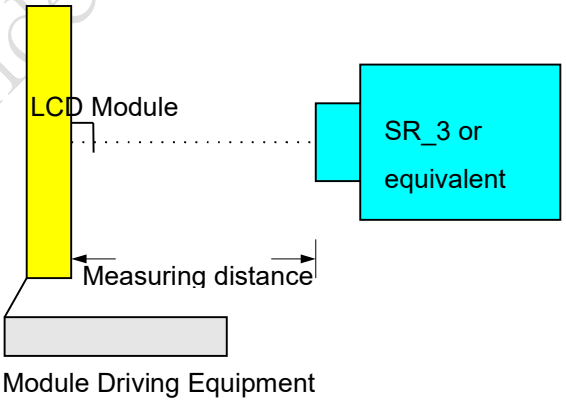
Note 1: Measurement method

1.1. Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

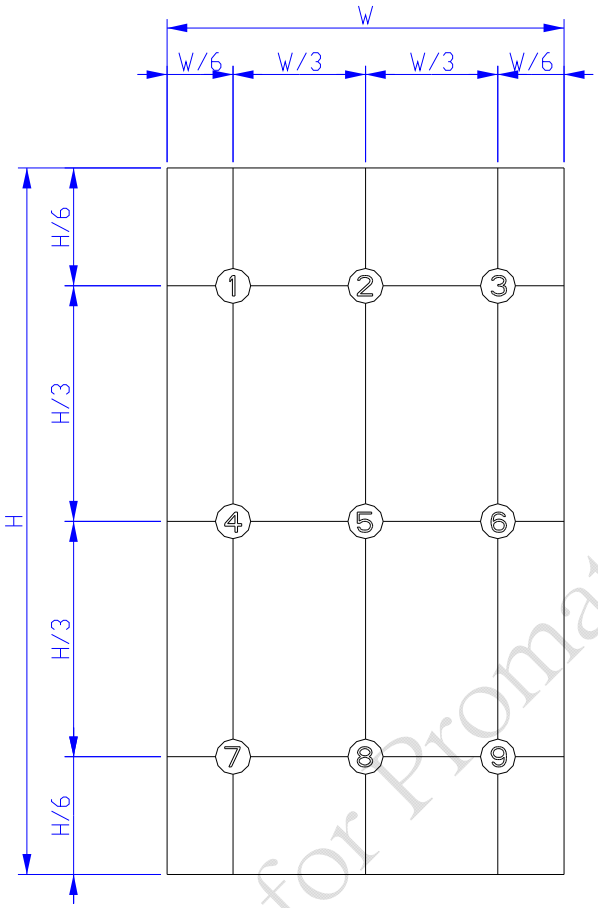
Aperture 1° with 50cm viewing distance

Test Point Center

Environment *< 1 lux*



Note 2: Definition of 9 points position (Display active area: 68.04 x 120.96)



Note 3: The luminance uniformity of 9 points is defined by dividing the minimum luminance values by the maximum test point luminance

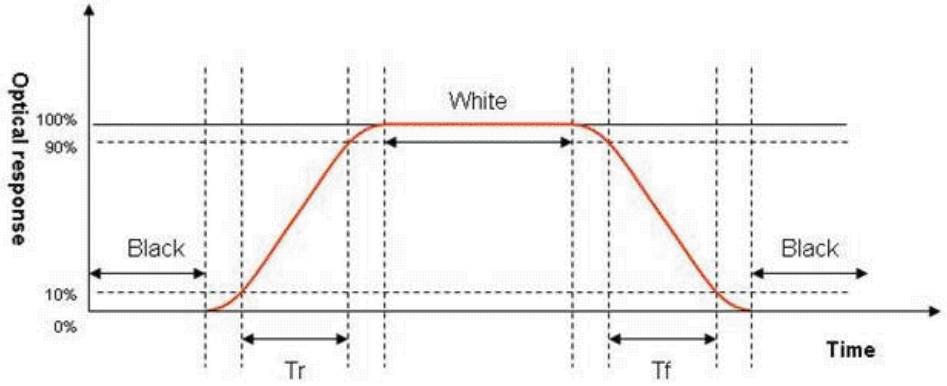
$$\delta_{W9} = \frac{\text{Minimum Brightness of 9 points}}{\text{Maximum Brightness of 9 points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

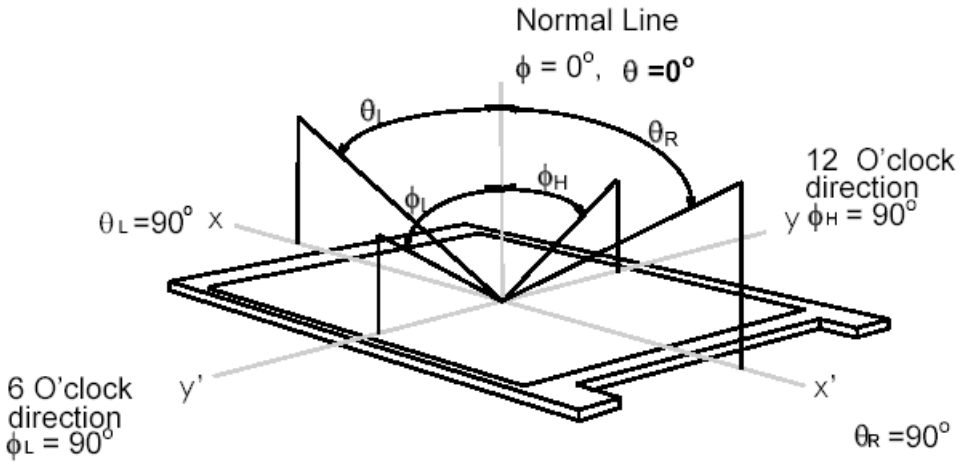
Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



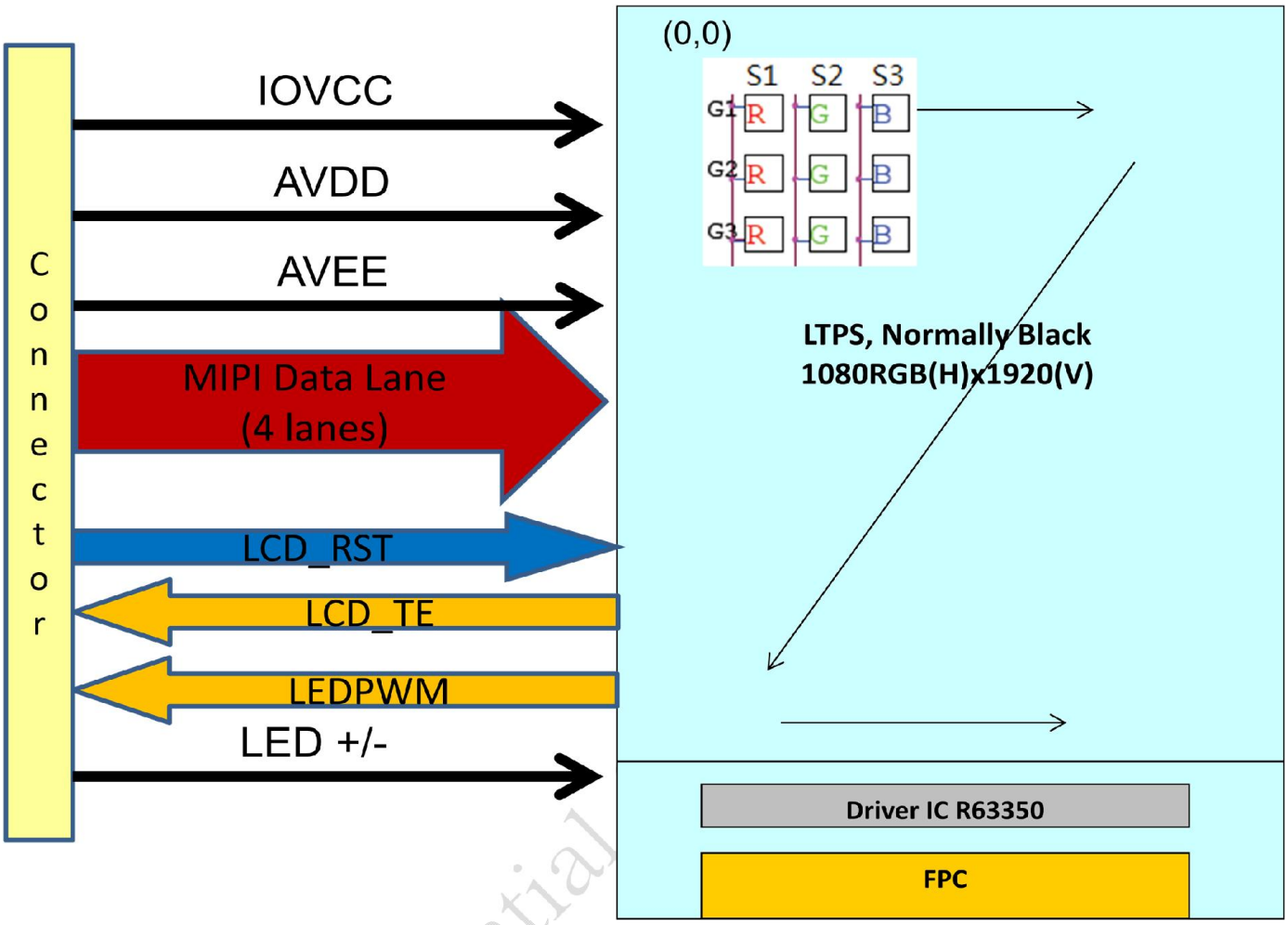
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 5.5 inch color TFT/LCD module:



4. Absolute Maximum Ratings

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit
Analog Supply Voltage	AVDD	-0.3	6.5	[Volt]
Analog Supply Voltage	AVEE	-6.5	0.3	[Volt]
Supply Voltage for IO	IOVCC	-0.3	4.6	[Volt]
Input Voltage	VIN	-0.3	IOVCC+0.3	[Volt]

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	-20	70	[°C]
Storage Temperature	TST	-30	80	[°C]

Note: Maximum Wet-Bulb should be 39 °C and no condensation.

5. Electrical Characteristics

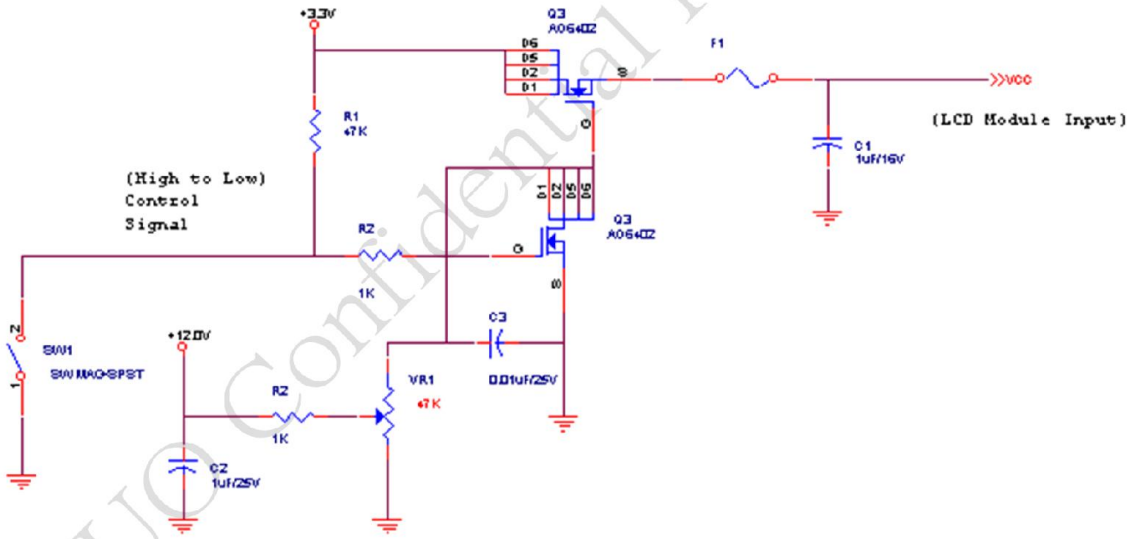
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are shown as follows;

Symbol	Parameter	Min	Typ	Max	Units	Remark
AVDD	Analog Supply Voltage	4.5	5.0	5.5	[Volt]	
AVEE	Analog Supply Voltage	-5.5	-5.0	-4.5	[Volt]	
IOVCC	Supply Voltage for IO	1.62	1.80	1.98	[Volt]	
IAVDD	AVDD Current	-	10	14	[mA]	Note 1
IAVEE	AVEE Current	-	6.2	10	[mA]	Note 1
IIOVCC	IOVCC Current	-	14	16	[mA]	Note 1
VIH	Input high-level Voltage	0.7 x IOVCC	-	IOVCC	[Volt]	
VIL	Input low-level Voltage	0	-	0.3 x IOVCC	[Volt]	
VOH	Output high-level Voltage	0.8 x IOVCC	-	IOVCC	[Volt]	
VOL	Output low-level Voltage	0	-	0.2 x IOVCC	[Volt]	

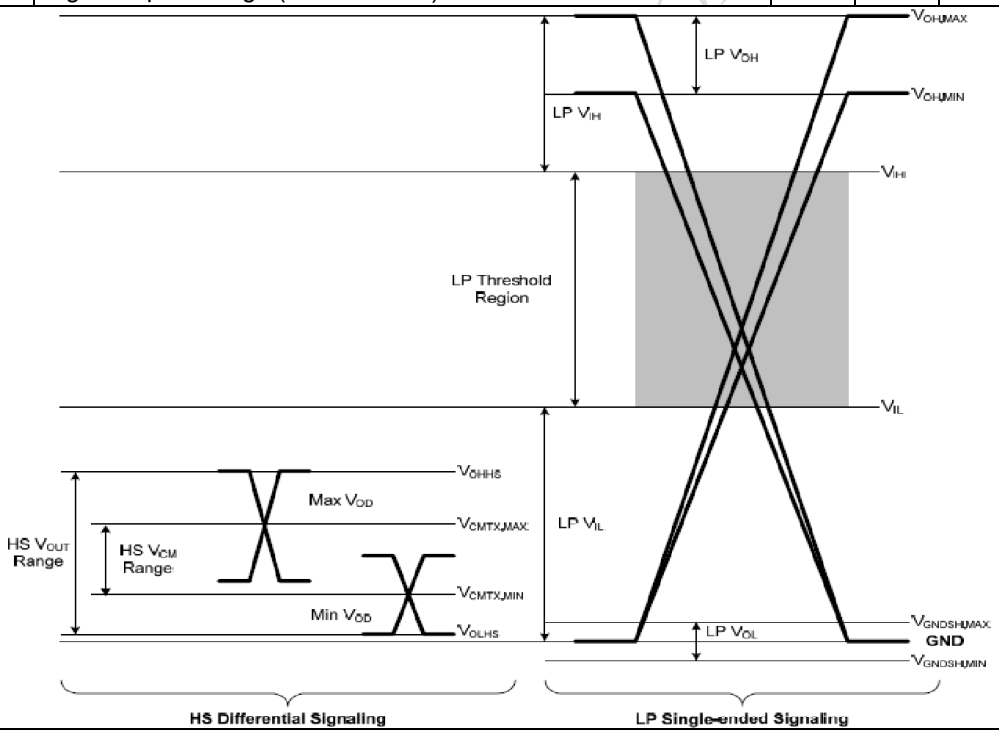
Note 1: Measurement condition:



5.1.2 Signal Electrical Characteristics

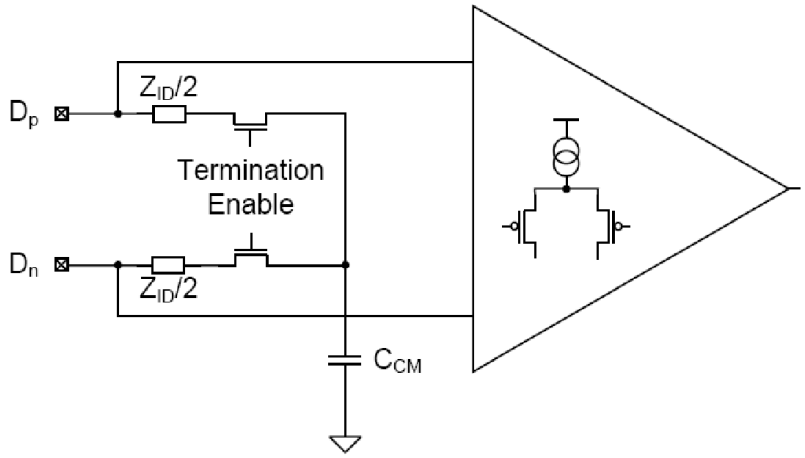
- MIPI DC characteristics are as follows :

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	155	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV



MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

- HS RX Scheme

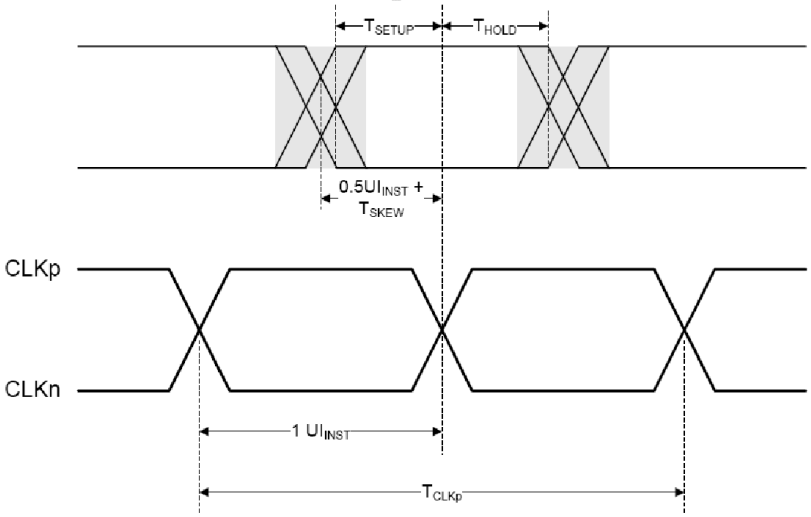


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.25			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.25			UI_{INST}	2

Note:

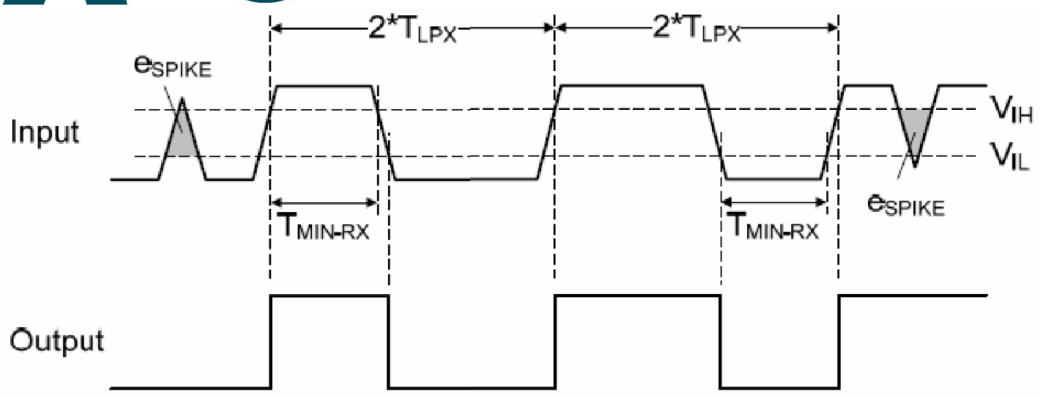
1. Total silicon and package delay budget of 0.25*UI_{INST}
2. Total setup and hold window for receiver of 0.5 *UI_{INST}

- High Speed Data Transmission: Data to Clock Timing

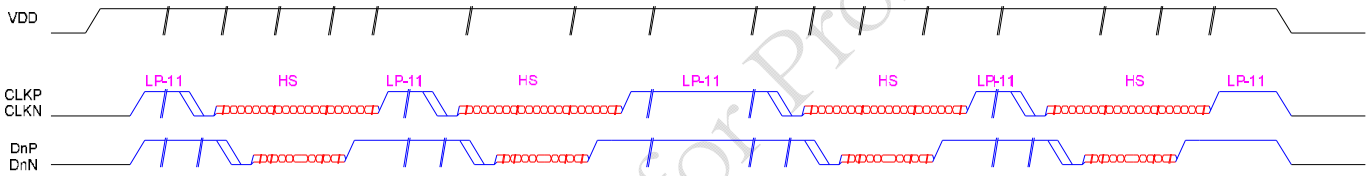


LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

- Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns

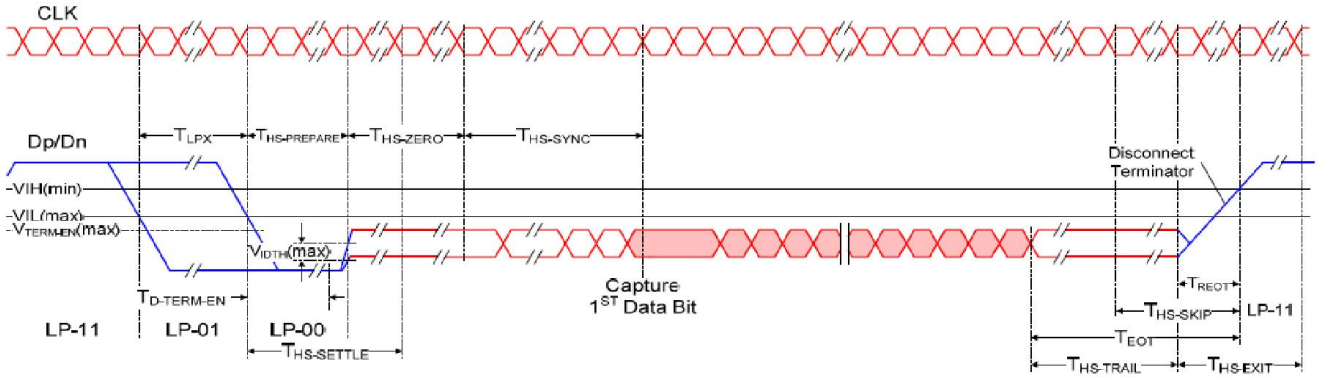
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	

TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

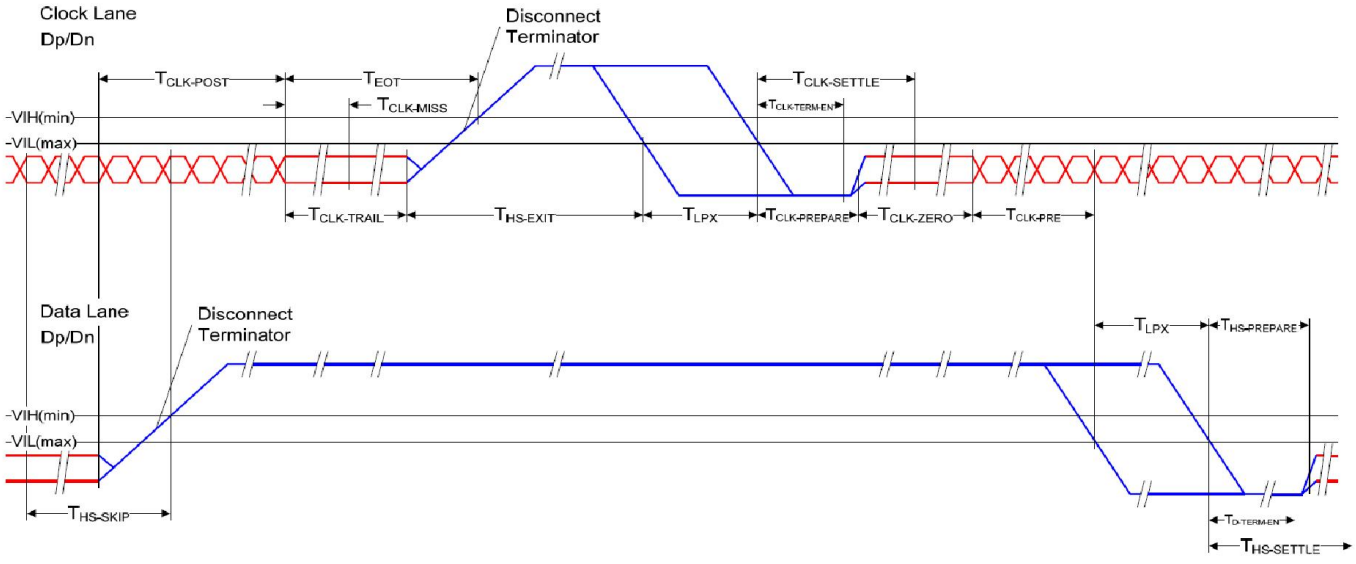
Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
3. The I-chip of AUO use is not support BTA (BTA define ignore).

- High-Speed Data Transmission in Bursts



- Switching the Clock Lane between Clock Transmission and Low-Power Mode



5.2 Backlight Unit

5.2.1 Parameter guideline for LED

Following characteristics are measured under a stable condition using an inverter at 25℃ (Room Temperature):

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
IF	LED Forward Current	-	20	-	mA	Ta = 25°C 40 mA for 2 parallel
VLED	LED Forward Voltage	-	21.35		[Volt]	I_F = 20 mA, Ta = 25°C
PLED	LED Power Consumption	-	0.854		Watt	I_F = 20 mA, Ta = 25°C w/o efficiency
LED life time		15,000	-	-	Hrs	I_F = 20 mA, Ta = 25°C

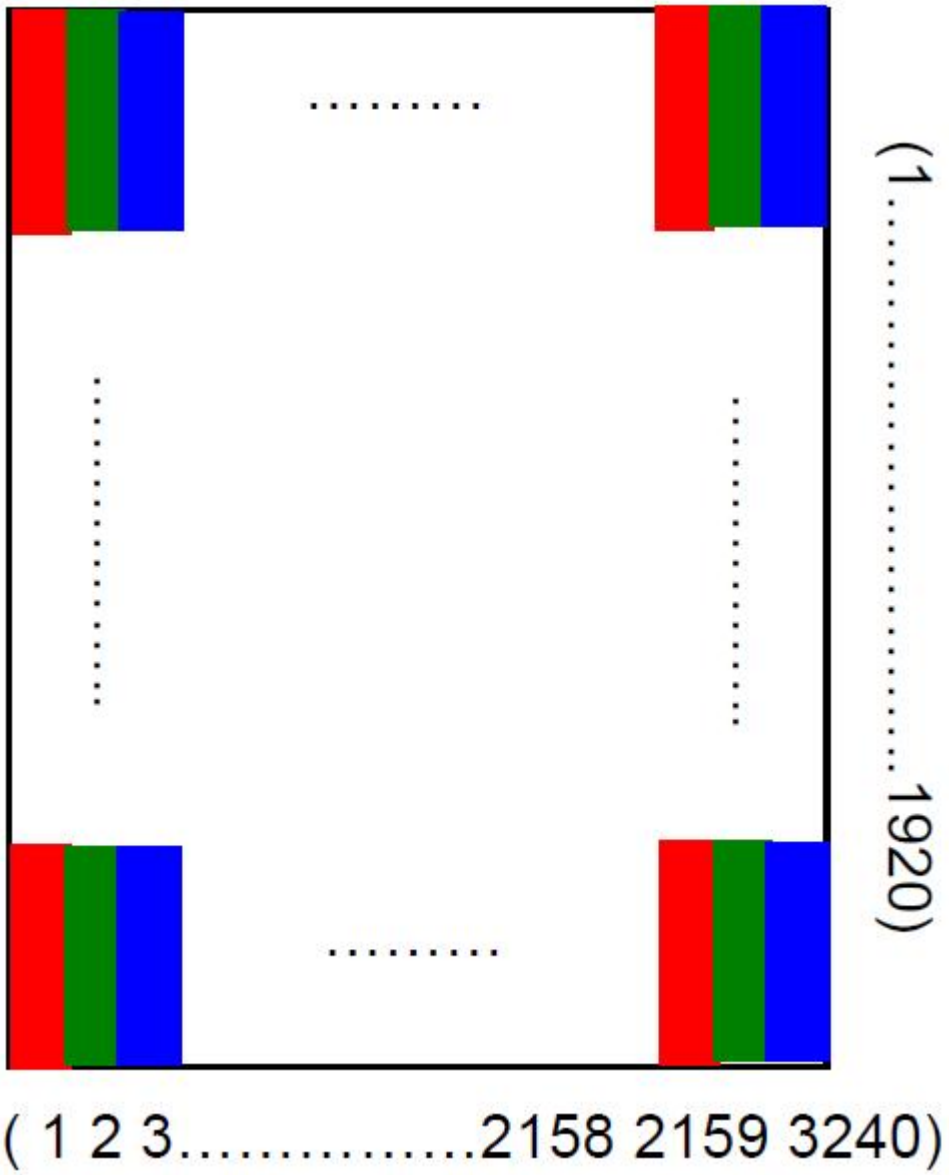
Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Signal Description

6.2.1 LCD MIPI Interface pin description

Pin no	Symbol	Description	Remark
1	LEDA	LED Anode	
2	LEDA	LED Anode	
3	LEDK1	LED Cathode	
4	LEDK2	LED Cathode	
5	NC	NO connection	
6	GND	GND for internal logic and interface pins. GND=0V.	
7	AVDD	Power supply to analog circuit.	
8	AVEE	Power supply to analog circuit.	
9	IOVCC	Power supply to interface pins.	
10	GND	GND for internal logic and interface pins. GND=0V.	
11	LCD_RST	Reset pin.	
12	LCD_TE	Tearing effect output signal. By register settings, it can be used as a verify signal for NVM write. Leave it open when not in use.	
13	GND	GND for internal logic and interface pins. GND=0V.	
14	LEDPWM	Control signal for brightness of LED backlight.	
15	GND	GND for internal logic and interface pins. GND=0V.	
16	MIPI_D2P+	Mipi Differential signal D2+	
17	MIPI_D2N-	Mipi Differential signal D2-	
18	GND	GND for internal logic and interface pins. GND=0V.	
19	MIPI_D1P+	Mipi Differential signal D1+	
20	MIPI_D1N-	Mipi Differential signal D1-	
21	GND	GND for internal logic and interface pins. GND=0V.	
22	MIPI_CLKP+	Mipi Differential signal Clock+	
23	MIPI_CLKN-	Mipi Differential signal Clock-	
24	GND	GND for internal logic and interface pins. GND=0V.	
25	MIPI_D0P+	Mipi Differential signal D0+	
26	MIPI_D0N-	Mipi Differential signal D0-	
27	GND	GND for internal logic and interface pins. GND=0V.	
28	MIPI_D3P+	Mipi Differential signal D3+	
29	MIPI_D3N-	Mipi Differential signal D3-	
30	GND	GND for internal logic and interface pins. GND=0V.	

6.2.2 LCD Connector

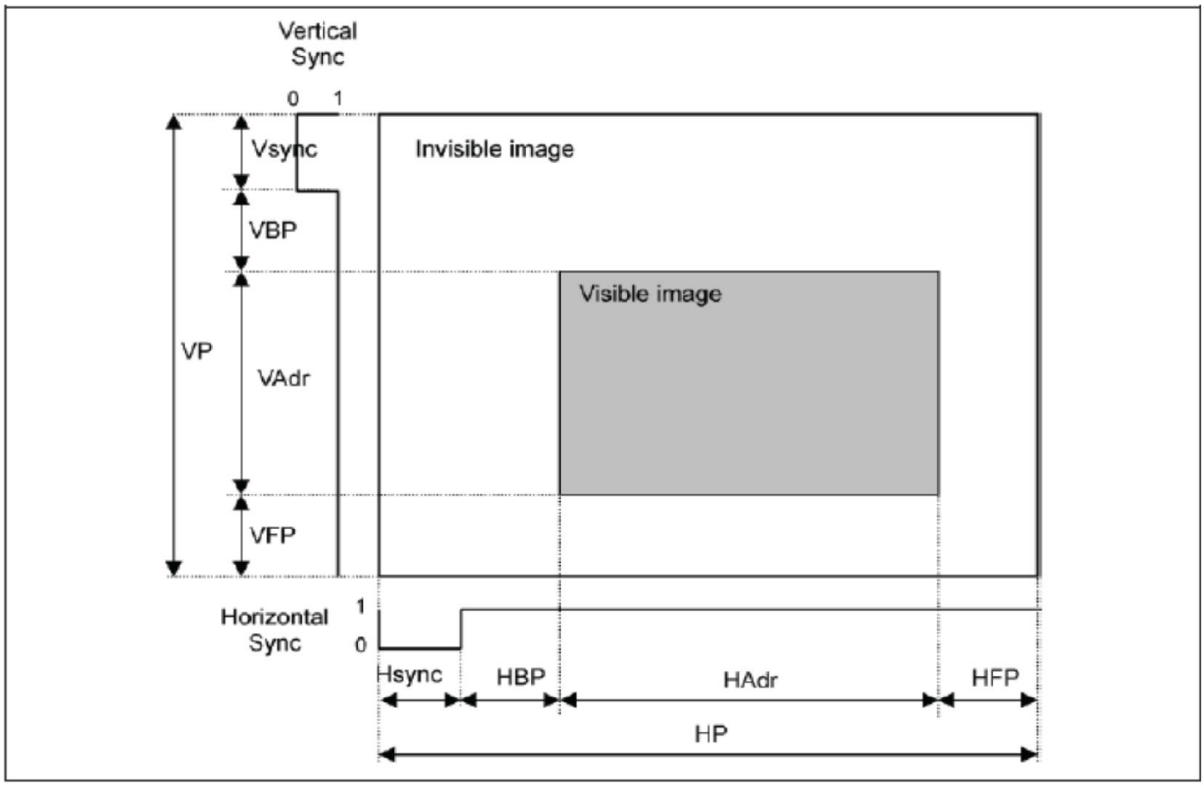
Connector Name / Designation	Signal Connector
Manufacturer	Hirose or compatible
Connector Model Number	FPC type
Adaptable Plug	FH34SRJ-30S-0.5SH(50) or compatible

6.3 Interface Timing

● Timing Characteristics

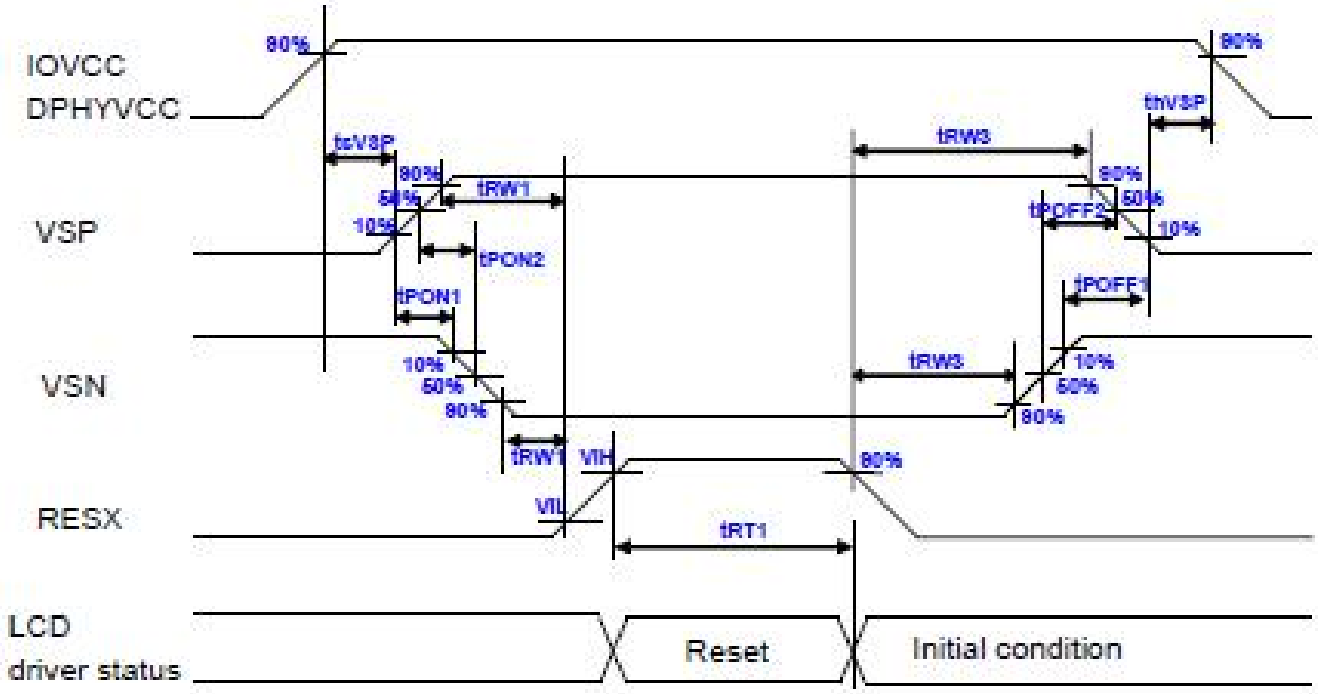
● Basically, interface timings should match the 720 x 1280 /60 Hz manufacturing guide line timing.

ITEM			SYNBOL	min	typ	max	UNIT
LCD	Frame Rate		-		60		Hz
Timing	DCLK	Frequency	fCLK		70.45		MHz
	Horizontal	Horizontal total time	tHP		1200		t_{CLK}
		Horizontal Active time	tHadr		1080		t_{CLK}
		Horizontal Pulse Width	tHsync		20		t_{CLK}
		Horizontal Back Porch	tHBP		20		t_{CLK}
		Horizontal Front Porch	tHFP		80	-	t_{CLK}
	Vertical	Vertical total time	tvp		1957		t_H
		Vertical Active time	tVadr		1920		t_H
		Vertical Pulse Width	tVsync		2	-	t_H
		Vertical Back Porch	tVBP		31	-	t_H
		Vertical Front Porch	tVFP		4	-	t_H
Pixel Fomat					8		Data bit/ pixel
Lane					4		Lane



6.4 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



Item	Symbol	Unit	Test Condition	Min.	Max.
VSP-VSN delay time(10% to 10%)	tPON1	us	Power On	0	-
VSP-VSN delay time(50% to 50%)	tPON2	us	Power On	0	-
System power on to VSP ON time	tsVSP	ms	Power On	1	-
VSN-VSP delay time(10% to 10%)	tPOFF1	us	Power Off	0	-
VSN-VSP delay time(50% to 50%)	tPOFF2	us	Power Off	0	-
VSP OFF to system power off time	thVSP	us	Power Off	0	-

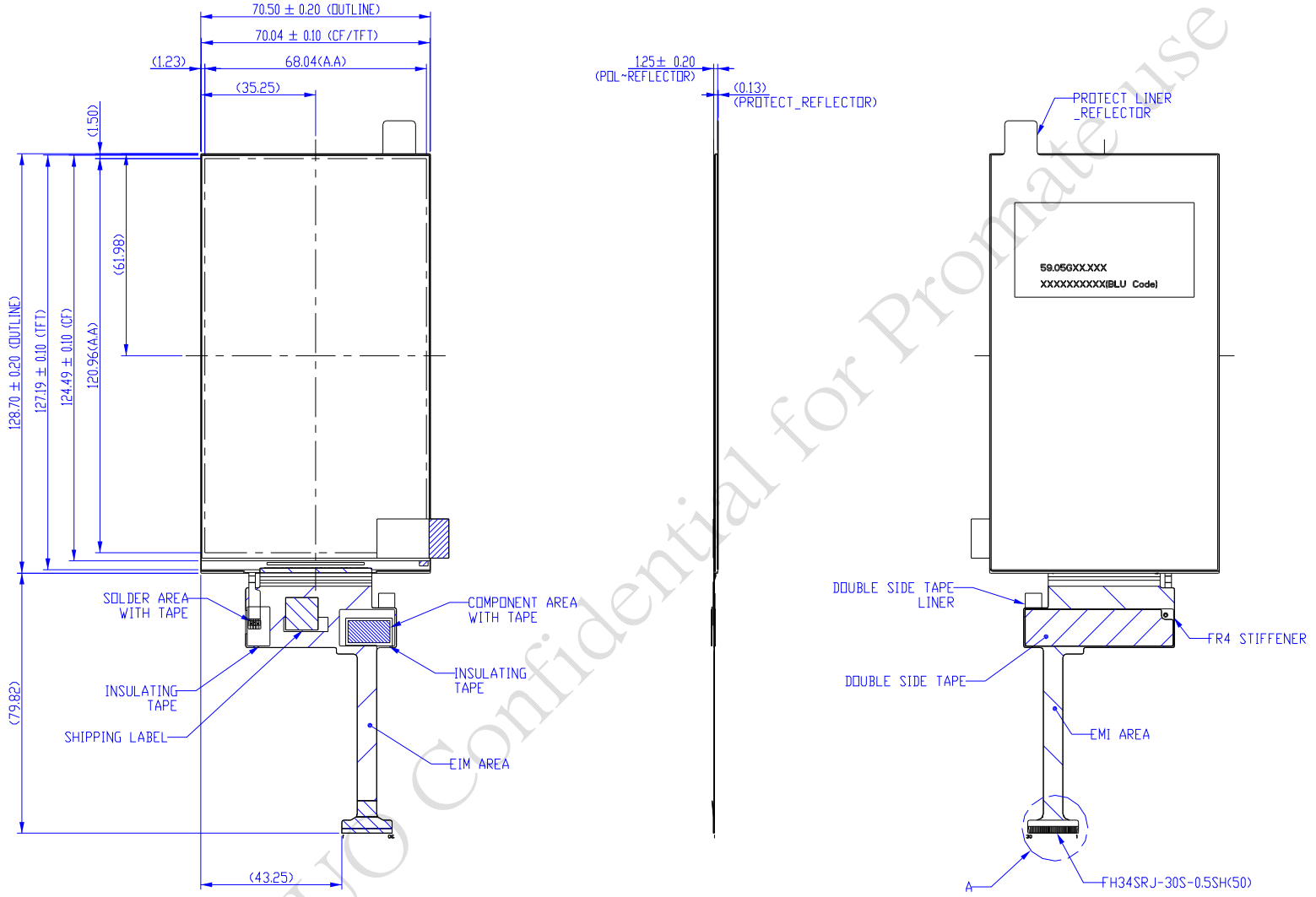
7. Reliability Test Criteria

Items	Required Condition	Note
Temperature Humidity Bias	60 °C, 90%RH, 240 hours	
High Temperature Operation	70 °C, 240 hours	
Low Temperature Operation	-20 °C, 240 hours	
Hot Storage	80 °C, 240 hours	
Cold Storage	-30 °C, 240 hours	
Thermal Shock Test	-30 °C / 1 hr, 70 °C / 1 hr, 50cycles	
EMI	30M~230MHz : under 24dB 231M~1GHz : under 31dB	
ESD	Contact : ±4KV Air : ±8KV	

Note1:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- In the standard condition, there is not display function NG issue occurred.

8. Mechanical Characteristics



9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

Size: 10mm x 10mm

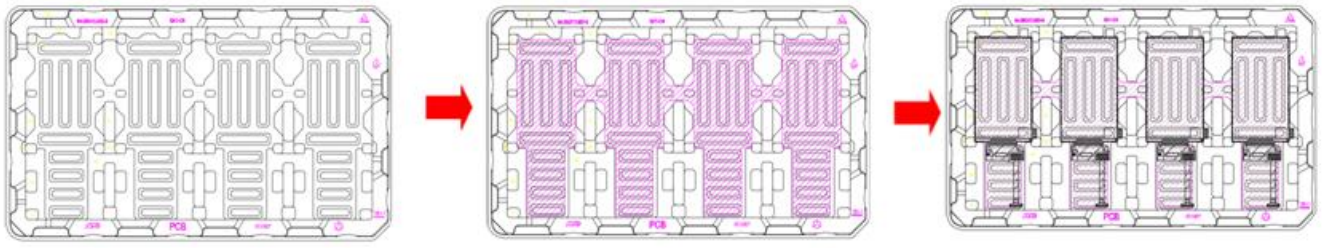
Label size : 10 x 10 mm
Label thickness: 0.072mm

- **QR code size : 6.4 x 6.4**

9.2 Carton/Pallet Package

包裝流程圖
(初略圖例說明示意圖)

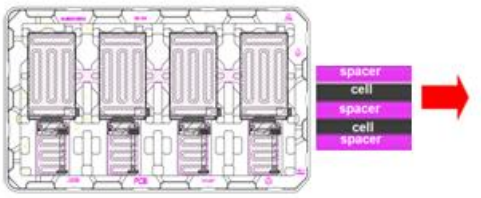
Packing instruction
(Brief Illustration)



PET Tray

3 PCS EPE Spacer/ 1Tray

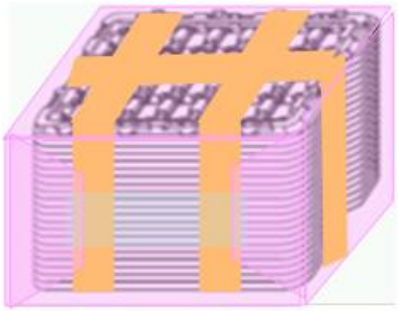
1 tray contains 8 modules.
The display is face up.



1 PCS Tray+3 PCS EPE Spacer
8 PCS Panel

Should be turned 180˚ and then stacked.
18tray + 1dummy tray

Taped the package by as showed method Double Cross.



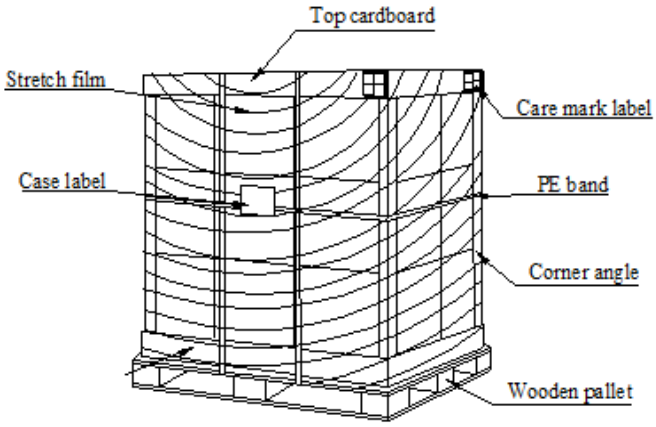
Antistatic Bag Pack the bag, and then tape with scotch tape.

Placing EPE SET into carton such as left-top picture.

The cushion of this product is EPE Box.

Cover with EPE Cushion on top

To pack the box by scotch tape as H shape.



Max capacity：144 module per carton

Max weight：6.7 kg per carton

Outside dimension of carton：520mm(L)* 340mm(W)*250mm(H)

Pallet size：1150 mm * 1070 mm * 135mm New T42

Max module by air：(2 *3) *5 layers, one pallet put 30 boxes, total 4320 pcs module

Max module by sea：(2 *3) *5 layers, one pallet put 30 boxes, total 4320 pcs module

Max module by sea_HQ：(2 *3) *5 layers, one pallet put 30 boxes, total 4320 pcs module

10 Safety

10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

10.2 Materials

10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

UL 60950-1 second edition	U.S.A. Information Technology Equipment