N and P Channel Enhancement Mode Power MOSFET

Description

This Product uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

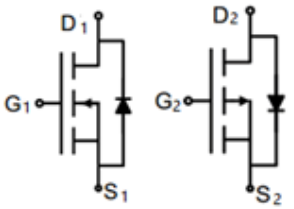
General Features

- **NMOS**
- V_{DS} 100V
- I_D (at V_{GS} = 10V) 5A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 170mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 180mΩ

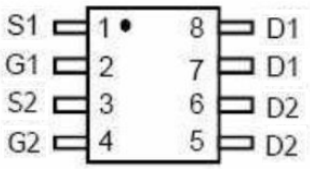
- **PMOS**
- V_{DS} -100V
- I_D (at V_{GS} = 10V) -6A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 200mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

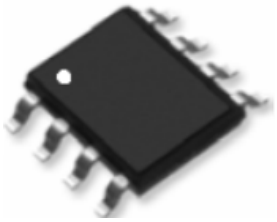
- Power switch
- DC/DC converters



Schematic diagram



Marking and pin assignment



SOP-8

Device	Package	Marking	Packaging
G05NP10S	SOP-8双基	G05NP10	4000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	100	-100	V
Continuous Drain Current	I_D	5	-6	A
Pulsed Drain Current (note1)	I_{DM}	20	-24	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	3	2.5	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

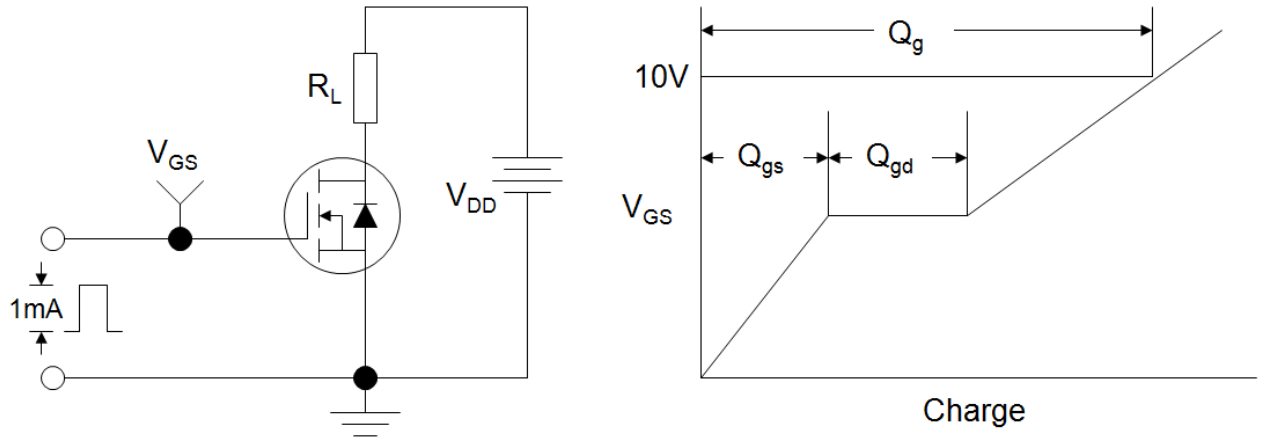
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	41.7	50	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 100V, V_{GS} = 0V, T_J = 25ºC	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1	2.2	3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 1A	--	127	170	mΩ
		V_{GS} = 4.5V, I_D = 1A	--	144	180	
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=5A	--	8	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	--	797	--	pF
Output Capacitance	C_{oss}		--	138	--	
Reverse Transfer Capacitance	C_{rss}		--	104	--	
Total Gate Charge	Q_g	V_{DD} = 50V, I_D = 5A, V_{GS} = 10V	--	18	--	nC
Gate-Source Charge	Q_{gs}		--	3.7	--	
Gate-Drain Charge	Q_{gd}		--	5.4	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30V, I_D = 2A, R_G = 2.5Ω	--	12	--	ns
Turn-on Rise Time	t_r		--	9.4	--	
Turn-off Delay Time	$t_{d(off)}$		--	37	--	
Turn-off Fall Time	t_f		--	11.1	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	6	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 6A, V_{GS} = 0V	--	--	1.2	V

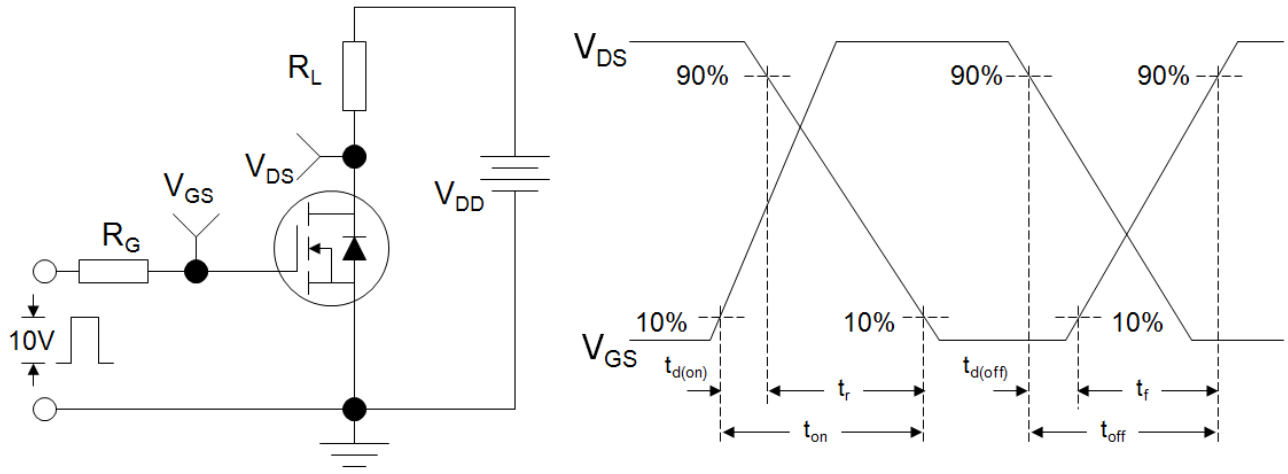
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

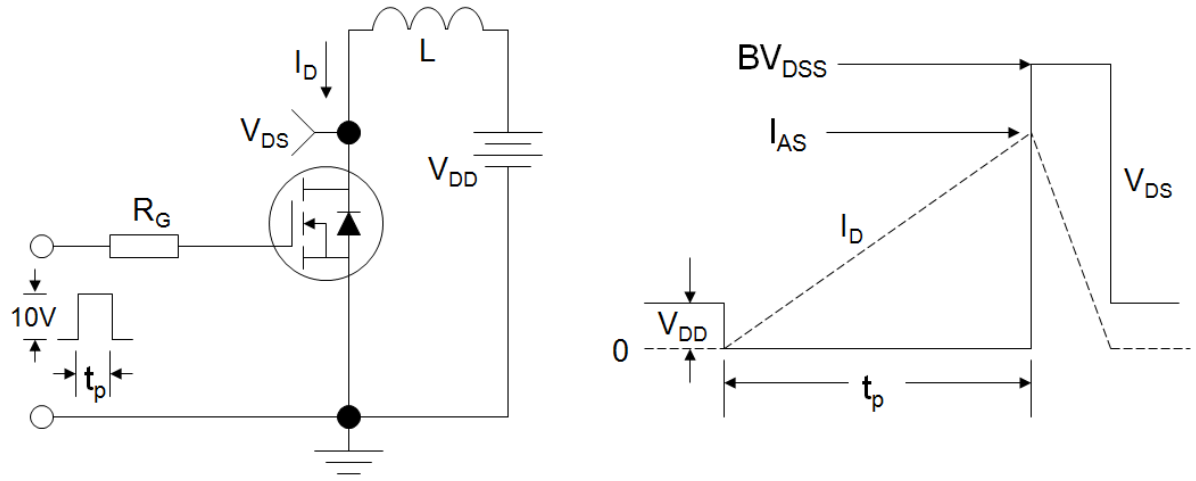
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

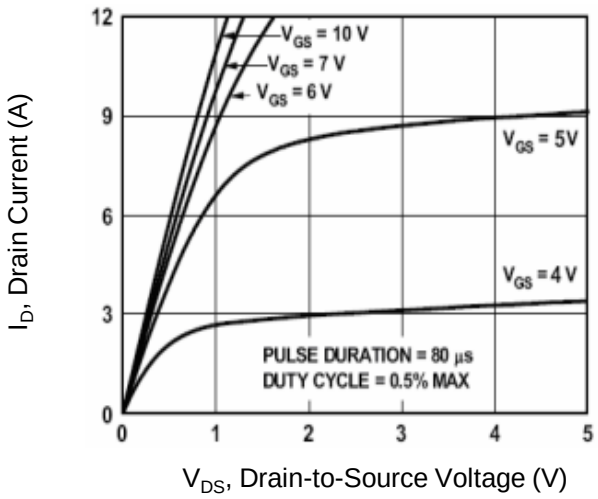


Figure 2. Transfer Characteristics

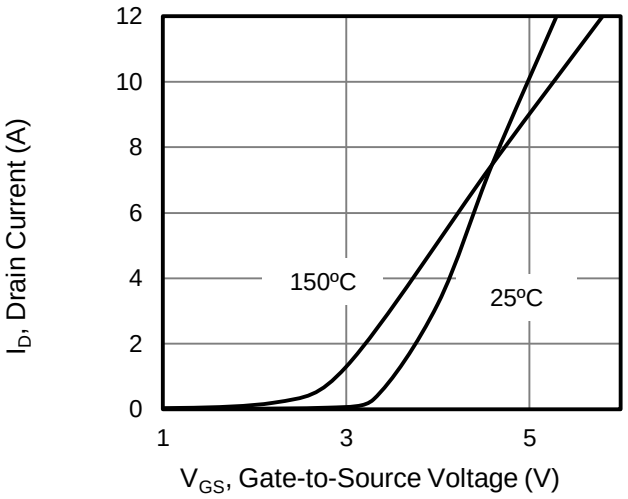


Figure 3.Drain-Source On-Resistance

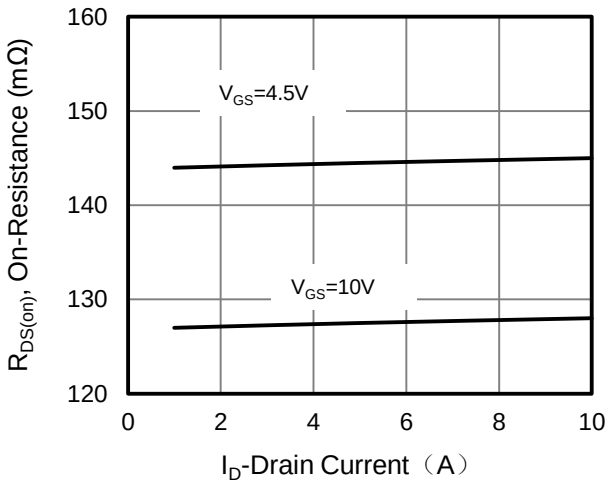


Figure 4. Gate Charge

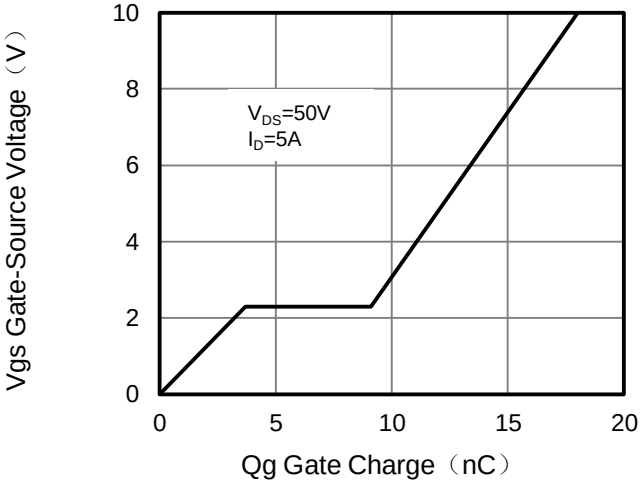


Figure 5. Capacitance

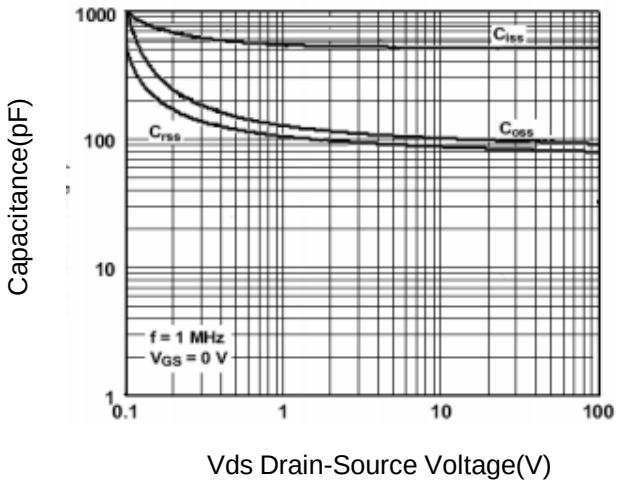
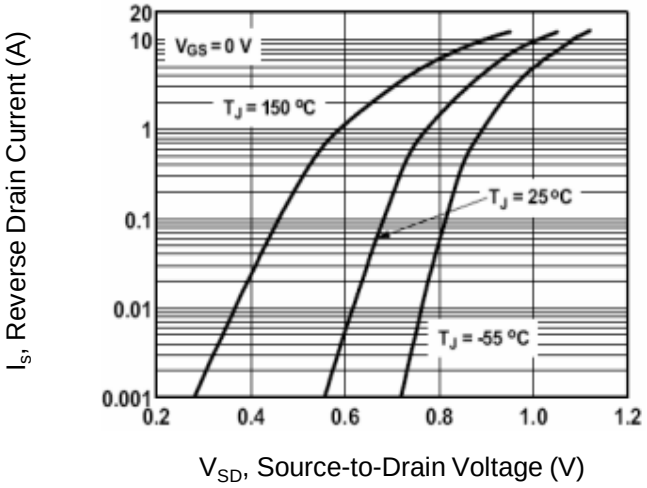


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

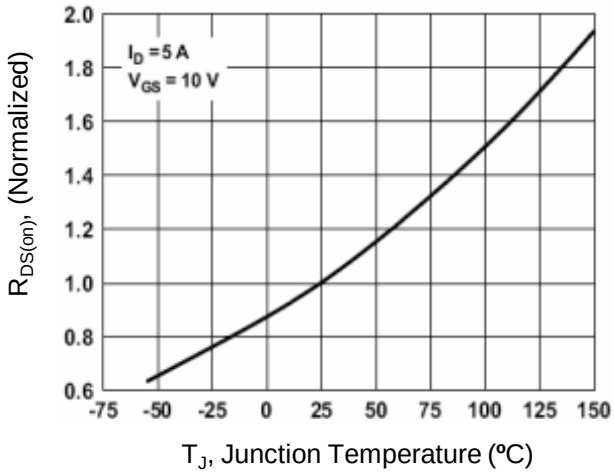


Figure 10. Safe Operation Area

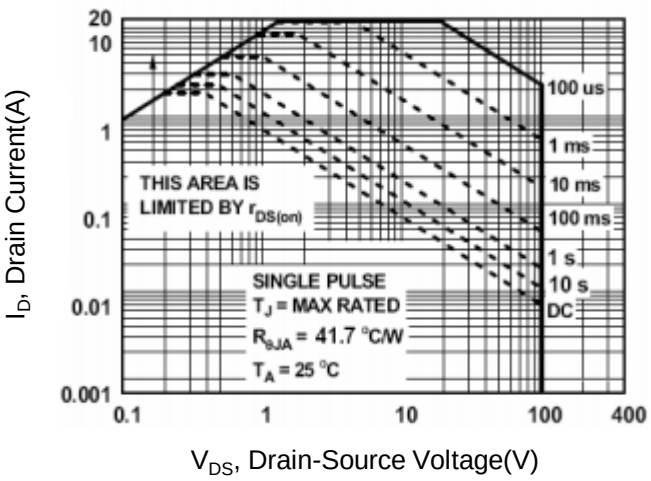
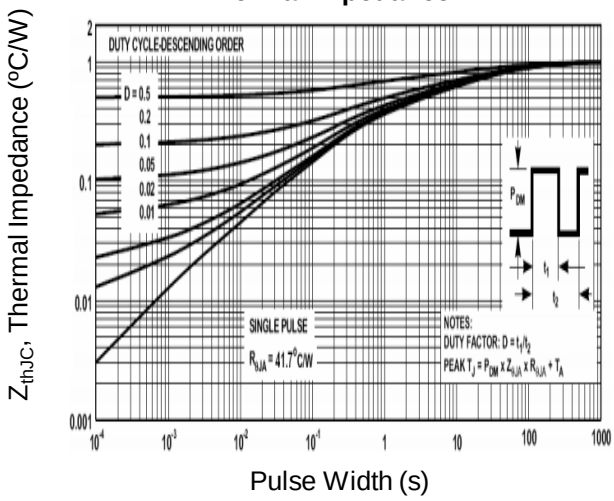


Figure 9. Normalized Maximum Transient Thermal Impedance

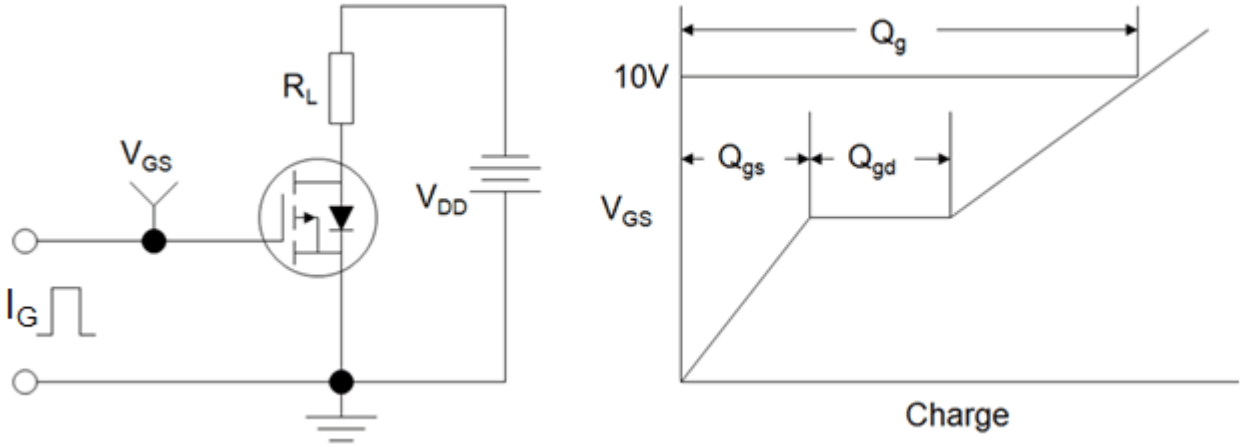


PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V, T_J = 25ºC	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	uA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-2.2	-3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -6A	--	193	200	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=-3A	2	--	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz	--	760	--	pF
Output Capacitance	C_{oss}		--	260	--	
Reverse Transfer Capacitance	C_{rss}		--	170	--	
Total Gate Charge	Q_g	V_{DD} = -50V, I_D = -3A, V_{GS} = -10V	--	25	--	nC
Gate-Source Charge	Q_{gs}		--	5	--	
Gate-Drain Charge	Q_{gd}		--	7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -50V, I_D = -3A, R_G = 9Ω	--	14	--	ns
Turn-on Rise Time	t_r		--	18	--	
Turn-off Delay Time	$t_{d(off)}$		--	50	--	
Turn-off Fall Time	t_f		--	18	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-3	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -3A, V_{GS} = 0V	--	--	-1.2	V

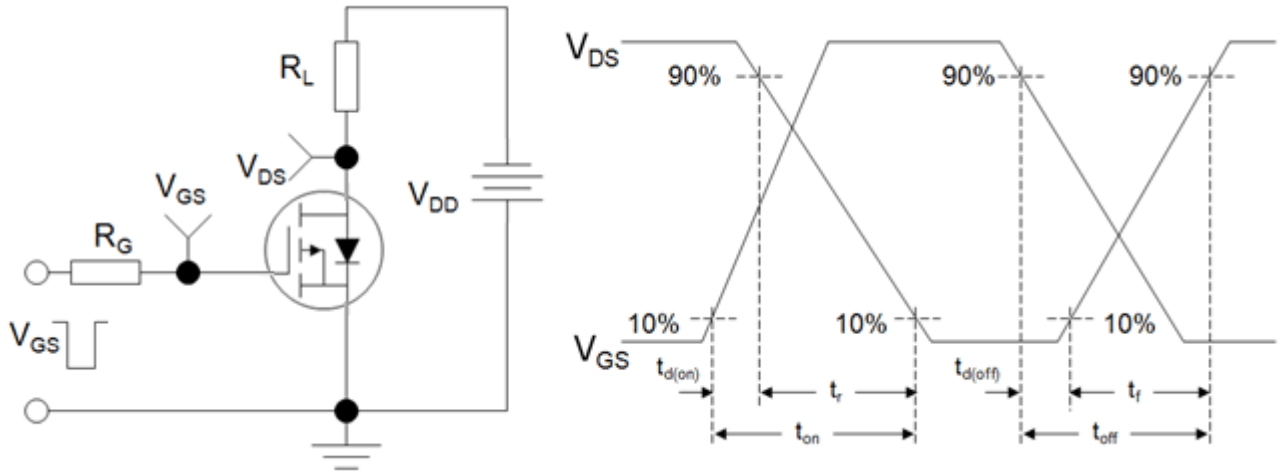
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

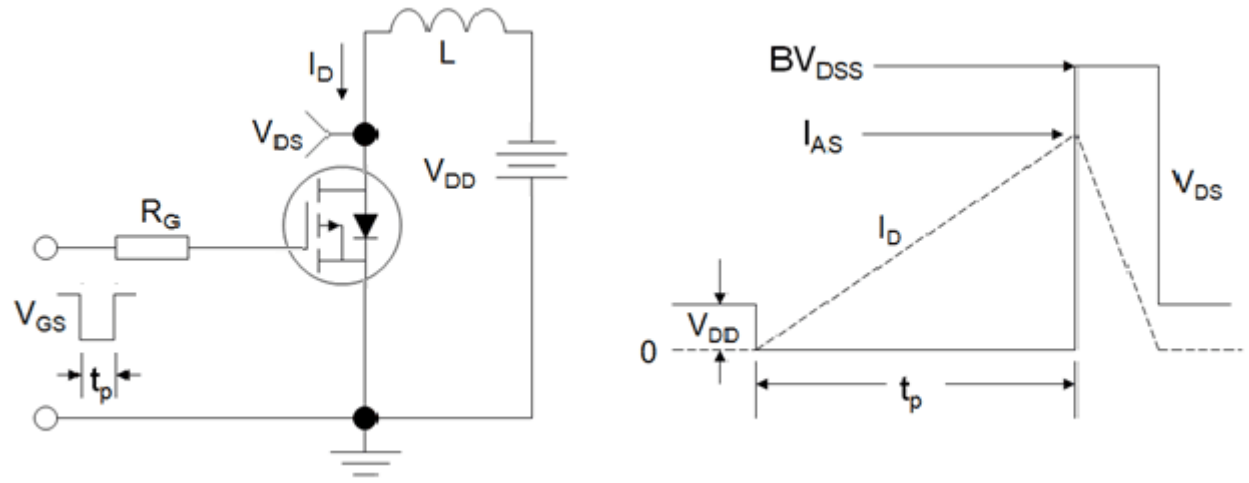
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

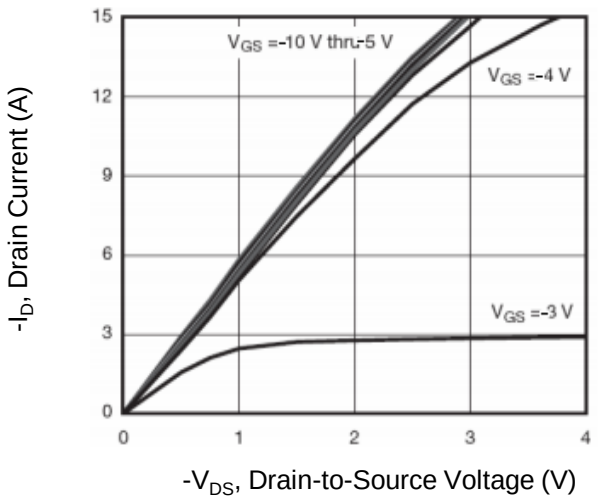


Figure 2. Transfer Characteristics

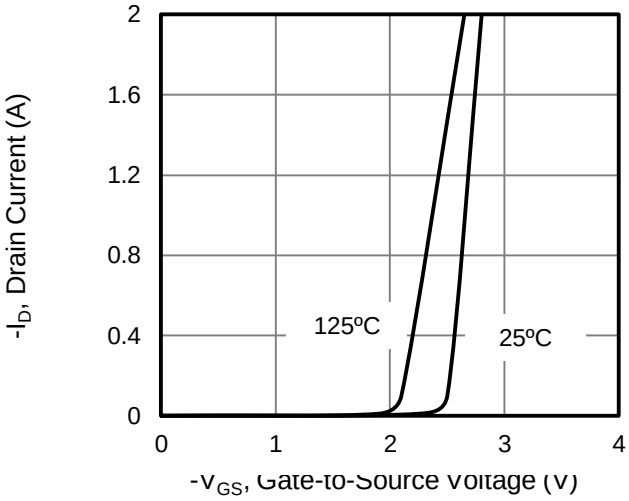


Figure 3.Rdson-Drain Current

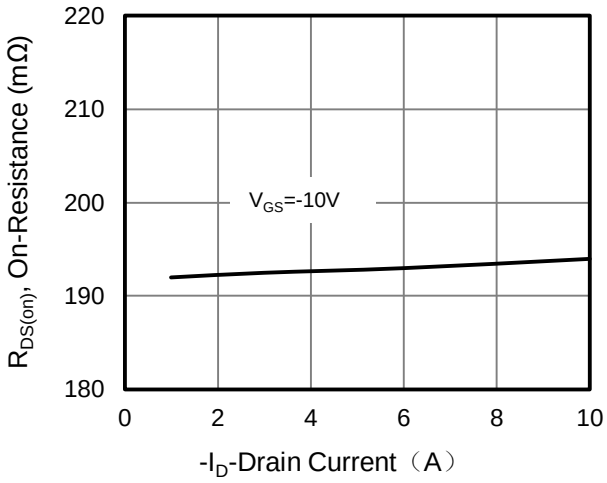


Figure 4. Gate Charge

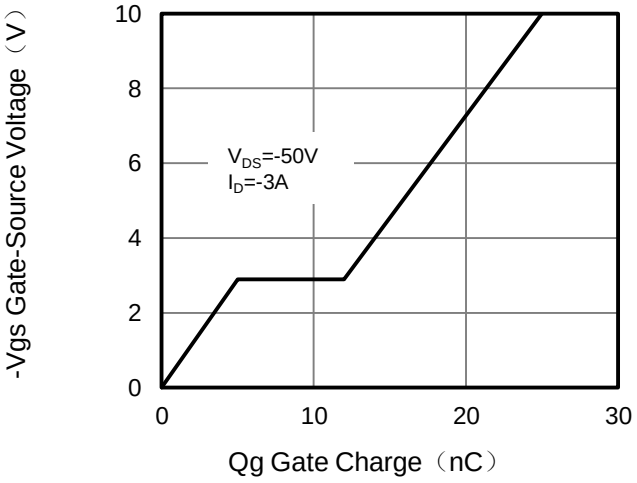


Figure 5. Capacitance

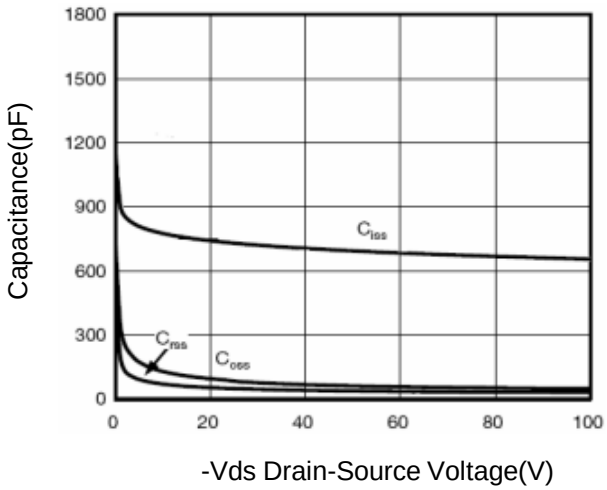
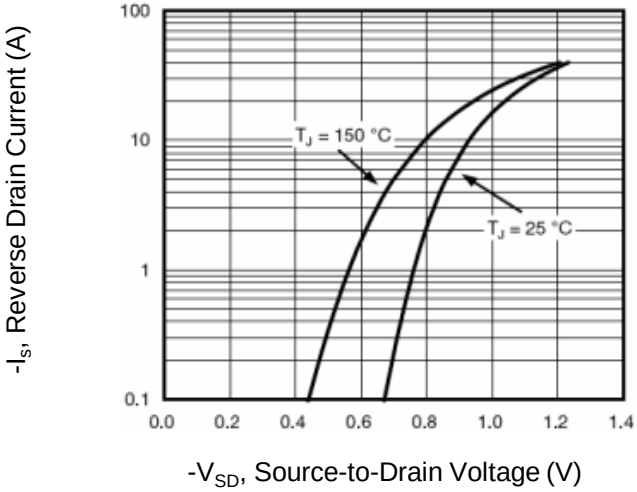


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

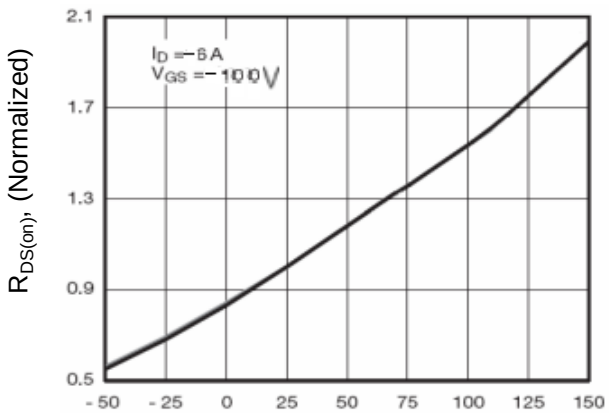


Figure 10. Safe Operation Area

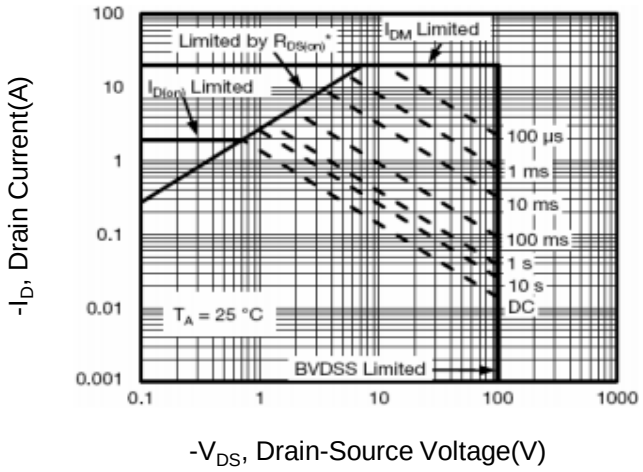
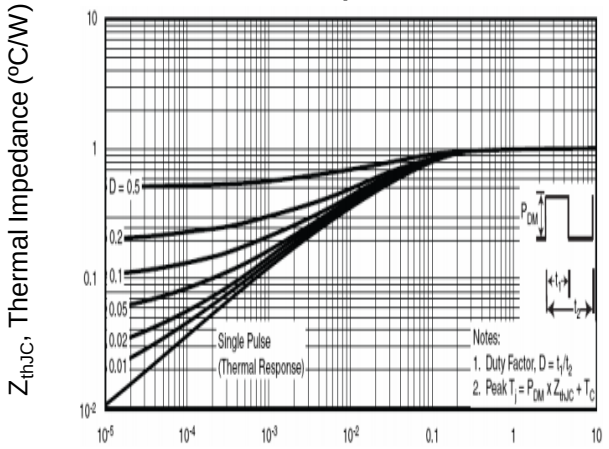
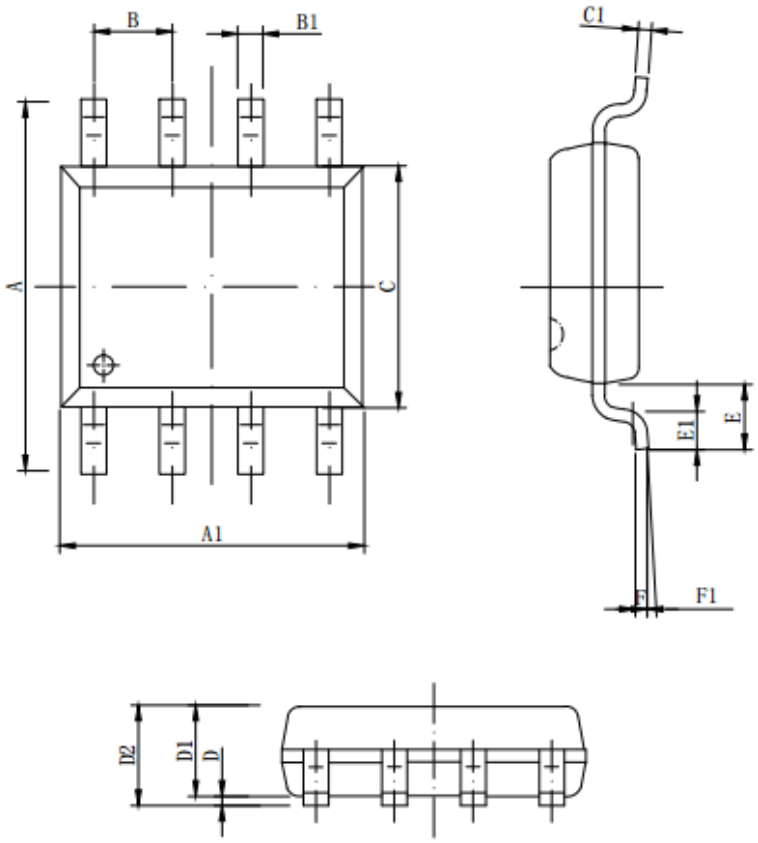


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B		1.270BSC	
B1	0.35^8x	0.40^8x	0.45^8x
C	3.780	3.880	3.980
C1	--	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
D2	1.500	1.600	1.700
E		1.060REF	
E1	0.400	0.700	0.100
F		0.250BSC	
F1	2°	4°	6°