



AU OPTRONICS CORPORATION

Product Functional Specifications

8.4" SVGA Color TFT-LCD Module with Touch Panel

Model Name: G084SN05 V.5

| Approved by | Prepared by |
|-------------|-------------|
| | |

GDBD Marketing Division / AU Optronics Corporation

| Customer | Checked & Approved by |
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| | |



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8.4 inch SVGA Color TFT LCD Module
Model Name: G084SN05 V.5

Preliminary Specification
 Final Specification



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II. Record of Revision

| Version and Date | Page | Old Description | New Description | Remark |
|------------------|------|-----------------|-----------------|--------|
| 0.1 2006/5/10 | All | First Draft | | |



1.0 Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnection from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open nor modify the module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case if a module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CCFL Reflector edge softly. Otherwise the TFT module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the interface Connector of the TFT module.
- 11) After installation of the TFT module into an enclosure, do not twist nor bend the TFT module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT module from outside. Otherwise the TFT module may be damaged.
- 12) Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
- 13) Small amount of materials having no flammability grade is used in the LCD module should be supplied by power complied with requirements of Limited Power Source, or be applied exemption.
- 14) The LCD module is designed so that the CCFL in it is supplied by Limited Current Circuit. Do not connect the CCFL in Hazardous Voltage Circuit.



2.0 General Description

This specification applies to the 8.4 inch color TFT LCD module G084SN05 V.5.

This module is designed for display units for Industrial Applications.

The screen format is intended to support the SVGA 800(H) x 600(V) and VGA 640(H) x 480(V) (through internal video scaling) screen and 262k colors (6bits RGB).

Input signals can be either digital 6bit RGB or analog RGB. Reverse scan function can also be activated through the digital input signal.

The module does not contain an inverter card for backlight.

All components with RoHS compliance.

2.1 Display Characteristics

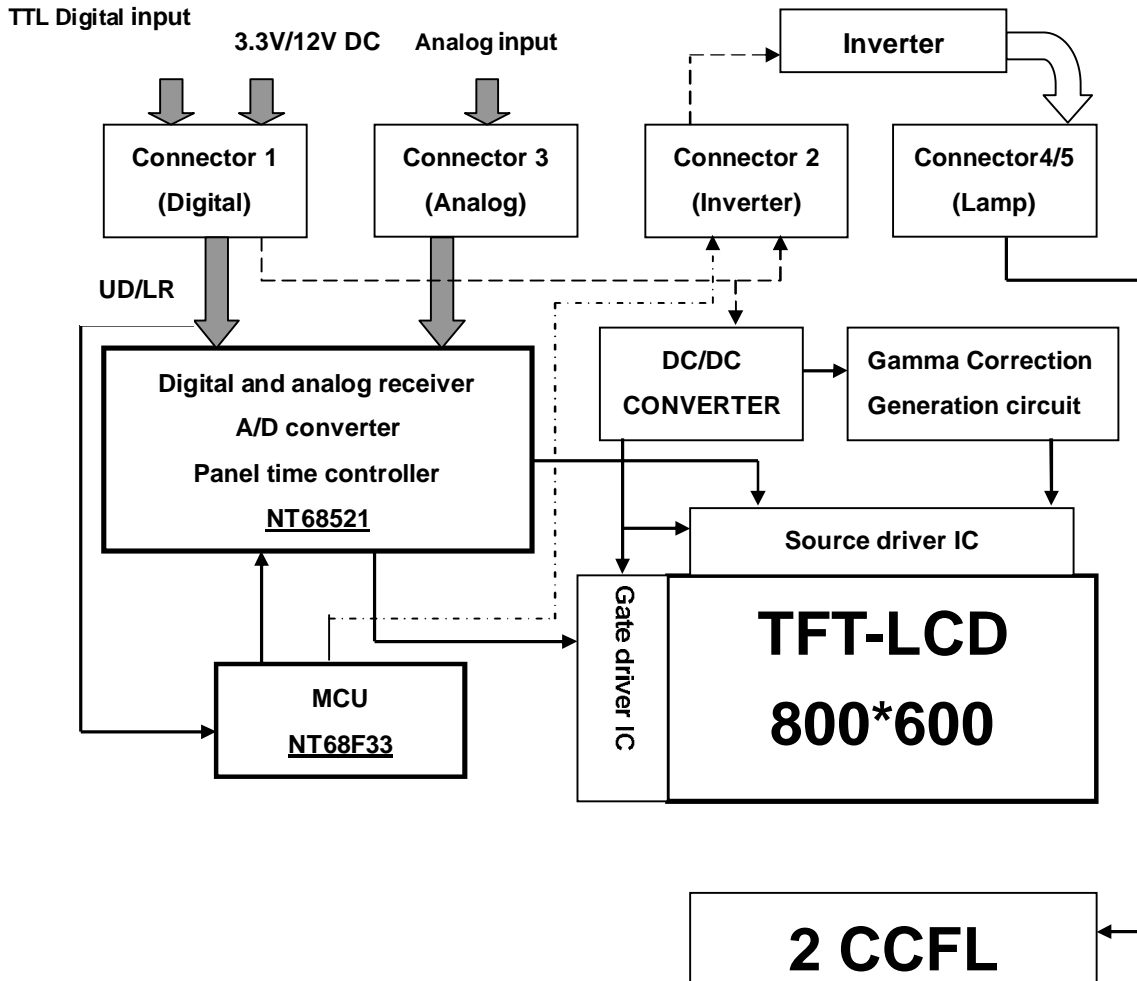
The following items are characteristics summary on the table under 25°C condition :

| Items | Unit | Specifications |
|---|----------------------|---------------------------------------|
| Screen Diagonal | [mm] | 213.4 (8.4") |
| Active Area | [mm] | 170.4(H) x 127.8(V) |
| Pixel H x V | | 800(x3) x 600 |
| Pixel Pitch | [mm] | 0.213(H) x 0.213(V) |
| Pixel Arrangement | | R.G.B. Vertical Stripe |
| Display Mode | | Normally White |
| Typical White Luminance (ICFL=6 mA) | [cd/m ²] | 350 Typ. (center) |
| Contrast Ratio | | 350 : 1 Typ. |
| Optical Rise Time/Fall Time | [msec] | 10/25 Typ. |
| Nominal Input Voltage VDD | [Volt] | +3.3 Typ. |
| Typical Power Consumption (VDD line + VCFL line) | [Watt] | 6.8 Typ |
| Weight | [Grams] | 260 ±10 |
| Physical Size | [mm] | 203(W) x 142.5(H) x 12(D) |
| Electrical Interface | | 6bit RGB / analog RGB |
| Support Color | | Native 262K colors (RGB 6-bit driver) |
| Temperature Range | | |
| Operating | [°C] | 0 to +50 |
| Storage(Shipping) | [°C] | -20 to +60 |



2.2 Functional Block Diagram

The following diagram shows the functional block of the 8.4 inches Color TFT LCD Module :



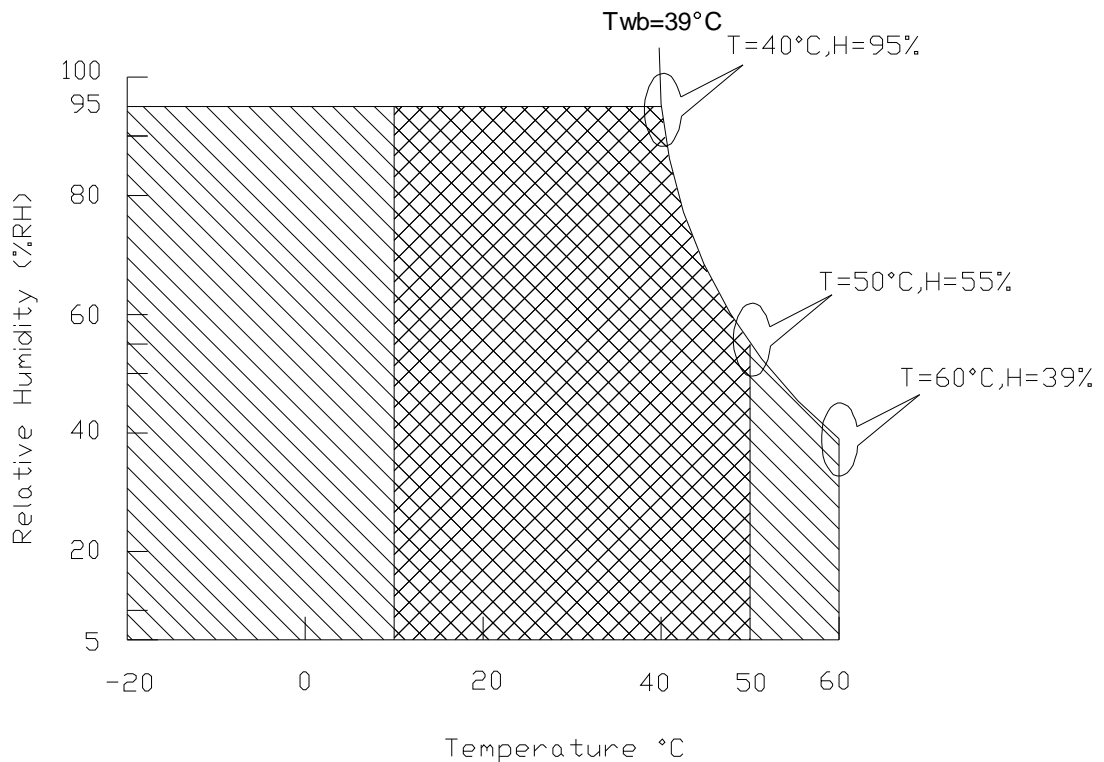


3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as follows :

| Item | Symbol | Min | Max | Unit | Conditions |
|-------------------------|--------|------|---------|---------|------------|
| Logic/LCD Drive Voltage | VDD | -0.3 | +6.0 | [Volt] | |
| Input Voltage of Signal | Vin | -0.3 | VDD+0.3 | [Volt] | |
| CCFL Current | ICFL | 4 | 7 | [mA]rms | |
| CCFL Ignition Voltage | Vs | | 670 | Vrms | T=25°C |
| | | | 870 | | T=0°C |
| Operating Temperature | TOP | 0 | +50 | [°C] | Note1 |
| Operating Humidity | HOP | 8 | 95 | [%RH] | Note1 |
| Storage Temperature | TST | -20 | +60 | [°C] | Note1 |
| Storage Humidity | HST | 5 | 95 | [%RH] | Note1 |

Note1 : Maximum Wet-Bulb should be 39°C and no condensation.



Operating Range



Storage Range



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4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 °C condition :

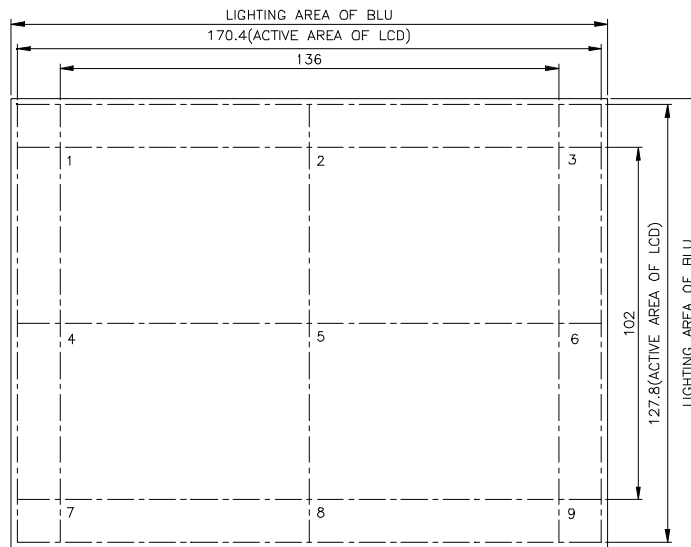
| Item | Unit | Conditions | Min. | Typ. | Max. |
|---|----------------------|---------------------|------|------|------|
| Viewing Angle | [degree] | Horizontal (Right) | — | 60 | — |
| K : Contrast ratio | [degree] | K \geq 10 (Left) | — | 60 | — |
| | [degree] | Vertical (Upper) | — | 60 | — |
| | [degree] | K \geq 10 (Lower) | — | 40 | — |
| | | | | | |
| White Uniformity | | 9 Points | — | — | 1.6 |
| Contrast ratio | | $\theta = 0^\circ$ | 400 | 500 | — |
| Response Time (Room Temp) | [msec] | Rising | — | 10 | 20 |
| | [msec] | Falling | — | 25 | 30 |
| Color Chromaticity Coordinates(CIE) | | Red x | 0.53 | 0.56 | 0.59 |
| | | Red y | 0.29 | 0.32 | 0.35 |
| | | Green x | 0.27 | 0.3 | 0.33 |
| | | Green y | 0.52 | 0.55 | 0.58 |
| | | Blue x | 0.12 | 0.15 | 0.18 |
| | | Blue y | 0.09 | 0.12 | 0.15 |
| | | White x | 0.28 | 0.31 | 0.34 |
| | | White y | 0.3 | 0.33 | 0.36 |
| White Luminance (ICFL 6mA) | [cd/m ²] | $\theta = 0^\circ$ | 280 | 350 | — |



Note 1: Definition of white uniformity:

White uniformity is calculated with the following formula.
Luminance are measured at the following nine points (1~9).

$$\delta_w = \frac{\text{Maximum Brightness of nine points}}{\text{Minimum Brightness of nine points}}$$





5.0 Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name | Connector 1 | Connector 2 | Connector 3 | Connector 4/5 |
|--------------------|---------------------|----------------|---------------|---------------|
| Description | Digital Signal | Lam Control | Analog Signal | Lamp Power |
| Manufacturer | Kyocera Elco | JST | HIROSE | JST |
| Type / Part Number | 04 6274 036 000 800 | S6B-ZR-SM3A-TF | DF13B-9P-1.25 | BHR-03VS-1 |
| Mating Connector | | | | B-BHS-1-TB |

5.2 Signal Pin

5.2.1 Digital Input Signal (Connector 1)

| Pin No. | Signal Name | Pin No. | Signal Name |
|---------|-------------|---------|-------------|
| 1 | GND | 2 | DCLK_IN |
| 3 | DE_IN | 4 | HSYNC_IN |
| 5 | VSYNC_IN | 6 | GND |
| 7 | RIN0 | 8 | RIN1 |
| 9 | RIN2 | 10 | RIN3 |
| 11 | RIN4 | 12 | RIN5 |
| 13 | GIN0 | 14 | GIN1 |
| 15 | GIN2 | 16 | GIN3 |
| 17 | GIN4 | 18 | GIN5 |
| 19 | BIN0 | 20 | BIN1 |
| 21 | BIN2 | 22 | BIN3 |
| 23 | BIN4 | 24 | BIN5 |
| 25 | GND | 26 | REV(Note 1) |
| 27 | VDD | 28 | VDD |
| 29 | VDD | 30 | DIMMER |
| 31 | GND | 32 | GND |
| 33 | GND | 34 | VBL |
| 35 | VBL | 36 | VBL |



Note 1: Selection of scanning mode (please refer to the following table)

| Setting of scancontrol input | Input Signal | Scanning direction |
|------------------------------|--------------|---|
| REV (No.26 pin) | Lo | From up to down, and from left to right |
| REV (No.26 pin) | Hi | From down to up, and from right to left |

5.2.2 Analog Input Signal (Connector 3)

| Pin No. | Signal Name | Pin No. | Signal Name |
|---------|-------------|---------|-------------|
| 1 | VGA_HSYNC | 2 | VGA_VSYNC |
| 3 | AGNF | 4 | RED |
| 5 | RED_GND | 6 | GREEN_GND |
| 7 | GREEN | 8 | BLUE_GND |
| 9 | BLUE | | |

5.2.3 Inverter Output Signal (Connector 2)

| Pin No. | Signal Name | Pin No. | Signal Name |
|---------|-------------|---------|-------------|
| 1 | VBL | 2 | GND |
| 3 | VBLCTRL | 4 | DIMMER |
| 5 | GND | | |



5.3 Signal Description

5.3.1 Digital Input Pin Description (Connector 1)

| Signal Name | Description |
|-------------|--|
| VSS | GND |
| REV | Trigger of reverse scan function |
| VDD | +3.3V Power Supply |
| GND | Ground |
| VBL | Inverter Power Supply |
| DIMMER | Brightness of Backlight Control Signal |

| Signal Name | Description | |
|-------------|--|---|
| RIN0 | Red Data 5 (MSB) | Red-pixel Data Each red pixel's brightness data consists of 6 bits pixel data. |
| RIN1 | Red Data 4 | |
| RIN2 | Red Data 3 | |
| RIN3 | Red Data 2 | |
| RIN4 | Red Data 1 | |
| RIN5 | Red Data 0 (LSB) Red-pixel Data | |
| GIN0 | Green Data 5 (MSB) | Green-pixel Data Each green pixel's brightness data consists of 6 bits pixel data. |
| GIN1 | Green Data 4 | |
| GIN2 | Green Data 3 | |
| GIN3 | Green Data 2 | |
| GIN4 | Green Data 1 | |
| GIN5 | Green Data 0 (LSB) Green-pixel Data | |
| BIN0 | Blue Data 5 (MSB) | Blue-pixel Data Each blue pixel's brightness data consists of 6 bits pixel data. |
| BIN1 | Blue Data 4 | |
| BIN2 | Blue Data 3 | |
| BIN3 | Blue Data 2 | |
| BIN4 | Blue Data 1 | |
| BIN5 | Blue Data 0 (LSB) Blue-pixel Data | |
| CLK | Data Clock | The typical frequency is 40MHz. The signal is used to strobe the pixel data and DE signals. |



| | | |
|-------|-----------------|--|
| | | All pixel data shall be valid at the falling edge when the DE signal is high. |
| DE | Display Timing | This signal is strobed at the falling edge of CLK. When the signal is high, the pixel data shall be valid to be displayed. |
| VSYNC | Vertical Sync | The signal is synchronized to CLK. |
| HSYNC | Horizontal Sync | The signal is synchronized to CLK. |

Note : Output signals from any system shall be low or Hi-Z state when VDD is off.

5.3.2 Analog Input Pin Description (Connector 3)

| Signal Name | Description |
|-------------|------------------------------------|
| VGA_HSYNC | The signal is synchronized to CLK |
| VGA_VSYNC | The signal is synchronized to CLK. |
| RED | Analog R Signal Input |
| GREEN | Analog G Signal Input |
| BLUE | Analog B Signal Input |
| RED_GND | A_GND |
| GREEN_GND | |
| BLUE_GND | |

5.3.3 Inverter Control Pin Description (Connector 2)

| Signal Name | Description |
|-------------|--|
| VBL | Inverter power |
| GND | GND |
| DIMMER | Brightness of Backlight control signal |
| VBLCTRL | Inverter Power Control Signal |

5.3.4 Lamp Power (Connector 4/5)

Connector: JST BHR-03VS-1, Mating connector: JST SM03(4.0)B-BHS-1-TB

| Pin no. | Symbol | Function | Remark |
|---------|--------|--------------------------|---------------------------|
| 1 | H | CCFL power supply (H.V.) | Cable color: Pink |
| 2 | NC | No connection | |
| 3 | L | CCFL power supply(GND.) | Cable color: Black |



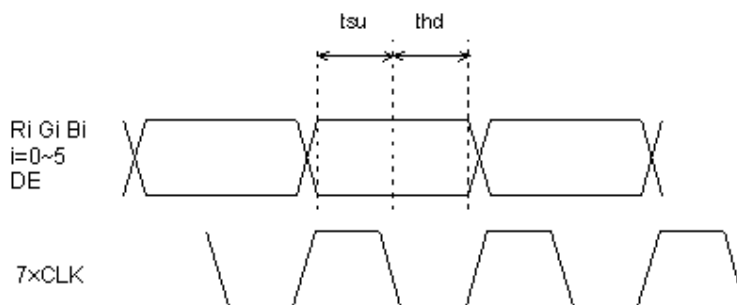
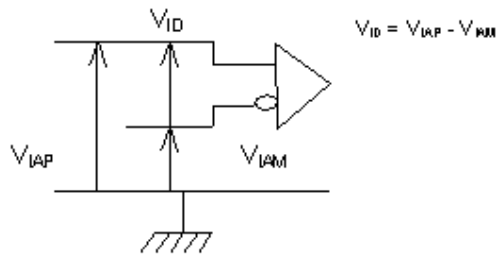
5.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86(Texas Instruments) in detail.

Signal electrical characteristics are as follows :

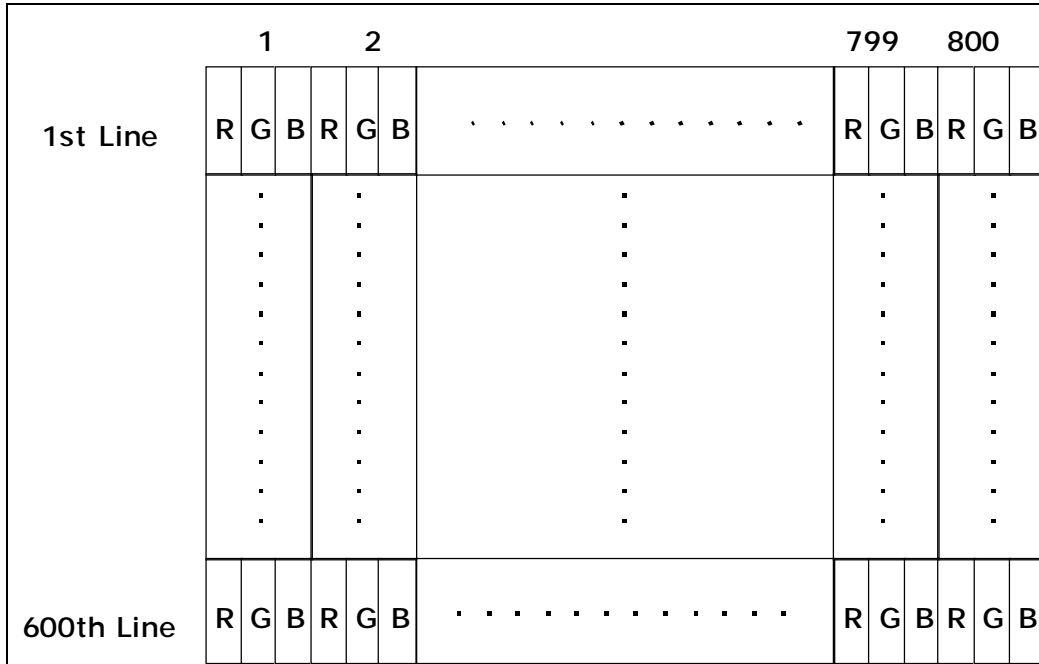
| Item | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------|------------|----------------------|------|----------------------------|------|
| The differential level | $ V_{ID} $ | 0.1 | - | 0.6 | V |
| The common mode input voltage | V_{IC} | $\frac{ V_{ID} }{2}$ | - | $2.4 - \frac{ V_{ID} }{2}$ | V |
| The input setup time | t_{su} | 0.5 | - | - | Ns |
| The input hold time | t_{hd} | 0.5 | - | - | Ns |
| High-level input voltage | V_{IAP} | 2.0 | | | V |
| Low-level input voltage | V_{IAM} | | | 0.8 | V |
| Clock frequency | CLK | 31 | | 68 | MHz |





6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format :



6.1 Scanning Direction

Following picture figures shows the image seen from the front view. The arrow indicate the direction of scan.



Fig. 1 Normal scan (REV=Lo)



Fig. 2 Reverse scan (REV=Hi)



7.0 Parameter guideline for CCFL inverter

| Parameter | Min | Typ | Max | Units | Condition |
|------------------------------------|-----|--------|-----|-------------------|-------------|
| White Luminance | 280 | 350 | - | Cd/m ² | At 6mA ICFL |
| CCFL current (ICFL) | 4 | 6 | 7 | mArms | Note1 |
| CCFL Frequency (FCFL) | 40 | 50 | 80 | KHz | Note4 |
| CCFL Ignition Voltage (Vs) | | | 670 | Vrms | Note 1 |
| | | | 870 | | Note 3 |
| CCFL Voltage (Reference) (VCFL) | | TBD | | Vrms | Note1 |
| CCFL Power consumption (PCFL) | | TBD | | W | Note2 |
| Lamp Life Time | - | 50,000 | - | Hr | Note1, 5 |

Note1 : T=25°C

Note2 : Inverter should be designed with the characteristic of lamp. When you are designing the inverter, the output voltage of the inverter should comply with the following conditions.

- (1). The area under the positive and negative cycles of the waveform of the lamp current and lamp voltage should be area symmetric (the symmetric ratio should be larger than 90%).
- (2). There should not be any spikes in the waveform.
- (3). The waveform should be sine wave as possible.
- (4). Lamp current should not exceed the maximum value within the operating temperature (It is prohibited to over the maximum lamp current even if operated in the non-guaranteed temperature). When lamp current is over the maximum value for a long time, it may cause fire. Therefore, it is recommend that the inverter should have the current limit circuit.

Note3 : The inverter open voltage should be designed larger than the lamp starting voltage at T=0°C, otherwise backlight may be blinking for a moment after turning on or not be able to turn on. The open voltage should be measured after ballast capacitor. If an inverter has shutdown function it should keep its open voltage for longer than 1 second even if lamp connector is open.

Note4 : Lamp frequency may produce interference with horizontal synchronous frequency and this may cause line flow on the display. Therefore lamp frequency shall be detached from the horizontal synchronous frequency and its harmonics as far as possible in order to avoid interference.

Note5 : Brightness (ICFL = 6mA) to drop to 50% of the initial value.



8.0 Interface Timings

Basically, interface timing should match the VESA 800x600 /60Hz(VG901101) manufacturing guide line timing. (VGA)

8.1 Timing Characteristics

8.1.1 SVGA MODE

(a) DE mode

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------|--------|------|------|------|------|--------|
| Clock frequency | Fck | 36 | 40 | 50 | MHz | |
| Horizontal blanking | Thb1 | 18 | 256 | 624 | Clk | |
| Vertical blanking | Tvb1 | 3 | 28 | 184 | Th | |

(b) HV mode

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-------------------------|--------|------|------|------|------|--------|
| Clock frequency | Fck | 36 | 40 | 50 | MHz | |
| Hsync period | Th | 1018 | 1056 | 1424 | Clk | |
| Hsync pulse width | Thw | 2 | 128 | - | Clk | |
| Hsync front porch | Thf | 8 | 40 | | Clk | |
| Hsync back porch | Thb | 4 | 88 | | Clk | |
| Hsync Active | | | 800 | | Clk | |
| Hsync blanking | Thb1 | 218 | 256 | 624 | Clk | |
| Vsync period | Tv | 625 | 628 | 784 | Th | |
| Vsync pulse width | Tvw | 1 | 4 | | Th | |
| Vsync front porch | Tvf | 0 | 1 | | Th | |
| Vsync blanking | Tvb1 | 25 | 28 | 184 | Th | |
| Vsync Active | | | 600 | | Th | |
| Hsync/Vsync phase shift | Tvpd | 0 | 320 | | Clk | |



| Item | Symbol | Value | Unit | Description |
|--------------------------|--------|-------|------|--|
| Horizontal display start | The | 218 | Clk | After falling edge of Hsync, counting 218clk, then getting valid data from 219th clk's data. |
| Vertical display start | Tve | 25 | Th | After falling edge of Vsync, counting 25th, then getting 26th Th's data. |

8.1.2 VGA MODE

(a)DE mode

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------|--------|------|------|------|------|--------|
| Clock frequency | Fck | - | 25.2 | 36 | MHz | |
| Horizontal blanking | Thb1 | - | 160 | 192 | Clk | |
| Vertical blanking | Tvb1 | - | 45 | 77 | Th | |

(b)HV mode

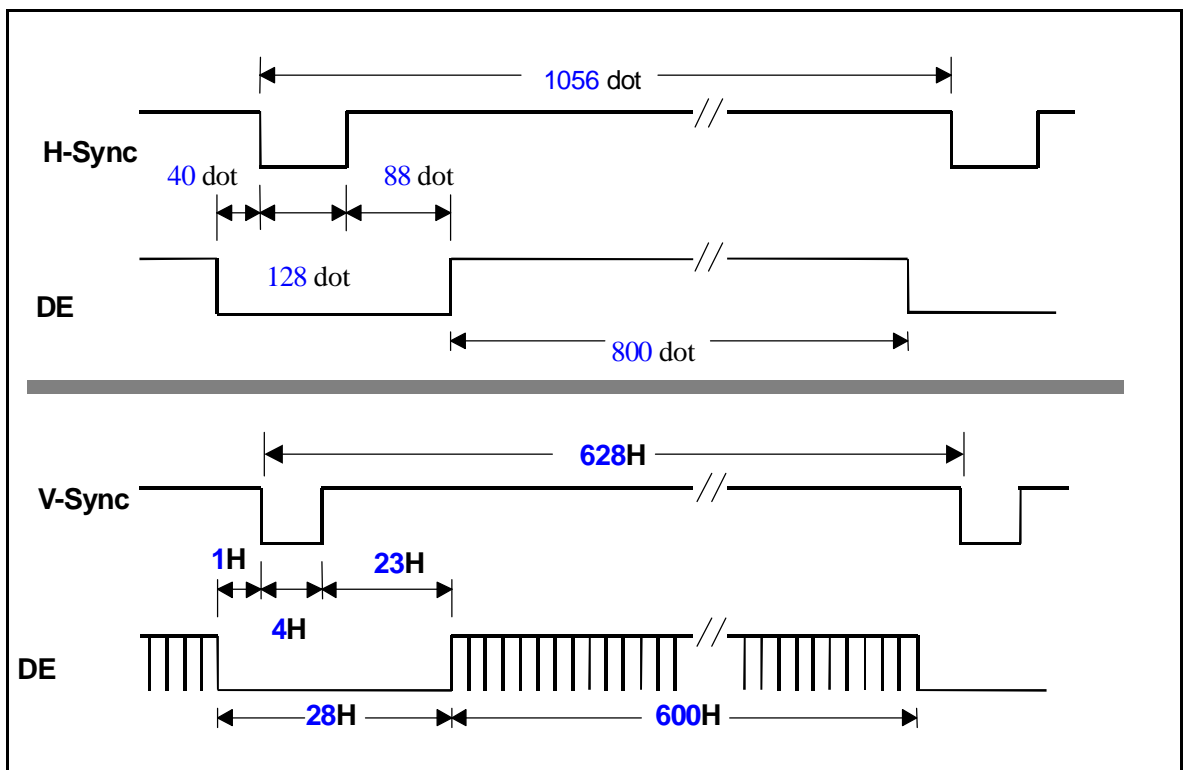
| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-------------------------|--------|------|------|------|------|--------|
| Clock frequency | Fck | - | 25.2 | 36 | MHz | |
| Hsync period | Th | 680 | 800 | 832 | Clk | |
| Hsync pulse width | Thw | - | 96 | 120 | Clk | |
| Hsync front porch | Thf | - | 8 | 56 | Clk | |
| Hsync back porch | Thb | - | 40 | 80 | Clk | |
| Hsync blanking | Thb1 | - | 160 | 192 | Clk | |
| Hsync Active | | | 640 | | Clk | |
| Vsync period | Tv | 484 | 525 | 557 | Th | |
| Vsync pulse width | Tvw | - | 2 | 3 | Th | |
| Vsync front porch | Tvf | - | 2 | - | Th | |
| Vsync blanking | Tvb1 | - | 45 | 77 | Th | |
| Vsync active | | | 480 | | Th | |
| Hsync/Vsync phase shift | Tvpd | 0 | 320 | - | Clk | |



| Item | Symbol | Value | Unit | Description |
|--------------------------|--------|-------|------|--|
| Horizontal display start | The | 160 | Clk | After falling edge of Hsync, counting 218c lk, then getting valid data from 219th clk 's data. |
| Vertical display start | Tve | 45 | Th | After falling edge of Vsync, counting 25 th, then getting 26th Th's data. |

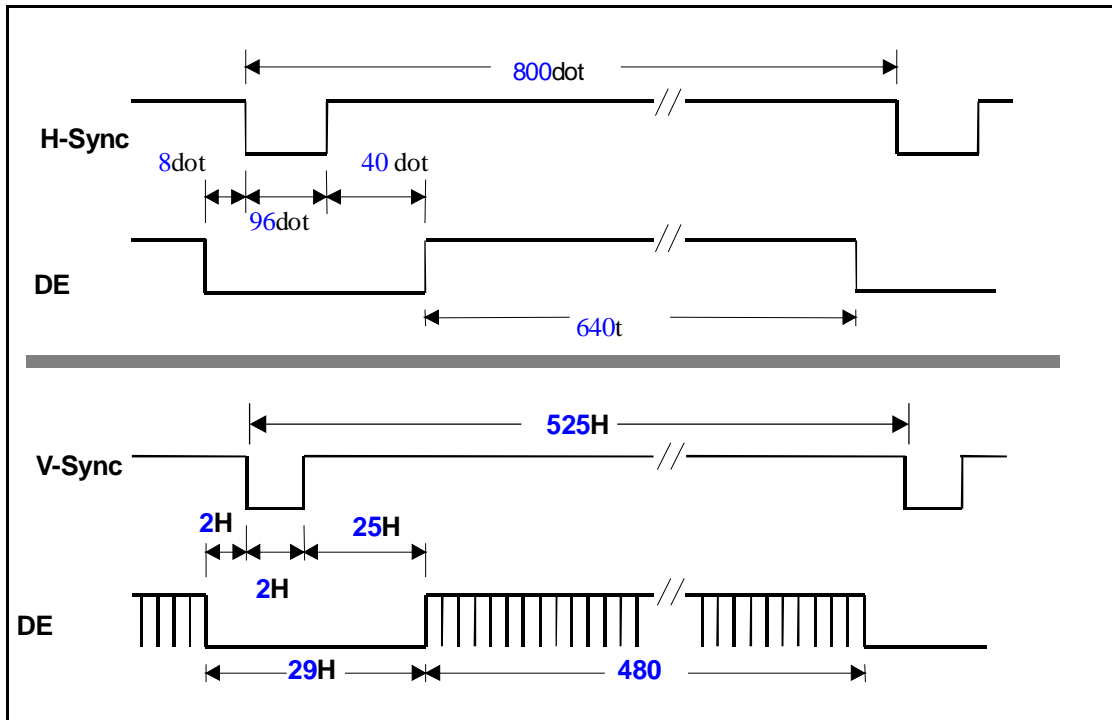
8.2 Timing Definition

8.2.1 SVGA MODE





8.2.2 VGA MODE



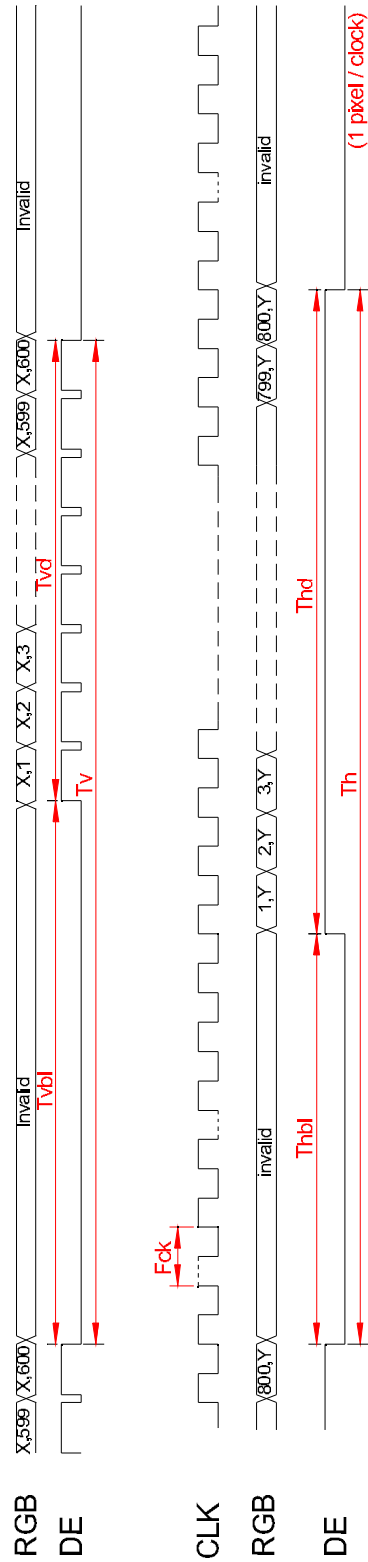


Fig.3 Timing Chart

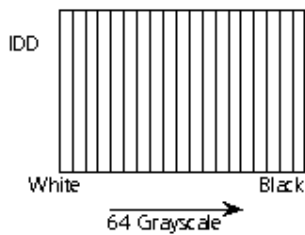


9.0 Power Consumption

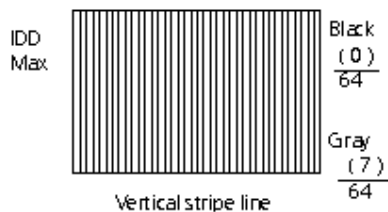
Input power specifications are as follows :

| Symbol | Parameter | Min | Typ | Max | Units | Condition |
|------------|-------------------------|-----|------|------|--------|------------------------|
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | V | |
| PDD (SVGA) | VDD Power | - | 1.98 | 2.31 | W | |
| IDD (SVGA) | IDD Current | - | 600 | 700 | mArms | Note 1 Note 2 (Max) |
| PDD (VGA) | VDD Power | - | 1.88 | 2.21 | W | |
| IDD (VGA) | IDD Current max | - | 570 | 670 | mArms | Note 1 Note 2 (Max) |
| V_{RP} | Power Ripple Voltage | - | 100 | - | mVp-p | |
| I_{RUSH} | Inrush Current | - | 1500 | - | mApeak | |

Note 1: Effective value (mArms) at $V_{CC} = 3.3\text{ V}/25^{\circ}\text{C}$.



Note 2:



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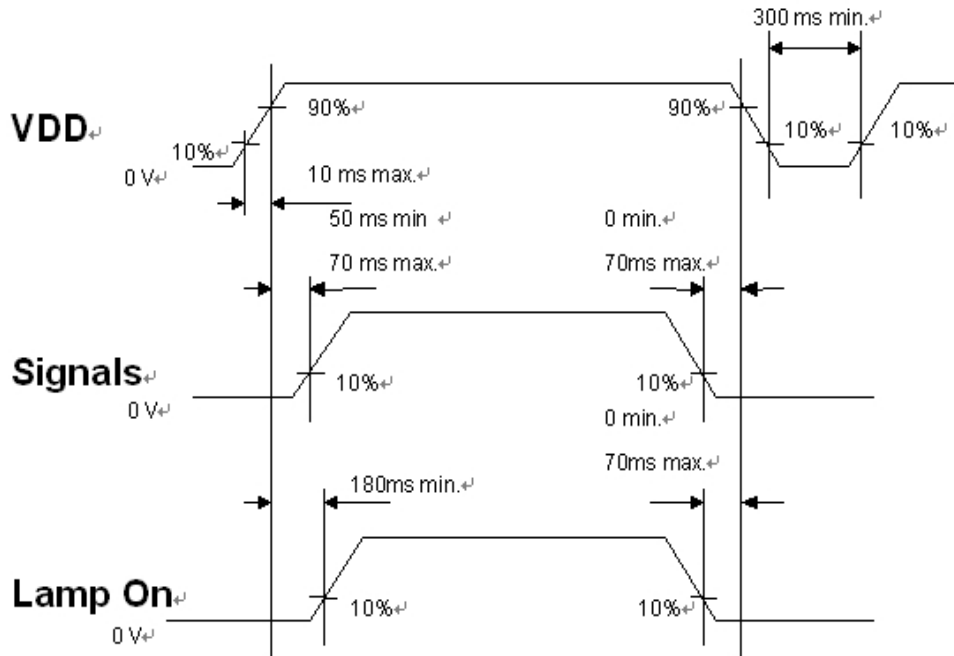
G084SN05 V.5 ver.0.1

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10.0 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.





11.0 Reliability Test Items

Environment test condition

| No | Test Item | Condition | Remark |
|----|--|--|------------|
| 1 | High temperature storage test | Ta=60°C 300Hrs | Note 1,2,3 |
| 2 | Low temperature storage test | Ta= -20°C 300Hrs | Note 1,2,3 |
| 3 | High temperature operation test | Ta=50°C 300Hrs | Note 1,2,3 |
| 4 | Low temperature operation test | Ta=0°C 300Hrs | Note 1,2,3 |
| 5 | High temperature & high humidity operation | 40°C, 90%RH, 300Hrs (No condensation) | Note 1,2,3 |
| 6 | Thermal Shock Test (non-operation) | -20°C/30 min, 60°C/30 min 100cycles | Note 1,2,3 |
| 7 | Vibration test (non-operation) | Vibration level :1.5 G Waveform: Sinusoidal vibration Bandwidth : 10-500-10Hz/2.5min Duration: X, Y, Z 30min One time each direction | Note 1,2,3 |
| 8 | Shock test (non-operation) | Shock level: 50G Waveform: Half sine wave, 20ms Direction: ±X, ±Y, ±Z One time each direction | Note 1,2,3 |
| 9 | Electrostatic discharge (non-operation) | 150 pF,150Ω,10kV,1 second, 9 position on the panel, 10 times each place | Note 3 |

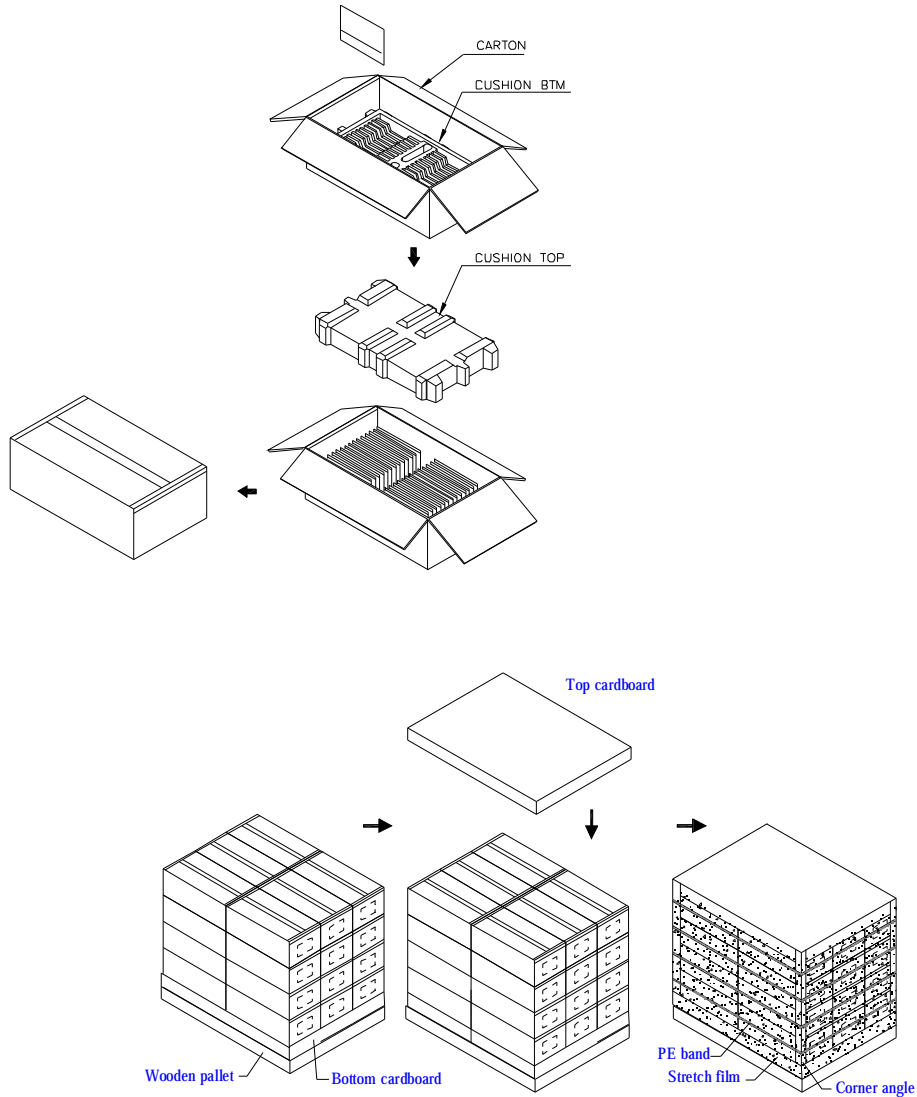
Note 1: Evaluation should be tested after storage at room temperature for one hour.

Note 2: There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

Note 3: Judgment: Function and display OK.



12.0 Packing



Note : Limit of box palletizing = Max 4 layers (ship and stock conditions)

Note:

1. Maximum Capacity: 30 LCD Module Carton
2. Carton outside dimension: 405 (L)mm x 328 (W)mm x 301 (H)mm
3. Maximum 24 of corrugated carton on wooden pallet.
(3 x 2 x 4 layers : maximum 24 boxes per pallet: 720 pcs modules)

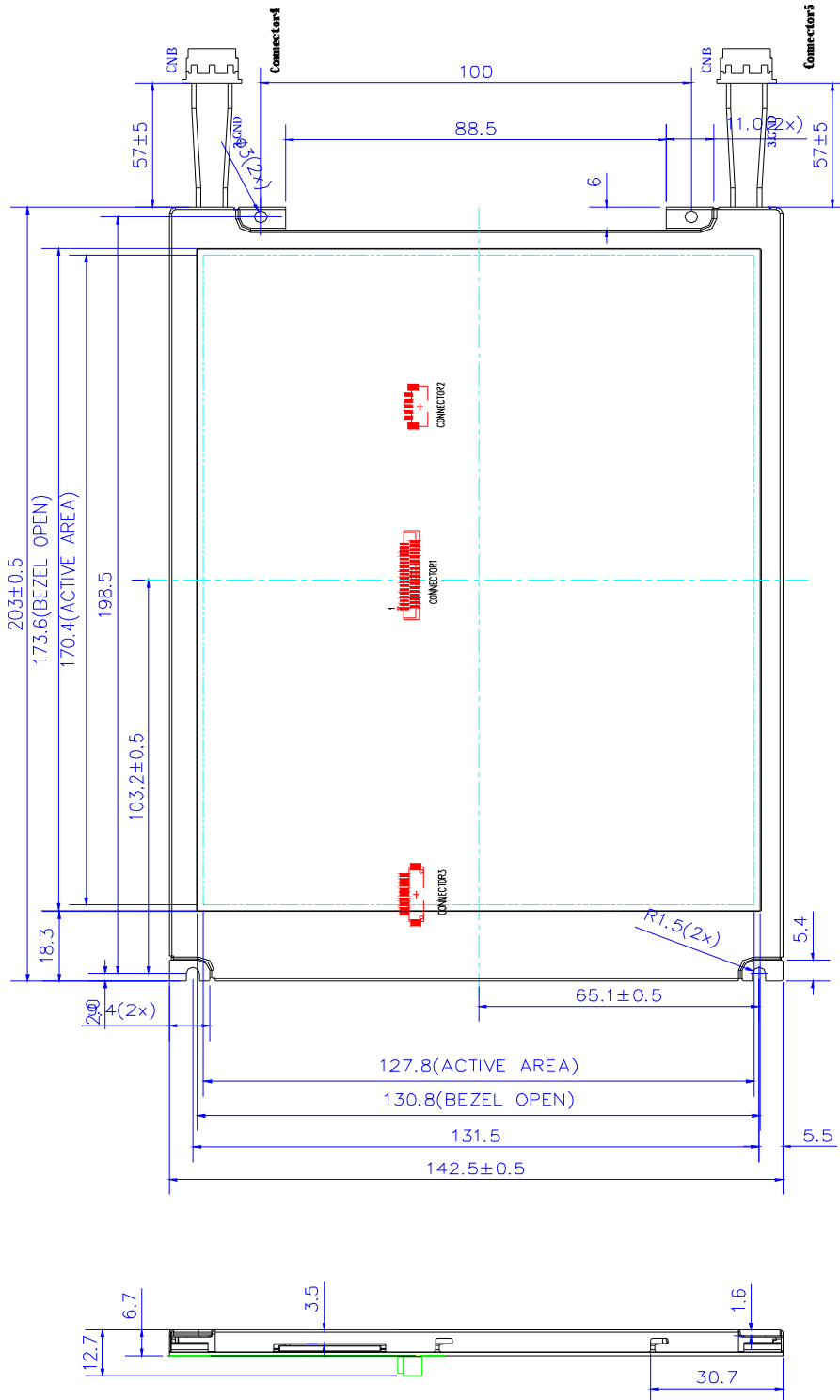
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13.Mechanical Characteristics(front)



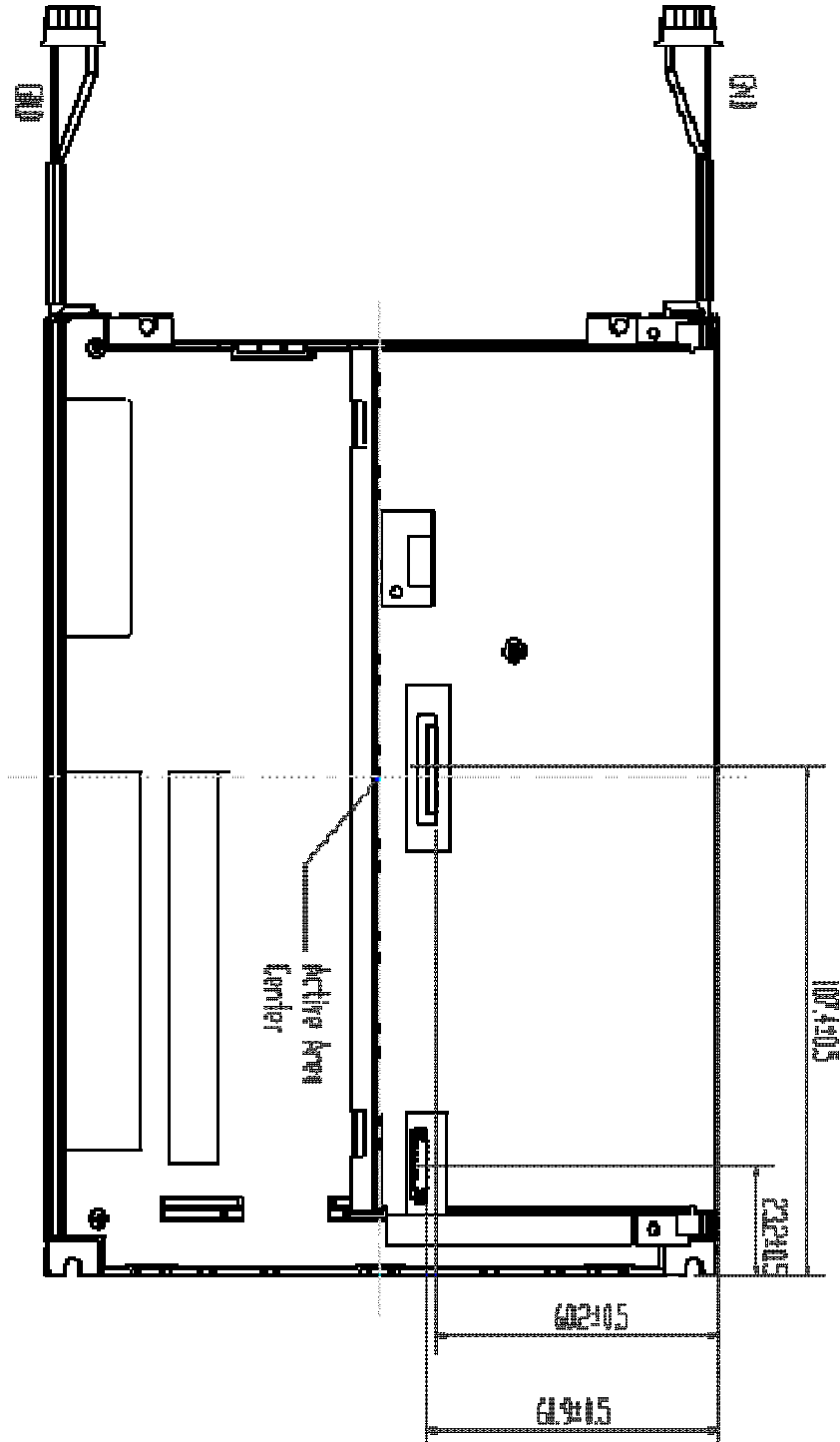
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14.Mechanical Characteristics(back)



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