() Preliminary Specifications
(v) Final Specifications

Module	10.1 Inch Color TFT-LCD
Model Name	G101EAN02.401

Customer	**Date**
Checked & Approved by	

Approved by	**Date**
LeaDer Feng	2021/05/13
Prepared by	
Jon Tseng	2021/05/13
General Display Business Unit/ AUO Display Plus Corporation	

2. General Description

G101EAN02.401 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel and LED backlight Back viewsystem. The screen format is intended to support the 16:10 WXGA, 1200(H) x 800(V) screen and 16.7M colors (RGB 6-bits + FRC) with LED backlight driving circuit. All input signals are eDP 1.2 interface compatible.

2.1 Display Characteristics

The following items are characteristics summary under 25 ºC condition:

Items	Unit	Specifications
Screen Diagonal	[inch]	10.1”
Active Area	[mm]	216.96(H) x 135.6(V)
Pixels H x V		1280 x 3(RGB) x 800
Pixel Pitch	[mm]	0.1695X 0.1695
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		AHVA, Normally Black
Nominal Input Voltage VDD	[Volt]	3.3 (Typical)
Power Consumption	[Watt]	Logic Power : 1.29W(Max)@White pattern 3.3V input LED power max 3.024 W
Weight (Max.)	[Grams]	200
Physical Size (Max.)	[mm]	228.22(H) x148.3(V) x 2.97(t) Max (Panel side) 4.8(t) Max (PCBA side)
Electrical Interface		1Lane eDP1.2
Surface Treatment		HC
Support Color		16.7M colors (RGB 6-bit + FRC)
Temperature Range Operating Storage (Non-Operating)	 [ºC] [ºC]	 0 to +60 (Front and rear surface) -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m2]	I_{LED}= 22mA (center)	320	400	---	
Uniformity	%	5 points	70%		---	
Contrast Ratio			600	800	---	
Response Time	[msec]	Rising + Falling	---	29	38	
Viewing Angle	[degree]	Horizontal (Right) CR = 10	80	89	---	
	[degree]	(Left)	80	89	---	
	[degree]	Vertical (Upper) CR = 10	80	89	---	
	[degree]	(Lower)	80	89	---	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.532	0.582	0.632	
		Red y	0.295	0.345	0.395	
		Green x	0.290	0.340	0.390	
		Green y	0.522	0.572	0.622	
		Blue x	0.112	0.162	0.212	
		Blue y	0.077	0.127	0.177	
		White x	0.263	0.313	0.363	
		White y	0.279	0.329	0.379	
Color Gamut	%		---	45	---	

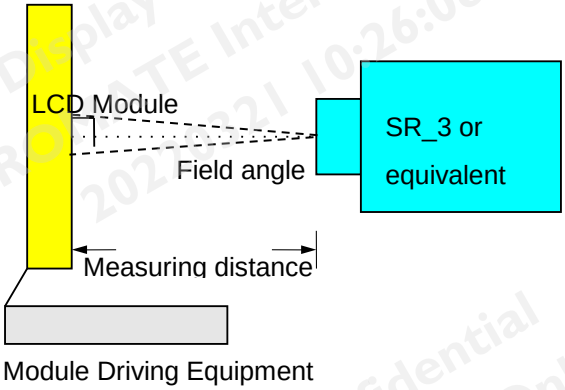
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

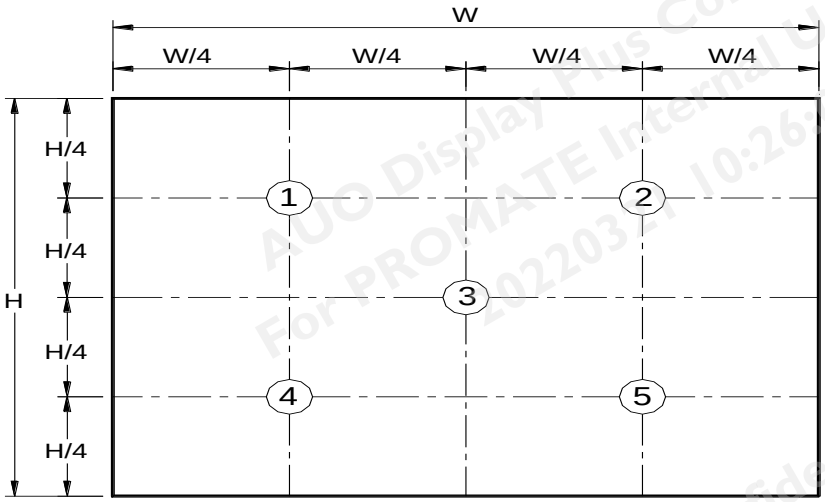
Aperture Field angle 2◦ with 50cm measuring distance

Test Point Follow Note 2 position

Environment *< 1 lux*



Note 2: Definition of 5 points position



Note 3: The luminance uniformity of 5 points is defined by dividing the minimum luminance values by the maximum test point luminance

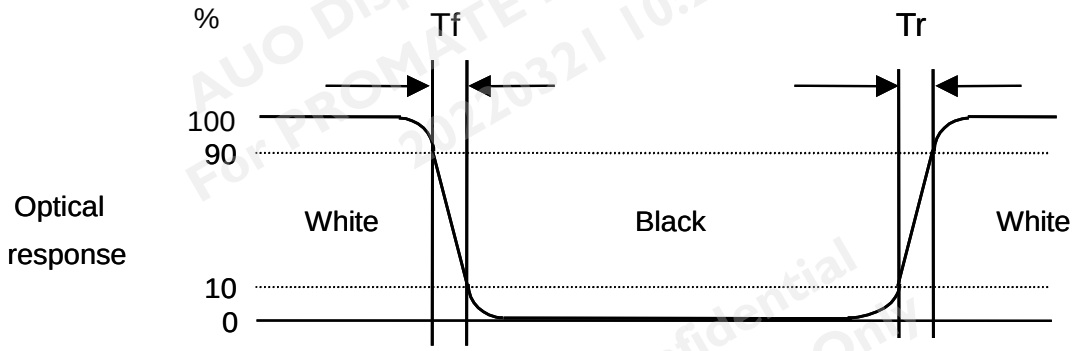
$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

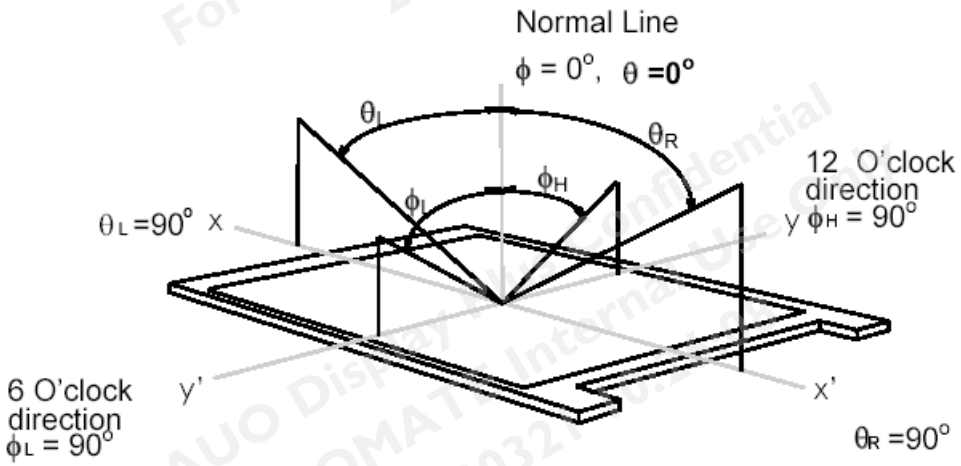
Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



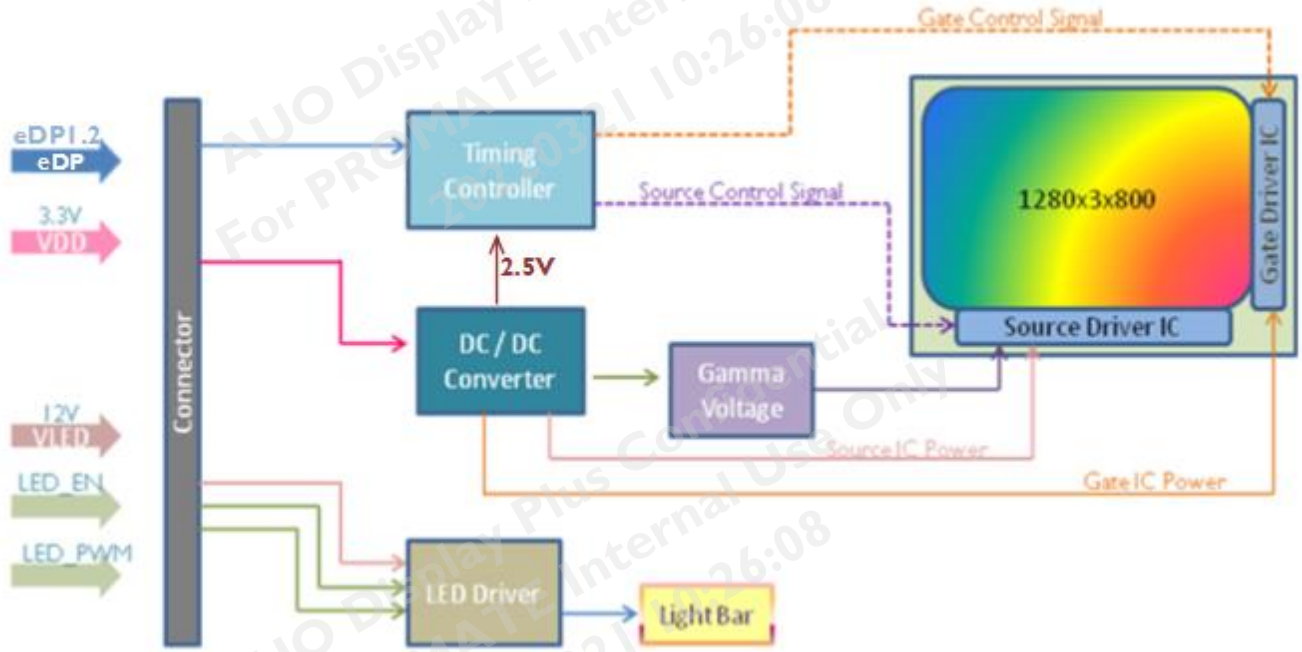
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inch color TFT/LCD module:



4. Absolute Maximum Ratings

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit
Logic/LCD drive Voltage	VDD	-0.3	3.6	[Volt]

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	0	+60	[°C]
Humidity	HOP	5	90	[%RH]
Storage Temperature	TST	-20	+60	[°C]
Storage Humidity	HST	5	90	[%RH]

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: Maximum wet-bulb temperature is less than 39℃ and no condensation

Note 4: Operating temperature means “Front and rear surface” of panel

5. Electrical Characteristics

5.1 TFT LCD Module

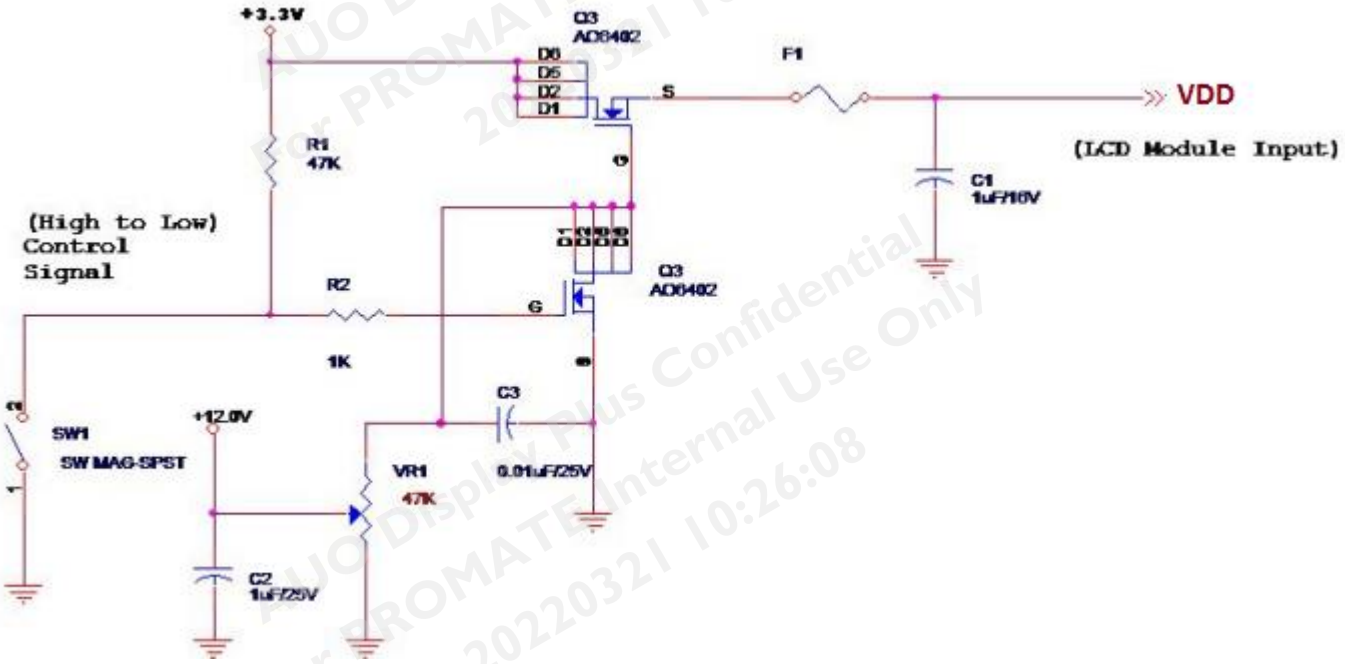
5.1.1 Power Specification

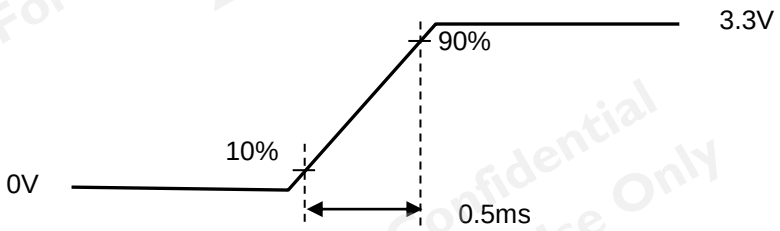
The power specification are measured under 25℃ and frame frenquency under 60Hz

Symbol	Parameter	Min	Typ	Max	Units	Remark
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
IDD	VDD Current	-	357.6	388.8	[mA]	All White Pattern (VDD=3.3V, at 60Hz)
Irush	LCD Inrush Current	-	-	1500	[mA]	Note 1
PDD	VDD Power	-	1.18	1.29	[Watt]	All White Pattern (VDD=3.3V, at 60Hz)

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2：Measure Condition



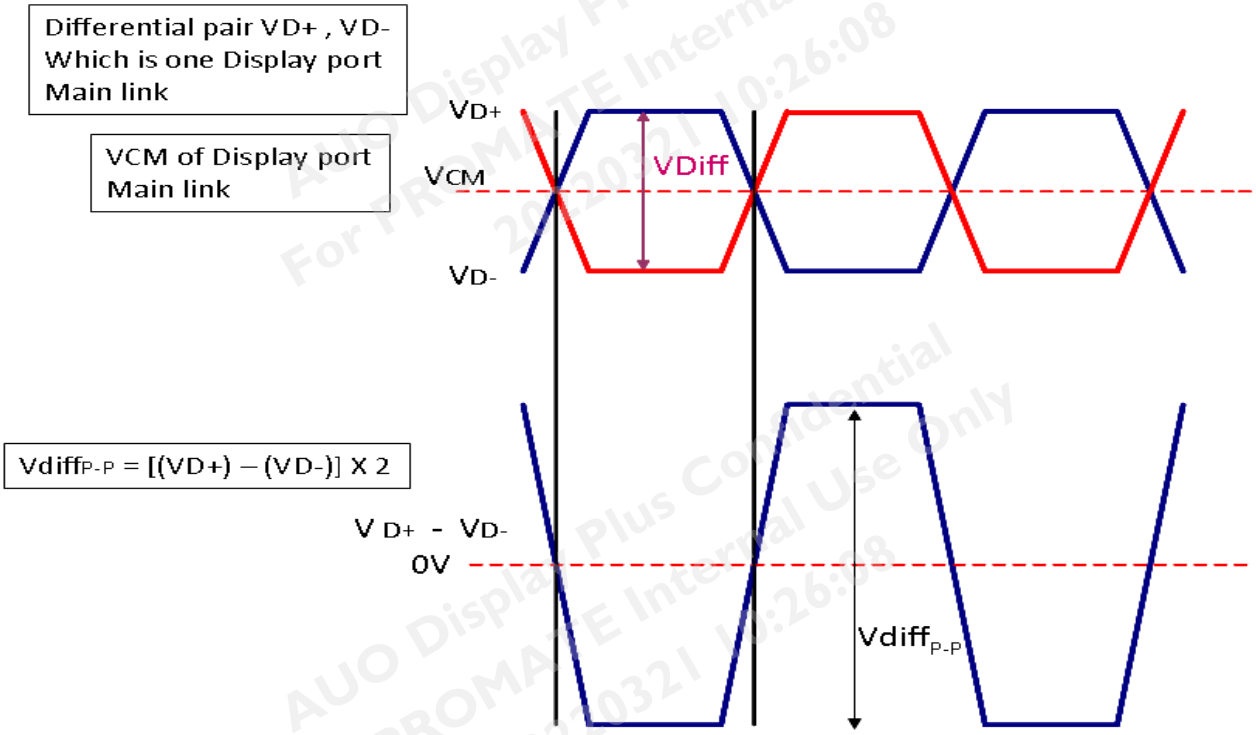


VDD rising time

5.1.2 Signal Electrical Characteristics

Signal electrical characteristics are as follows:

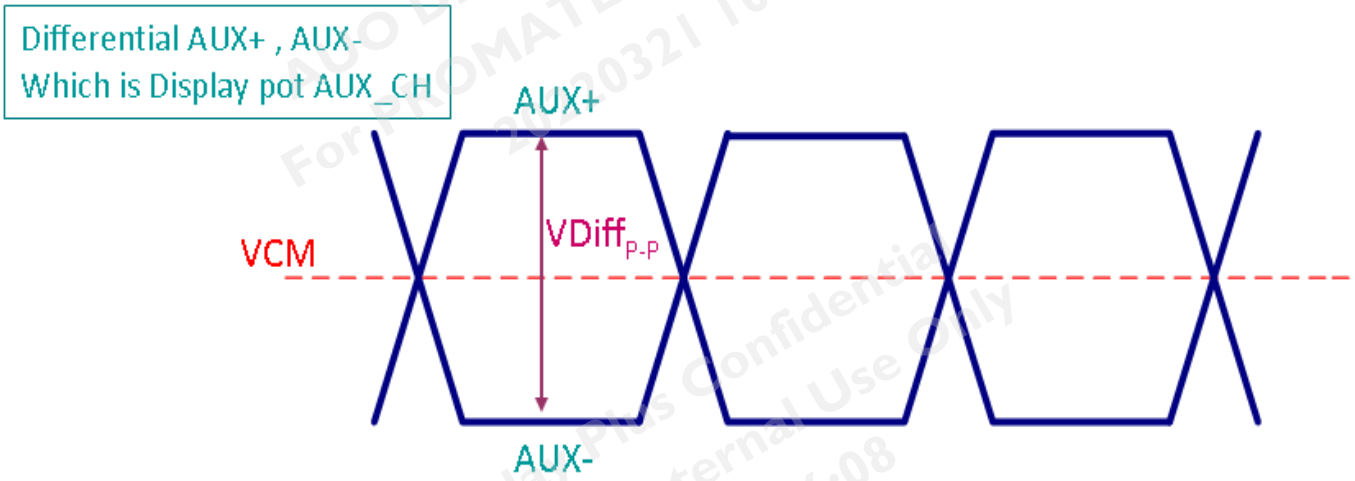
Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Follow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6-	0.8	V

Follow as VESA display port standard V1.1a.

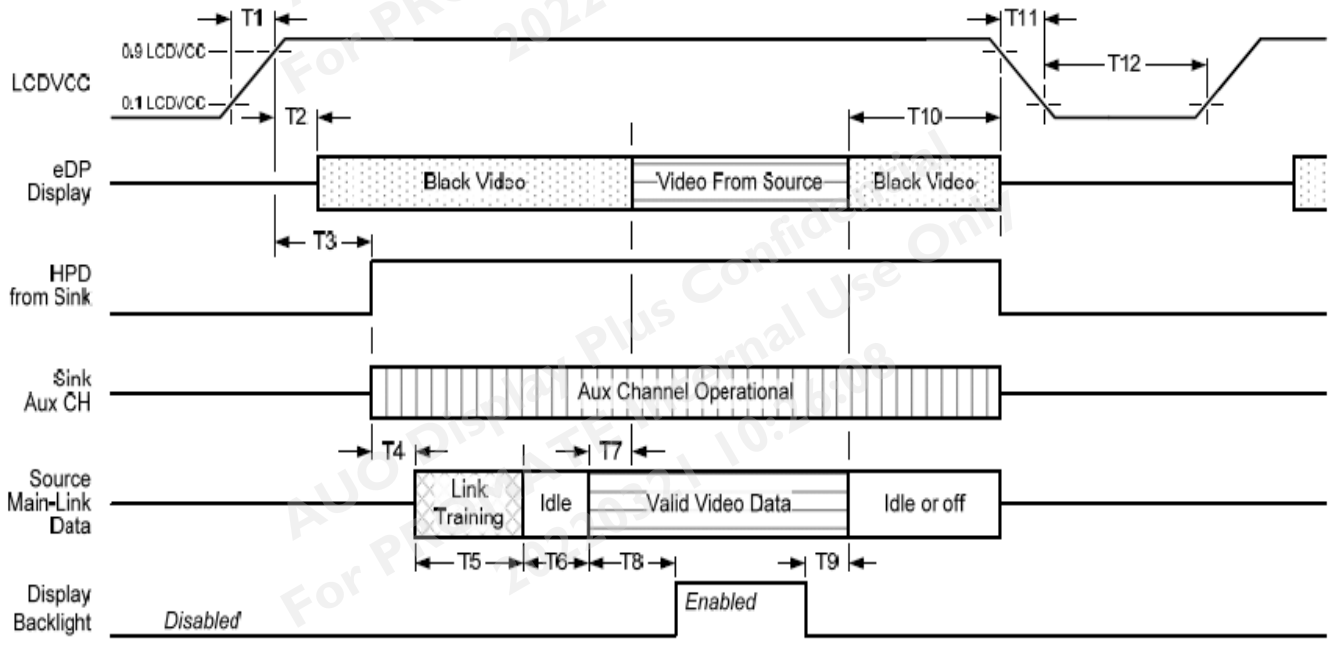
Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	2.75	V

Follow as VESA display port standard V1.1a.

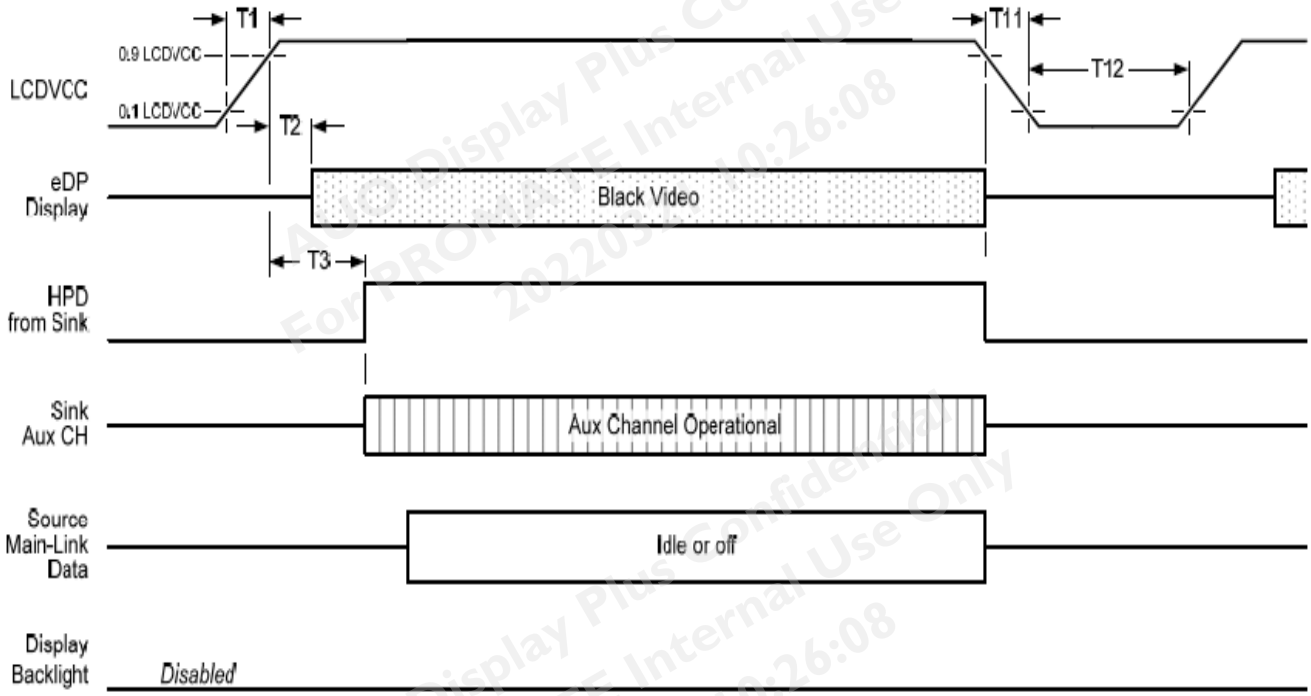
5.1.3 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

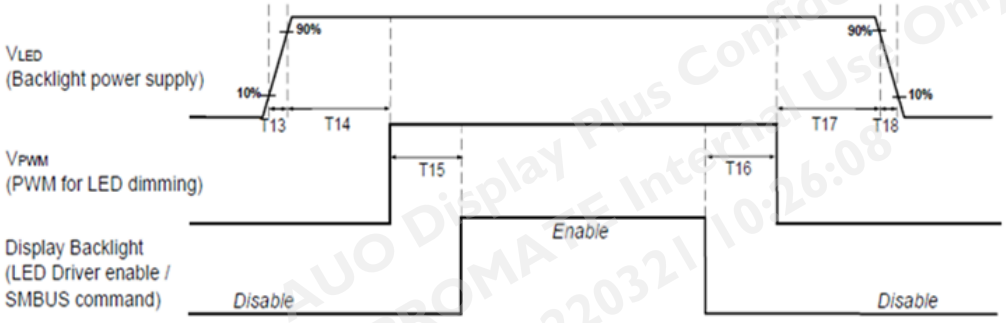
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:

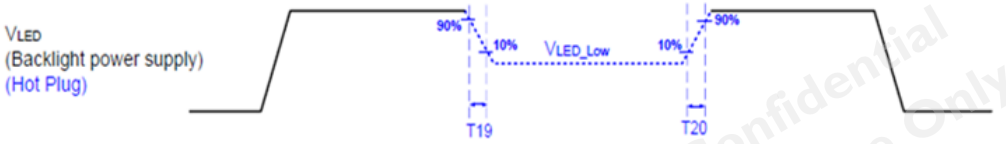


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



5.2 Backlight Unit

5.2.1 Parameter guideline for LED

Following characteristics are measured under a stable condition using an inverter at 25℃(Room Temperature):

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
VLED	Input Voltage	10.8	12	13.2	[Volt]	
I_{VLED}	Input Current	---	222	252	[mA]	100% Brightness (VLED = 12V)
P_{VLED}	Power Consumption	---	2.664	3.024	[Watt]	100% Brightness (VLED = 12V)
I_F	LED Forward Current	---	22	---	[mA]	Ta = 25ºC
VEN	LED Enable Input High Level	2.3	-	5.5	[Volt]	
	LED Enable Input Low Level	-	-	0.3	[Volt]	
VPWM	PWM Logic Input High Level	2.3	-	5.5	[Volt]	
	PWM Logic Input Low Level	-	-	0.3	[Volt]	
PWM Input Frequency	FPWM	200	1K	20K	Hz	
PWM Duty Ratio	Duty	1		100	%	
Operation Life	---	20,000	30,000	---	Hrs	(Ta=25℃), Note 2 IF=22 mA

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: V_{LED}, I_{VLED}, P_{VLED} are defined for LED backlight.(100% duty of PWM dimming)

Note 3: If G101EAN02.401 module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 4: Operating life means brightness goes down to 50% initial brightness. Minimum operating life time is estimated data.

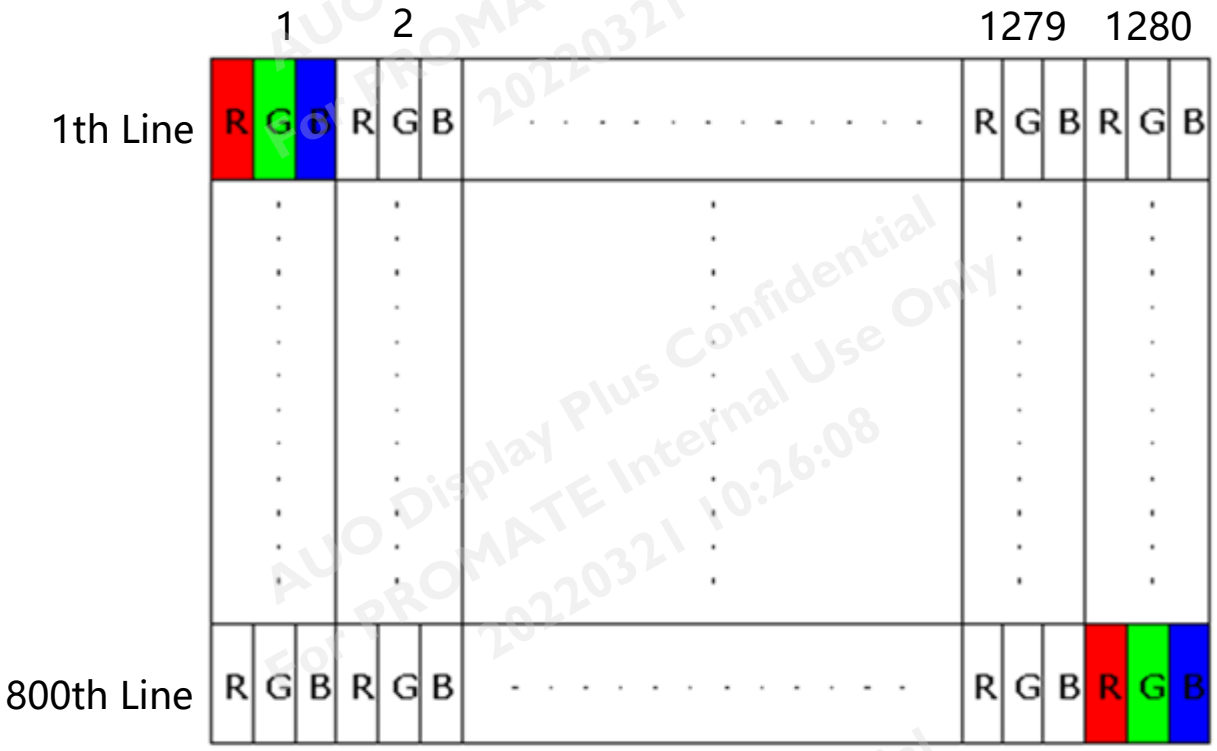
Note 5: Measured in panel VLED

Note 6: If the PWM duty ratio(min) is set between 5% to 1%, the PWM input frequency should be set below 1KHz. The brightness-duty characteristic might not be able to keep in it's linearity if the dimming control is operated in 1% to 10% range.

6. Signal Characteristic

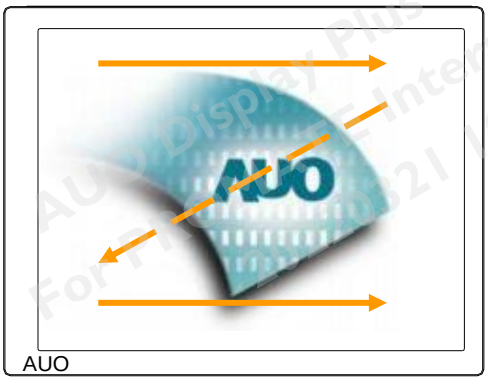
6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Signal Description

The following figures show the image seen from the front view. The arrow indicates the direction of scan.



6.2.1 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	No Connect
2	GND	Ground
3	NC	NC
4	NC	NC
5	GND	Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	GND	Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	GND	Ground
12	VDD	LCD logic and driver power
13	VDD	LCD logic and driver power
14	NC	No connect
15	GND	ground
16	GND	ground
17	HPD	HPD signale pin
18	BL_GND	Backlight_ground
19	BL_GND	Backlight_ground
20	BL_GND	Backlight_ground
21	BL_GND	Backlight_ground
22	BL_Enable	Backlight On / Off
23	BL PWM DIM	System PWM signal Input
24	NC	No connect
25	NC	No connect
26	BL_PWR	Backlight power (10.8V~13.2V)
27	BL_PWR	Backlight power (10.8V~13.2V)
28	BL_PWR	Backlight power (10.8V~13.2V)
29	BL_PWR	Backlight power (10.8V~13.2V)
30	NC	No Connect

6.2.2 Connector

Connector Name / Designation	Signal Connector
Manufacturer	STM
Type / Part Number	MSAK24025P30 or compatible
Mating Housing/Part Number	I-PEX 20453-030T-11 or compatible

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		$1/T_{Clock}$	65.3	68.93	75	MHz
Vertical Section	Period	T_V	812	816	800+A	T_{Line}
	Active	T_{VD}	800			
	Blanking	T_{VB}	12	16	A	
Horizontal Section	Period	T_H	1340	1408	1280+B	T_{Clock}
	Active	T_{HD}	1280			
	Blanking	T_{HB}	60	128	B	

Note 1: The above is as optimized setting
Note 2: The maximum clock frequency = (800+A)*(1280+B)*60 < 75 MHz

7. Reliability Test Criteria

Items	Required Condition	Note
Temperature Humidity Bias	40 °C /90%,300Hr	
High Temperature Operation	60 °C, 300Hr (center point of panel surface)	
Low Temperature Operation	0 oC, 300Hr	
Hot Storage	60 °C, 300Hr	
Cold Storage	-20 °C, 300Hr	
Thermal Shock Test	-20 °C /30 min , 60 °C /30 min , 100cycles	
On/off test	On/10 sec, Off/10 sec, 30,000 cycles	
ESD	Contact : ± 8KV/ operation, Class B Air : ± 15KV / operation, Class B	Note 1
Shock test	50G,20ms,Half-sine wave,(±X, ±Y, ±Z), non-operation	
Vibration test	1.5G, (10~200Hz, random), 30 mins / axis (X, Y, Z),non-operation	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

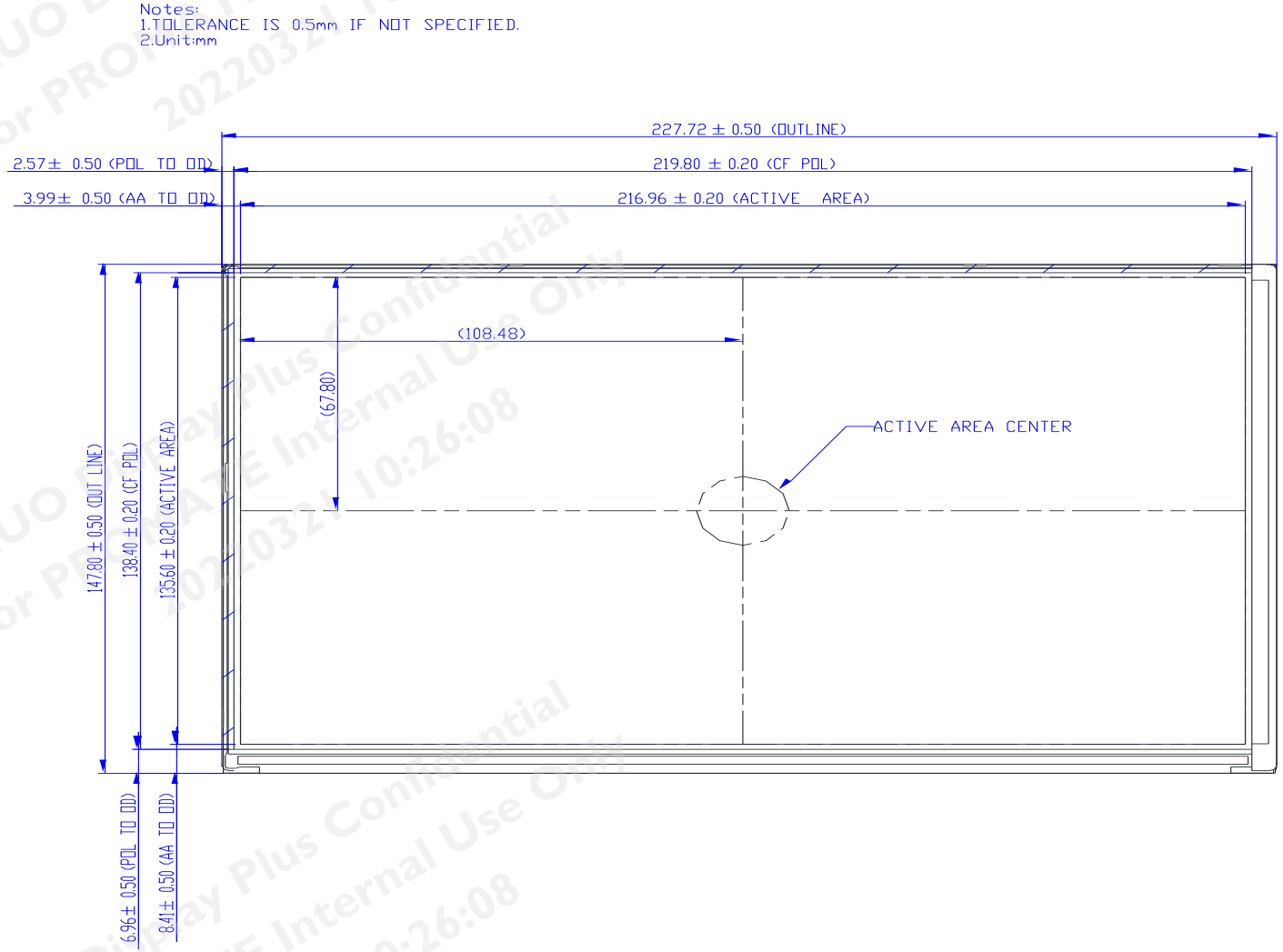
. Self-recoverable. No hardware failures.

Note2:

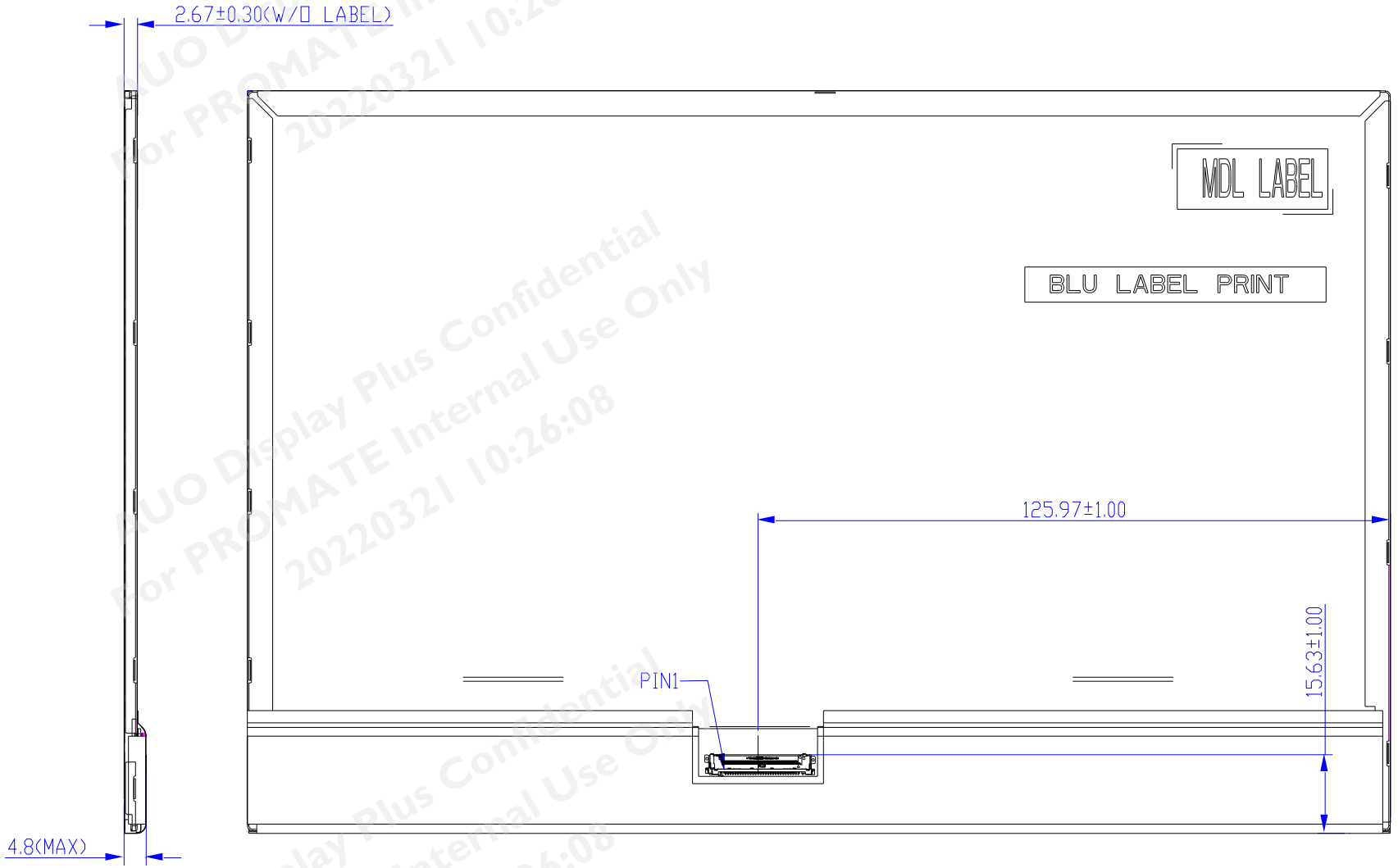
- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.

8. Mechanical Characteristics

8.1 Outline Dimension (Front View)



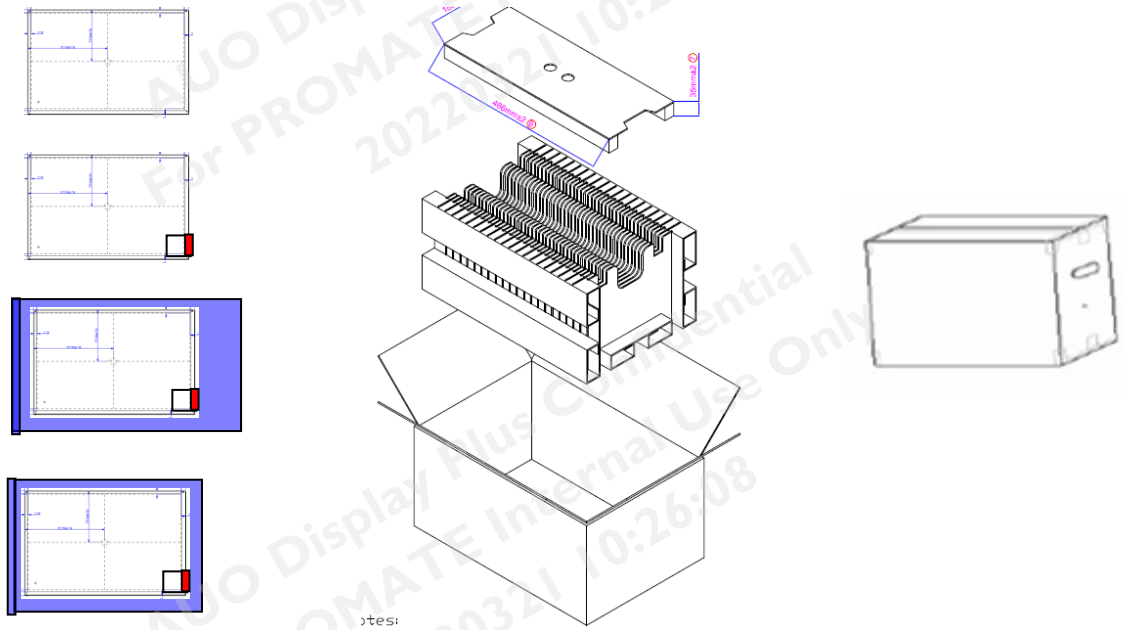
8.2 Outline Dimension (Rear View)



9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

9.2 Carton/Pallet Package



Max capacity：40 TFT-LCD module per carton

Outside dimension of carton: 484*328*257mm

Pallet size： 1150 mm * 980 mm * 132mm

Box stacked 5 layers

Box stacked

Module by air：(2 *3) *5 layers，one pallet put 30 boxes，total 1200pcs module
Module by sea：(2 *3) *5 layers + (2 *3) *2 layers , two pallet put 42 boxes，total 1680pcs module
Module by sea_HQ：(2 *3) *5 layers+(2 *3) *3 layers, two pallet put 48 boxes, total 1920pcs module

10 Safety

10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

10.2 Materials

10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

UL 60950-1 second edition	U.S.A. Information Technology Equipment