Product Specification

AU OPTRONICS CORPORATION

() Preliminary Specifications
(v) Final Specifications

Module	14'' inch Color TFT-LCD
Model Name	G140HAN01.1

Customer	***Date***	**Approved by**	**Date**
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2. General Description

This specification applies to the Color Active Matrix Liquid Crystal Display G140HAN01.1 composed of a TFT-LCD display, a driver and power supply circuit, and a LED backlight system. The screen format is intended to support the 16:9 FHD, 1920(H)X1080(V) screen and 262K colors with LED backlight driving circuit. All input signals are eDP(Embeded Display Port) interface compatible.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ºC condition:

Items	Unit	Specifications
Screen Diagonal	[mm]	354.95
Active Area	[mm]	309.37mm x 174.02mm
Resolution		1920 (H) x 3(RGB) x 1080 (V)
Pixel Pitch	[mm]	0.161(H) x 0.161 (V)
Pixel Arrangement		RGB Vertical Strip
Display Mode		Normal Black
Nominal Input Voltage VDD	[Volt]	+3.3V typ
Power Consumption	[Watt]	7.2W Max (include logic and Blu power)
Weight	[Grams]	580g Max
Physical Size	[mm]	319mm(H)x190.76mm(V)x7.8mm(D) (typ.), non PCBA side 4.9mm , ,
Electrical Interface		2 lan eDP 1.2
Surface Treatment		Glare, Hardness 3H
Support Color		6 bit + FRC
Temperature Range Operating Storage (Non-Operating)	 [ºC] [ºC]	 0 ~ +50 -20 ~ +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

Item	Unit	Conditions		Min.	Typ.	Max.	Note
White Luminance	cd/m^2			320	400		1
Uniformity	%	5 points		75			2,3
Contrast Ratio	--				800		4
Response Time	msec	Rising			15	20	5
		Falling			10	15	
		Rising + Falling			25	35	
Viewing Angle	degree	Horizontal CR >= 10	(Right)	85	89		6
			(Left)	85	89		
		Vertical CR >= 10	(Upper)	85	89		
			(Lower)	85	89		
Color / Chromaticity Coordinates (CIE 1931)	--	Red x		0.584	0.634	0.684	
		Red y		0.283	0.333	0.383	
		Green x		0.257	0.307	0.357	
		Green y		0.565	0.615	0.665	
		Blue x		0.108	0.158	0.208	
		Blue y		0.003	0.053	0.103	
		White x		0.263	0.313	0.363	
		White y		0.279	0.329	0.379	
Color Gamut	%				72		

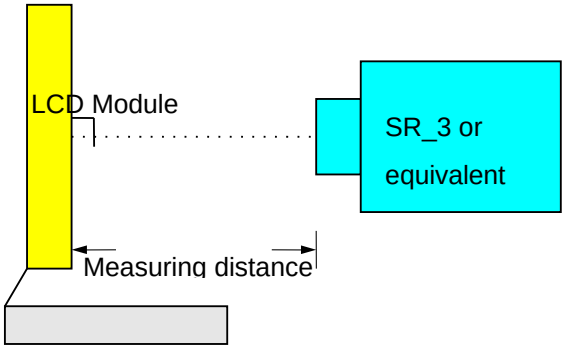
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

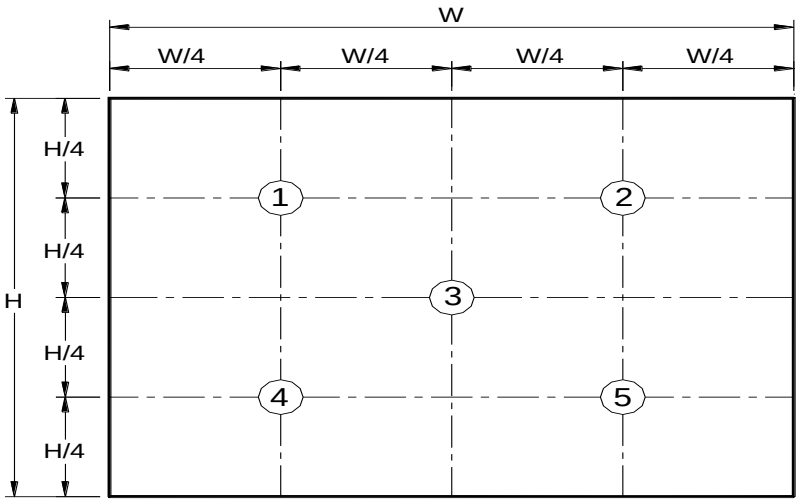
Aperture 1◦ with 50cm viewing distance

Test Point Center

Environment *< 1 lux*



Note 2: Definition of 5 points position



Note 3: The luminance uniformity of 5 points is defined by dividing the minimum luminance values by the maximum test point luminance

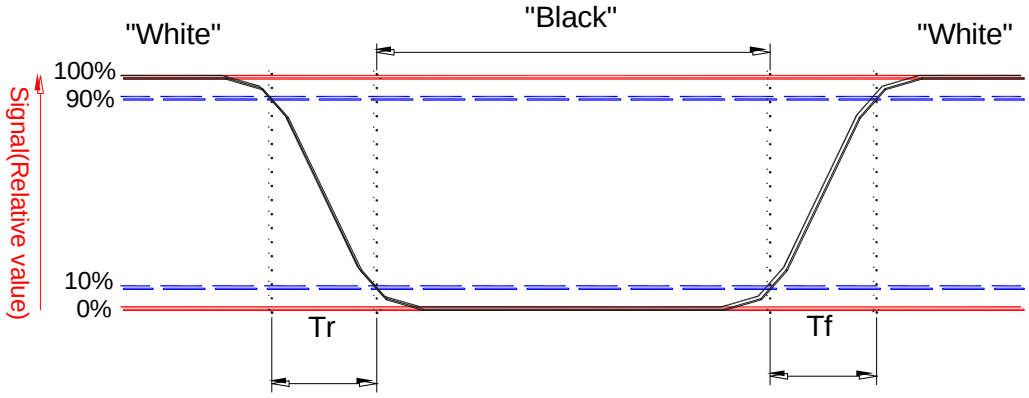
$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

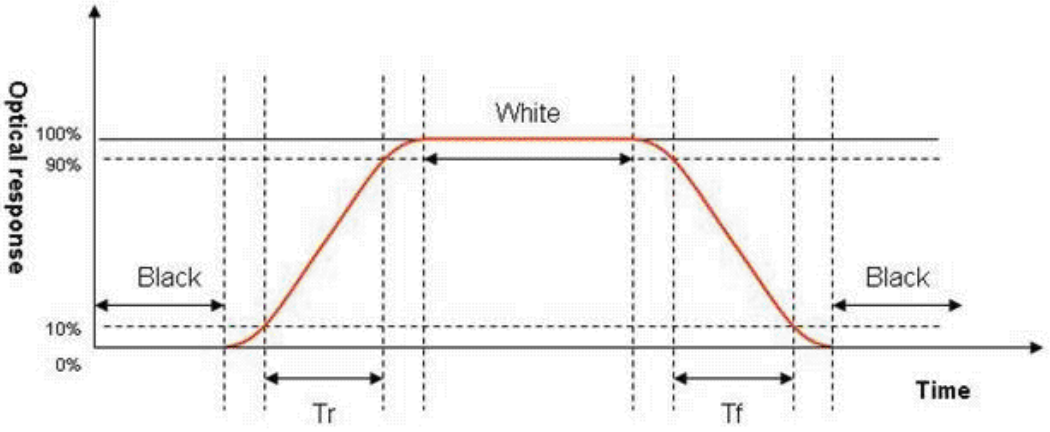
Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

Note 5: Definition of response time:

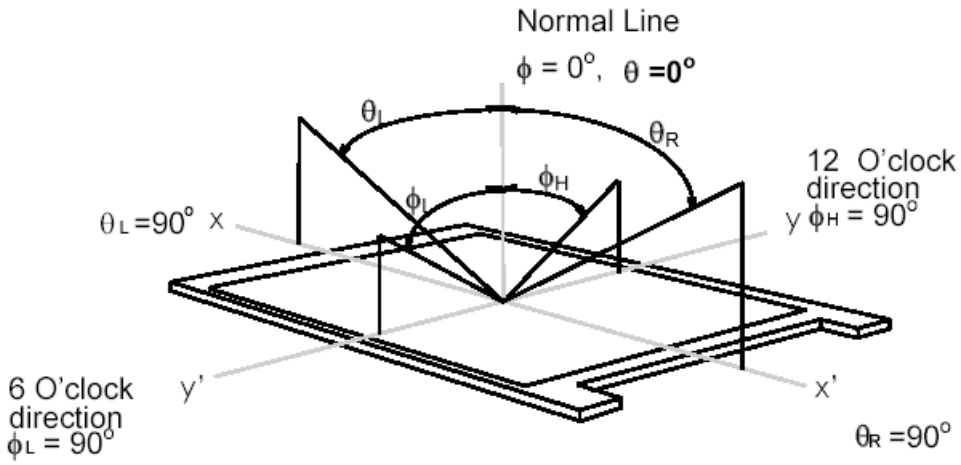
The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.





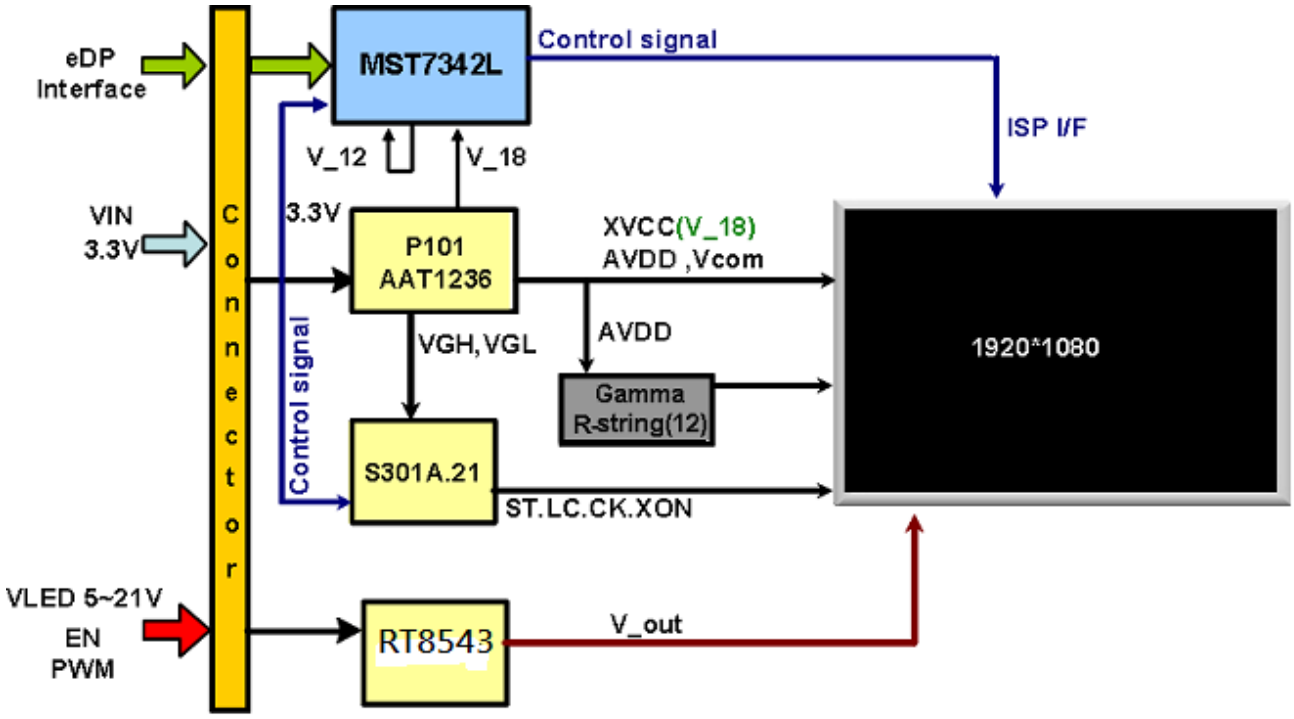
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 14 inch color TFT/LCD module:



4. Absolute Maximum Ratings

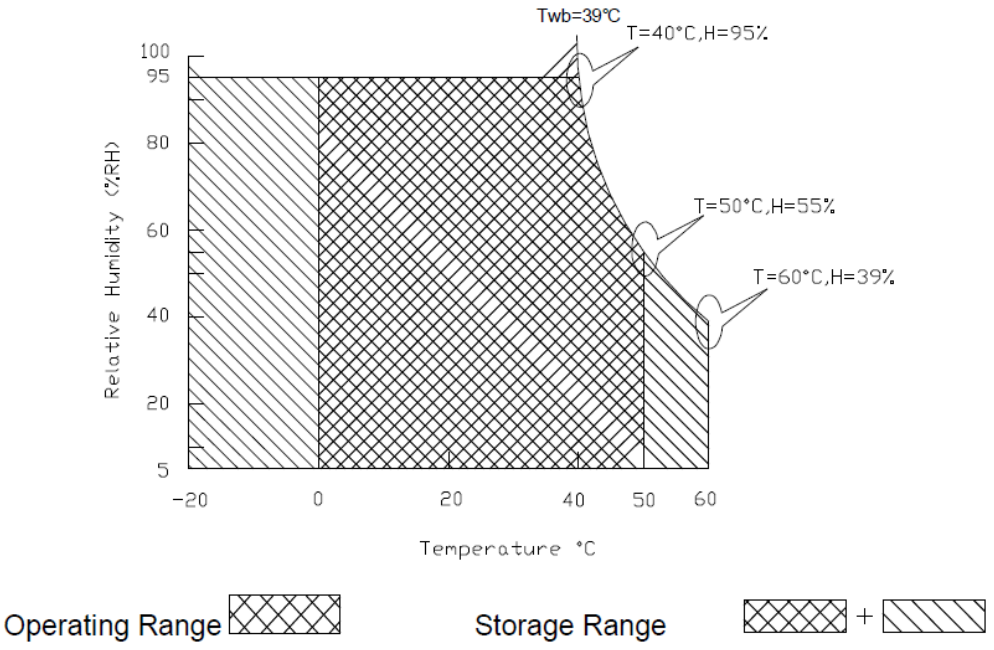
4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit
Logic/LCD drive Voltage	Vin	-0.3	+4.0	[Volt]

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	0	50	[°C]
Operation Humidity	HOP	5	95	[%RH]
Storage Temperature	TST	-20	60	[°C]
Storage Humidity	HST	5	95	[%RH]

Note: Maximum Wet-Bulb should be 39 °C and no condensation.



5. Electrical Characteristics

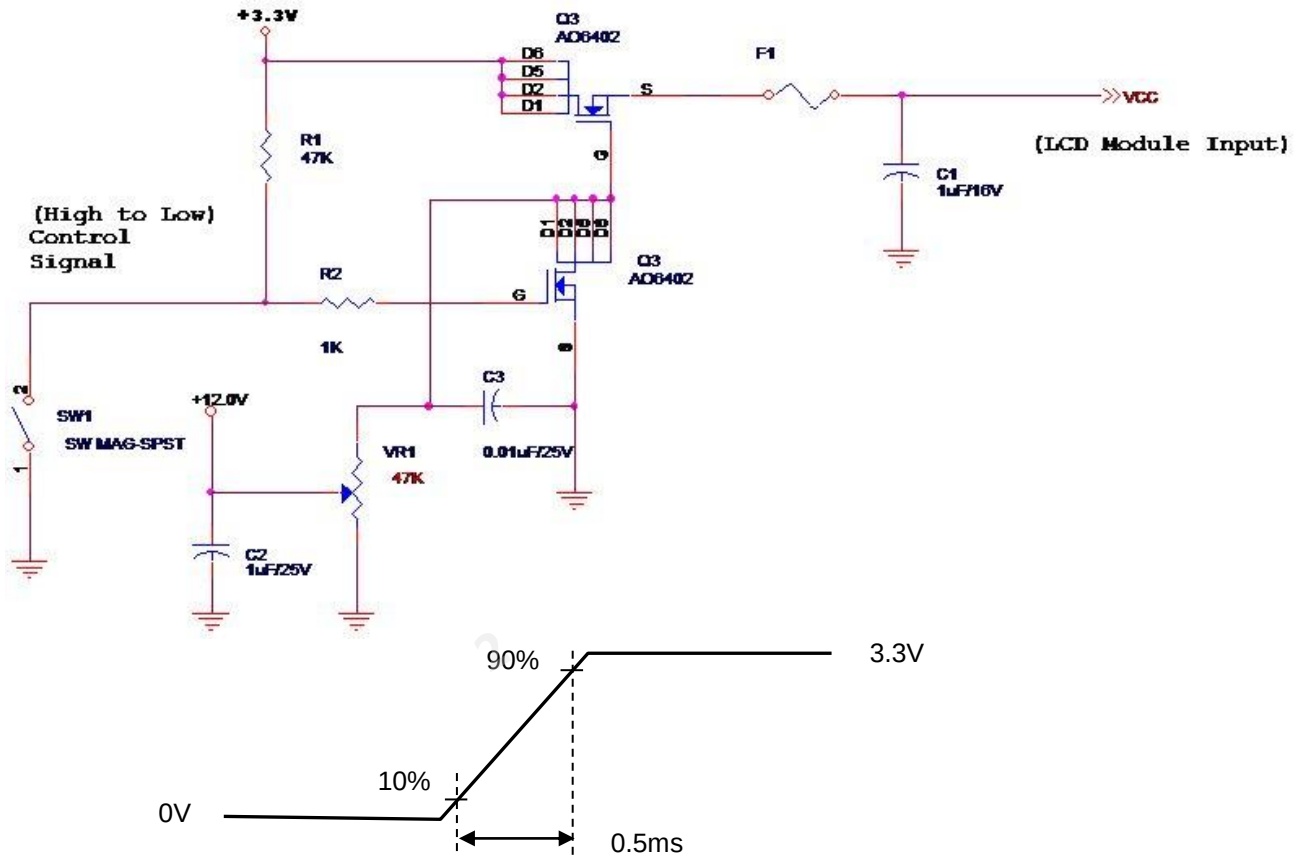
5.1 TFT LCD Module

Input power specifications are as follows; The power specification are measured under 25℃ and frame frenquency under 60Hz

Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power			1.1	[Watt]	1
IDD	IDD Current			367	[mA]	1
IRush	Inrush Current			2000	[mA]	2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Mosaic pattern (PDD (max) = VDD(min) x IDD(max))

Note 2：Measure Condition



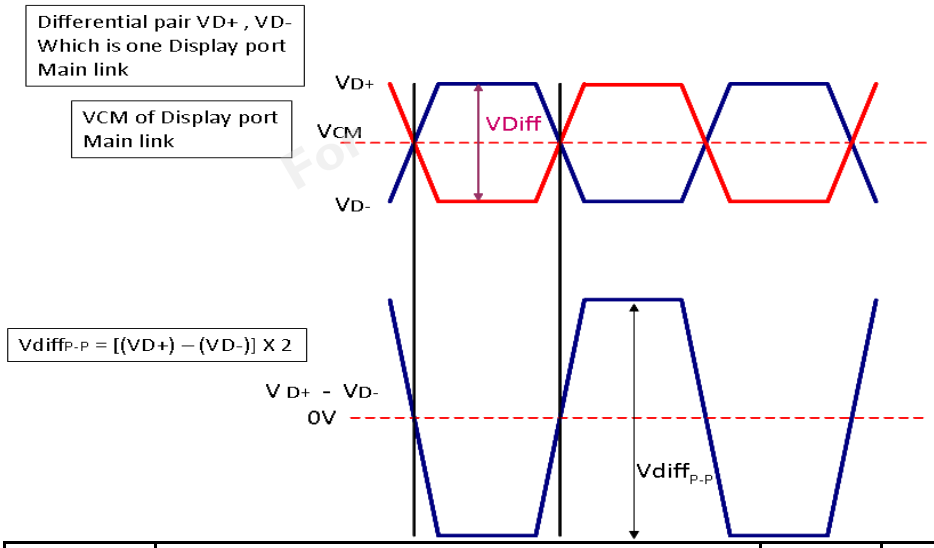
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

Display Port main link signal:

Signal electrical characteristics are as follows;



Symble	Parameter	Min	Typ.	Max	Unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	150		1320	mV

Follow as VESA display port standard V1.3

Display Port VHPD signal:

Symble	Parameter	Min	Typ	Max	Unit	Note
VHPD	HPD Voltage	2.25		3.6	V	

Follow as VESA display port standard V1.

5.2 Backlight Unit

Parameter guideline for LED

Following characteristics are measured under a stable condition using an inverter at 25℃ (Room Temperature):

LED characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
PLED	Backlight Power Consumption	--	5.54	6.1	[Watt]	Ta = 25°C, Note 1 Vin =12V
LTLED	LED Life-Time	50000	--	--	Hour	Ta = 25°C, Note2

Note 1: Calculator value for reference P_{LED} = V_F (Normal Distribution) * I_F (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

Backlight input signal characteristics

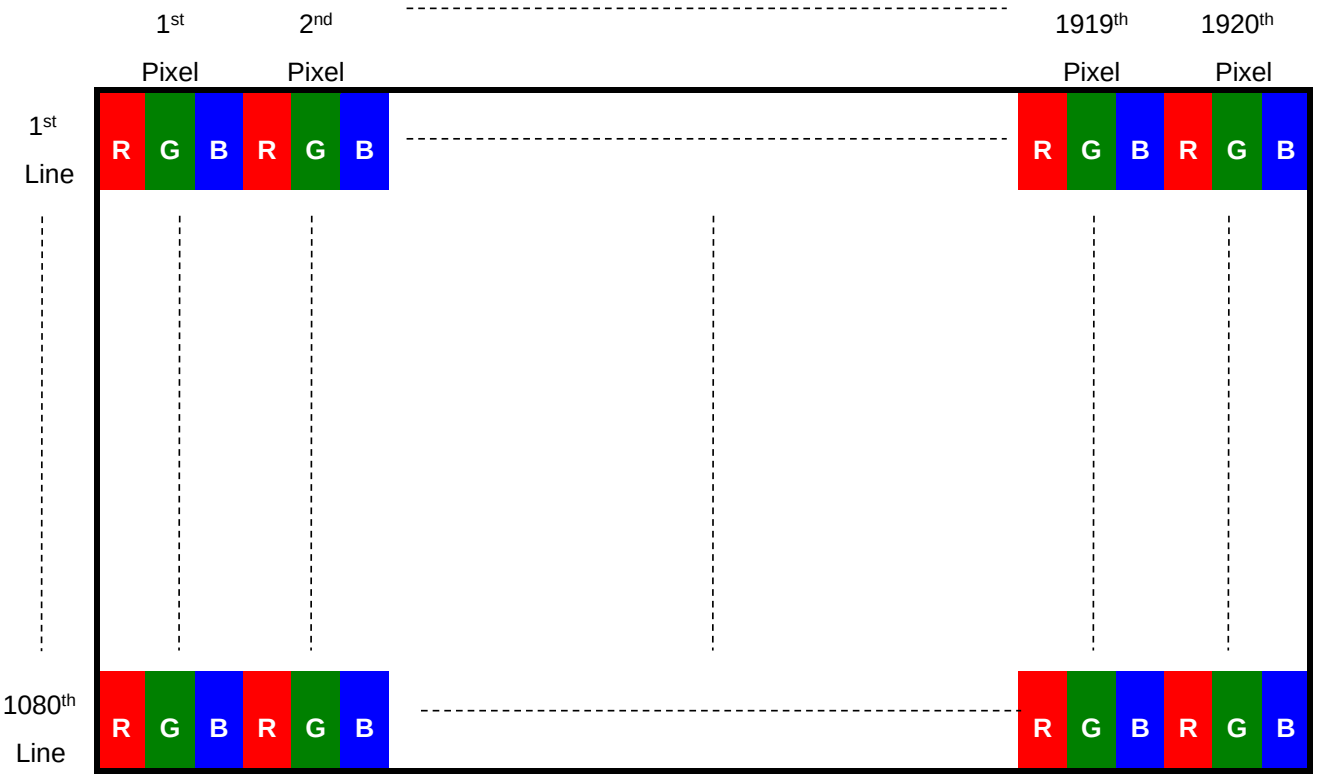
Symbol	Parameter	Min	Typ	Max	Units	Remark
VLED (Note 1)	LED Power Supply	6.5	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
VLED_EN	LED Enable Input High Level	2.5	--	5.5	[Volt]	
	LED Enable Input Low Level	--	--	0.7	[Volt]	
VPWM_EN	PWM Logic Input High Level	2.5	--	5.5	[Volt]	
	PWM Logic Input Low Level	--	--	0.7	[Volt]	
FPWM	PWM Input Frequency *1	200	1K	20K	Hz	
Duty	PWM Duty Ratio	5	--	100	%	

Note1: Measured on panel VLED

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Integration Interface Requirement

6.2.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

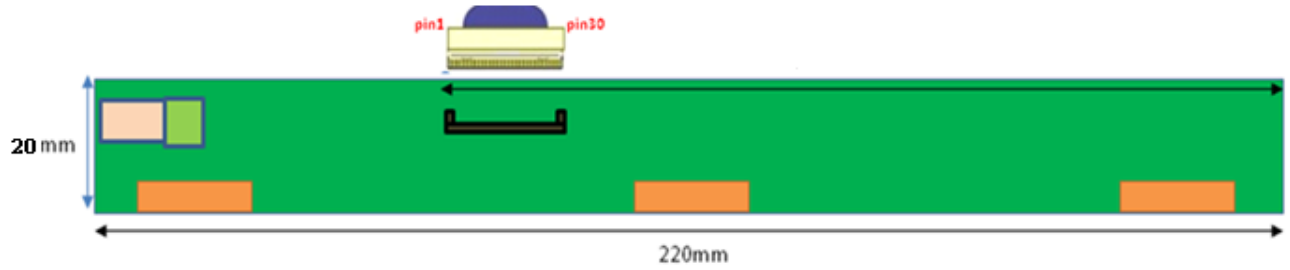
Connector Name / Designation	For Signal Connector
Manufacturer	IPEX or compatible
Type / Part Number	IPEX 20455-030E-12
Mating Housing/Part Number	IPEX 20453-030T-11 or compatible

6.2.2 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

Pin No,	Signal	Description
1	NC	NO Connect
2	H_GND	High Speed Ground
3	Lane1_N	Comp Signal Link Lane 1
4	Lane1_P	True Signal Link Lane 1
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	LCD_Self_Test	LCD Panel Self Test Enable
15	LCD_GND	LCD logic and driver ground
16	LCD_GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight On / Off
23	BL_PWM_DIM	System PWM signal Input
24	NC	No connect

25	NC	No connect
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No connect



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.

6.3 Interface Timing

6.3.1 Timing Characteristics

Basically, interface timings should match the 1920x1080 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-		60	-	Hz
Clock frequency		1/ T_{Clock}		141		MHz
Vertical Section	Period	T_V		1116	1080+A	T_{Line}
	Active	T_{VD}		1080		
	Blanking	T_{VB}		36	A	
Horizontal Section	Period	T_H		2104	1920+B	T_{Clock}
	Active	T_{HD}		1920		
	Blanking	T_{HB}		184		

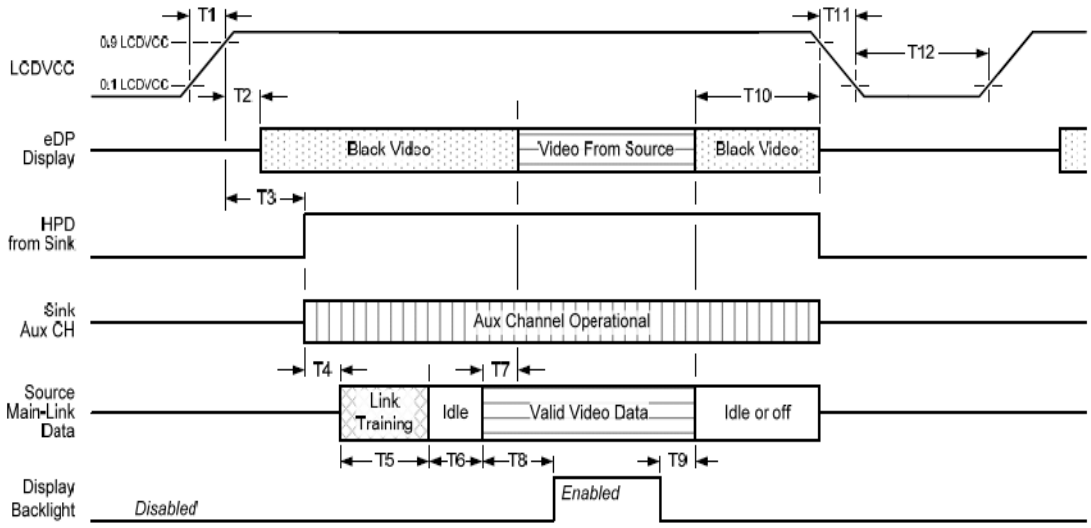
Note 1 : The above is as temporary setting

Note 2 : The maximum clock frequency = (1920+B)*(1080+A)*60 < 149.1 MHz

6.4 Power ON / OFF Sequence

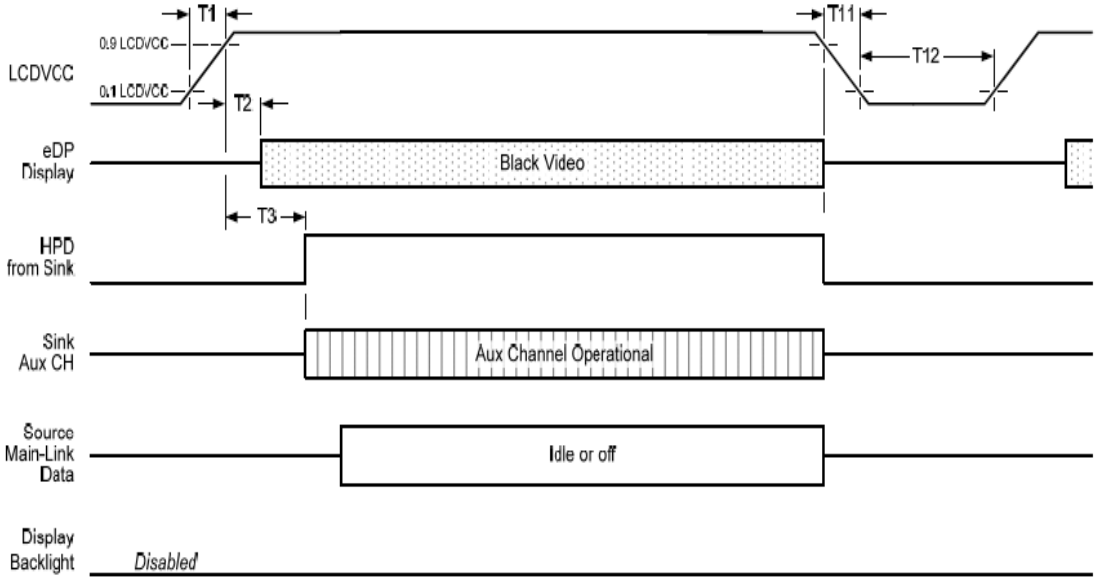
Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off

Display Port Panel Power Sequence



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH Transaction Only



Display port interface power up/down sequence, AUX_CH transaction only

Display Port Panel Power Sequence Timing Parameter

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	0ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	500ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:

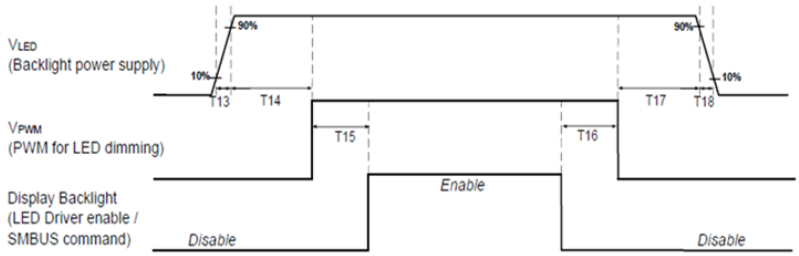
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).

-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port Panel B/L Power Sequence Timing Parameter

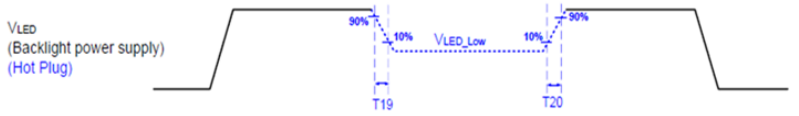


	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Reliability Test Criteria

Items	Required Condition	Note
Temperature Humidity Bias	40 °C /90%,300Hr	
High Temperature Operation	50 °C, 300Hr (center point of panel surface)	
Low Temperature Operation	0 °C, 300Hr	
Hot Storage	60 °C, 300 hours	
Cold Storage	-20 °C, 300 hours	
Thermal Shock Test	-20 °C /30 min ,60 °C /30 min ,100cycles, 40 °C minimun ramp rate	
Hot Start Test	70 °C /1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	-20 °C /1 Hr min. power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	50G,20ms,Half-sine wave,(+-X,+-Y,+-Z)	
Vibration Test (Non-Operating)	1.5G, 10~200~10Hz, Sine wave 30mins/axis, 3 direction (X, Y, Z)	
On/off test	On/10 sec, Off/10 sec, 30,000 cycles	
ESD	Contact : ± 8KV/ operation, Class B Air : ± 15KV / operation, Class B	Note 1
EMI	30-230 MHz, limit 40 dBu V/m, 230-1000 MHz, limit 47 dBu V/m	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

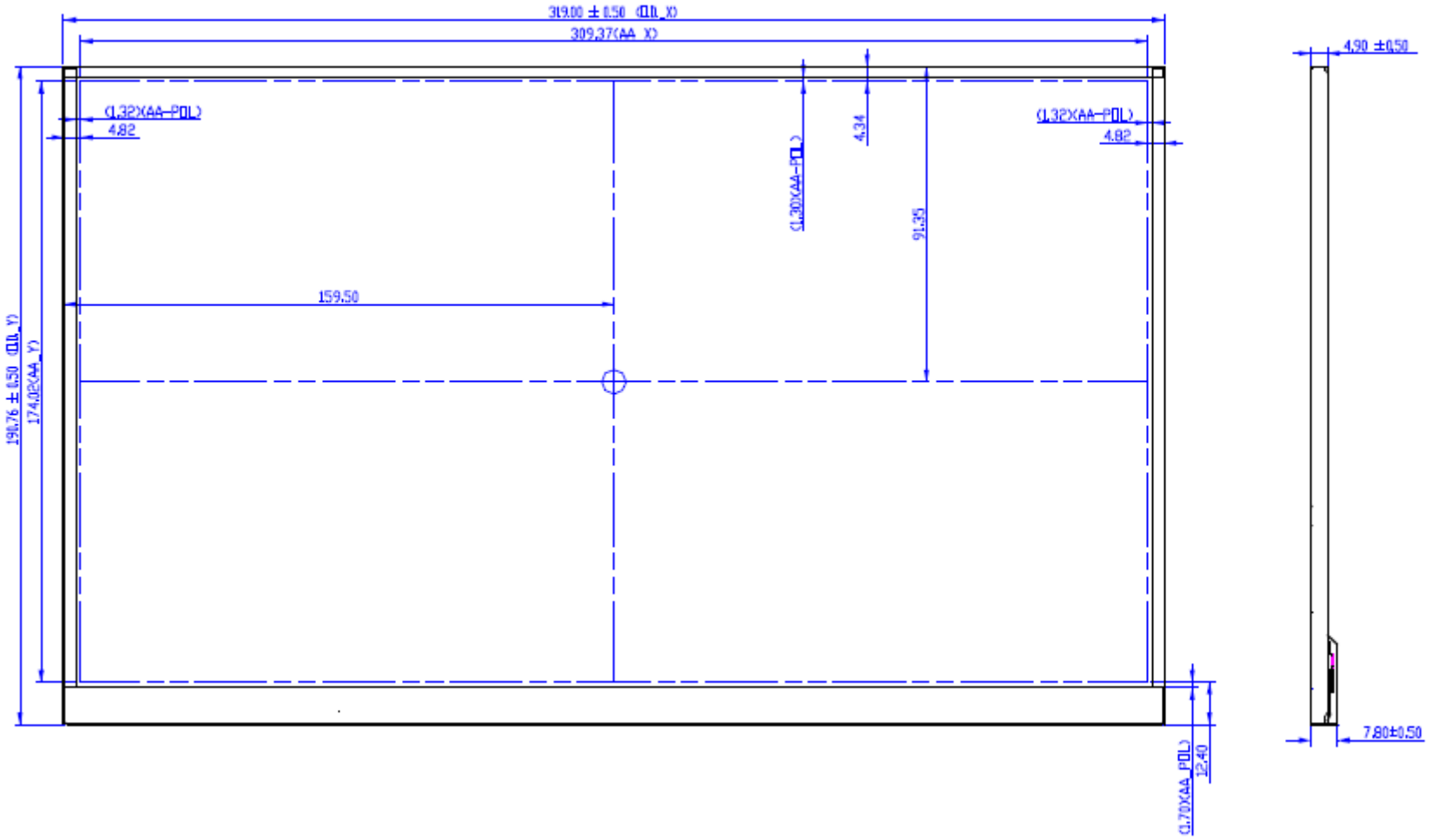
. Self-recoverable. No hardware failures.

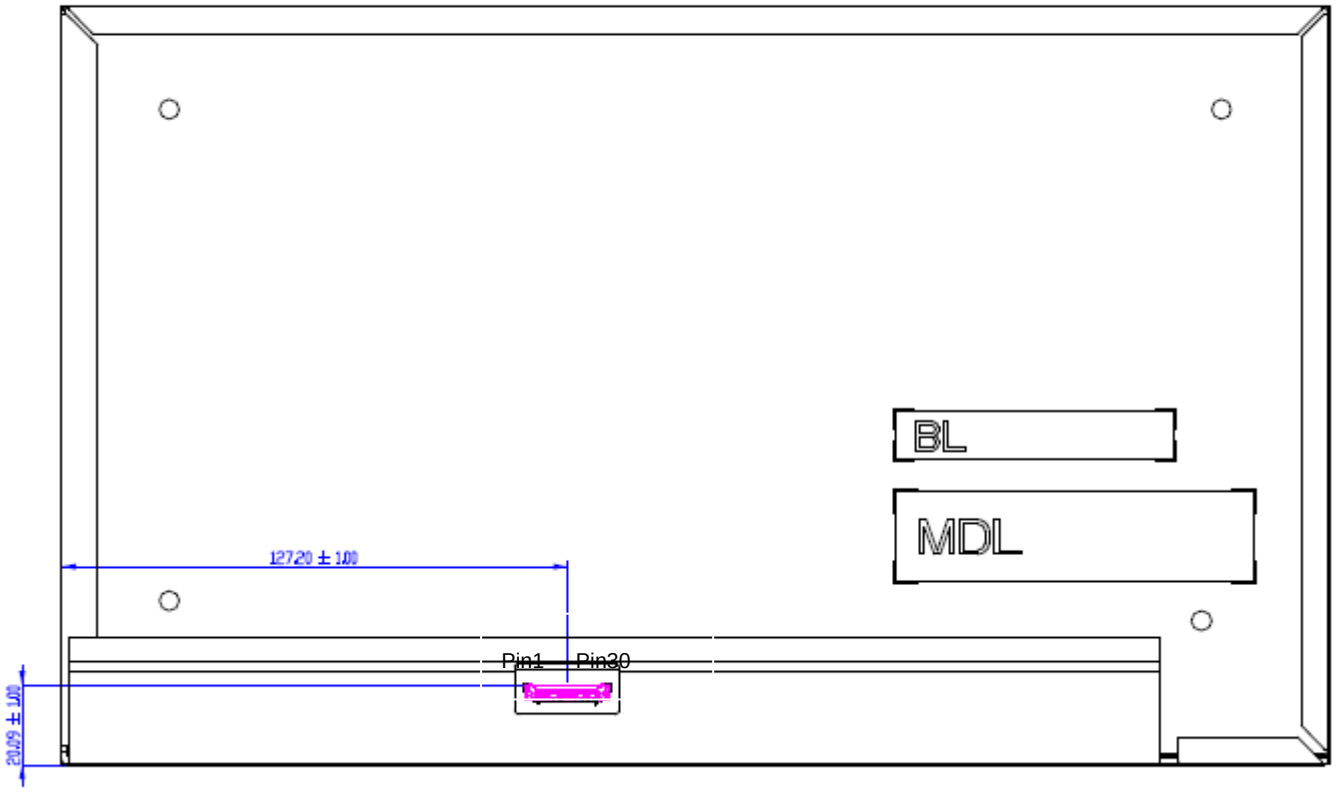
Note2:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.

8. Mechanical Characteristics

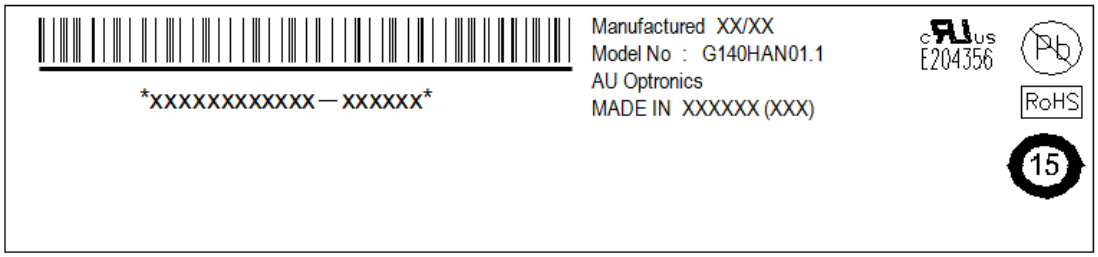
8.1 LCM Outline Dimension



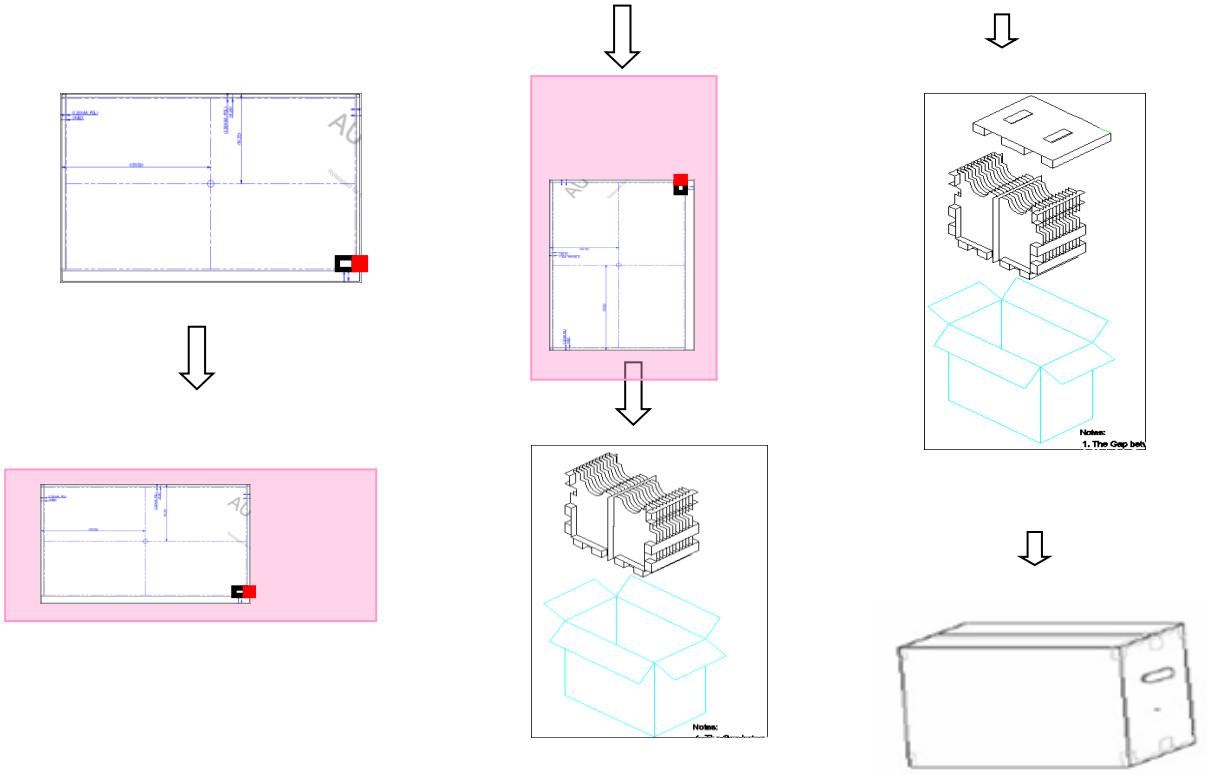

BL
MDL
127.20 ± 1.00
Pin1
Pin30
20.09 ± 1.00

9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)



9.2 Carton Package



Max capacity：22 pcs TFT-LCD module per carton

Max weight: 14.56 kg per carton

Outside dimension of carton: 484(L) mm x 279(W) mm x 432(H) mm

Pallet size：1150 * 910 * 132mm

Module by air：(2 *3) *3 layers，one pallet put 18 boxes，total 396pcs module

Module by sea：One pallet (2 *3) *3 layers + One pallet (2 *3) *1 layers，total 528pcs module

Module by sea_ HQ : One pallet (2 *3) *3 layers + One pallet (2 *3) *2ayers Total 660pcs module