2W Stereo Audio Amplifier

Features

- **Depop Circuitry Integrated**
- **Output Power at 1% THD+N, VDD=5V**
  --2W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Bridge-Tied Load (BTL), Single-Ended (SE)**
- **Shutdown Control Available**
- **Thermal protection**
- **Surface-Mount Power Package**
  20-Pin TSSOP-P

Applications

- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

General Description

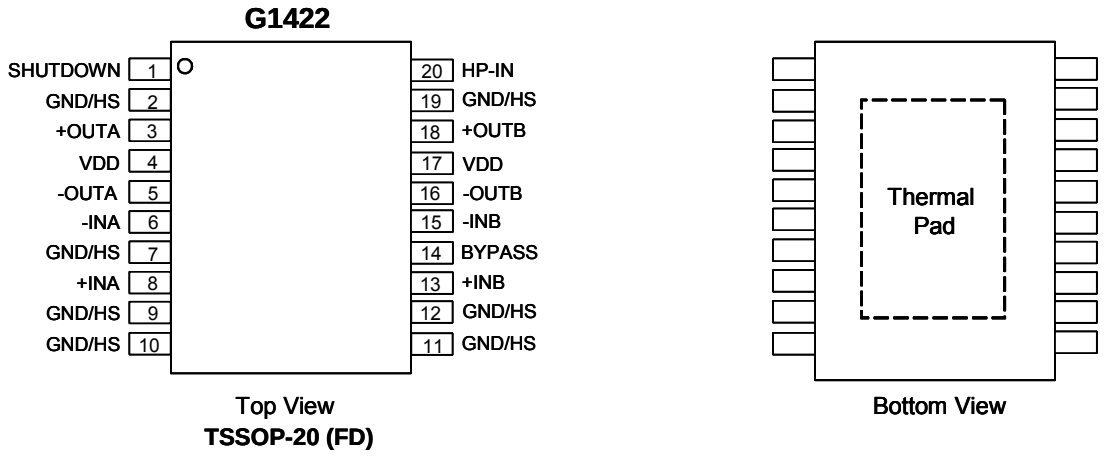
The G1422 is a stereo audio power amplifier in 20pin TSSOP thermal pad package. It can drive 2W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage. Its THD is smaller than 1% under the above operation condition. To simplify the audio system design in the notebook application, the G1422 supports the Bridge-Tied Load (BTL) mode for driving the speakers, Single-End (SE) mode for driving the headphone. For the low current consumption applications, the SHDN mode is supported to disable the G1422 when it is idle. The current consumption can be further reduced to below 2μA.

Ordering Information

ORDER NUMBER	ORDER NUMBER (Pb free)	MARKING	TEMP. RANGE	PACKAGE
G1422F2U	G1422F2Uf	G1422	-40°C to +85°C	TSSOP-20 (FD)

Note:F2: TSSOP-20 (FD)
U: Tape & Reel

Pin Configuration



Top View
TSSOP-20 (FD)

Bottom View

Note: Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Absolute Maximum Ratings

Supply Voltage, V_{CC}.....6V
Operating Ambient Temperature Range
T_A.....-40°C to +85°C
Maximum Junction Temperature, T_J.....150°C
Storage Temperature Range, T_{STG}.....-65°C to+150°C
Reflow Temperature (soldering, 10sec).....260°C

Power Dissipation (1)
$T_A \le 25°C$.....2.7W
$T_A \le 70°C$.....1.7W
$T_A \le 85°C$.....1.4W
Electrostatic Discharge, V_{ESD}
Human body mode.....-3000 to 3000(2)

Note:
(1): Recommended PCB Layout
(2): Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, V_{DD} = 5.0V, T_A=+25°C, unless otherwise noted

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Supply Current	I_{DD}	V_{DD} = 5V	Stereo BTL	---	8.5	15	mA
			STEREO SE	---	4	8	
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2		---	5	50	mV
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V		---	0.1	2	μA
Headphone High Input Voltage	V_{IH}			4	---	---	V
Headphone Low Input Voltage	V_{IL}			---	---	0.8	V

(AC Operation Characteristics, V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω	---	2	---	W
		THD = 1%, BTL, R_L = 8Ω	---	1.25	---	
		THD = 10%, BTL, R_L = 4Ω	---	2.5	---	
		THD = 10%, BTL, R_L = 8Ω	---	1.6	---	
		THD = 1%, SE, R_L = 4Ω	---	550	---	mW
		THD = 1%, SE, R_L = 8Ω	---	340	---	
		THD = 10%, SE, R_L = 4Ω	---	700	---	
		THD = 10%, SE, R_L L = 8Ω	---	440	---	
		THD = 0.5%, SE, R_L = 32Ω	---	92	---	
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω	---	300	---	m%
		P_O = 1W, BTL, R_L = 8Ω	---	100	---	
		P_O = 75mW, SE, R_L = 32Ω	---	15	---	
		V_I = 1V, RL = 10KΩ, G = 1, SE	---	2.5	---	
Maximum output power bandwidth	B_{OM}	G = 1, THD = 1%	---	20	---	kHz
Phase margin		R_L = 4Ω, Open Load	---	65	---	°
Power supply ripple rejection	PSRR	f = 120Hz	---	75	---	dB
Channel-to-channel output separation		f = 1kHz	---	80	---	dB
Input separation			---	80	---	dB
BTL attenuation in SE mode			---	85	---	dB
Input impedance	ZI		---	2	---	MΩ
Signal-to-noise ratio		P_O = 500mW, BTL	---	90	---	dB
Output noise voltage	V_n	Output noise voltage	---	55	---	μV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

Typical Characteristics

Table of Graphs

			FIGURE
THD +N Total harmonic distortion plus noise		vs Frequency	2,4,6,9,11,15,17
		vs Output Power	1,3,5,7,8,10,12,13,14,16,18
V_n	Output noise voltage	vs Frequency	20
	Supply ripple rejection ratio	vs Frequency	19
	Crosstalk	vs Frequency	22,23
	Open loop response	vs Frequency	21
I_{DD}	Supply current	Vs Supply Voltage	24
P_O	Output power	vs Load Resistance	25,26
		Vs Load Resistance	27,28
P_D	Power dissipation	vs Output Power	29,30,31,32

Total Harmonic Distortion Plus Noise vs Output Power

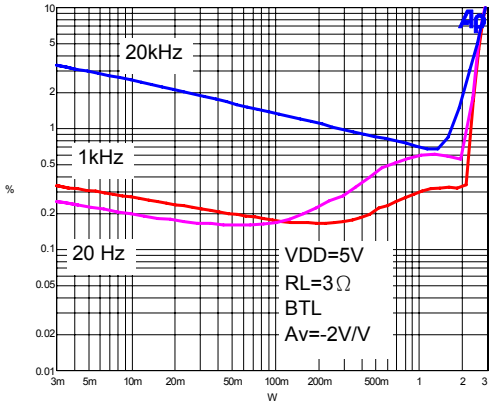


Figure 1

Total Harmonic Distortion Plus Noise vs Frequency

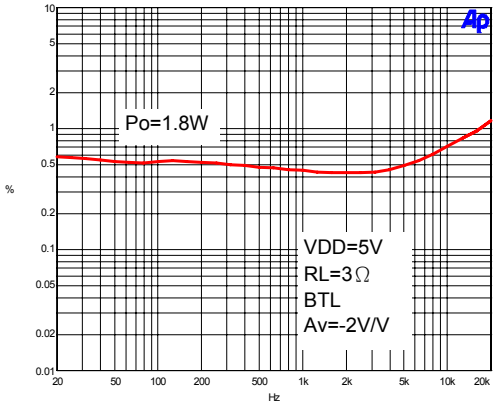


Figure 2

Total Harmonic Distortion Plus Noise vs Output Power

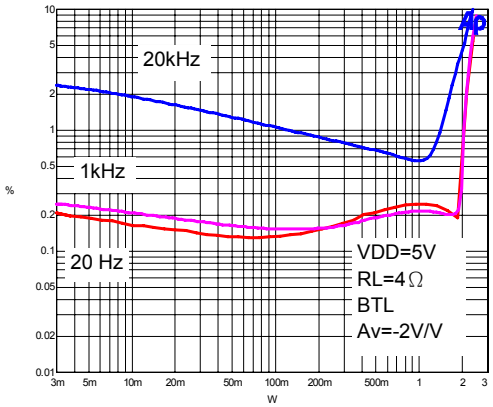


Figure 3

Total Harmonic Distortion Plus Noise vs Frequency

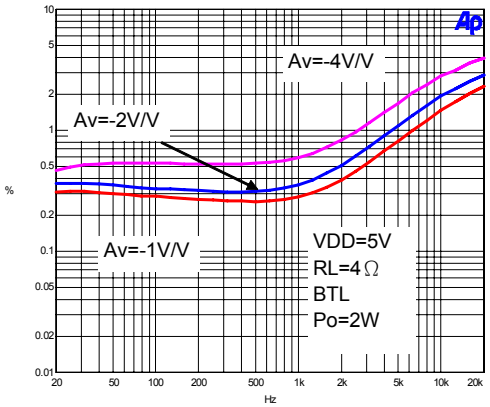


Figure 4

Total Harmonic Distortion Plus Noise vs Output Power

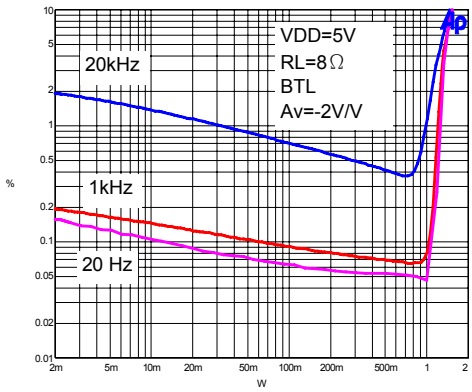


Figure 5

Total Harmonic Distortion Plus Noise vs Frequency

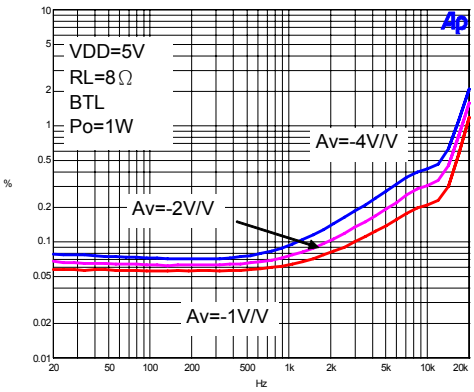


Figure 6

Total Harmonic Distortion Plus Noise vs Output Power

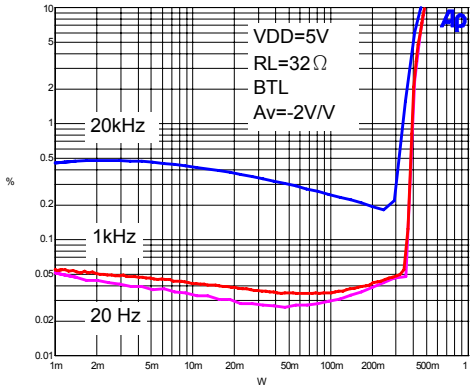


Figure 7

Total Harmonic Distortion Plus Noise vs Frequency

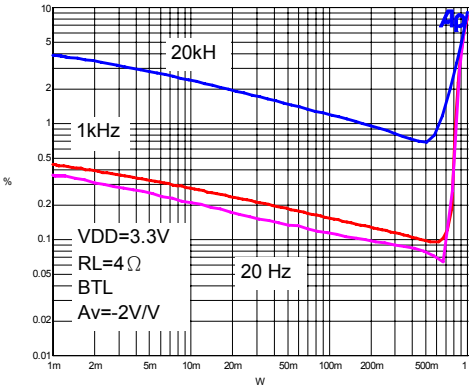


Figure 8

Total Harmonic Distortion Plus Noise vs Frequency

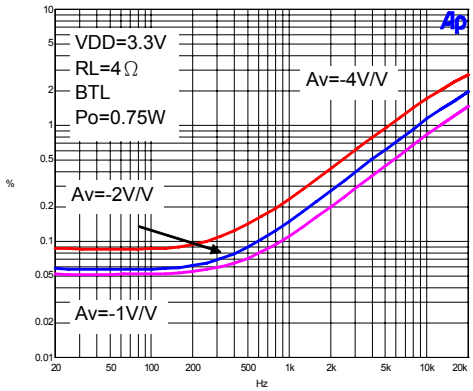


Figure 9

Total Harmonic Distortion Plus Noise vs Output Power

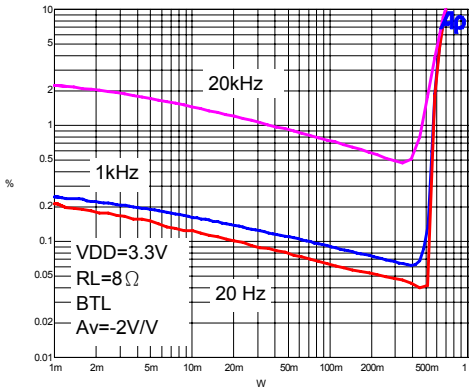


Figure 10

Total Harmonic Distortion Plus Noise vs Frequency

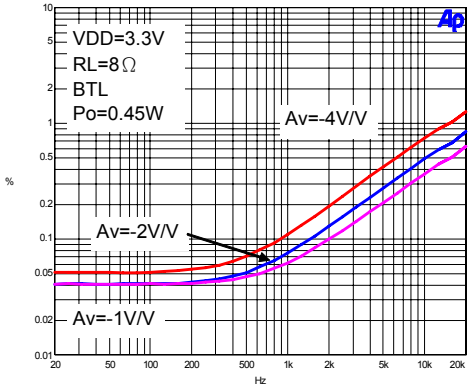


Figure 11

Total Harmonic Distortion Plus Noise vs Output Power

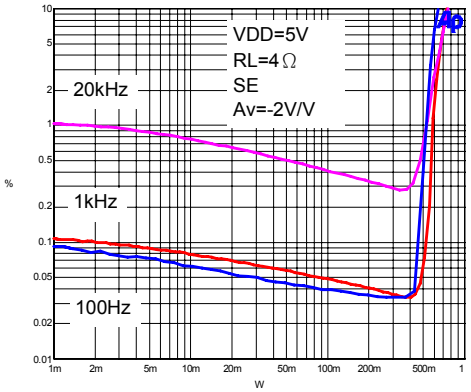


Figure 12

Total Harmonic Distortion Plus Noise vs Output Power

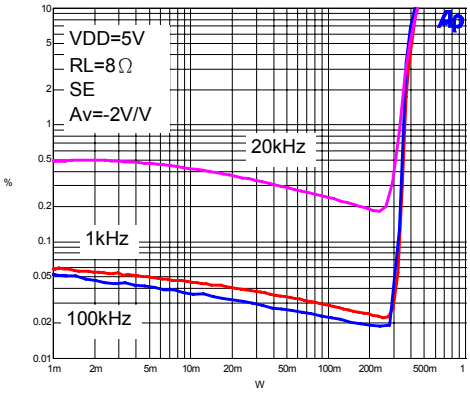


Figure 13

Total Harmonic Distortion Plus Noise vs Output Power

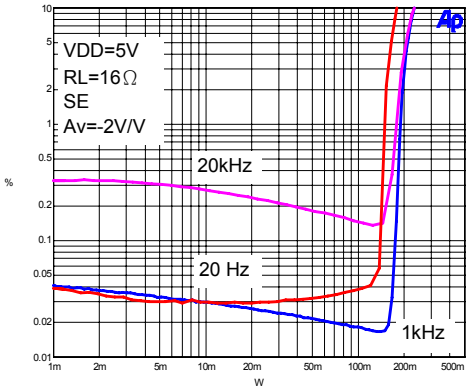


Figure 14

Total Harmonic Distortion Plus Noise vs Frequency

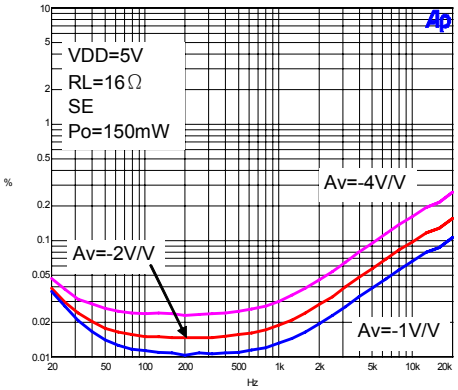


Figure 15

Total Harmonic Distortion Plus Noise vs Output Power

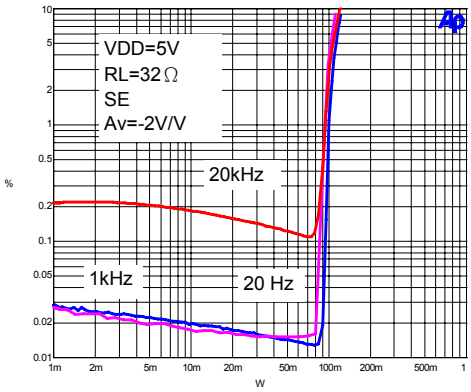


Figure 16

Total Harmonic Distortion Plus Noise vs Frequency

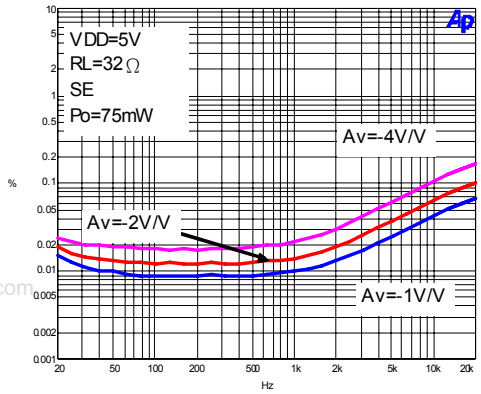


Figure 17

Total Harmonic Distortion Plus Noise vs Output Power

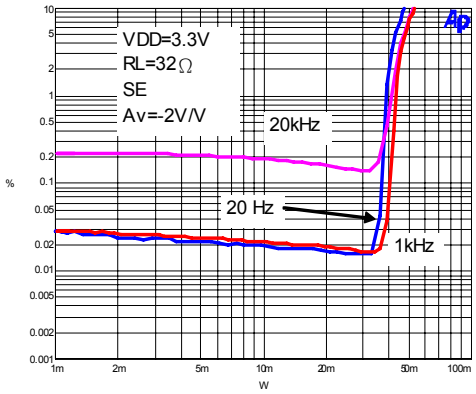


Figure 18

Supply Ripple Rejection Ratio vs Frequency

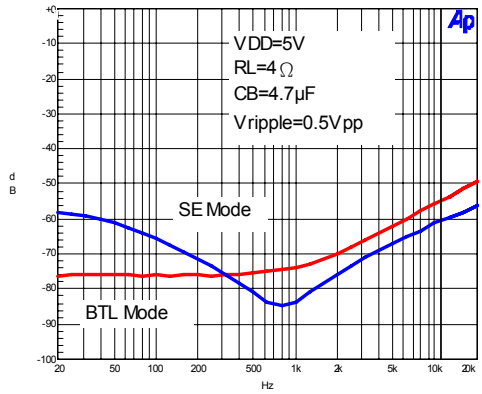


Figure 19

Output Noise Voltage vs Frequency

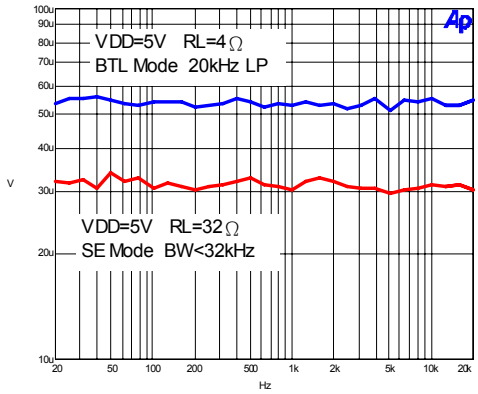


Figure 20

Open Loop Response

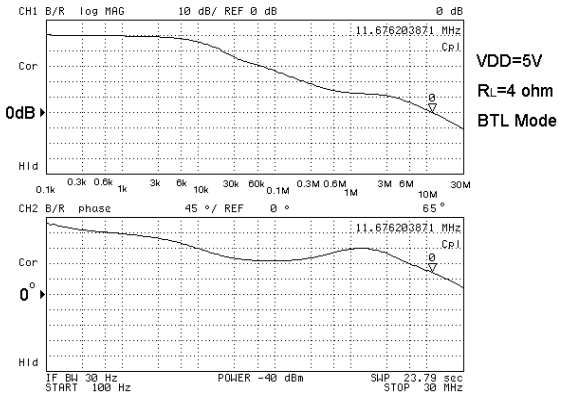


Figure 21

Channel Separation

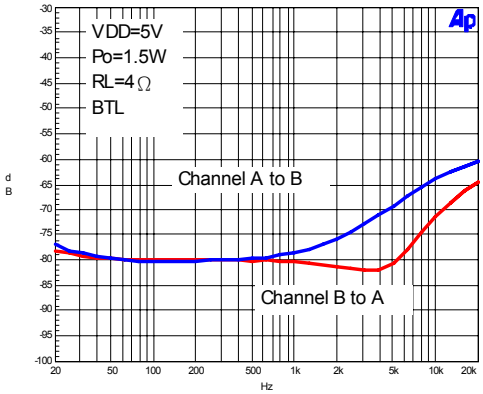


Figure 22

Channel Separation

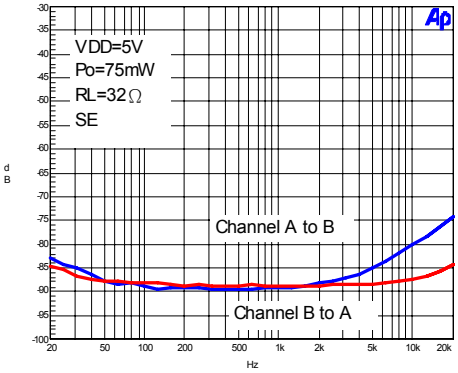


Figure 23

Supply Current vs Supply Voltage

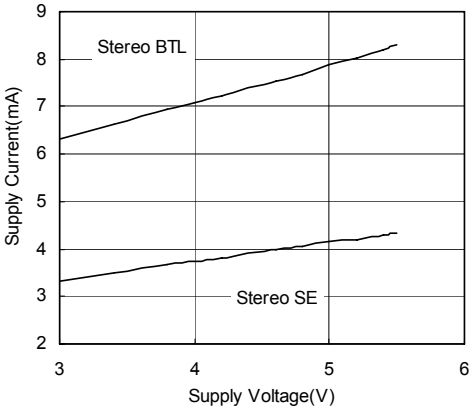


Figure 24

Output Power vs Supply Voltage

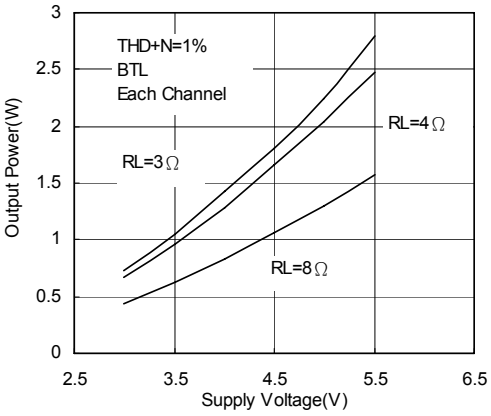


Figure 25

Output Power vs Supply Voltage

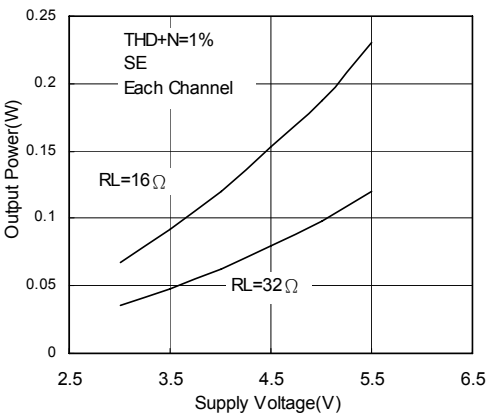


Figure 26

Output Power vs Load Resistance

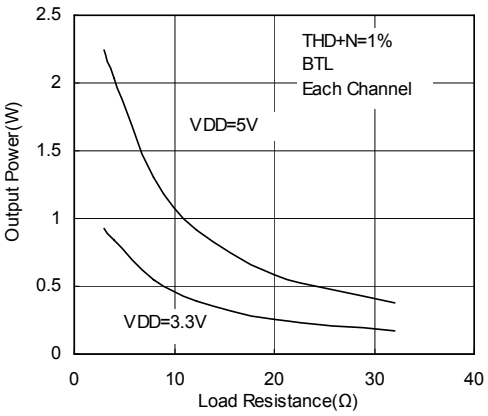


Figure 27

Output Power vs Loard Resistance

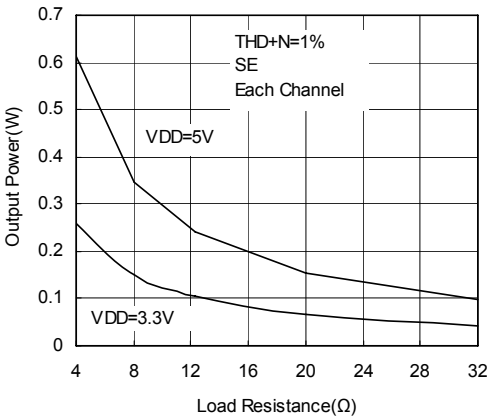


Figure 28

Power Dippipation vs Output Power

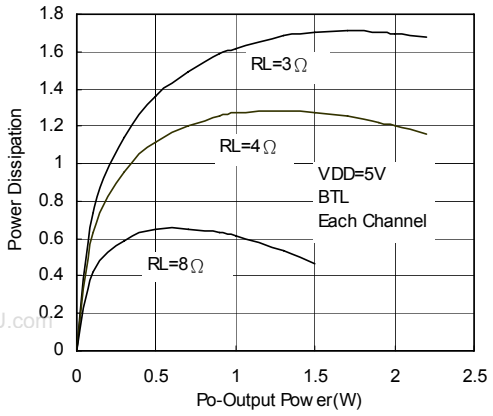


Figure 29

Power Dissipation vs Output Power

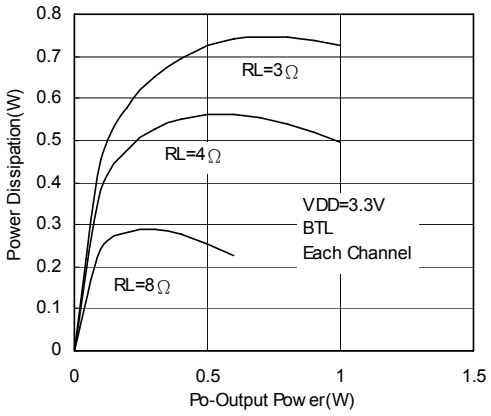


Figure 30

Power Dissipation vs Output Power

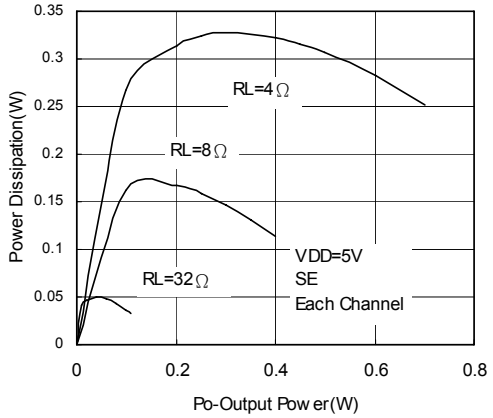


Figure 31

Power Dissipation vs Output Power

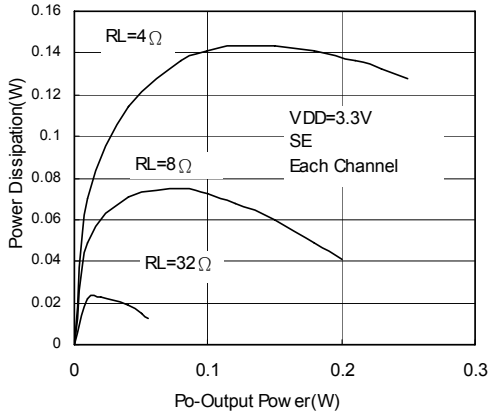
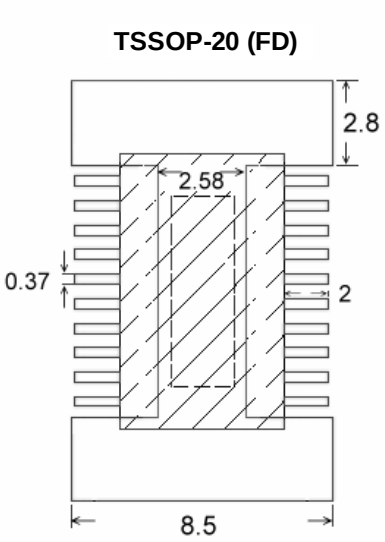


Figure 32

Recommended Minimum Footprint

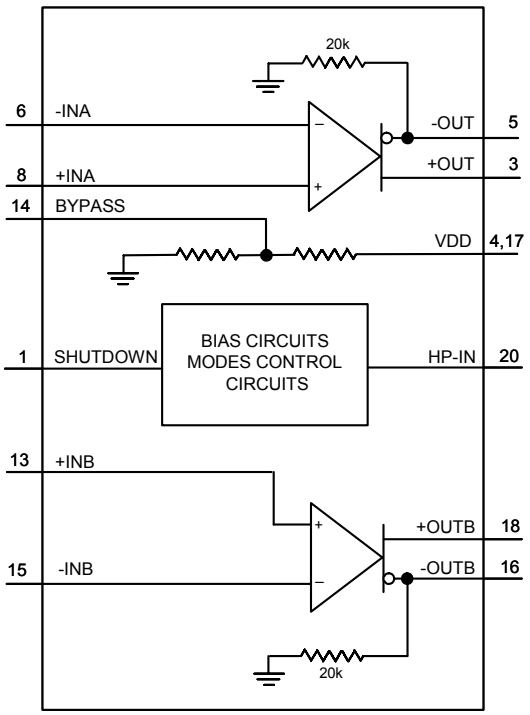
TSSOP-20 (FD)



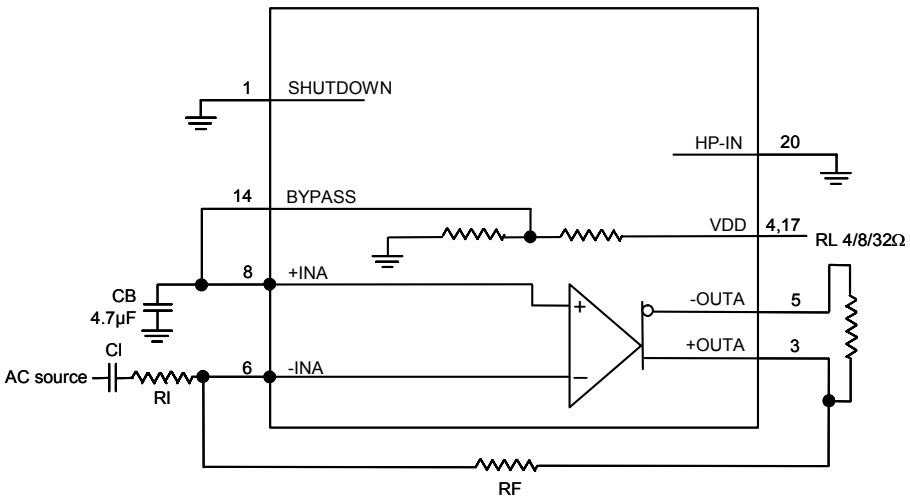
Pin Description

PIN	NAME	I/O	FUNCTION
1	SHUTDOWN	I	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD} is below 2μA.
2,7,9,10,11,12,19	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
3	+OUTA	O	A channel + output in BTL mode, high impedance state in SE mode
4,17	VDD		Supply voltage for circuitry.
5	-OUTA	O	A channel - output in BTL mode, - output in SE mode.
6	-INA	I	A channel input signal I, selected when MUXCTRL is held low.
8	+INA	I	A channel positive input of OPAMP, biasing DC operation of OPAMP
13	+INB	I	B channel positive input of OPAMP, biasing DC operation of OPAMP
14	BYPASS		Connect to voltage divider for internal mid-supply bias.
15	-INB	I	B channel input signal I, selected when MUXCTRL is held low.
16	-OUTB	O	B channel - output in BTL mode, - output in SE mode.
18	+OUTB	O	B channel + output in BTL mode, high impedance state in SE mode
20	HP-IN	I	Mode control signal input, hold low for BTL mode, hold high for SE mode.
Thermal Pad			Recommend connecting the Thermal Pad to the GND for excellent power dissipation.

Block Diagram

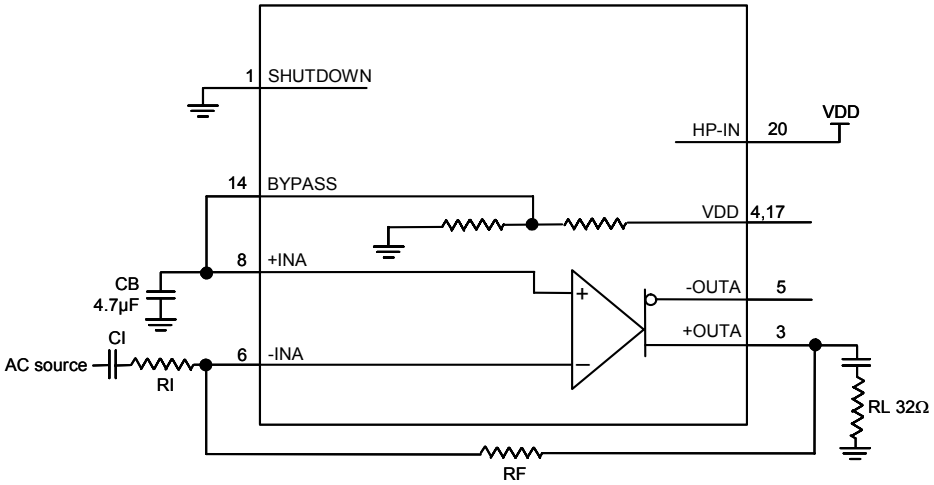


Parameter Measurement Information



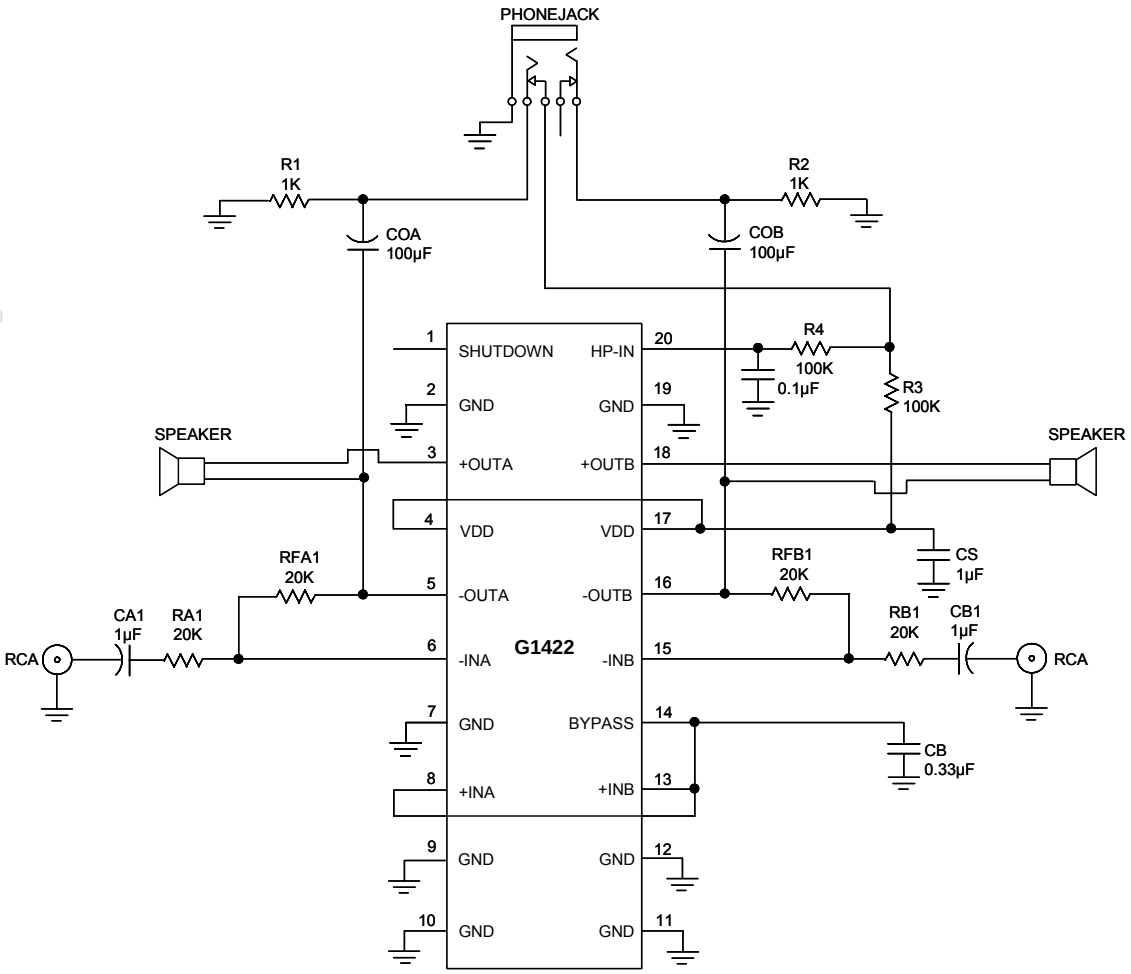
BTL Mode Test Circuit

Parameter Measurement Information (Continued)



SE Mode Test Circuit

Application Circuits



Logical Truth Table

INPUTS		AMPLIFIER STATES		
HP-IN	Shutdown	A/B Out-	A/B Out+	Mode
X	High	----	----	Mute
Low	Low	BTL Output	BTL Output	BTL
Low	Low	BTL Output	BTL Output	BTL
High	Low	SE Output	----	SE
High	Low	SE Output	----	SE

Application Information

Single Ended Mode Operation

The G1422 can drive clean, low distortion SE output power into headphone loads (generally 16Ω or 32Ω) as in Figure A. Please refer to **Electrical Characteristics** to see the performances. A coupling capacitor is needed to block the dc offset voltage, allowing pure ac signals into headphone loads. Choosing the coupling capacitor will also determine the 3 dB point of the high-pass filter network, as Figure B.

$$f_C = 1/(2\pi R_L C_C)$$

For example, a 68uF capacitor with 32Ω headphone load would attenuate low frequency performance below 73Hz. So the coupling capacitor should be well chosen to achieve the excellent bass performance when in SE mode operation.

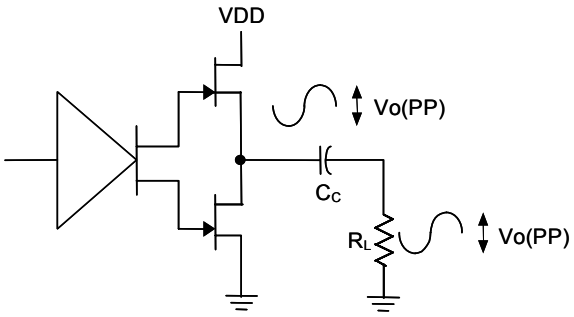


Figure A

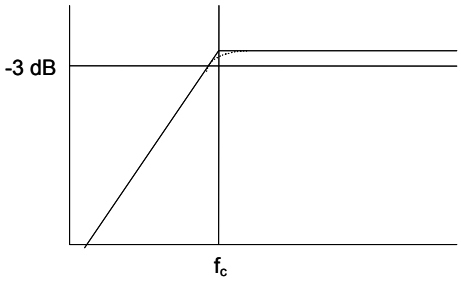


Figure B

Bridged-Tied Load Mode Operation

The G1422 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure C shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage V_O(PP) on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc offsets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.

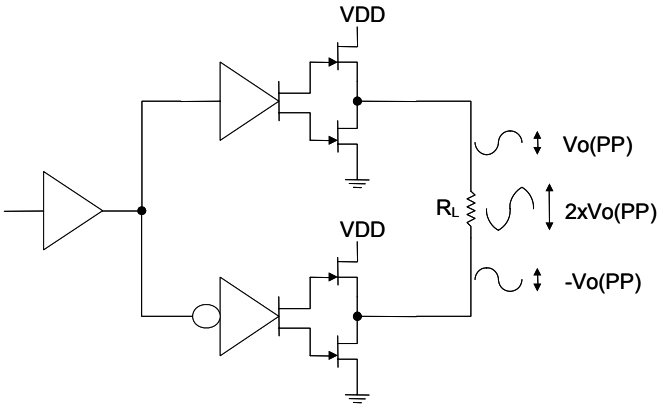


Figure C

SHUTDOWN Mode Operations

The G1422 implements the shutdown mode operations to reduce supply current, $I_{DD,}$ to the absolute minimum level during nonuse periods for battery-power conservation. When the shutdown pin (pin 1) is pulled high, all linear amplifiers will be deactivated to mute the amplifier outputs. And The G1422 enters an extra low current consumption state, I_{DD} is smaller than 2μA. Shutdown pin should never be left unconnected, this floating condition will cause the amplifier operations unpredictable.

Optimizing DEPOP Operation

Circuitry has been implemented in the G1422 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B x 100k\Omega) \leqq 1/(C_I*(R_I+R_F))$. Where 100kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

De-popping circuitry of theG1422 is shown on Figure D. The PNP transistor limits the voltage drop across the 225kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

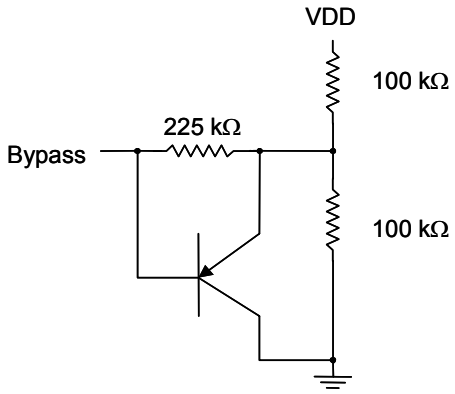
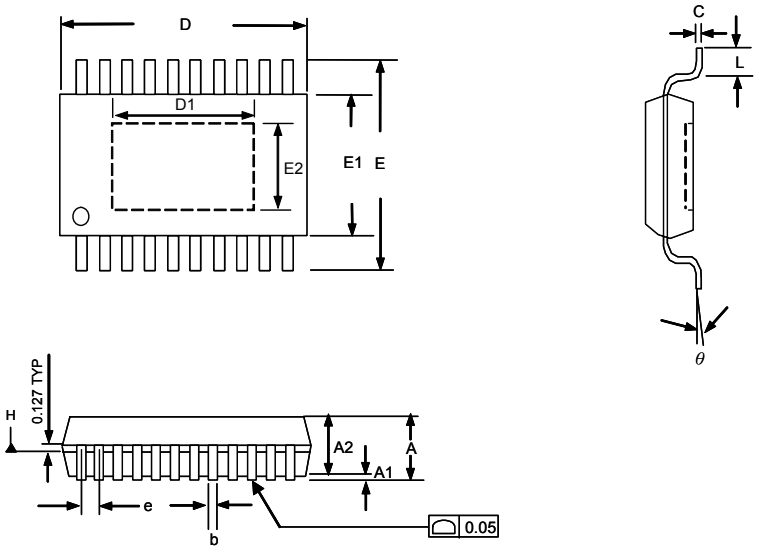


Figure D

Package Information



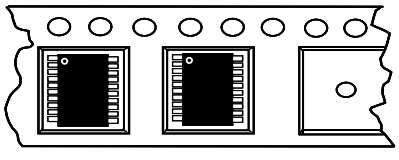
TSSOP-20 (FD) Package

Note:

1. JEDCE outline: MP-153 AC/MO-153 ACT (thermally enhanced variations only)
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
3. Dimension “E1” does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the “b” dimension at maximum material conditions. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimensions “D” and “E1” to be determined at datum plane “H”.

SYMBOLS	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-----	-----	1.20	-----	-----	0.047
A1	0.00	-----	0.15	0.000	-----	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.20	-----	-----	0.008	-----	-----
D	6.40	6.50	6.60	0.252	0.256	0.260
D1	3.90	-----	4.40	0.154	-----	0.173
E	6.40 BSC			0.252 BSC		
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.70	-----	3.20	0.106	-----	0.126
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	-----	8°	0°	-----	8°

Taping Specification



Feed Direction
Typical TSSOP Package Orientation

PACKAGE	Q’TY/BY REEL
TSSOP-20 (FD)	2,500 ea