G1427

Global Mixed-mode Technology Inc.

2W Stereo Audio Amplifier
6dB\10dB\15.6dB\21.6dB Selectable Gain Settings

Features

- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **Depop Circuitry Integrated**
- **Output Power at 1% THD+N, VDD=5V**
  --2.0W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Bridge-Tied Load (BTL), Single-Ended (SE)**
- **Stereo Input MUX**
- **PC-Beep Input**
- **Fully differential Input**
- **Shutdown Control Available**
- **Surface-Mount Power Package**
  24-Pin TSSOP-P

Applications

- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

General Description

G1427 is a stereo audio power amplifier in 24pin TSSOP thermal pad package. It can drive 2.0W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage. Its THD is smaller than 1% under the above operation condition. To simplify the audio system design in the notebook application, G1427 supports the Bridge-Tied Load (BTL) mode for driving the speakers, Single-End (SE) mode for driving the headphone. For the low current consumption applications, the SHDN mode is supported to disable G1427 when it is idle. The current consumption can be reduced to 160µA (typically).
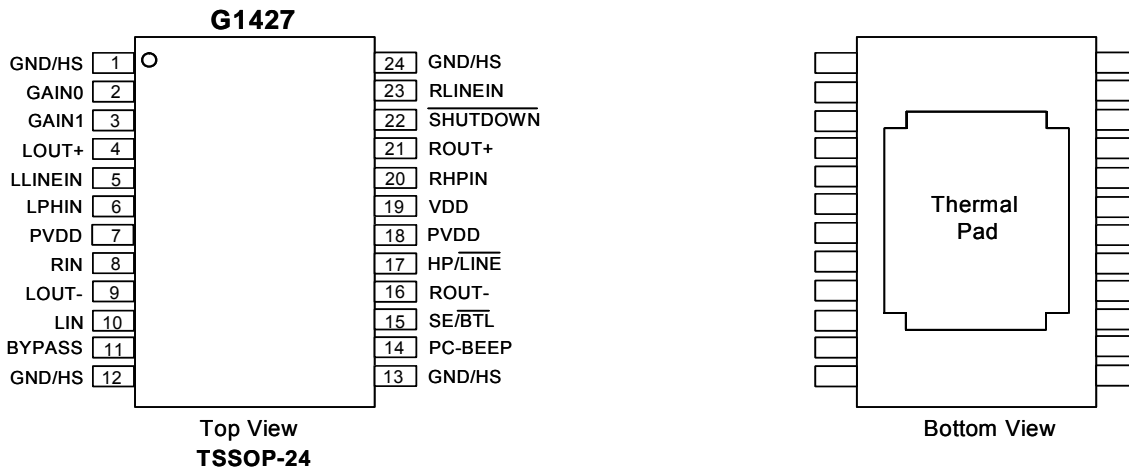
Amplifier gain is internally configured and controlled by two terminals (GAIN0, GAIN1). BTL gain settings of 6dB, 10dB, 15.6dB, 21.6dB are provided, while SE gain is always configured as 4.1dB (inverting) for headphone driving. G1427 also supports two input paths, that means two different amplitude AC signals can be applied and chosen by setting HP/$\overline{\text{LINE}}$ pin. It enhances the hardware designing flexibility.

Ordering Information

ORDER NUMBER	ORDER NUMBER (Pb free)	TEMP. RANGE	PACKAGE
G1427F31U	G1427F31Uf	-40°C to +85°C	TSSOP-24 (FD)

Note: U:Tape & Reel
(FD): Thermal Pad

Pin Configuration

G1427

GND/HS	1	24	GND/HS
GAIN0	2	23	RLINEIN
GAIN1	3	22	$\overline{\text{SHUTDOWN}}$
LOUT+	4	21	ROUT+
LLINEIN	5	20	RHPIN
LPHIN	6	19	VDD
PVDD	7	18	PVDD
RIN	8	17	HP/$\overline{\text{LINE}}$
LOUT-	9	16	ROUT-
LIN	10	15	SE/$\overline{\text{BTL}}$
BYPASS	11	14	PC-BEEP
GND/HS	12	13	GND/HS

Top View
TSSOP-24

Thermal Pad

Bottom View

Absolute Maximum Ratings

Supply Voltage, V_{CC}…………………...….…….……..6V

Operating Ambient Temperature Range

T_A…….…………………..……………….-40°C to +85°C

Maximum Junction Temperature, T_J…...…….……150°C

Storage Temperature Range, T_{STG}…....-65°C to+150°C

Reflow Temperature (soldering, 10sec)……...……260°C

Power Dissipation [1]

   $T_A \leq$ 25°C ………...……………………………..2.7W

   $T_A \leq$ 70°C ………...……………………………..1.7W

Electrostatic Discharge, V_{ESD}

Human body mode..……………………….…………3000[2]

Note:

[1] : Recommended PCB Layout

[2] : Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, T_A=+25°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Supply voltage VDD	V_{DD}			4.5	5	5.5	V
High-Level Input voltage, V_{IH}	V_{IH}	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, GAIN0, GAIN1		2	---	---	V
Low-Level Input voltage, V_{IL}	V_{IL}	SE/$\overline{BTL}$, HP/$\overline{LINE}$, $\overline{SHUTDOWN}$, GAIN0, GAIN1		---	---	0.8	V
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2		---	5	50	mV
Supply Current in Mute Mode	I_{DD}	V_{DD} = 5V	Stereo BTL	---	7.5	13	mA
			Stereo SE		4	7	
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V		---	160	300	µA

(AC Operation Characteristics, V_{DD} = 5.0V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω G=-2V/V	---	2	---	W
		THD = 1%, BTL, R_L = 8Ω G=-2V/V	---	1.25	---	
		THD = 10%, BTL, R_L = 4Ω G=-2V/V	---	2.5	---	
		THD = 10%, BTL, R_L = 8Ω G=-2V/V	---	1.6	---	
		THD = 0.1%, SE, R_L = 32Ω	---	85	---	mW
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω G=-2V/V	---	100	---	m%
		P_O = 1W, BTL, R_L = 8Ω G=-2V/V	---	60	---	
		P_O = 75mW, SE, R_L = 32Ω	---	80	---	
		V_I = 1V, RL = 10KΩ, SE	---	30	---	
Maximum output power bandwidth	B_{OM}	THD = 5%	---	>15	---	kHz
Power supply ripple rejection	PSRR	F=1kHz, BTL mode G=-2V/V C_{BYP}=1µF	---	68	---	dB
Channel-to-channel output separation		f = 1kHz	---	80	---	dB
Line/HP input separation			---	80	---	dB
BTL attenuation in SE mode			---	85	---	dB
Input impedance	ZI		See Table 2			MΩ
Signal-to-noise ratio		P_O = 500mW, BTL, G=-2V/V	---	90	---	dB
Output noise voltage	V_n	BTL, G=-2V/V, A Weighted filter	---	45	---	µV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

Typical Characteristics
Table of Graphs

			FIGURE
THD +N Total Harmonic Distortion Plus Noise		vs Frequency	1,2,7,8,13,14,19,21
		vs Output Power	3,4,5,6,9,10,11,12,15,16,17,18,20
		vs Output Voltage	22
V_n	Output Noise Voltage	vs Frequency	27
	Supply Ripple Rejection Ratio	vs Frequency	23,24
	Crosstalk	vs Frequency	25,26
P_O	Output Power	vs Load Resistance	28,29
P_D	Power Dissipation	vs Output Power	30,31

Total Harmonic Distortion Plus Noise vs Output Frequency
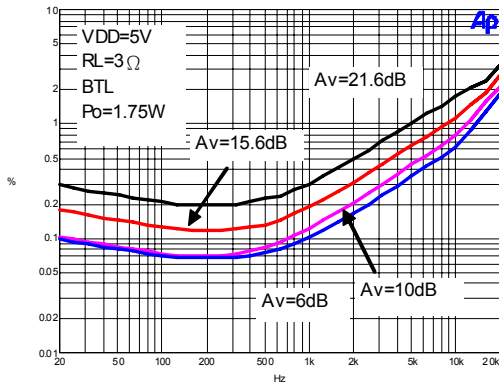
Figure 1

Total Harmonic Distortion Plus Noise vs Output Frequency
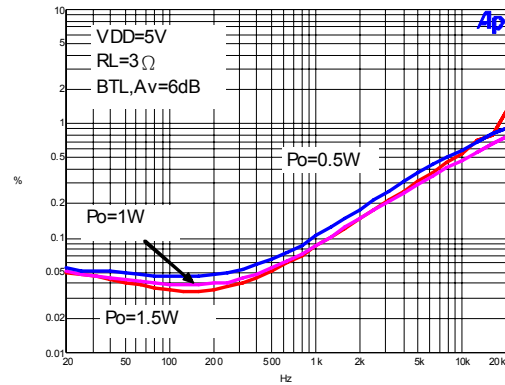
Figure 2

Total Harmonic Distortion Plus Noise vs Output Power
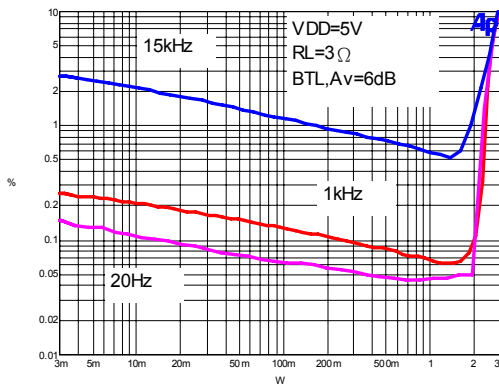
Figure 3

Total Harmonic Distortion Plus Noise vs Output Power
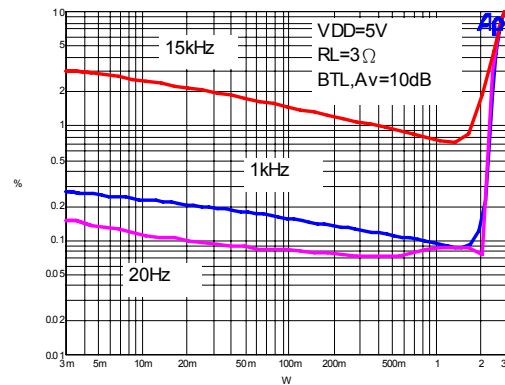
Figure 4

**Total Harmonic Distortion Plus
Noise vs Output Power**
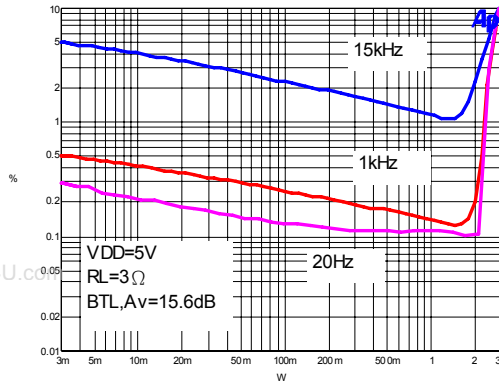
Figure 5

**Total Harmonic Distortion Plus
Noise vs Output Power**
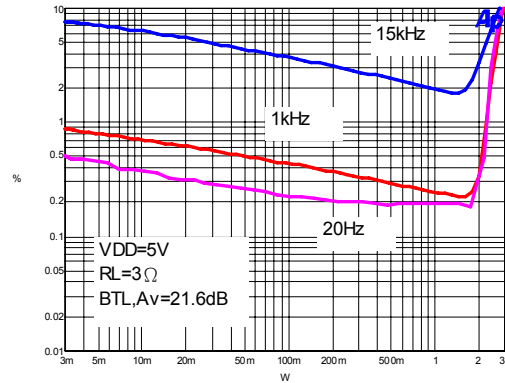
Figure 6

**Total Harmonic Distortion Plus
Noise vs Frequency**
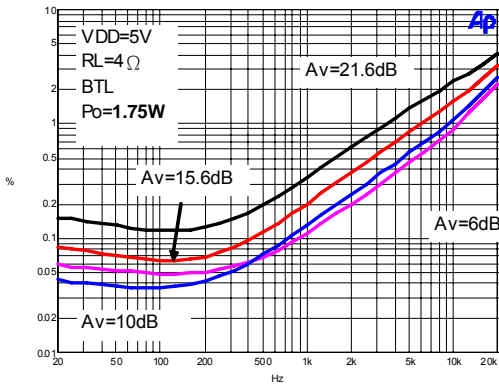
Figure 7

**Total Harmonic Distortion Plus
Noise vs Frequency**
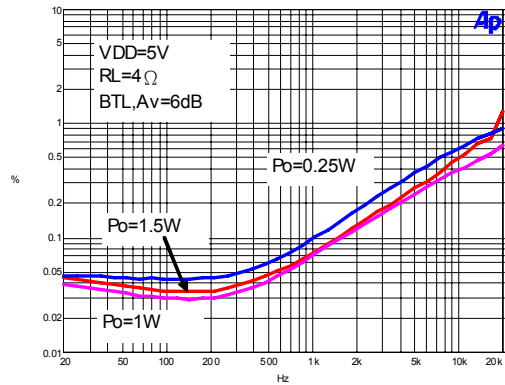
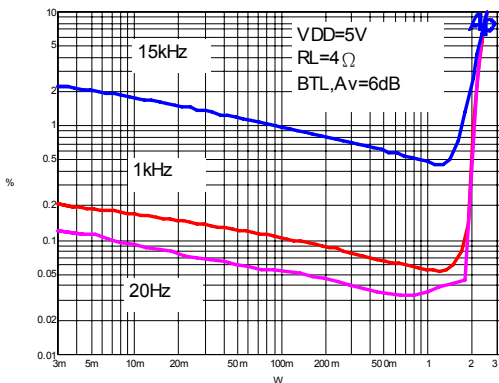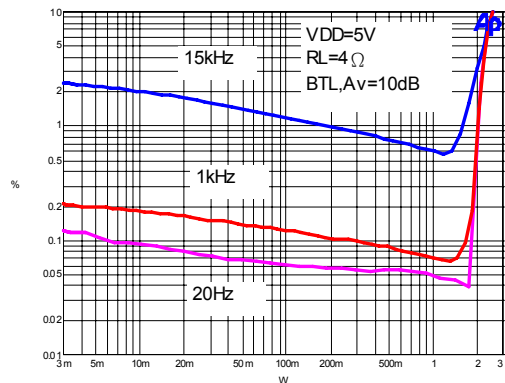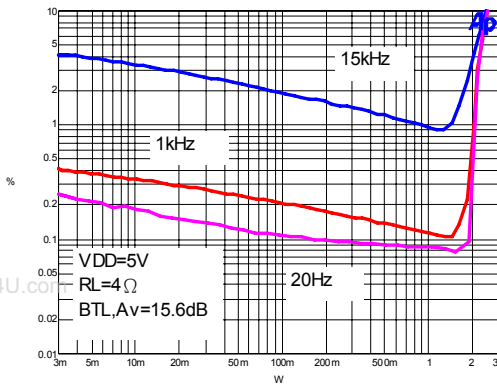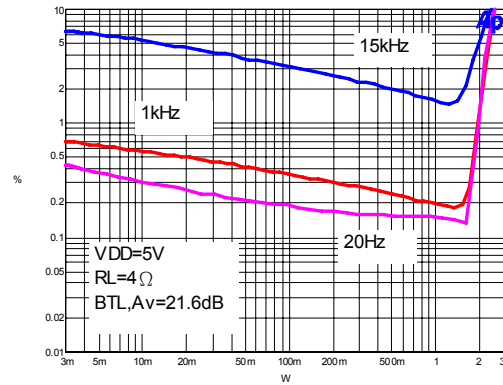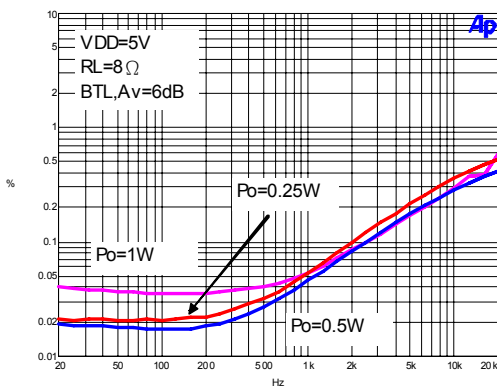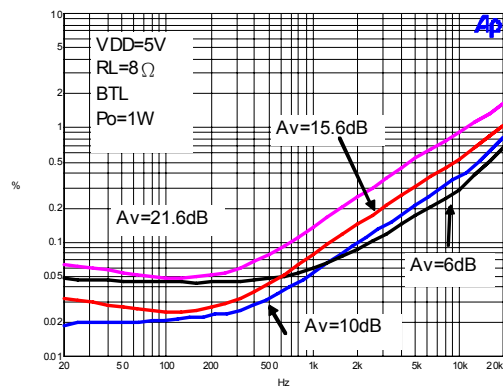

Figure 8

**Total Harmonic Distortion Plus
Noise vs Output Power**

Figure 9

**Total Harmonic Distortion Plus
Noise vs Output Power**

Figure 10

**Total Harmonic Distortion Plus
Noise vs Output Power**

Figure 11

**Total Harmonic Distortion Plus
Noise vs Output Power**

Figure 12

**Total Harmonic Distortion Plus
Noise vs Frequency**

Figure 13

**Total Harmonic Distortion Plus
Noise vs Frequency**

Figure 14

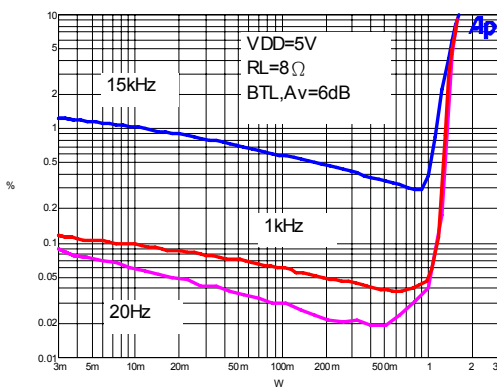**Total Harmonic Distortion Plus
Noise vs Output Power**

Figure 15

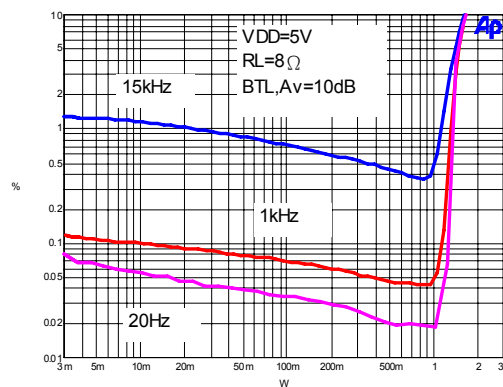**Total Harmonic Distortion Plus
Noise vs Output Power**

Figure 16

**Total Harmonic Distortion Plus
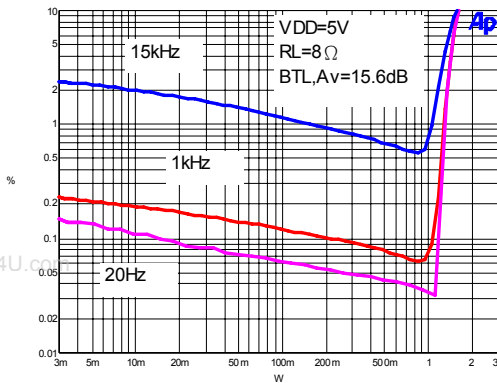Noise vs Output Power**

Figure 17

**Total Harmonic Distortion Plus
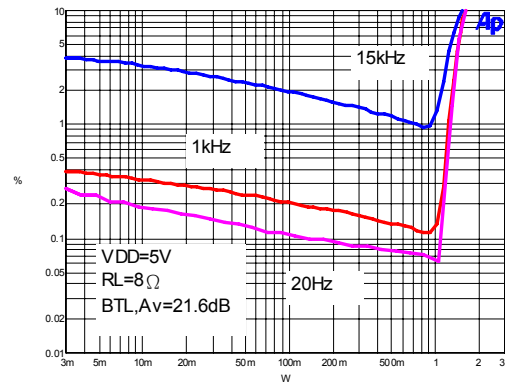Noise vs Output Power**

Figure 18

**Total Harmonic Distortion Plus
Noise vs Frequency**
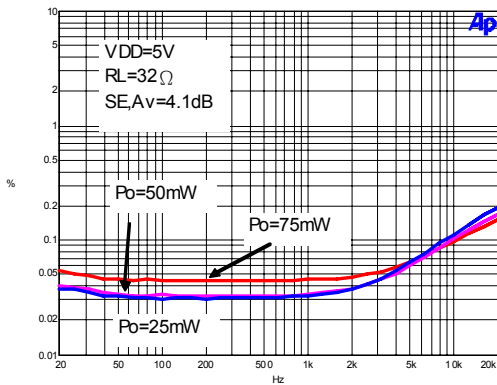

Figure 19

**Total Harmonic Distortion Plus
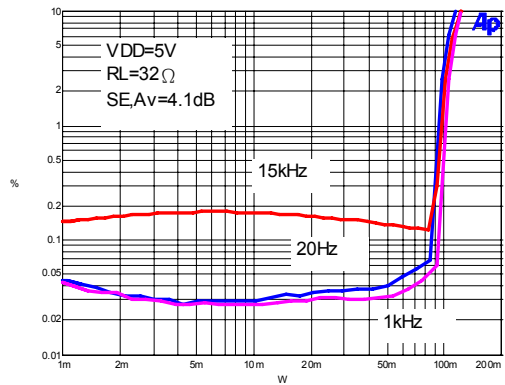Noise vs Output Power**

Figure 20
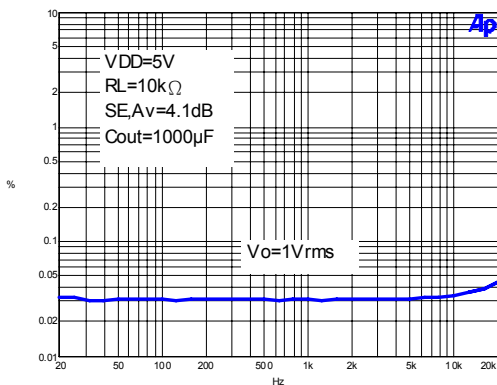
**Total Harmonic Distortion Plus
Noise vs Frequency**
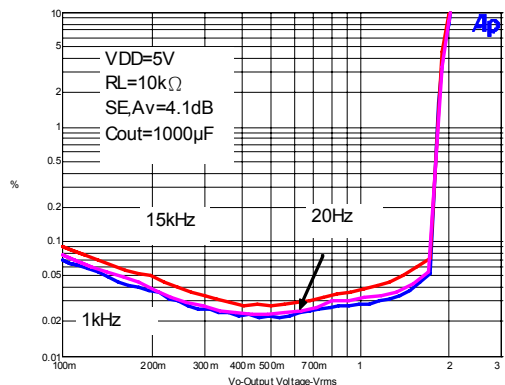

Figure 21

**Total Harmonic Distortion Plus
Noise vs Output Voltage**

Figure 22

6

Supply Ripple Rejection Ratio vs Frequency

VDD=5V
RL=8Ω
Cb=1µF
BTL

Av=21.6dB

Av=6dB
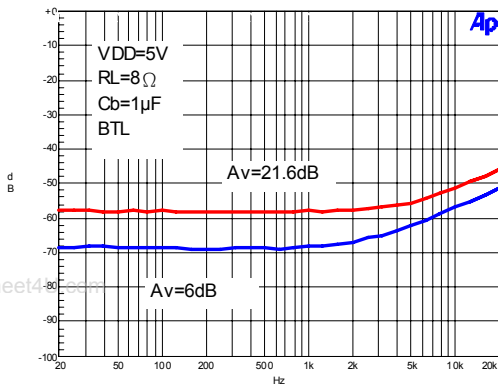
Figure 23

Supply Ripple Rejection Ratio vs Frequency

VDD=5V
RL=8Ω
Cb=1µF
SE
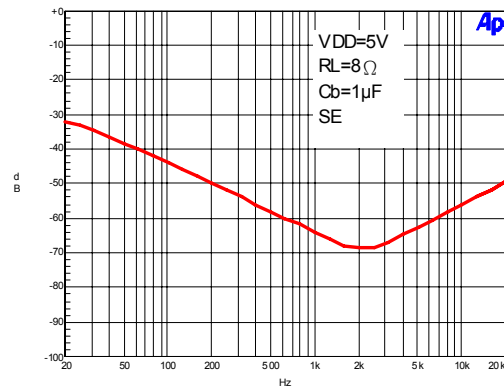
Figure 24

Channel Separation

VDD=5V
Po=1W
RL=8Ω
BTL,Av=6dB

L TO R

R TO L
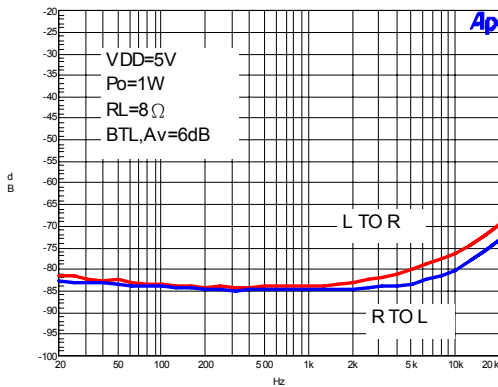
Figure 25

Channel Separation

VDD=5V
Po=1W
RL=8Ω
SE,Av=4.1dB

L TO R

R TO L
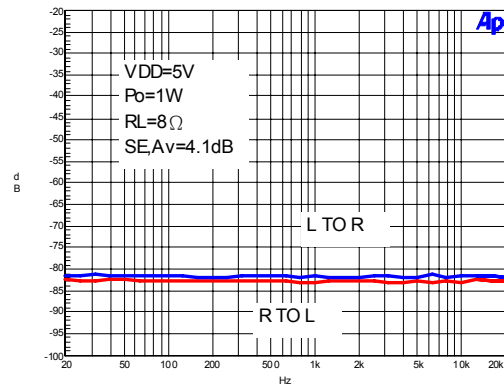
Figure 26

Output Noise vs Frequency

VDD=5V
RL=4Ω
BTL,Av=6dB
A-Weighted filter
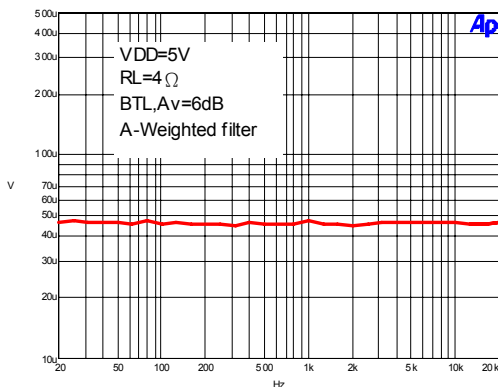
Figure 27

Output Power vs Load Resistance

VDD=5V
THD+N=1%
BTL
Each Channel
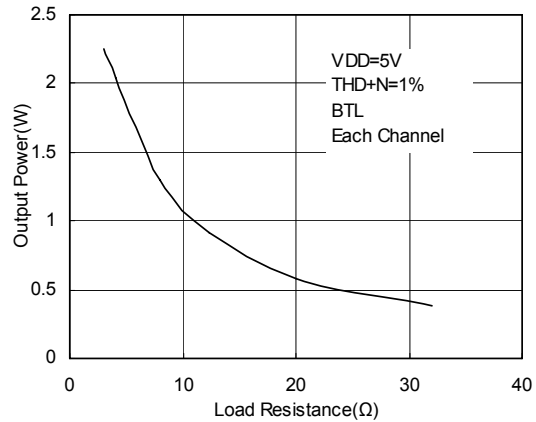
Figure 28

Output Power vs Load Resistance

VDD=5V
THD+N=1%
SE
Each Channel
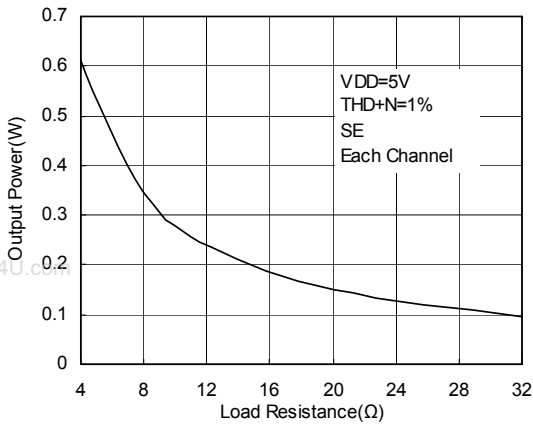
Figure 29

Power Dissipation vs Output Power

RL=3Ω

RL=4Ω

VDD=5V
BTL
Each Channel

RL=8Ω
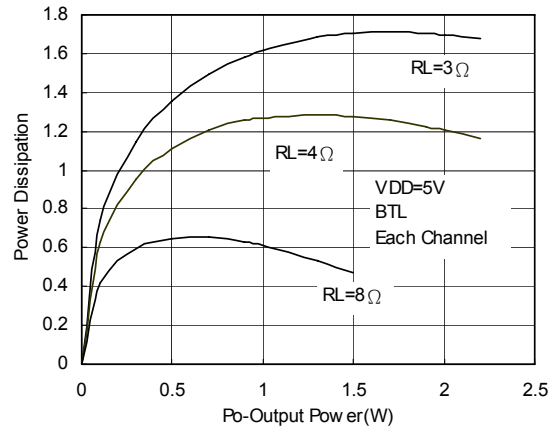
Figure 30

Power Dissipation vs Output Power

RL=4Ω

VDD=5V
SE
Each Channel

RL=8Ω

RL=32Ω
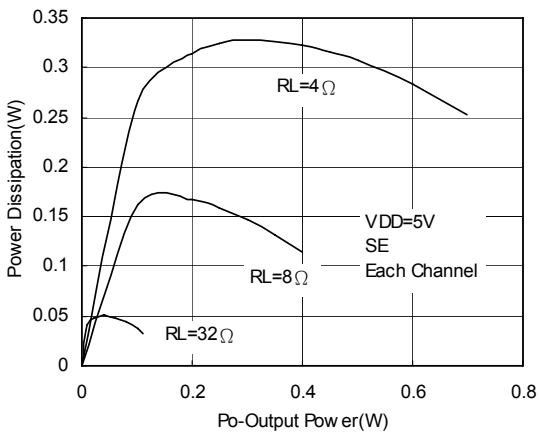
Figure 31

Recommend PCB Footprint

3.9mm

0.37mm

TS8OP-P 24

2 mm

8.1 mm
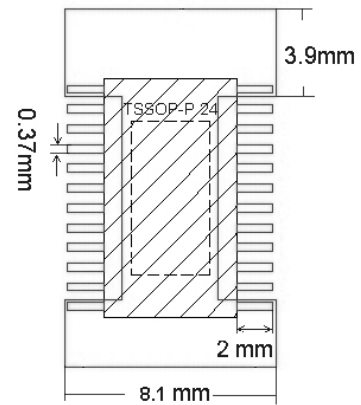
Pin Description

| PIN	NAME	I/O	FUNCTION
1,12,13,24	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
2	GAIN0	I	Bit 0 of gain control
3	GAIN1	I	Bit 1 of gain control
4	LOUT+	O	Left channel + output in BTL mode, + output in SE mode.
5	LLINEIN	I	Left channel line input, selected when HP/$\overline{\text{LINE}}$ pin is held low.
6	LPHIN	I	Left channel headphone input, selected when HP/$\overline{\text{LINE}}$ pin is held high.
7,18	PVDD	I	Power supply for output stages.
8	RIN	I	Common right input for fully differential inputs. AC ground for single-ended inputs.
9	LOUT-	O	Left channel - output in BTL mode, and high impedance in SE mode.
10	LIN	I	Common left input for fully differential inputs. AC ground for single-ended inputs.
11	BYPASS		Tap to voltage divider for internal mid-supply bias generator.
14	PC-BEEP	I	The input for PC-BEEP mode. PC-BEEP is enabled when at least eight continuous > 1-V_{PP} (peak to peak) square waves is input to PC-BEEP pin.
15	SE/$\overline{\text{BTL}}$	I	Hold low for BTL mode, hold high for SE mode.
16	ROUT-	O	Right channel - output in BTL mode, high impedance state in SE mode.
17	HP/$\overline{\text{LINE}}$	I	MUX control input, hold high to select headphone inputs (6,20), hold low to select line inputs (5,23).
19	VDD		Analog VDD input supply. This terminal needs to be isolated from PVDD to achieve highest performance.
20	RHPIN	I	Right channel headphone input, selected when HP/$\overline{\text{LINE}}$ pin is held high.
21	ROUT+	O	Right channel + output in BTL mode, positive output in SE mode.
22	$\overline{\text{SHUTDOWN}}$	I	Places entire IC in shutdown mode when held low, expect PC-BEEP remains active.
23	RLINEIN	I	Right channel line input, selected when HP/$\overline{\text{LINE}}$ pin is held low.
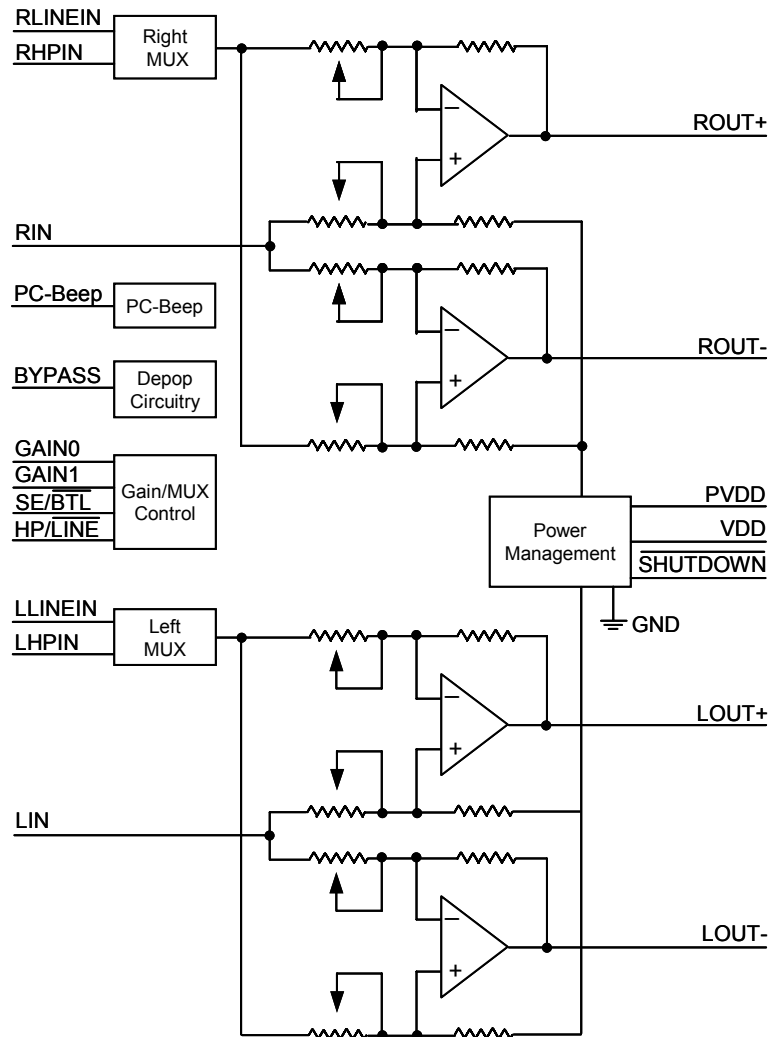
Block Diagram
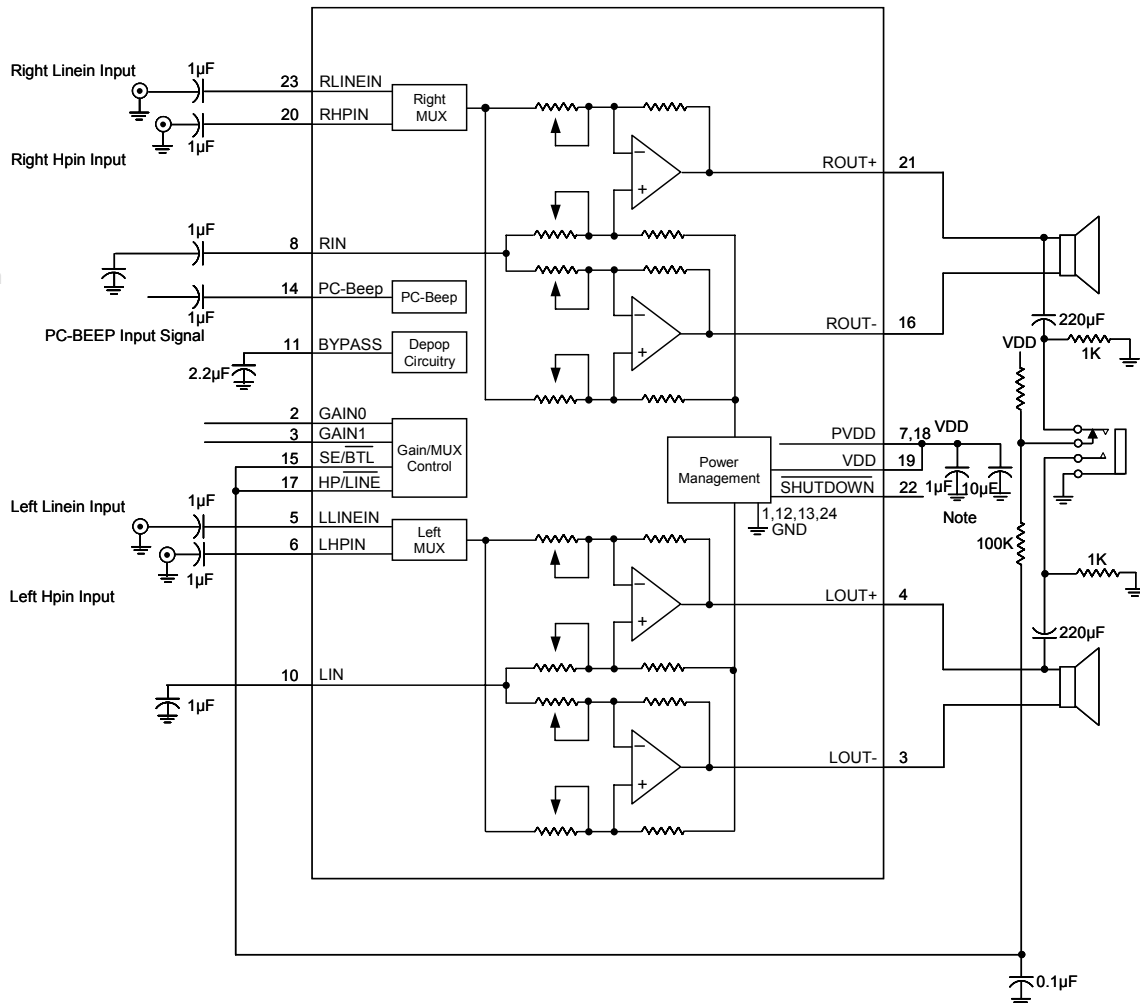
Application Circuit
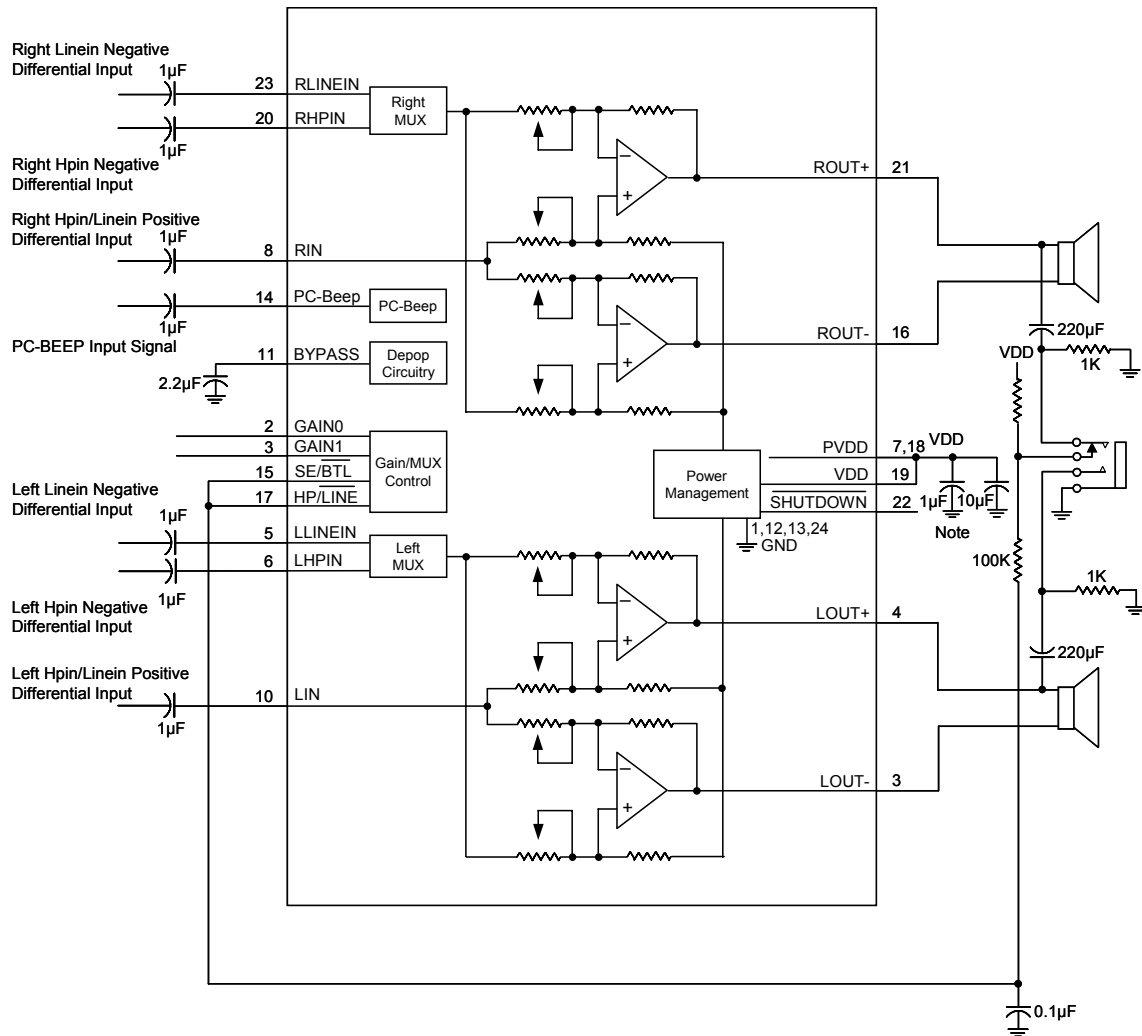
Application Circuit Using Differential Inputs

Note: 1µF ceramic capacitor should be placed as close as possible to the IC to filter the higher-frequency noise.

Application Circuit (continued)

Application Circuit Using Single-Ended Inputs

Note: 1µF ceramic capacitor should be placed as close as possible to the IC to filter the higher-frequency noise.

Application Information
Gain setting via GAIN0 and GAIN1 inputs
The internal gain setting is determined by two input terminals, GAIN0 and GAIN1. The gains listed in Table 1 are realized by changing the taps on the input resistors inside the amplifier. This will cause the internal input impedance, Z_I, to be dependent on the gain setting. Although the real input impedance will shift by 30% due to process variation from part-to-part, the actual gain settings are controlled by the ratios of the resistors and the actual gain distribution from part-to-part is quite good.

Table 1

GAIN0	GAIN1	$\overline{\text{SE}/\text{BTL}}$	A_V (dB)
0	0	0	6
0	1	0	10
1	0	0	15.6
1	1	0	21.6
X	X	1	4.1

Input Resistance
The typical input impedance at each gain setting is given in the Table 2. Each gain setting is achieved by varying the input resistance of the amplifier, which can be over 3 times from its minimum value to the maximum value. As a result, if a single capacitor is used in the input high pass filter, the -3dB or cut-off frequency will be also change over 3 times. To reduce the variation of the cut-off frequency, an additional resistor can be connected from the input pin of the amplifier to the ground, as shown in Figure 1. With the extra resistor, the cut-off frequency can be re-calculated using equation : $f_{-3dB} = 1/2\pi C(R\|R_I)$. Using small external R can reduce the variation of the cut-off frequency. But the side effect is small external R will also let $(R\|R_I)$ become small, the cut-off frequency will be larger and degraded the bass-band performance. The other side effect is with extra power dissipation through the external resistor R to the ground. So using the external resistor R to flatting the variation of the cut-off frequency, the user must also consider the bass-band performance and the extra power dissipation to choose the accepted external resistor R value.
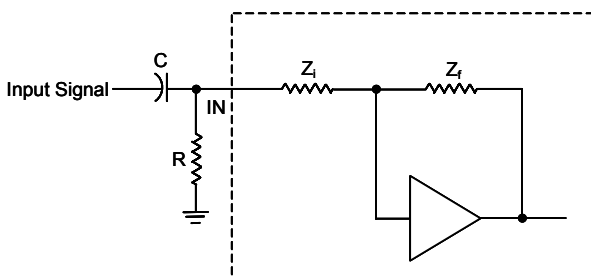

Figure 1

Table 2

Zi (Kohm)	A_V (dB)
30	21.6
45	15.6
70	10
90	6

Input Capacitor
In the typical application, an input capacitor C_i is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case ,C_i and the input impedance of the amplifier, Z_i, form a high-pass filter with the -3dB determined by the equation: $f_{-3dB} = 1/(2\pi R_I C_i)$

The value of C_i is important to consider as it directly affects the bass performance of the application circuit. For example, if the input resistor is 15kΩ, the input capacitor is 1µF, the flat bass response will be down to 10.6Hz.

Because the small leakage current of the input capacitors will cause the dc offset voltage at the input to the amplifier that reduces the operation headroom, especially at the high gain applications. The low-leakage tantalum or ceramic capacitors are suggested to be used as the input coupling capacitors. When using the polarized capacitors, it is important to let the positive side connecting to the higher dc level of the application.

Power Supply Decoupling
The G1427 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to make sure the output total harmonic distortion (THD) as low as possible. The optimum decoupling is using two capacitors with different types that target different types of noise on the power supply leads. For high frequency transients, spikes, a good low ESR ceramic capacitor works best, typically 0.1µF/1µF used and placed as close as possible to the G1427 VDD lead. A larger aluminum electrolytic capacitor of 10µF or greater placed near the device power is recommended for filtering low-frequency noise.

Optimizing DEPOP Operation
Circuitry has been implemented in G1427 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B \times 170k\Omega) \leq 1/(C_I*(R_I+R_F))$.

Where 170kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

De-popping circuitry of G1427 is shown as below Figure 2. The PNP transistor limits the voltage drop across the 120kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

For better performance, C_B is recommended to be at least 1.5 times of input coupling capacitor C_I. For example, if using 1µF input coupling capacitor, 2.2µF ceramic or tantalum low-ESR capacitors are recommended to achieve the better THD performance.
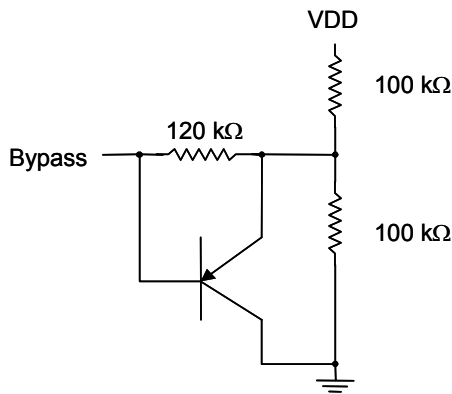
Output coupling capacitor

G1427 can drive clean, low distortion SE output power with gain –1V/V into headphone loads (generally 16Ω or 32Ω) as in Figure 3. Please refer to **Electrical Characteristics** to see the performances. A coupling capacitor is needed to block the dc-offset voltage, allowing pure ac signals into headphone loads. Choosing the coupling capacitor will also determine the -3dB point of the high-pass filter network, as Figure 4.

$$f_C = 1/(2\pi R_L C_C)$$

For example, a 220µF capacitor with 32Ω headphone load would attenuate low frequency performance below 22.6Hz. So the coupling capacitor should be well chosen to achieve the excellent bass performance when in SE mode operation.
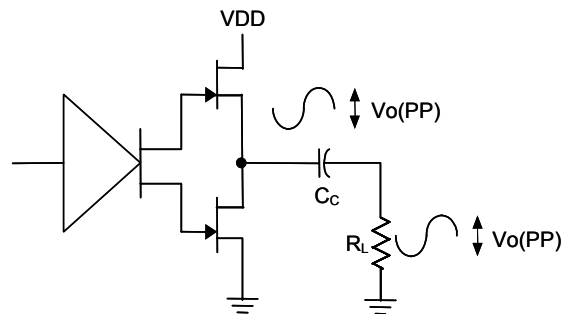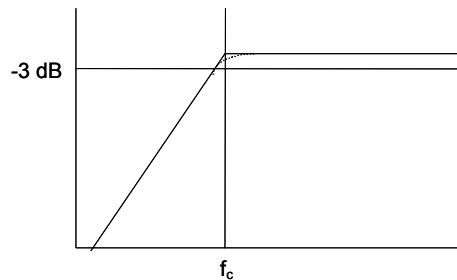
Figure 3

Figure 2

Figure 4

Bridged-Tied Load Mode Operation

G1427 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure 5 shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage $V_O(PP)$ on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc off-sets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.
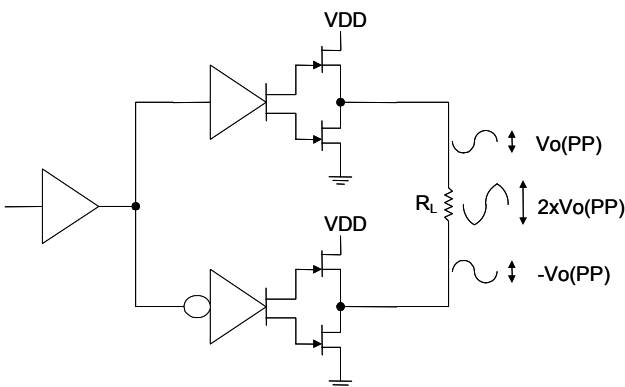
Input MUX And SE/$\overline{\text{BTL}}$ Operation

Figure 5

The G1427 allows two different input sources applied to the audio amplifiers, which can be independent to the SE/$\overline{\text{BTL}}$ setting. When HP/$\overline{\text{LINE}}$ is held high, the headphone inputs are active. When the HP/$\overline{\text{LINE}}$ is held low, the line inputs are selected.

When SE/$\overline{\text{BTL}}$ is held low, all four internal audio amplifiers are activated to drive the stereo speakers.

When SE/$\overline{\text{BTL}}$ is held high, two amplifiers are activated to drive the stereo headphones. The other two amplifiers are disable and keeping the outputs high impedance.

Shutdown mode

When the normal operation, the $\overline{\text{SHUTDOWN}}$ pin should be held high. Pulling $\overline{\text{SHUTDOWN}}$ low will mute the outputs and deactivate almost circuits except PC-BEEP monitoring block. At this moment, the current of this device will be reduced to about 160µA to save the battery energy. The $\overline{\text{SHUTDOWN}}$ pin should never be left unconnected during the normal applications.

INPUT *			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	head-phone	BTL
High	High	High	head-phone	SE

* Inputs should never be left unconnected

X= do not care

PC-BEEP Operation

The PC-BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with a few external components. It is activated automatically by detecting the PC-BEEP input. The preferred input signal is a square wave or pulse train with an amplitude of 1-V_{PP} or greater. To be accurately detected, the signal must be with at least 1-V_{PP} amplitude, 8 continuous rising edges, rise and fall times less than 0.1µs. When the signal is no longer detected, the amplifier will return its previous operating mode and volume setting.

When the PC-BEEP mode is activated, both the LINEIN and HPIN are deselected and the outputs will be driven in BTL mode with the signal from PC-BEEP. The gain setting will be also fixed at 0.3V/V, independent of the volume setting. If the device is in the SHUTDOWN mode, activating PC-BEEP will take the device out of shutdown mode and output the PC-BEEP input signal until the PC-BEEP signal no longer detected. And then the device will return the shutdown mode when no PC-BEEP signal is detected.
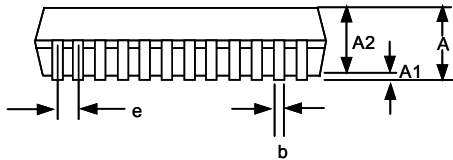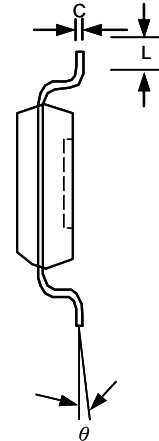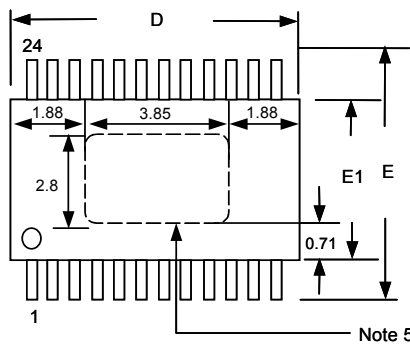
The PC-BEEP input can be dc-coupled to save the coupling capacitor. This pin is set at mid-rail normally when no signal is present.

If AC-coupling is desired, the value of the coupling capacitor should be chosen to satisfy the equation:

$$C_{PCB} \geq 1/(2 \pi f_{PCB}*150K\Omega)$$

C_{PCB} is the PC-BEEP AC-coupling capacitor. f_{PCB} is the frequency of applied PC-BEEP input signal.

Package Information
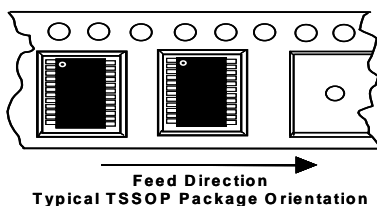

NOTE:
1. Package body sizes exclude mold flash protrusions or gate burrs
2. Tolerance ±0.1mm unless otherwise specified
3. Coplanarity : 0.1mm
4. Controlling dimension is millimeter. Converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Follow JEDEC MO-153

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-----	-----	1.15	-----	-----	0.045
A1	0.00	-----	0.10	0.000	-----	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	-----	0.30	0.007	-----	0.012
C	0.09	-----	0.20	0.004	-----	0.008
D	7.70	7.80	7.90	0.303	0.307	0.311
E	6.20	6.40	6.60	0.244	0.252	2.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-----	0.65	-----	-----	0.026	-----
L	0.45	0.60	0.75	0.018	0.024	0.030
y	-----	-----	0.10	-----	-----	0.004
θ	0°	-----	8°	0°	-----	8°

Taping Specification

Feed Direction
Typical TSSOP Package Orientation

PACKAGE	Q'TY/REEL
TSSOP-24 (FD)	2,500 ea

Ver: 1.3
Sep 23, 2005

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