2W Stereo Audio Amplifier

Features

- **Depop Circuitry Integrated**
- **Output Power at 1% THD+N, VDD=5V**
  --1.8W/CH (typical) into a 4Ω Load
  --1.2W/CH (typical) into a 8Ω Load
- **Bridge-Tied Load (BTL), Single-Ended (SE)**
- **Shutdown Control Available**
- **Dual Inline Package 16 pin (DIP16)**

Applications

- **Stereo Power Amplifiers for Notebooks or Desktop Computers**
- **Multimedia Monitors**
- **Stereo Power Amplifiers for Portable Audio Systems**

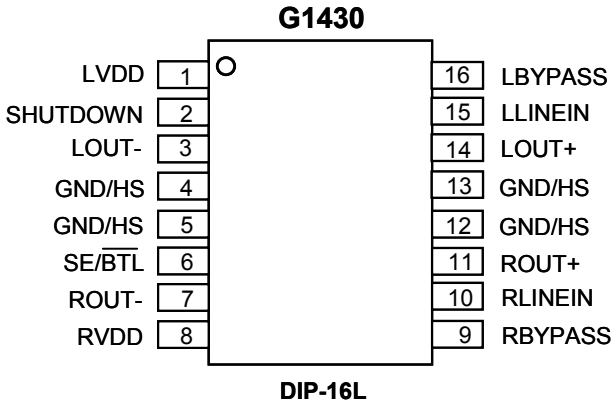
General Description

G1430 is a stereo audio power amplifier in 16pin Dual Inline Package. It can drive 1.8W continuous RMS power into 4Ω load per channel in Bridge-Tied Load (BTL) mode at 5V supply voltage. Its THD is smaller than 1% under the above operation condition. To simplify the audio system design in the notebook application, G1430 supports the Bridge-Tied Load (BTL) mode for driving the speakers, Single-End (SE) mode for driving the headphone. For the low current consumption applications, the SHDN mode is supported to disable G1430 when it is idle. The current consumption can be further reduced to below 5μA.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE
G1430Z4T	G1430	-40°C to +85°C	DIP-16L

Pin Configuration



DIP-16L

Absolute Maximum Ratings

Supply Voltage, V_{CC}.....6V
Operating Ambient Temperature Range
T_A.....-40°C to +85°C
Maximum Junction Temperature, T_J.....150°C
Storage Temperature Range, T_{STG}.....-65°C to+150°C
Soldering Temperature, 10seconds, T_S.....260°C

Power Dissipation (1)
$T_A \leq 25°C$.....2W
Electrostatic Discharge, V_{ESD}
Human body mode.....-3000 to 3000(2)

Note:
(1): Both dual channels could provide 1.8W peak output power at 4 ohm speaker, but continuous output power is limited by package (DIP-16) power dissipation : 2W at Ta=25 degree °C
(2): Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

Electrical Characteristics

DC Electrical Characteristics, T_A=+25°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT
Supply Current	I_{DD}	V_{DD} =3.3V	Stereo BTL	---	7	10	mA
			STEREO SE	---	3.5	6	
		V_{DD} = 5V	Stereo BTL	---	8	13	
			STEREO SE	---	4	6.5	
DC Differential Output Voltage	$V_{O(DIFF)}$	V_{DD} = 5V,Gain = 2		---	5	50	mV
Supply Current in Mute Mode	$I_{DD(MUTE)}$	V_{DD} = 5V	Stereo BTL	---	8	13	mA
			STEREO SE		4	6.5	
I_{DD} in Shutdown	I_{SD}	V_{DD} = 5V		---	2	5	μA

(AC Operation Characteristics, V_{DD} = 5V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω	---	1.8	---	W
		THD = 1%, BTL, R_L = 8Ω	---	1.12	---	
		THD = 10%, BTL, R_L = 4Ω	---	2	---	
		THD = 10%, BTL, R_L = 8Ω	---	1.4	---	
		THD = 1%, SE, R_L = 4Ω	---	500	---	mW
		THD = 1%, SE, R_L = 8Ω	---	320	---	
		THD = 10%, SE, R_L = 4Ω	---	650	---	
		THD = 10%, SE, R_L L = 8Ω	---	400	---	
		THD = 0.5%, SE, R_L = 32Ω	---	90	---	
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω	---	500	---	m%
		P_O = 1W, BTL, R_L = 8Ω	---	150	---	
		P_O = 75mW, SE, R_L = 32Ω	---	20	---	
		V_I = 1V, RL = 10KΩ, G = 1	---	10	---	
Maximum output power bandwidth	B_{OM}	G = 1, THD = 1%	---	20	---	kHz
Phase margin		R_L = 4Ω, Open Load	---	60	---	°
Power supply ripple rejection	PSRR	f = 120Hz	---	75	---	dB
Channel-to-channel output separation		f = 1kHz	---	82	---	dB
BTL attenuation in SE mode			---	85	---	dB
Input impedance	ZI		---	2	---	MΩ
Signal-to-noise ratio		P_O = 500mW, BTL	---	90	---	dB
Output noise voltage	V_n	Output noise voltage	---	55	---	μV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

(AC Operation Characteristics, V_{DD} = 3.3V, T_A=+25°C, R_L = 4Ω, unless otherwise noted)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output power (each channel) see Note	$P_{(OUT)}$	THD = 1%, BTL, R_L = 4Ω	---	0.8	---	W
		THD = 1%, BTL, R_L = 8Ω	---	0.5	---	
		THD = 10%, BTL, R_L = 4Ω	---	1	---	
		THD = 10%, BTL, R_L = 8Ω	---	0.6	---	
		THD = 1%, SE, R_L = 4Ω	---	230	---	mW
		THD = 1%, SE, R_L = 8Ω	---	140	---	
		THD = 10%, SE, R_L = 4Ω	---	290	---	
		THD = 10%, SE, R_L L = 8Ω	---	180	---	
		THD = 0.5%, SE, R_L = 32Ω	---	43	---	
Total harmonic distortion plus noise	THD+N	P_O = 1.6W, BTL, R_L = 4Ω	---	270	---	m%
		P_O = 1W, BTL, R_L = 8Ω	---	100	---	
		P_O = 75mW, SE, R_L = 32Ω	---	20	---	
		V_I = 1V, RL = 10KΩ, G = 1	---	10	---	
Maximum output power bandwidth	B_{OM}	G = 1, THD 1%	---	20	---	kHz
Phase margin		R_L = 4Ω, Open Load	---	60	---	°
Power supply ripple rejection	PSRR	f = 120Hz	---	75	---	dB
Channel-to-channel output separation		f = 1kHz	---	80	---	dB
BTL attenuation in SE mode			---	85	---	dB
Input impedance	ZI		---	2	---	MΩ
Signal-to-noise ratio		P_O = 500mW, BTL	---	90	---	dB
Output noise voltage	V_n	Output noise voltage	---	55	---	μV (rms)

Note :Output power is measured at the output terminals of the IC at 1kHz.

Pin Description

PIN	NAME	I/O	FUNCTION
1	LVDD	I	Supply voltage input for left channel and for primary bias circuits.
2	SHUTDOWN	I	Shutdown mode control signal input, places entire IC in shutdown mode when held high, I_{DD} = 5μA.
3	LOUT-	O	Left channel - output in BTL mode, high impedance state in SE mode.
4,5,12,13	GND/HS		Ground connection for circuitry, directly connected to thermal pad.
6	SE/ $\overline{BTL}$	I	Mode control signal input, hold low for BTL mode, hold high for SE mode.
7	ROUT-	O	Right channel - output in BTL mode, high impedance state in SE mode.
8	RVDD	I	Supply voltage input for right channel.
9	RBYPASS		Connect to voltage divider for right channel internal mid-supply bias.
10	RLINE IN	I	Right channel line input, selected when HP/pin is held low.
11	ROUT+	O	Right channel + output in BTL mode, + output in SE mode.
14	LOUT+	O	Left channel + output in BTL mode, + output in SE mode.
15	LLINE IN	I	Left channel line input, selected when HP/ pin is held low.
16	LBYPASS		Connect to voltage divider for left channel internal mid-supply bias.

Typical Characteristics

Table of Graphs

		FIGURE
THD +N Total harmonic distortion plus noise	vs Frequency	2,4,5,7,8,11,12,14,15,17,18,20,21,23,24,26,27,29,30,32,33
	vs Output power	1,3,6,9,10,13,16,19,22,25,28,31
V_n Output noise voltage	vs Frequency	34,35
Supply ripple rejection ratio	vs Frequency	36,37
Crosstalk	vs Frequency	38,39,40,41
Closed loop response	vs Frequency	42,43,44,45
I_{DD} Supply current	vs supply voltage	46
P_O Output power	vs supply voltage	47,48
	vs Load resistance	49,50
P_D Power dissipation	vs Output power	51,52,53,54

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

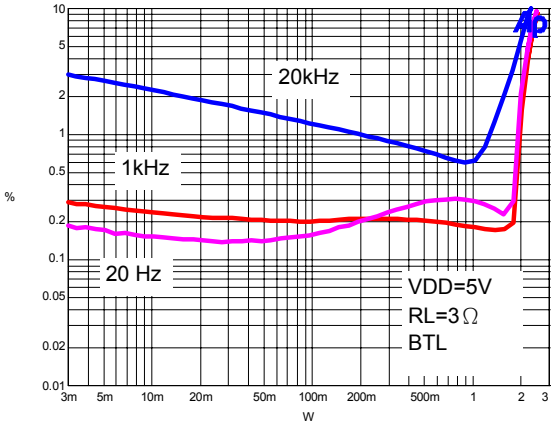


Figure 1

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

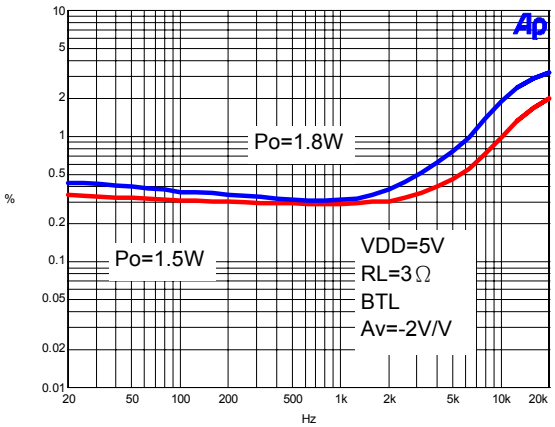


Figure 2

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

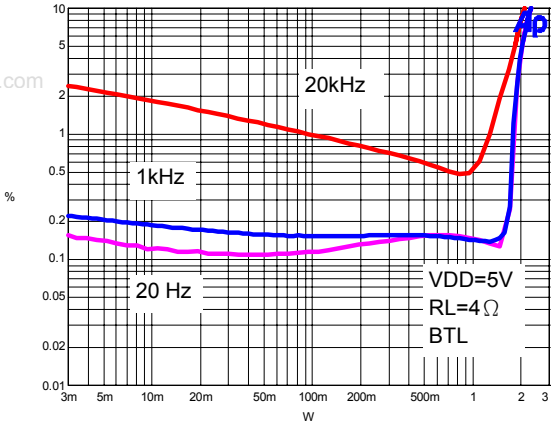


Figure 3

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

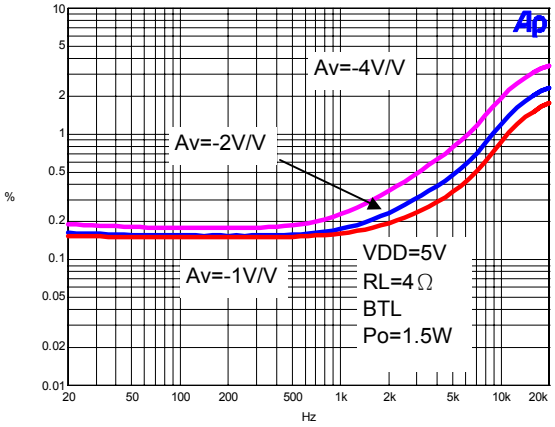


Figure 4

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

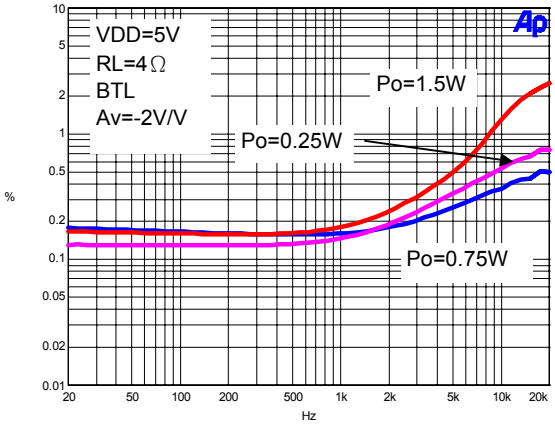


Figure 5

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

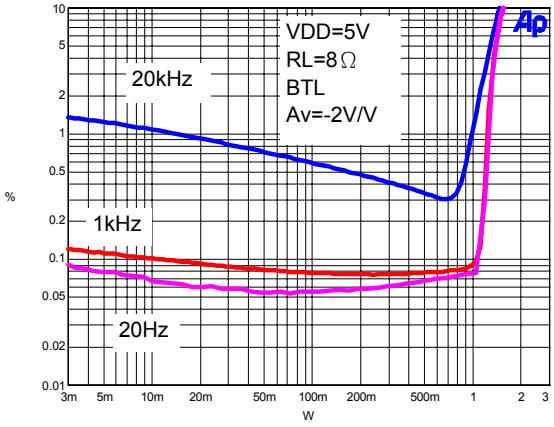


Figure 6

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

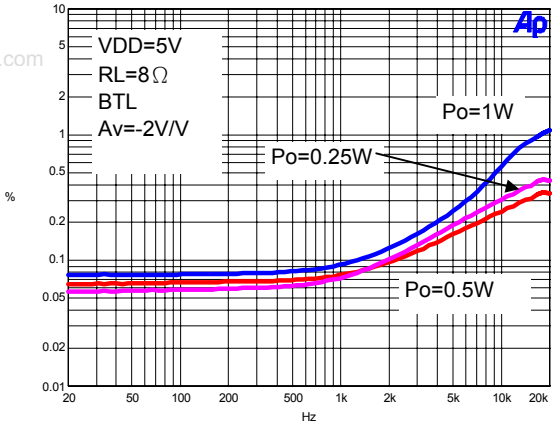


Figure 7

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

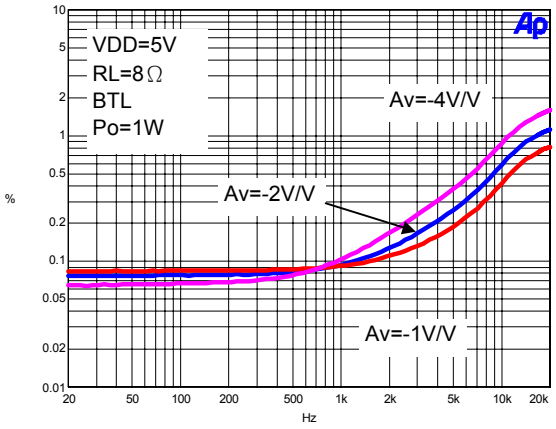


Figure 8

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

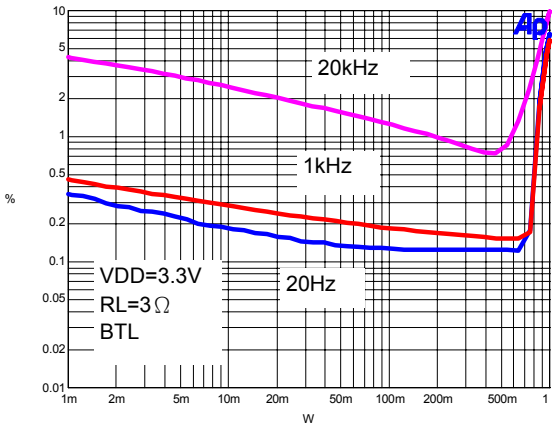


Figure 9

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

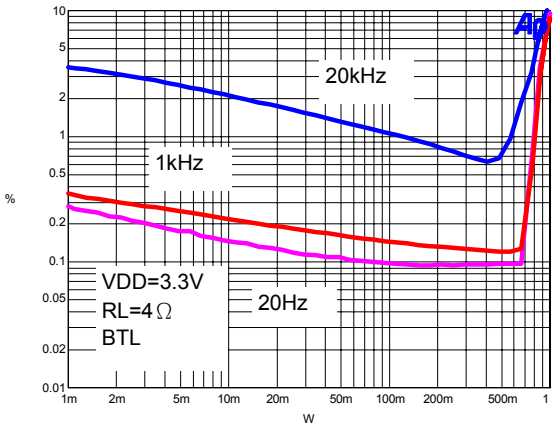


Figure 10

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

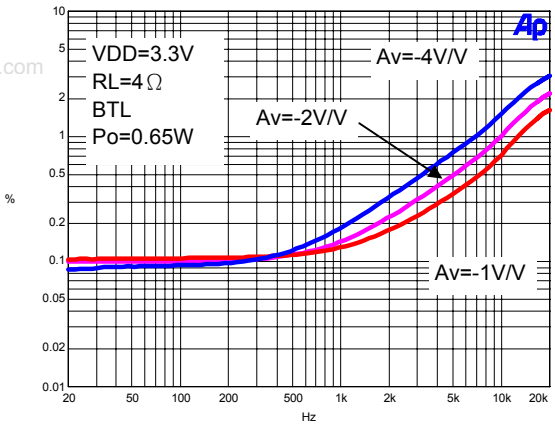


Figure 11

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

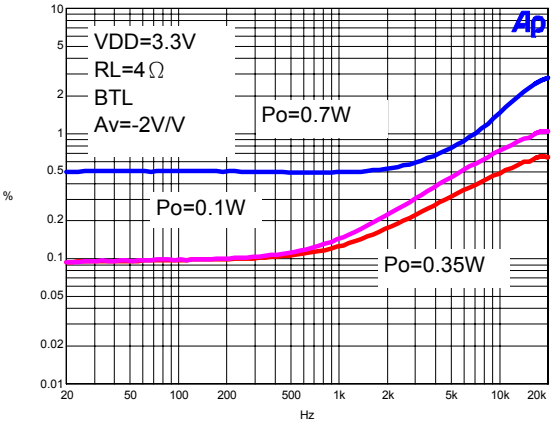


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

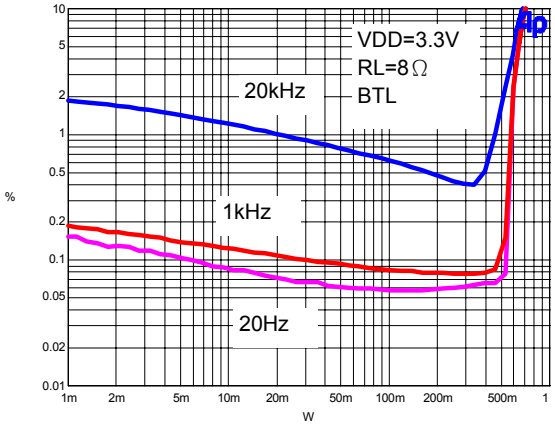


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

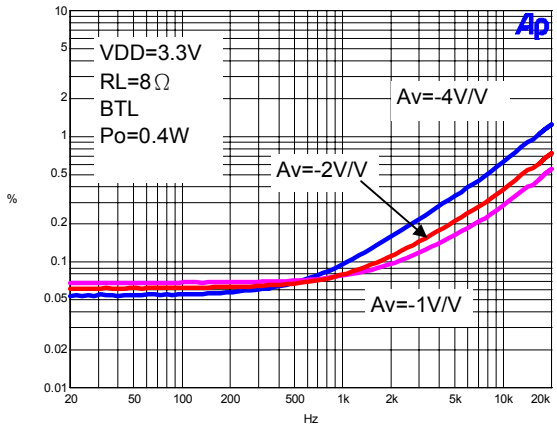


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

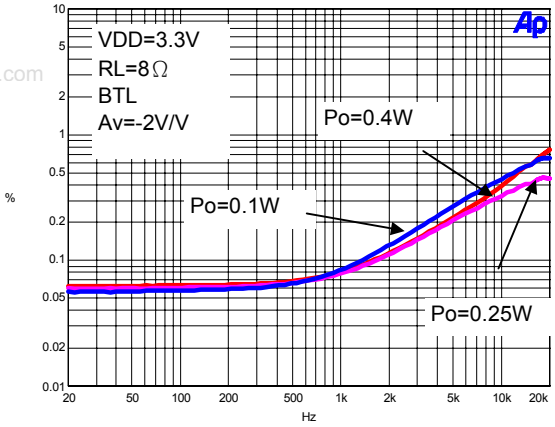


Figure 15

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

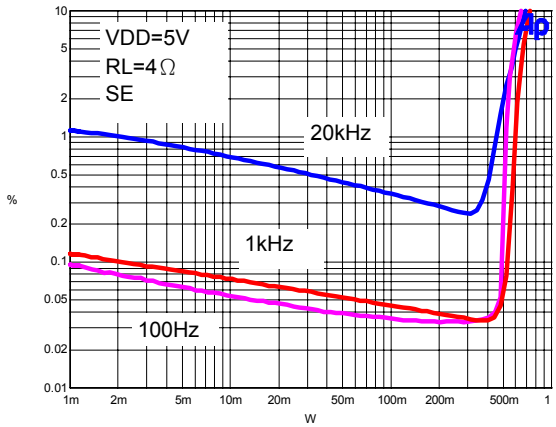


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

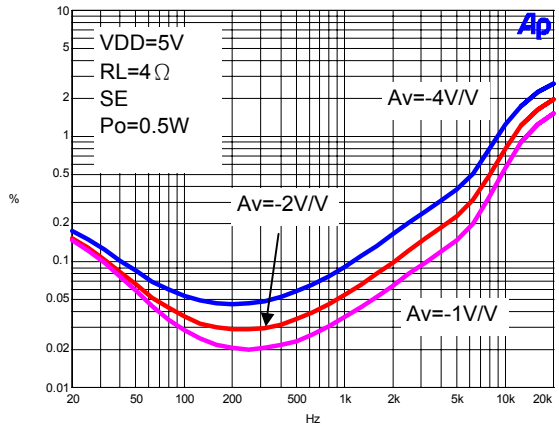


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

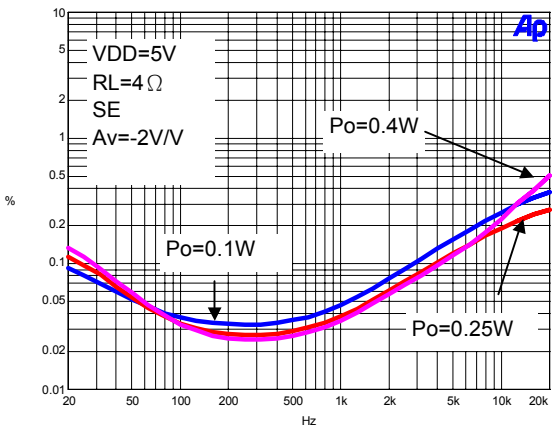


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

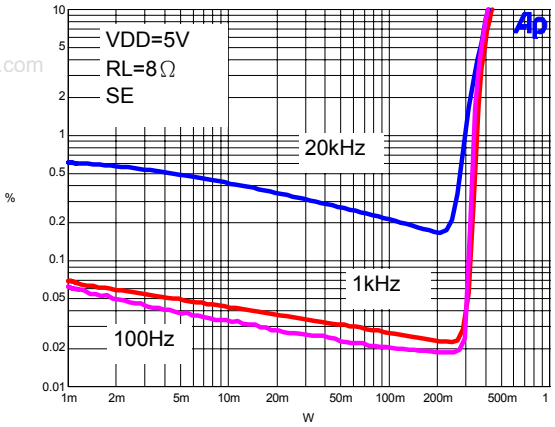


Figure 19

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

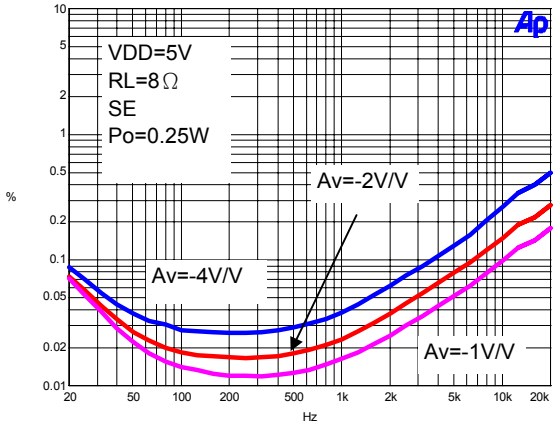


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

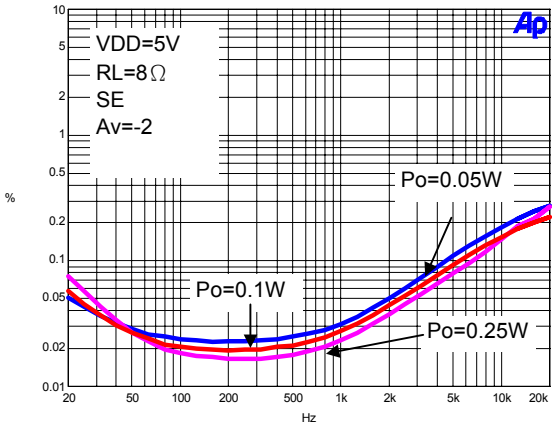


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

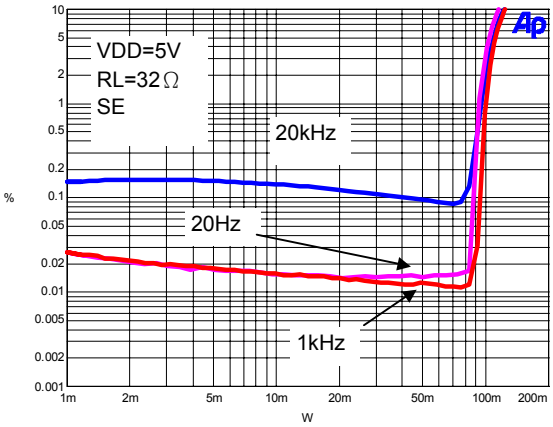


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

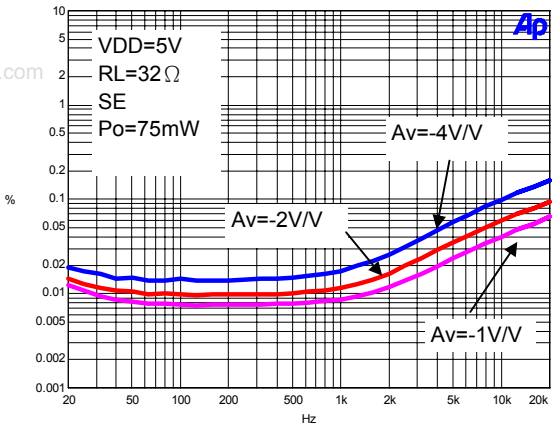


Figure 23

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

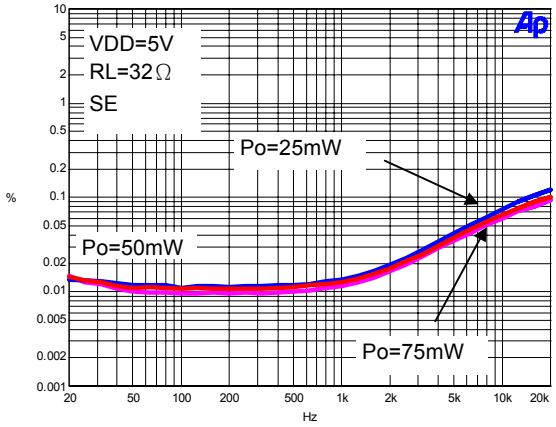


Figure 24

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

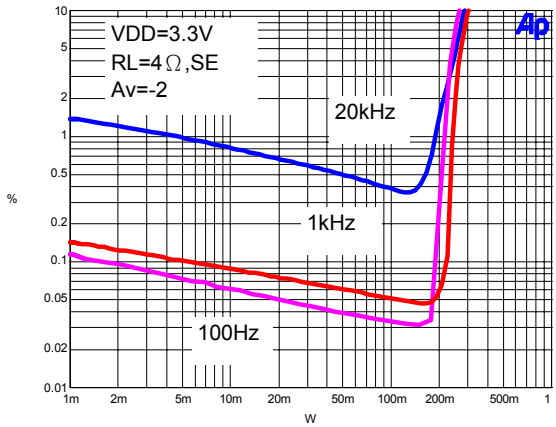


Figure 25

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

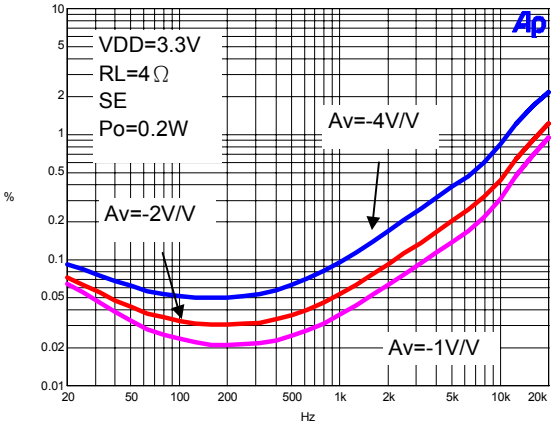


Figure 26

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

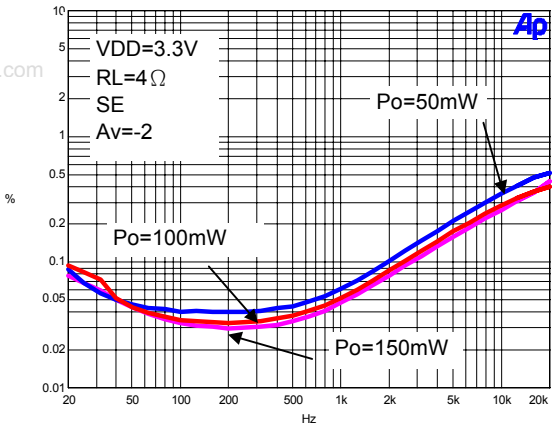


Figure 27

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

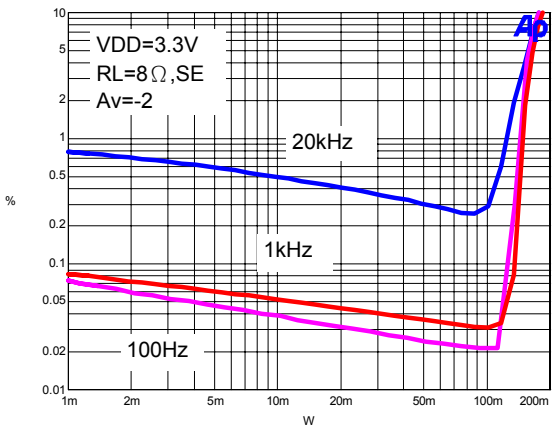


Figure 28

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

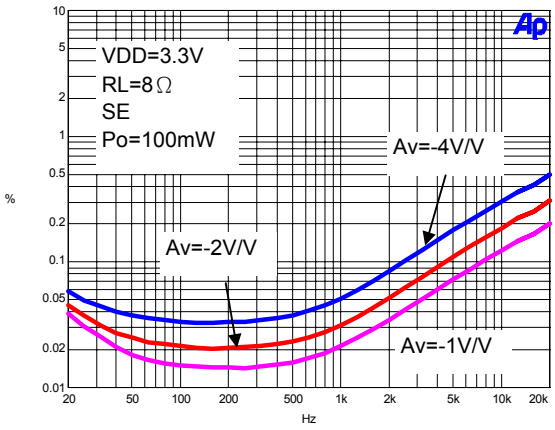


Figure 29

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

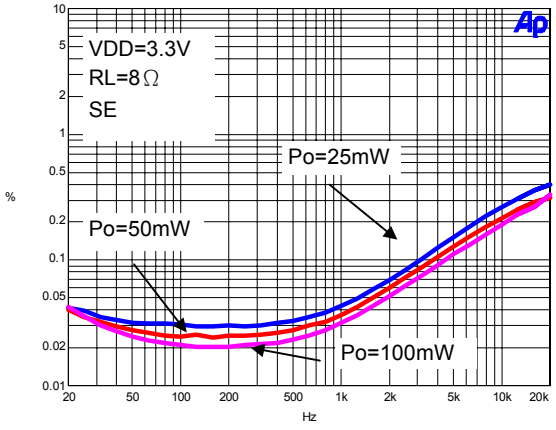


Figure 30

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

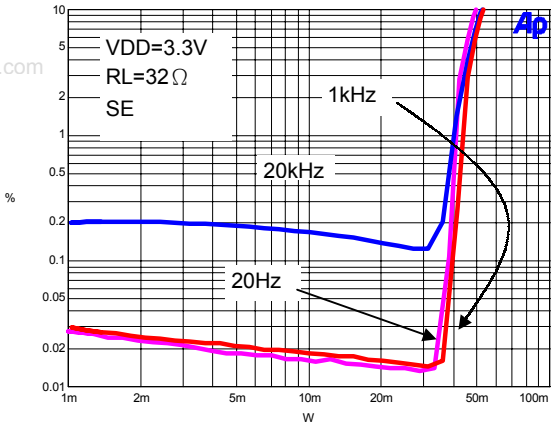


Figure 31

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

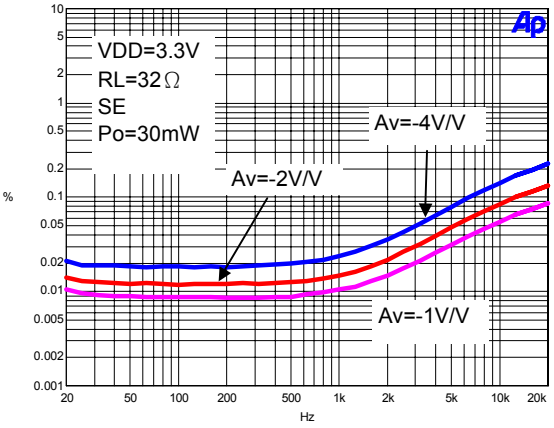


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT FREQUENCY

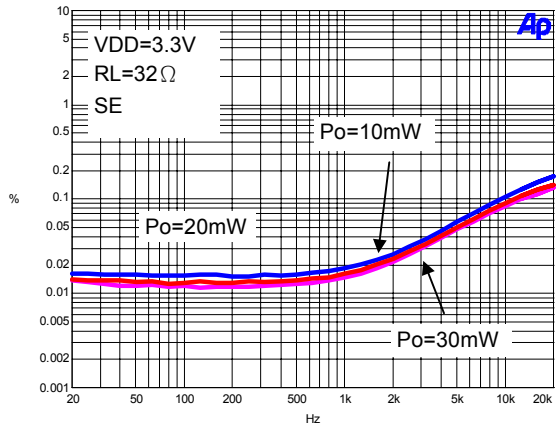


Figure 33

OUTPUT NOISE VOLTAGE vs FREQUENCY

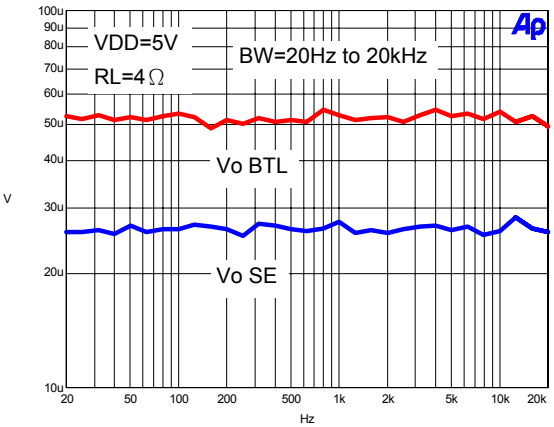


Figure 34

OUTPUT NOISE VOLTAGE vs FREQUENCY

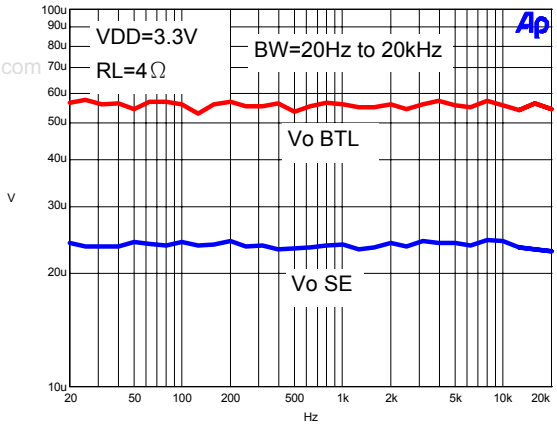


Figure 35

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

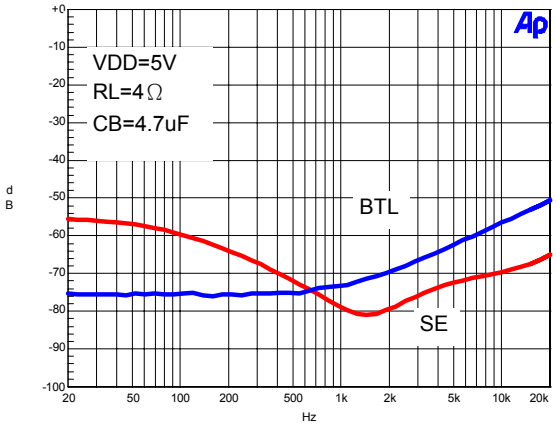


Figure 36

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

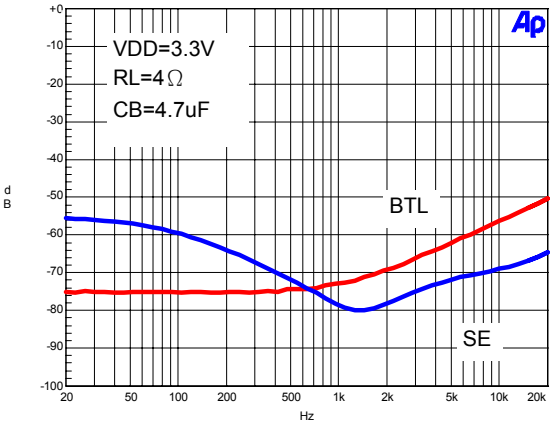


Figure 37

CROSSTALK vs FREQUENCY

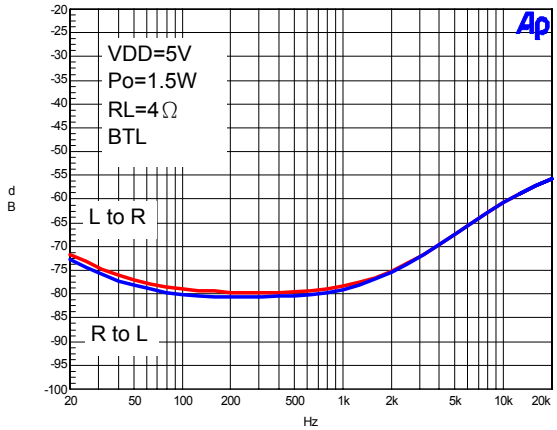


Figure 38

CROSSTALK vs FREQUENCY

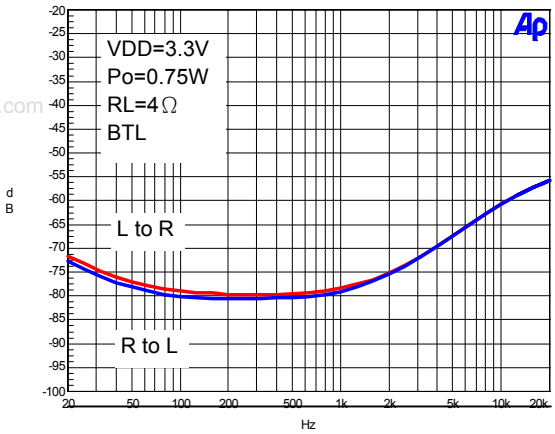


Figure 39

CROSSTALK vs FREQUENCY

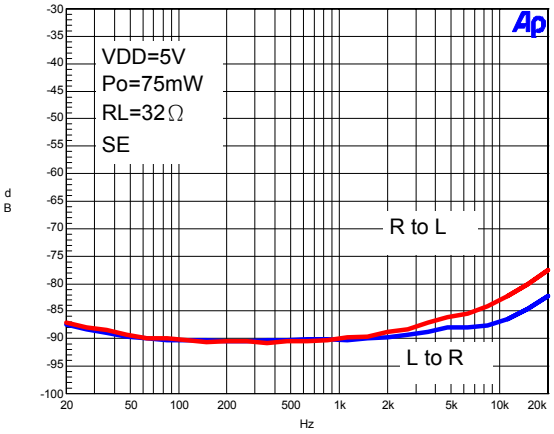


Figure 40

CROSSTALK vs FREQUENCY

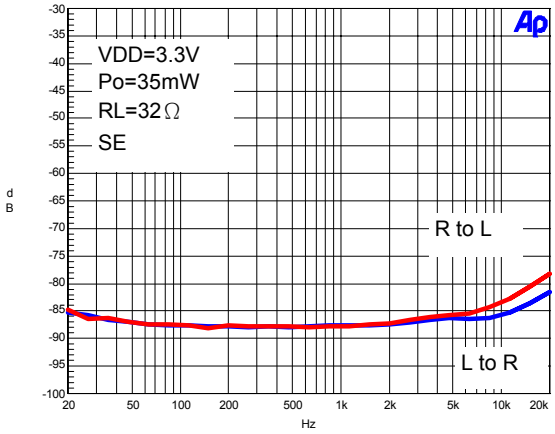


Figure 41

CLOSED LOOP RESPONSE

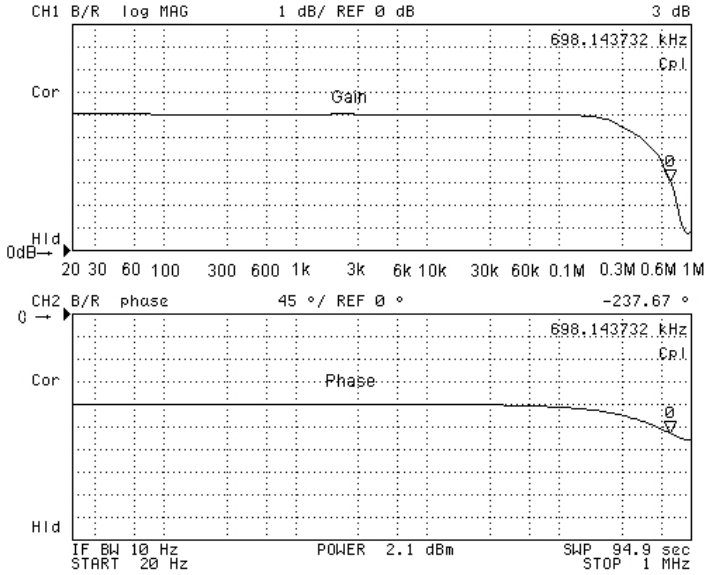


Figure 42

CLOSED LOOP RESPONSE

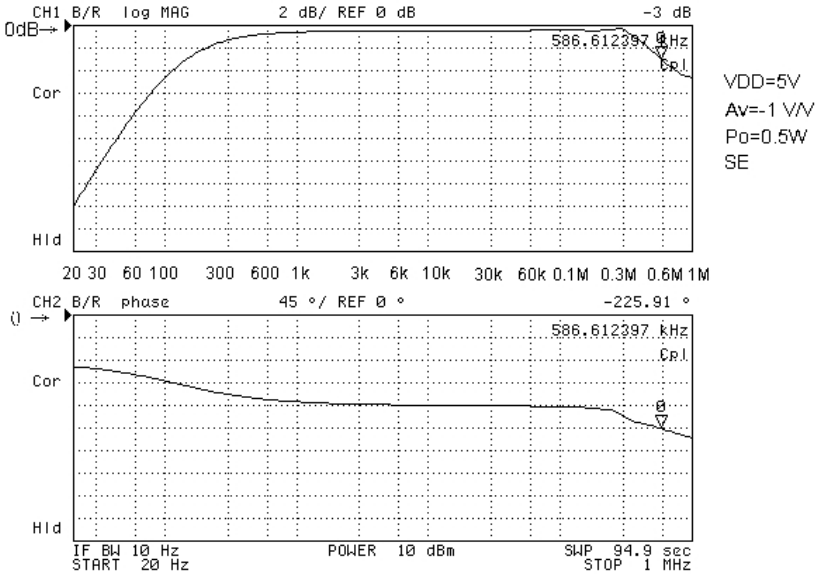


Figure 43

CLOSED LOOP RESPONSE

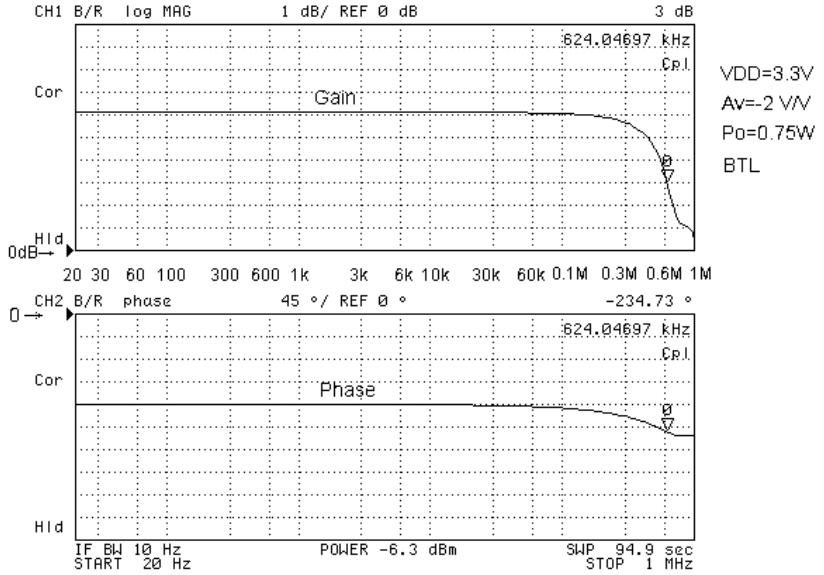


Figure 44

CLOSED LOOP RESPONSE

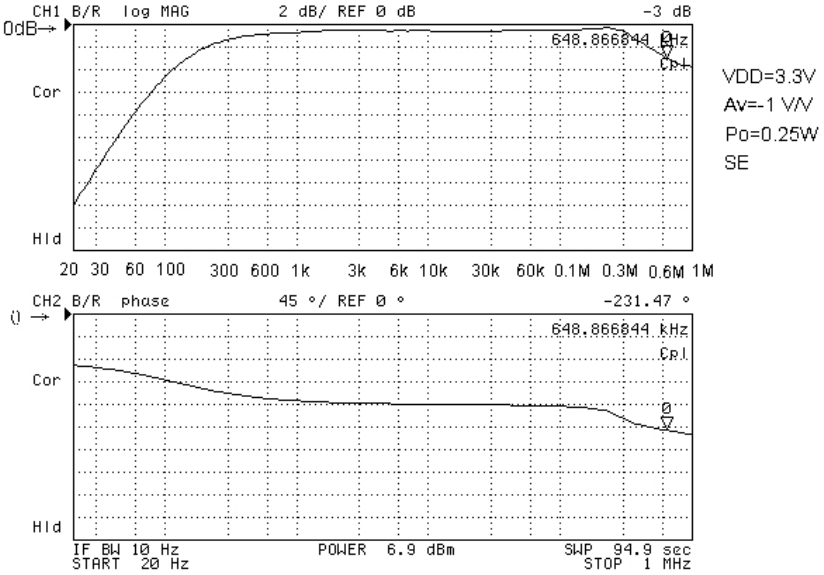


Figure 45

SUPPLY CURRENT vs SUPPLY VOLTAGE

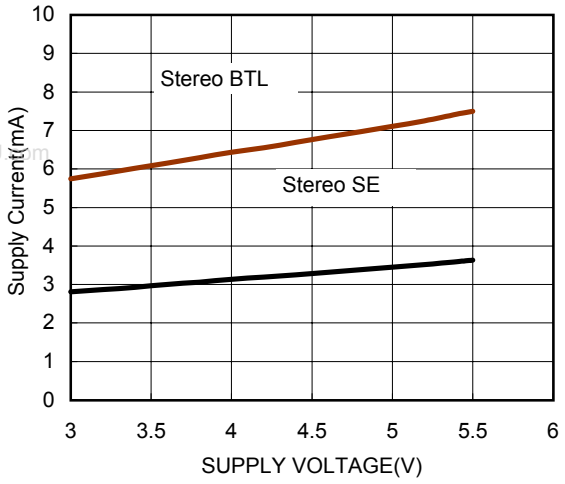


Figure 46

OUTPUT POWER vs SUPPLY VOLTAGE

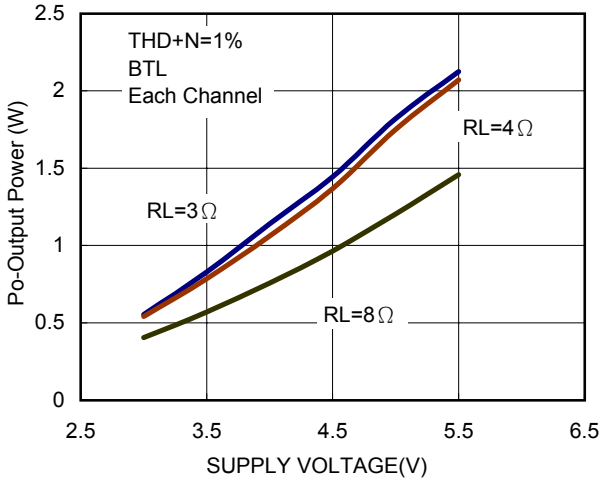


Figure 47

OUTPUT POWER vs SUPPLY VOLTAGE

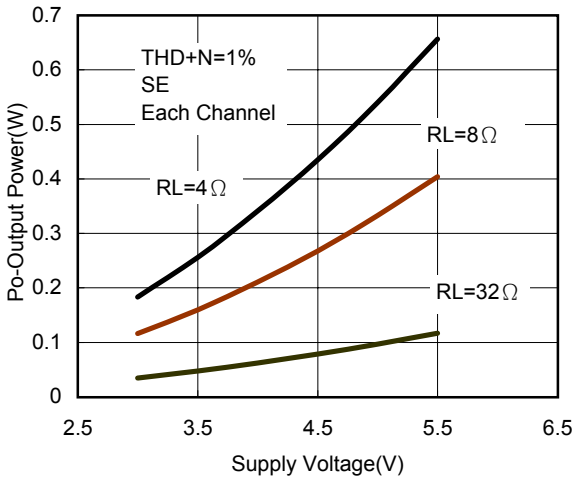


Figure 48

OUTPUT POWER vs LOAD RESISTANCE

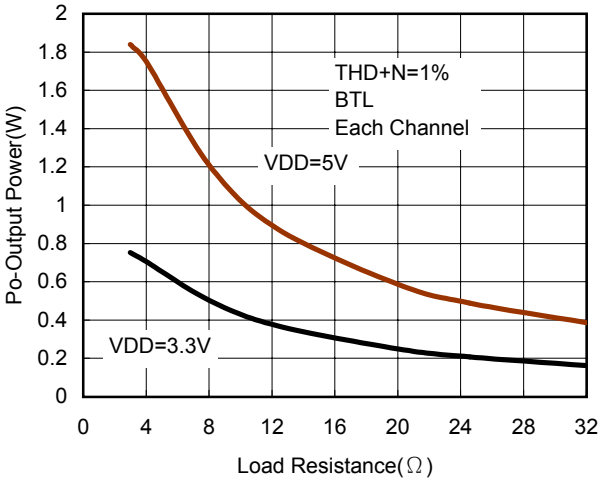


Figure 49

OUTPUT POWER vs LOAD RESISTANCE

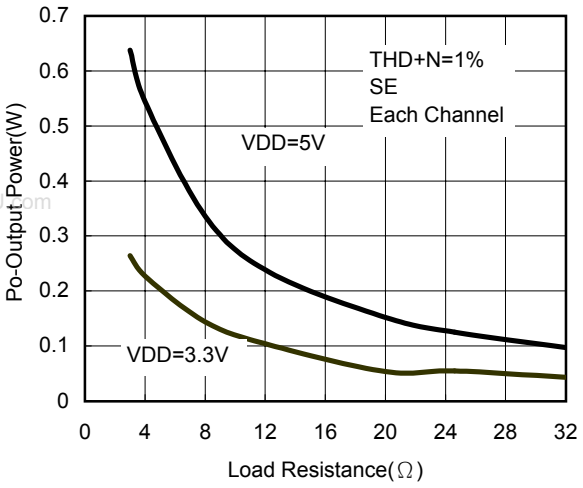


Figure 50

POWER DISSIPATION vs OUTPUT POWER

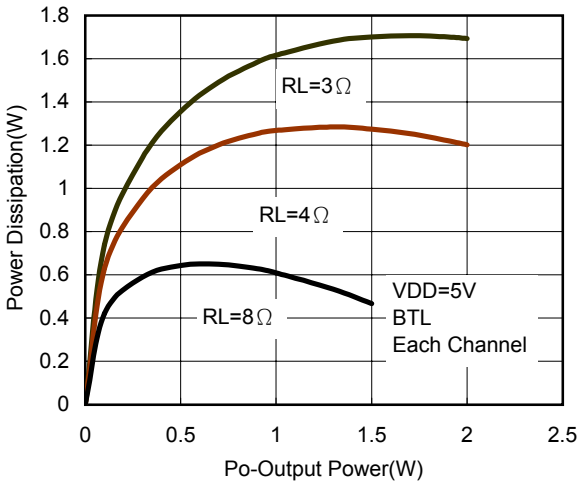


Figure 51

POWER DISSIPATION vs OUTPUT POWER

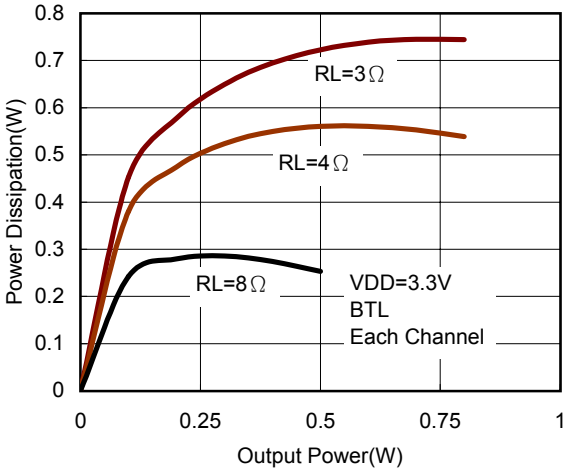


Figure 52

POWER DISSIPATION vs OUTPUT POWER

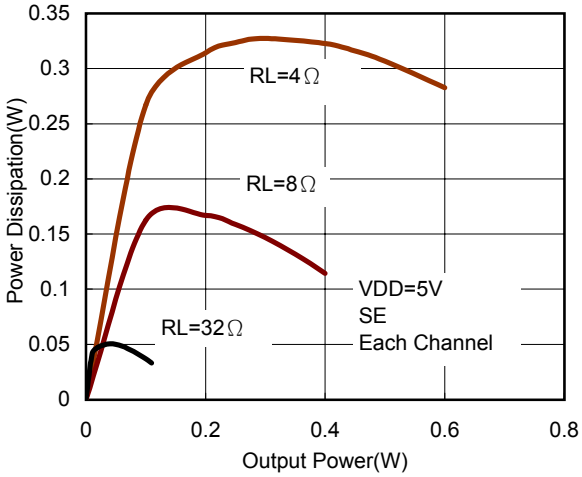


Figure 53

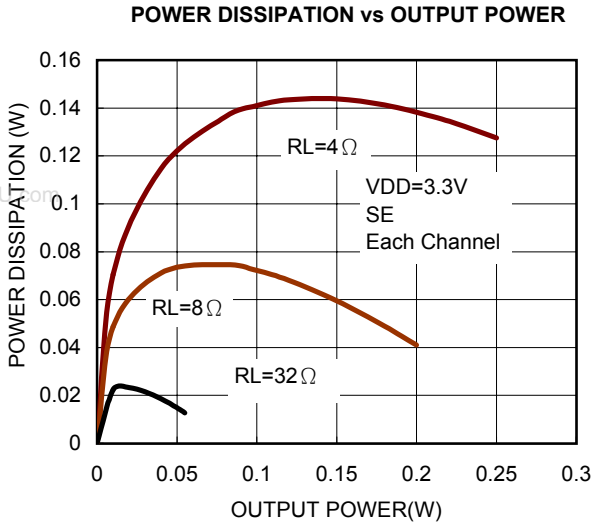
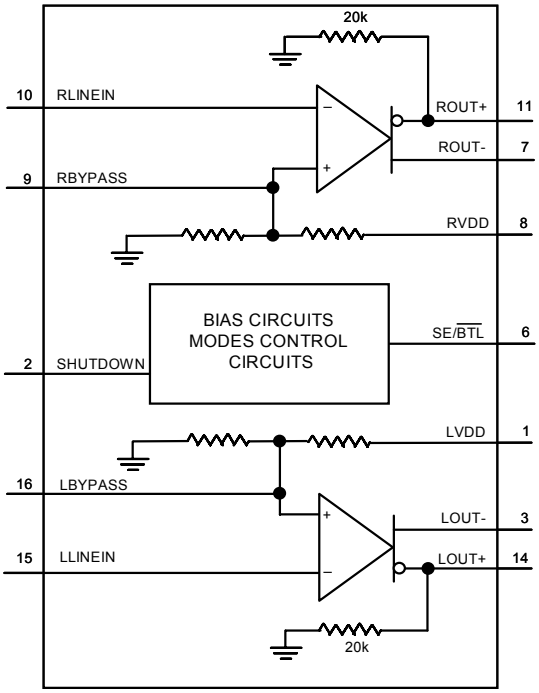
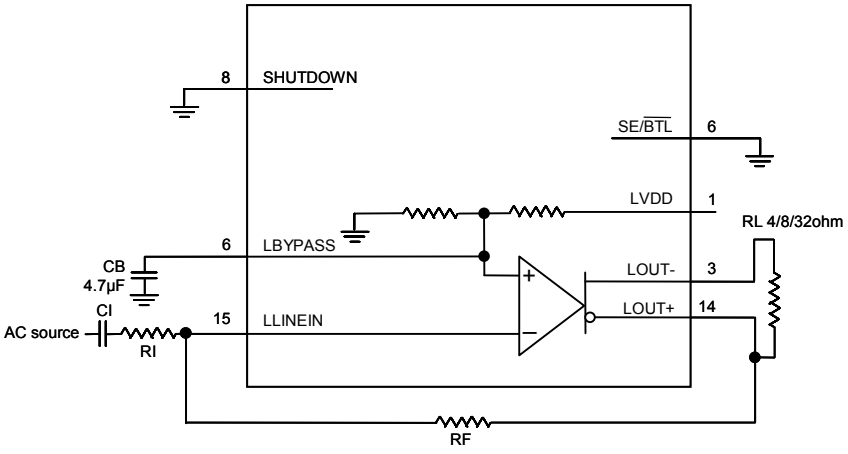


Figure 54

Block Diagram

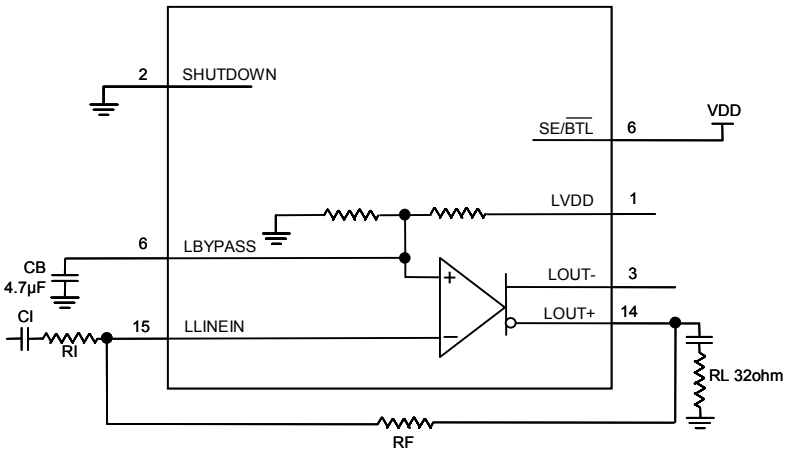


Parameter Measurement Information



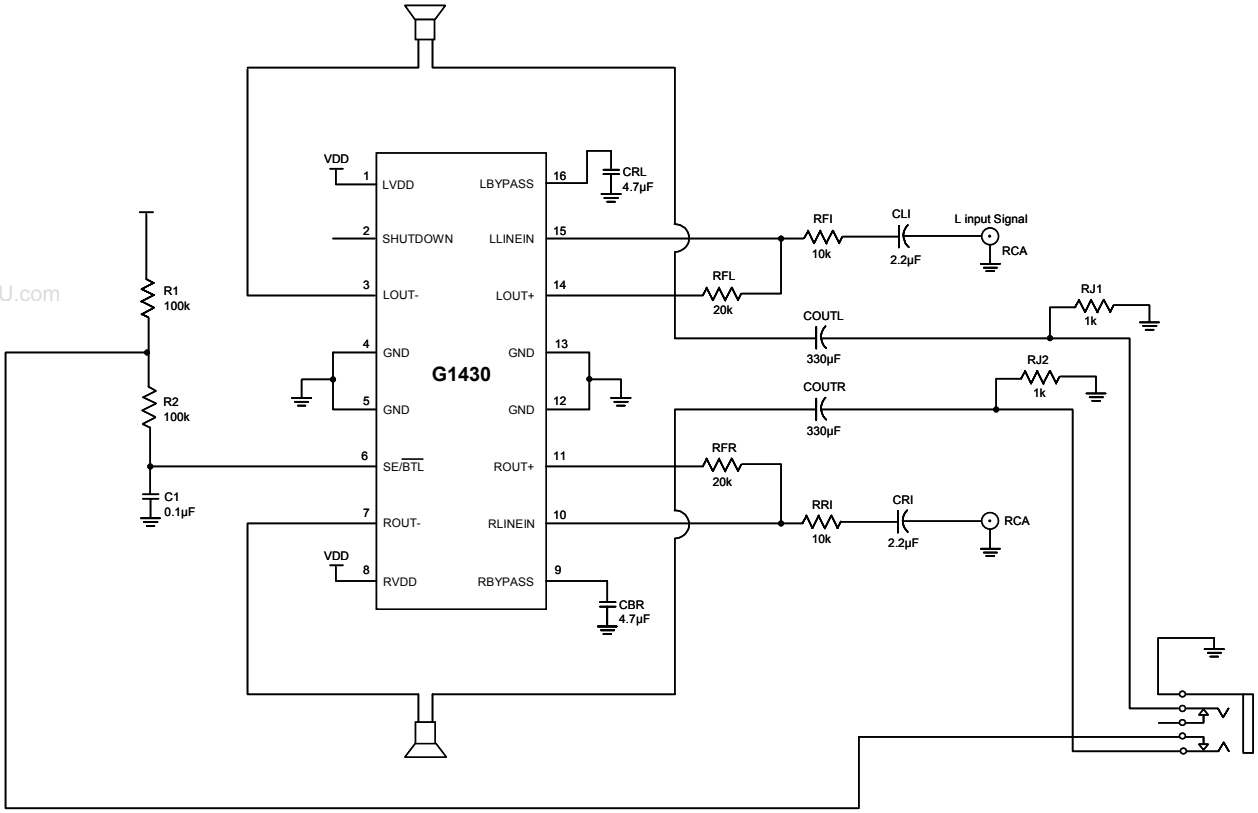
BTL Mode Test Circuit

Parameter Measurement Information (Continued)



SE Mode Test Circuit

Application Circuits



Logical Truth Table

INPUTS		AMPLIFIER STATES		
SE/$\overline{BTL}$	Shutdown	L/R Out+	L/R Out-	Mode
X	High	----	----	Mute
Low	Low	BTL Output	BTL Output	BTL
High	Low	SE Output	----	SE

Application Information

Single Ended Mode Operation

G1430 can drive clean, low distortion SE output power into headphone loads (generally 16Ω or 32Ω) as in Figure 1. Please refer to **Electrical Characteristics** to see the performances. A coupling capacitor is needed to block the dc offset voltage, allowing pure ac signals into headphone loads. Choosing the coupling capacitor will also determine the 3 dB point of the high-pass filter network, as Figure 2.

$$f_C = 1/(2\pi R_L C_C)$$

For example, a 68uF capacitor with 32Ω headphone load would attenuate low frequency performance below 73Hz. So the coupling capacitor should be well chosen to achieve the excellent bass performance when in SE mode operation.

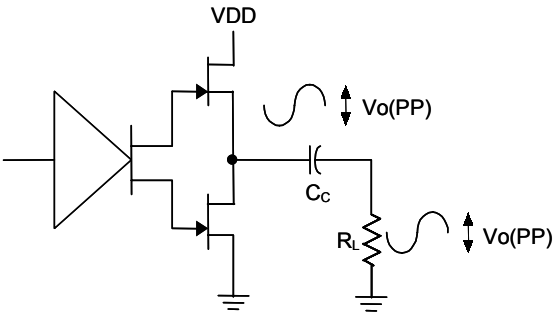


Figure 1

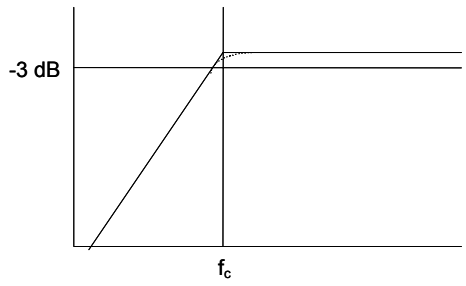


Figure 2

Bridged-Tied Load Mode Operation

G1430 has two linear amplifiers to drive both ends of the speaker load in Bridged-Tied Load (BTL) mode operation. Figure 3 shows the BTL configuration. The differential driving to the speaker load means that when one side is slewing up, the other side is slewing down, and vice versa. This configuration in effect will double the voltage swing on the load as compared to a ground reference load. In BTL mode, the peak-to-peak voltage V_O(PP) on the load will be two times than a ground reference configuration. The voltage on the load is doubled, this will also yield 4 times output power on the load at the same power supply rail and loading. Another benefit of using differential driving configuration is that BTL operation cancels the dc offsets, which eliminates the dc coupling capacitor that is needed to cancelled dc offsets in the ground reference configuration. Low-frequency performance is then limited only by the input network and speaker responses. Cost and PCB space can be minimized by eliminating the dc coupling capacitors.

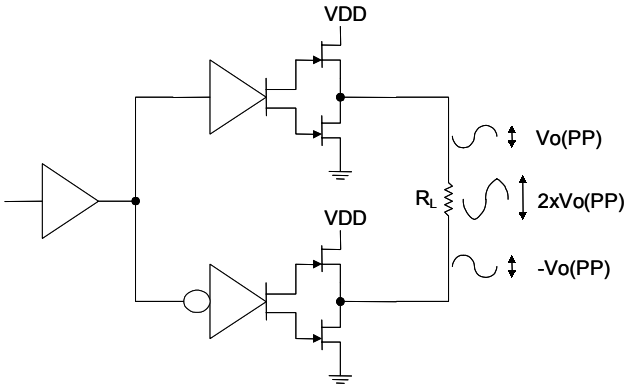


Figure 3

SHUTDOWN Mode Operations

G1430 implements the shutdown mode operations to reduce supply current, $I_{DD,}$ to the absolute minimum level during nonuse periods for battery-power conservation. When the shutdown pin (pin 2) is pulled high, all linear amplifiers will be deactivated to mute the amplifier outputs. And G1430 enters an extra low current consumption state, I_{DD} is smaller than 5μA. Shutdown pin should never be left unconnected, this floating condition will cause the amplifier operations unpredictable.

Optimizing DEPOP Operation

Circuitry has been implemented in G1430 to minimize the amount of popping heard at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker and making the differential voltage generated at the two ends of the speaker. To avoid the popping heard, the bypass capacitor should be chosen promptly, $1/(C_B x 100k\Omega) \leqq 1/(C_I*(R_I+R_F))$. Where 100kΩ is the output impedance of the mid-rail generator, C_B is the mid-rail bypass capacitor, C_I is the input coupling capacitor, R_I is the input impedance, R_F is the gain setting impedance which is on the feedback path. C_B is the most important capacitor. Besides it is used to reduce the popping, C_B can also determine the rate at which the amplifier starts up during startup or recovery from shutdown mode.

De-popping circuitry of G1430 is shown on Figure 4. The PNP transistor limits the voltage drop across the 50kΩ by slewing the internal node slowly when power is applied. At start-up, the voltage at BYPASS capacitor is 0. The PNP is ON to pull the mid-point of the bias circuit down. So the capacitor sees a lower effective voltage, and thus the charging is slower. This appears as a linear ramp (while the PNP transistor is conducting), followed by the expected exponential ramp of an R-C circuit.

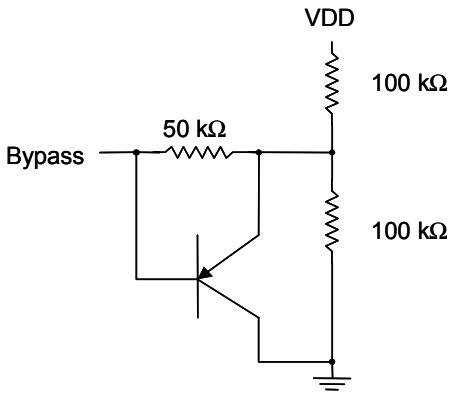
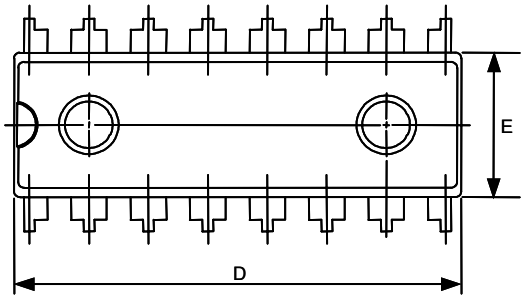
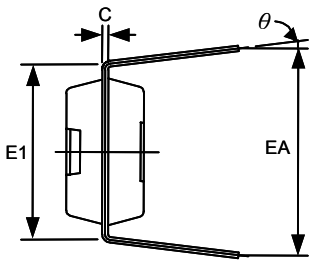
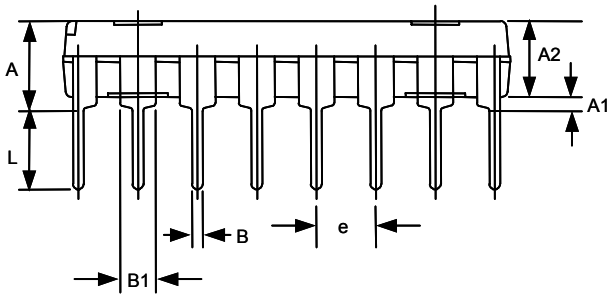


Figure 4

Package Information







DIP-16L Package

SYMBOL	DIMENSION IN MILIMETER			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-----	-----	4.318	-----	-----	0.170
A1	0.381	-----	-----	0.015	-----	0.015
A2	3.175	3.302	3.429	0.125	0.130	-----
B		0.457 TYP			0.018 TYP	
B1		1.527 TYP			0.060 TYP	
C	-----	0.254	-----	-----	0.010	-----
D	18.974	19.101	19.228	0.740	0.752	0.757
E	6.274	6.401	6.528	0.247	0.252	0.257
E1	7.366	7.62	7.874	0.290	0.300	0.310
EA	8.509	9.017	9.525	0.335	0.355	0.375
e		2.540 TYP			0.100 TYP	
L	3.048	3.302	3.556	0.120	0.130	0.140
θ	0°	-----	15°	0°	-----	15°