Coversheet

MODEL NO. : G1548FH101GF-001

ISSUED DATE: 2016-11-15

VERSION : A0

■**Preliminary Specification**

□**Final Product Specification**

Customer :_____

Approved by	Notes

GVO Confirmed :

Prepared by	Checked by	Approved by

This technical specification is subjected to change without notice.

Table of Contents

Record of Revision

Rev	Issue Date	Description	Editor
A0	2016.11.15	Draft	Zhao Tianyu

1 General Specifications

Feature		Spec	Remark
Display Spec	Screen Size (inch)	5.48	
	Display Mode	AMOLED	
	Resolution(dot)	1080(W)×1920(H)	
	Active Area(mm)	68.256(W)×121.344 (H)	
	Pixel Pitch (um)	94.8 (W)×63.2(H)	
	Technology Type	LTPS	
	Color Depth	16.7M	
	Interface	MIPI 4LANE	
	Surface Treatment	Hard Coating	
Mechanical Characteristics	With TP/Without TP	With TP(on Cell)	
	Module Outline Dimension(W x H x D) (mm)	73.56 (W)x148.86(H)x1.92(D)	Including Cover lens
	Weight (g)	TBD	
Electronic	Driver IC(Type)	RM67198	
	Touch IC(Type)	GT1151	

Note 1: Requirements on Environmental Protection: RoHS.

2 Input/output Terminals

2.1 Main FPC Pin Assignment

FPC connector: AXE340124, B-TO-B Connector.

Main board recommended connector: AXE440124 B-TO-B Connector.

No	Symbol	I/O	Description
1	VPP	P	Power supply for MTP Programming or Erase. If it is not used please open it.
2	D3N	I	MIPI data lane
3	NC		NC
4	D3P	I	MIPI data lane
5	ELON2	O	DC/DC Power IC S-Wire CTRL Pin
6	GND	GND	Ground
7	VDDP_EN	O	DC/DC Power Enable Pin
8	D0N	I/O	MIPI data lane
9	PCD	O	Panel Crack Detection Pin
10	D0P	I/O	MIPI data lane
11	TE	I	Sync Signal for preventing Tearing Effect
12	GND	GND	Ground
13	ERR_FG	O	MIPI Error Pin
14	CKN	I	MIPI clock lane
15	RESX	I	Display reset. Active low.
16	CKP	I	MIPI clock lane
17	VDDIO	P	Power supply for display logic circuits
18	GND	GND	Ground
19	TSP_1.8V	P	Power supply for display logic circuits
20	D1N	I	MIPI data lane
21	VLIN_6.5V	P	External Power Input for AVDD
22	D1P	I	MIPI data lane
23	VCI	P	Power supply for display analog circuits
24	GND	GND	Ground
25	TSP_SDA	I/O	SDA pin for TP

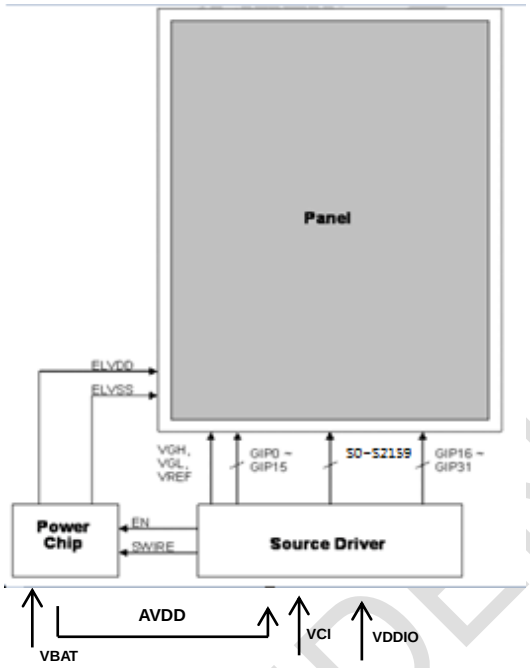
26	D2N	I	MIPI data lane
27	TSP_SCL	I	SCL pin for TP
28	D2P	I	MIPI data lane
29	TSP_ATTN	I	INT pin for TP
30	GND	GND	Ground
31	TSP_ 3.3V	P	Analog Power for TP
32	TSP_RESET	I	Reset Pin for TP, Active low.
33	TSP_1.8V	P	Power supply for TP logic circuits
34	NC		NC
35	ELVDD	P	Positive power supply for EL
36	ELVSS	P	Negative power supply for EL
37	ELVDD	P	Positive power supply for EL
38	ELVSS	P	Negative power supply for EL
39	ELVDD	P	Positive power supply for EL
40	ELVSS	P	Negative power supply for EL

Note: I=Input; O=Output; P=Power; I/O=Input / Output

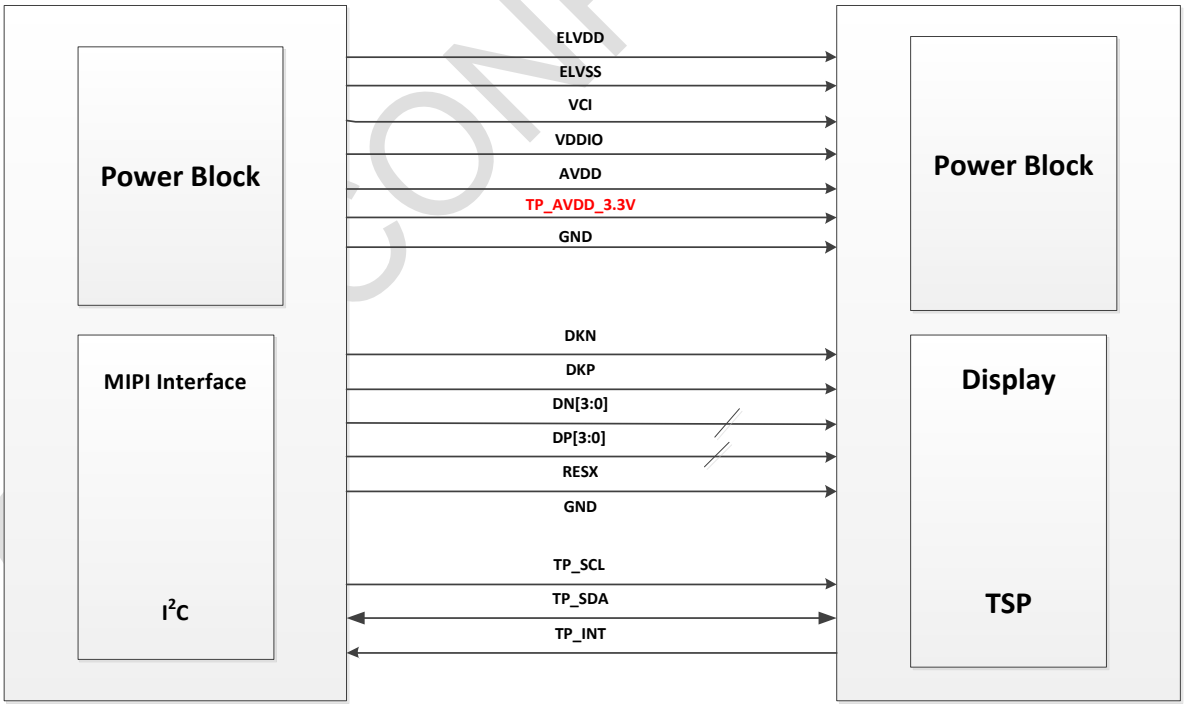
2.2 TP FPC Pin Assignment-On-cell TP Input / Output Signal Interface

No	Symbol	I/O	Description
1	TSP_DVDD_1.8V	Power	Power supply for display logic circuits
2	TSP_RESET	I	Reset Pin for TP, Active low
3	TSP_AVDD_3.3V	Power	Analog Power for TP
4	TSP_SDA	I/O	SDA pin for TP
5	TSP_SCL	I/O	SCL pin for TP
6	TSP_ATTN	I/O	INT pin for TP
7	GND	GND	Ground

2.3 Circuit block diagram (Display)



2.4 MCU and Display Module Interface Conflagration



3 Absolute Maximum Ratings

3.1 Driving AMOLED Panel

Maximum Ratings (Voltage Referenced to VSS) Vss=0V, Ta=25℃

Item	Symbol	MIN	MAX	Unit
Analog Power supply	VCI	-0.3	+5.0	V
Logic Power supply	VDDIO	-0.3	+4.0	V
Positive Power Input	ELVDD	-	+5.0	V
Negative Power Input	ELVSS	-5.0	-	V

Note: Functional operation should satisfy the limits in the Electrical Characteristics tables or Pin Description section. If the module exceeds the absolute maximum ratings, permanent damage may occur. Besides, if the module is operated with the absolute maximum ratings for a long time, the reliability may also drop.

4 Electrical Characteristics

4.1 Driving AMOLED Panel

Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit
Logic Power supply		VDDIO	1.65	1.80	3.30	V
Analog Power supply		VCI	2.65	2.80	3.60	V
ELVDD Supply Voltage		ELVDD	4.55	4.60	4.65	V
ELVSS Supply Voltage		ELVSS	-1	TBD	-5	V
Input Signal Voltage	High Level	VIH	0.80*VDDIO	-	VDDIO	V
	Low Level	VIL	0.00	-	0.20*VDDIO	V
Output Signal Voltage	High Level	VOH	0.80*VDDIO	-	VDDIO	V
	Low Level	VOL	0.00	-	0.20*VDDIO	V

Note1: The input digital voltage is the I/O reference voltage.

Note2: VDDIO usually ranges from 1.65V to 1.95 V. If VDDIO is changed, the remaining voltage needs to be changed to the same voltage as VDDIO.

4.2 Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD=4.6V	-	TBD	TBD	mW	Note1
		I_{NL}	ELVSS=TBD	-	191.80	TBD	mA	Note2
IC	Normal	I_{VCI}	VCI=2.8V		1.5	TBD	mA	-
		I_{IOVCC}	VDDIO=1.8V		42	TBD	mA	-
	Stand-by	I_{VCI}	VCI=2.8V		1	TBD	uA	-
		I_{IOVCC}	VDDIO=1.8V		1	TBD	uA	-

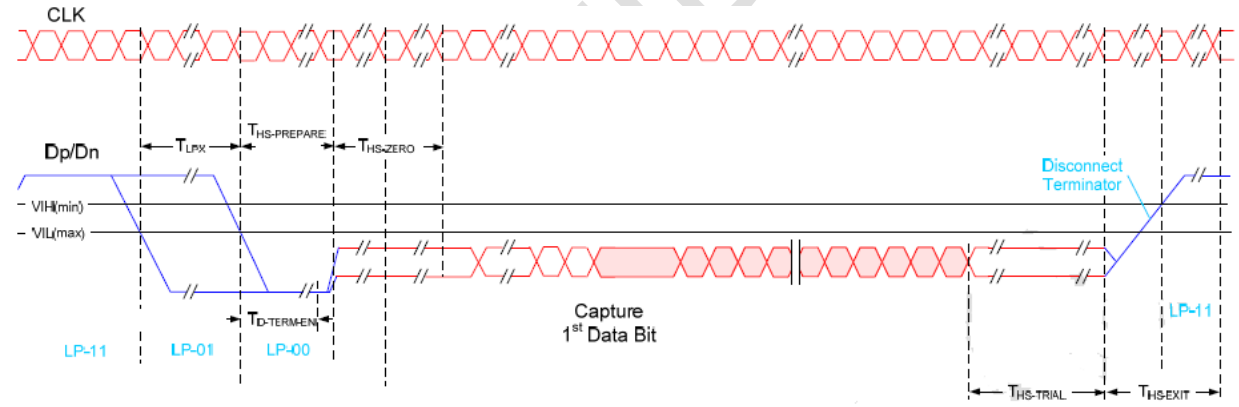
Note1: Based on L255 (350nit) full white pattern.

Note2: Video Mode 60Hz.

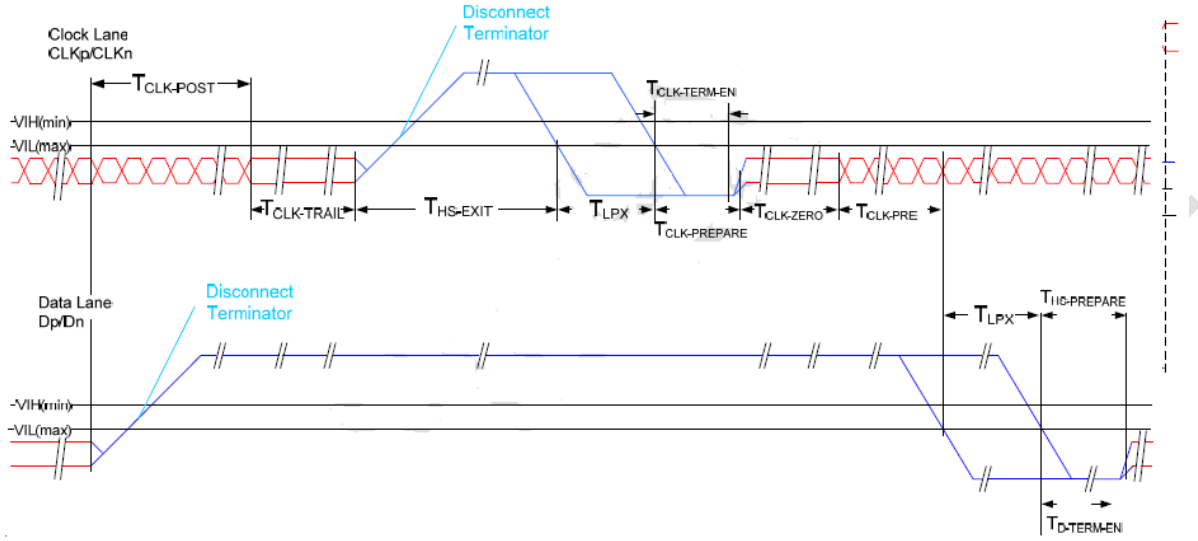
5 AC Characteristics

5.1 MIPI Interface Characteristics

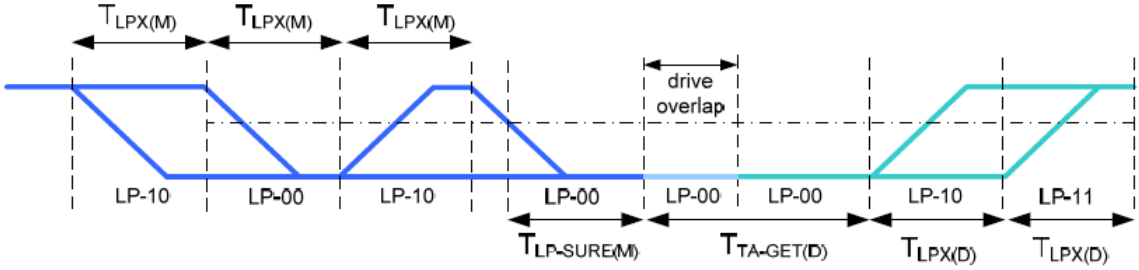
HS Data Transmission Burst



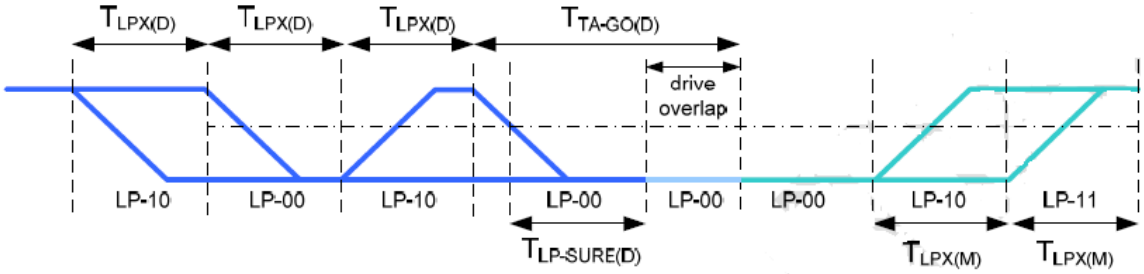
HS clock transmission



Turnaround Procedure



Bus turnaround (BAT) from MPU to display module timing



Timing Parameters：