



MODEL NO. : G1549HD112GF-001

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- Preliminary Specification
- Final Product Specification

Customer : \_\_\_\_\_

Approved by	Notes

GVO Confirmed :

Prepared by	Checked by	Approved by
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This technical specification is subjected to change without notice.



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### Record of Revision

Rev	Issue Date	Description	Editor
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## 1 General Specifications

	Feature	Spec	Remark
<b>Display Spec</b>	Screen Size (inch)	5.49	
	Display Mode	AMOLED	
	Resolution(dot)	720 (W) x RGB x 1280(H)	
	Active Area(mm)	68.40(W)×121.60 (H)	
	Pixel Pitch (um)	95.00(W) x 95.00 (H)	
	Pixel Configuration	V-Style3	
	Technology Type	LTPS	
	Color Depth	16.7M	
	Interface	MIPI 4LANE	
	Surface Treatment	Hard Coating	
<b>Mechanical Characteristics</b>	With TP/Without TP	With TP(on Cell)	
	Module Outline Dimension(W x H x D) (mm)	70.80(W) x128.47(H) x 0.80(D)	Excluding Cover lens
	Weight (g)	TBD	
<b>Electronic</b>	Driver IC(Type)	RM67120	
	Touch IC(Type)	GT1151	

Note 1: Requirements on Environmental Protection: RoHS.



## 2 Input/output Terminals

### 2.1 Main FPC Pin Assignment

FPC connector: AXE240044D (Panasonic).

Main board recommended connector: AXE140047D (Panasonic).

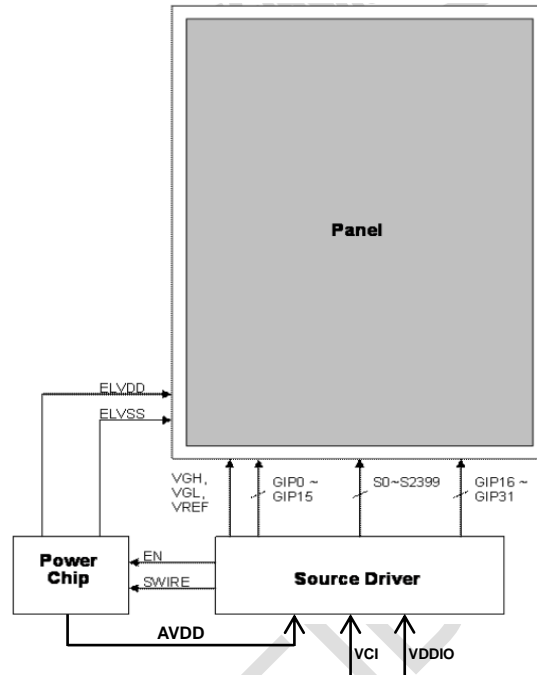
No	Symbol	I/O	Description
1	TP_DVDD	POWER	TP power supply for all GPIO pins. Leave it OPEN if is not used.
2	TP_AVDD	POWER	TP Analog power supply input
3	TP_SDA	I/O	Touch panel I2C data
4	TP_SCL	I/O	Touch panel I2C clock
5	TP_INT	O	Touch panel interrupt output
6	TP_RESET	I	Touch panel reset
7	SWIRE	O	Setting DC/DC Power IC ELVDD & ELVSS output voltage
8	OLED_EN	O	Enable DC-DC power IC,AVDD output
9	TE	O	Vsync signal to avoid Tearing Effect
10	VDDIO	POWER	Power supply for display logic circuit
11	AVDD	POWER	Display Driver IC Source Analog Power
12	VCI	POWER	Power supply for driver IC analog circuit
13	RESX	I	Driver IC Reset Pin
14	MTP_PWR	POWER	7.5 V, Gamma MTP function Pin. Must be left open or connected to GND in normal condition.
15	LCD_ID1	POWER	Module ID check ( Customer request ) .
16	LCD_ID0	POWER	Module ID check ( Customer request ) .
17	NC	NC	Not connected
18	ELVDD	POWER	Positive power supply for OLED
19	ELVDD	POWER	Positive power supply for OLED
20	ELVDD	POWER	Positive power supply for OLED
21	ELVSS	POWER	Negative power supply for OLED
22	ELVSS	POWER	Negative power supply for OLED
23	ELVSS	POWER	Negative power supply for OLED
24	NC	NC	Not connected
25	GND	GND	Ground



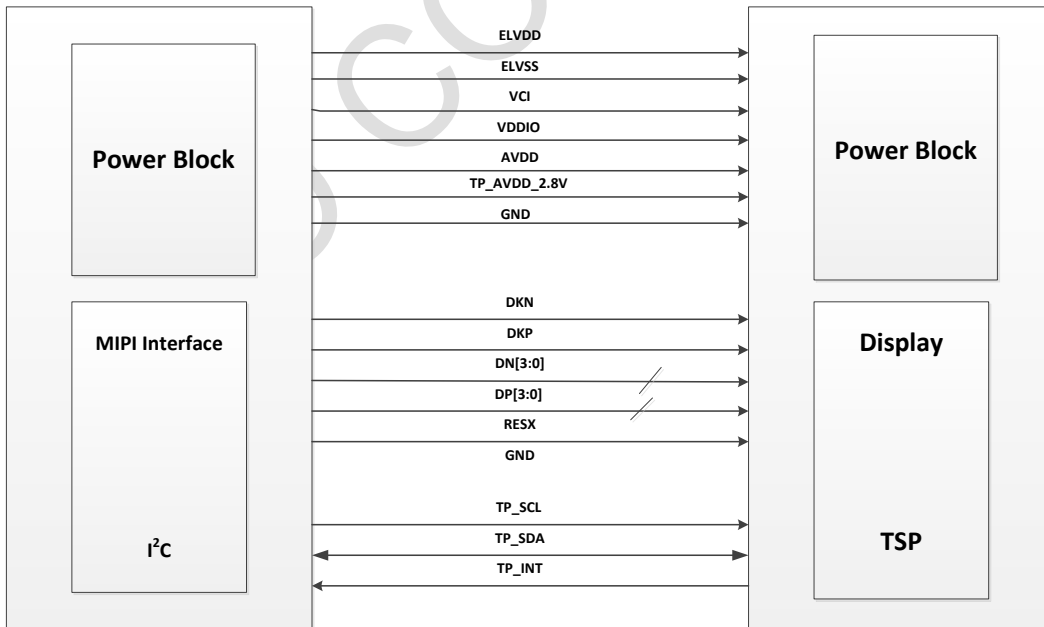
26	D2P	I	MIPI Data Lane2 +
27	D2N	I	MIPI Data Lane2 -
28	GND	GND	Ground
29	D1P	I	MIPI Data Lane1 +
30	D1N	I	MIPI Data Lane1 -
31	GND	GND	Ground
32	CKP	I	MIPI Clock Lane +
33	CKN	I	MIPI Clock Lane -
34	GND	GND	Ground
35	D0P	I	MIPI Data Lane0 +
36	D0N	I	MIPI Data Lane0 -
37	GND	GND	Ground
38	D3P	I	MIPI Data Lane3 +
39	D3N	I	MIPI Data Lane3 -
40	GND	GND	Ground

Note: I=Input; O=Output; P=Power; I/O=Input / Output

## 2.2 Circuit block diagram (Display)



## 2.3 MCU and Display Module Interface Conflagration







### 3 Absolute Maximum Ratings

#### 3.1 Driving AMOLED Panel

Maximum Ratings (Voltage Referenced to VSS) Vss=0V, Ta=25°C

Item	Symbol	MIN	MAX	Unit
Analog Power supply	VCI	-0.3	+5.0	V
Logic Power supply	VDDIO	-0.3	+4.0	V
Positive power for OLED	ELVDD	+4.0	+5.0	V
Negative power for OLED	ELVSS	-5.0	-1.0	V
Source Analog Power	AVDD	+3.5	+6.5	V
D0P, D0N D1P, D1N D2P, D2N D3P, D3N DKP, DKN	Differential Input	-0.3	+2.5	V
Touch analog power supply	TP_AVDD_2.8V	-0.3	+4.0	V
Touch IC input current at any pin		—	±100	mA

Note: Functional operation should satisfy the limits in the Electrical Characteristics tables or Pin Description section. If the module exceeds the absolute maximum ratings, permanent damage may occur. Besides, if the module is operated with the absolute maximum ratings for a long time, the reliability may also drop.

### 4 Electrical Characteristics

#### 4.1 Driving AMOLED Panel

Ta=25°C

Symbol	Item	MIN	TYP	MAX	Unit
VDDIO	Logic Power supply	1.65	1.80	3.30	V
VCI	Analog Power supply	2.65	2.80	3.60	V
AVDD	Source Analog Power	6.30	6.40	6.50	V
ELVDD	Default Positive Output Voltage		4.60		V
	Positive Output voltage total variation	-0.80		+0.80	%
ELVSS	Default Negative Output voltage		-4.00		V
	Negative output voltage total variation	-1.00		+1.00	%
TP_AVDD_2.8V	Touch analog power supply	2.70	2.80	3.60	V
VIH	Logic high/low level	High Level	0.80*VDDIO	-	VDDIO



VIL	Input voltage	Low Level	0.00	-	0.20*VDDIO	V
VOH	Logic high/low level	High Level	0.80*VDDIO	-	VDDIO	V
VOL	Output voltage	Low Level	0.00	-	0.20*VDDIO	V

#### 4.2 Current Consumption

Item	Symbol	Condition	Typ.	Max.	Unit	Remark	
Panel Power	$P_{NL}$	ELVDD=4.6V ELVSS=-4V VCI=2.8V	TBD	TBD	mW	Note1	
	$I_{NL}$		TBD	TBD	mA	Note1	
IC	Normal	VDDIO=1.8V AVDD=6.4V	$I_{AVDD}$	TBD	TBD	mA	Note2、 Note 3
			$I_{VCI}$	TBD	TBD	mA	Note2、 Note 3
			$I_{VDDIO}$	TBD	TBD	mA	Note2、 Note 3
	Stand-by	VCI=2.8V VDDIO=1.8V	$I_{AVDD}$		TBD	uA	Note3
			$I_{VCI}$	20	70	uA	Note3
			$I_{VDDIO}$	5	10	uA	Note3

Note1: Based on L255 (350nits) full white pattern.

Note2: Video Mode 60Hz.

Note3: RESX=High

## 5 AC Characteristics

### 5.1 Input Timing

Table 5-1 Input Timing

Resolution		720RGB X 1280			Unit	Note
Input Timing	Symbol	Min.	Typ.	Max.		
PCLK Frequency	-	57.7	63.2	132.1	MHz	-
Horizontal Active Area	THA	-	720	-	PCLK	-
Horizontal Back Porch	THB	10	16	255	PCLK	-
Horizontal Front Porch	THF	10	16	255	PCLK	-
Horizontal Total	THT	740	784	1230	PCLK	-
Vertical Active Area	TVA	-	1280	-	THT	-
Vertical Back Porch	TVB	10	16	255	THT	-
Vertical Front Porch	TVF	10	16	255	THT	-
Vertical Total	TVT	1300	1344	1790	THT	-
Vertical Frequency	-	-	60	-	Hz	-

### 5.2 MIPI Interface Characteristics

#### 5.2.1 General Description

The communication can be separated 2 different levels between the MCU and the display module:

- Interface Level: Low level communication
- Packet Level: High level communication

#### 5.2.2 Interface Level Communication

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane0 can be driven in Low Power (LP) or High Speed (HS) mode. Data lane1~3 can be driven in High Speed mode only.

	Lane support mode	MPU(Host)	(Slave)
Clock Lane	Unidirectional lane ★High-Speed Clock only ★Simplified Escape Mode (ULPS Only)		
Data lane0	Bi-directional lane ★Forward high-speed only ★Bi-directional Escape Mode ★Bi-direction LPDT		
Data lane1	Unidirectional lane ★ Forward high-speed only ★Simplified Escape Mode (ULPS Only)		
Data lane2	Unidirectional lane ★Forward high-speed only		

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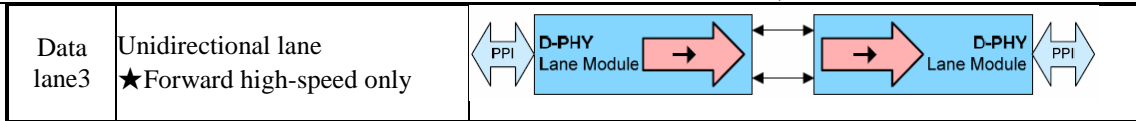


Figure 5-1 Lane types and support mode

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Figure 5-2 High Speed and Low-Power Lane Pair State Descriptions

### 5.2.3 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP=Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP=Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences. The principal flow chart of the different clock lanes power modes is illustrated below.

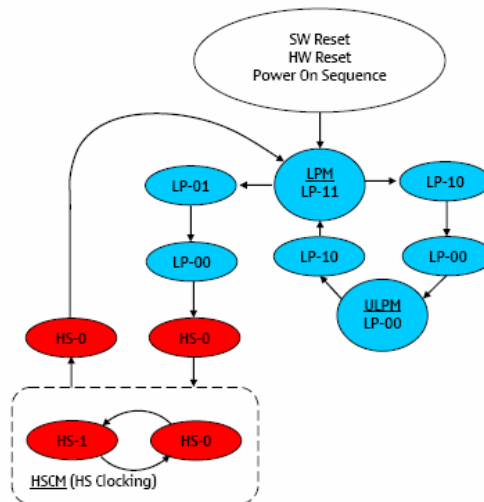


Figure 5-3 Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

### 5.2.4 DSI Data Lanes

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI\_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI\_D0 data lane pair)

These modes and their entering codes are defined on the following table.

Table 5-2 Entering and leaving sequences

	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	LP-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

### 5.2.5 Packet Level Communication

#### 5.2.5.1 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSMT) modes.

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

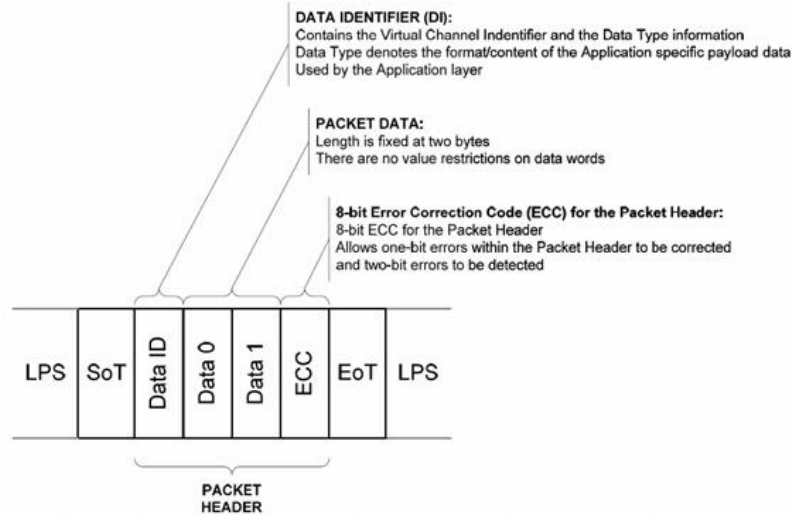


Figure 5-4 Short packet structure

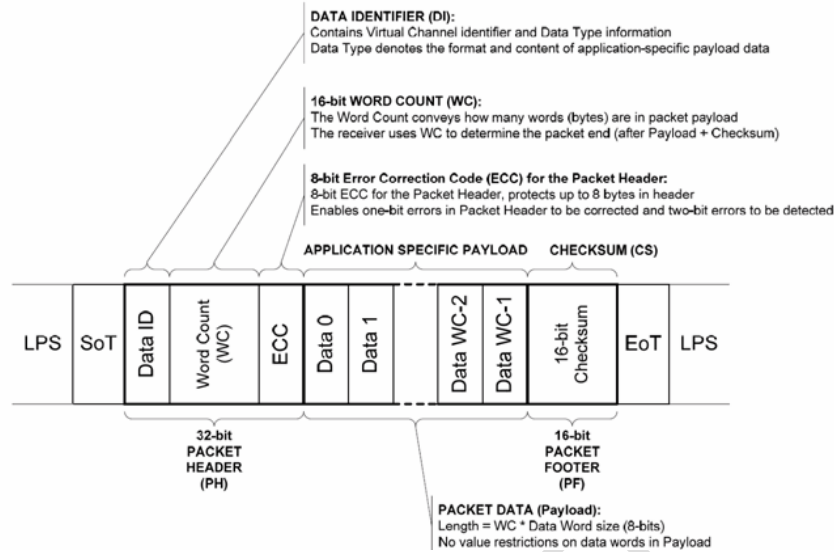


Figure 5-5 Long packet structure

### 5.2.5.2 Packet Transmissions

#### Packet from the MCU to the display module

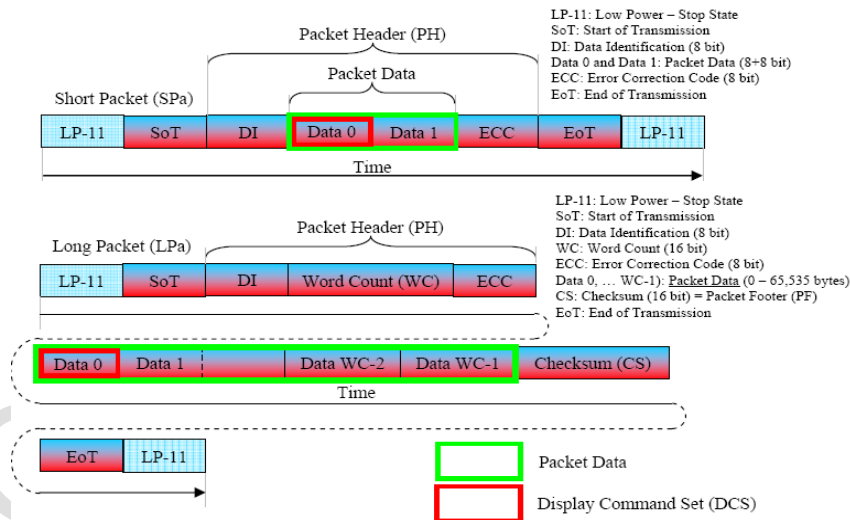


Figure 5-6 DCS on the short packet and long packet

#### Packet from the display module to the MCU

##### Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

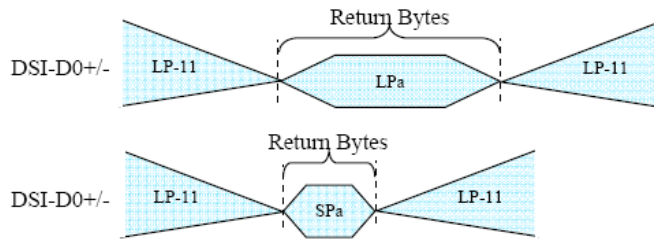
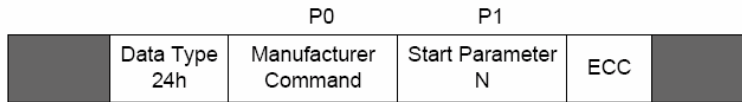


Figure 5-7 Return bytes on single packet

### 5.2.6 Customer-defined Generic Read Data Type Format

The short packet of Data Type 24h (Generic READ, 2 parameters) specifies the register content for read and the nth parameter that will begin reading. After Data Type 24h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

Packet Structure (processor → peripheral)



Low Power Data Transfer (peripheral → processor)

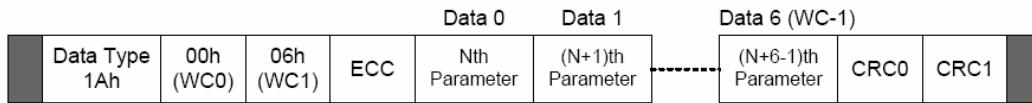
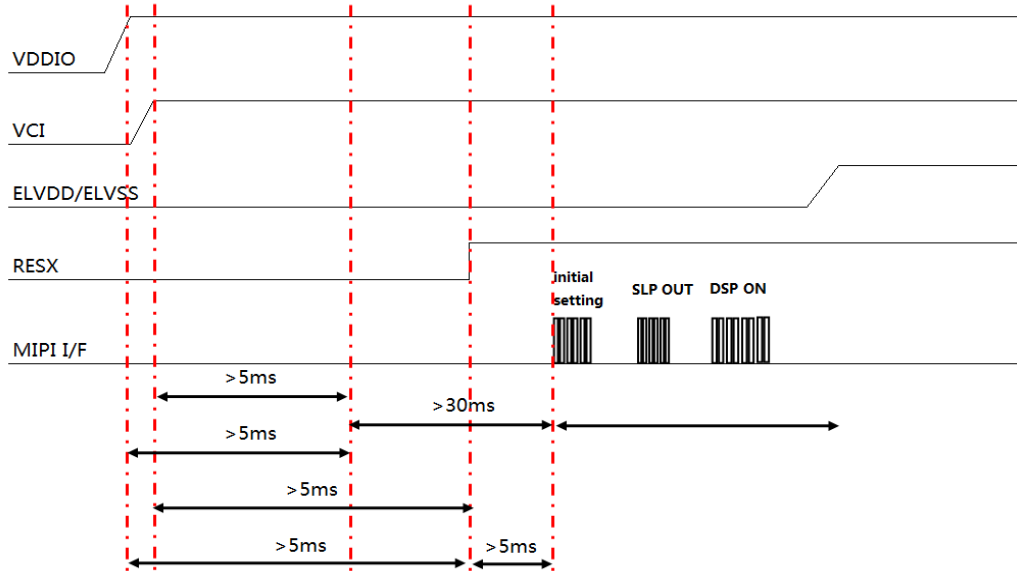


Figure 5-8 Generic read data type format

## 6 Recommended Operating Sequence

### 6.1 Display Power on / off Sequence

#### 6.1.1 Power On Sequence



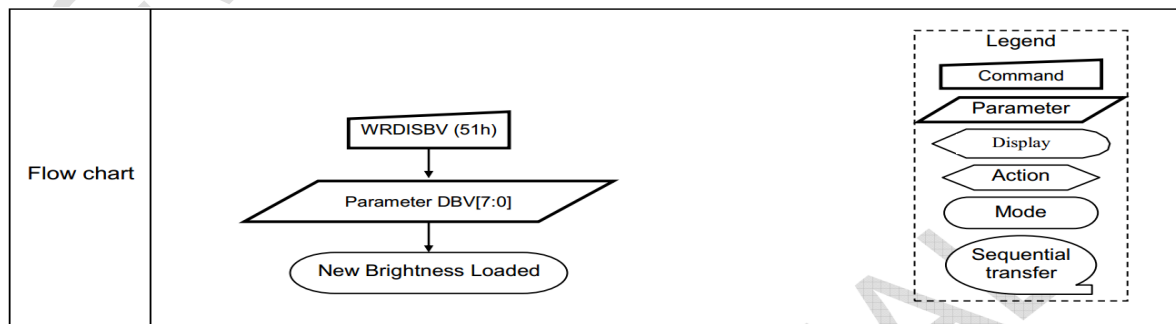
### 6.2 Display Initial code

TBD

### 6.3 Brightness control

**Use “command 5100h, data xxh” to adjust the Manual Brightness value of the display:** In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.

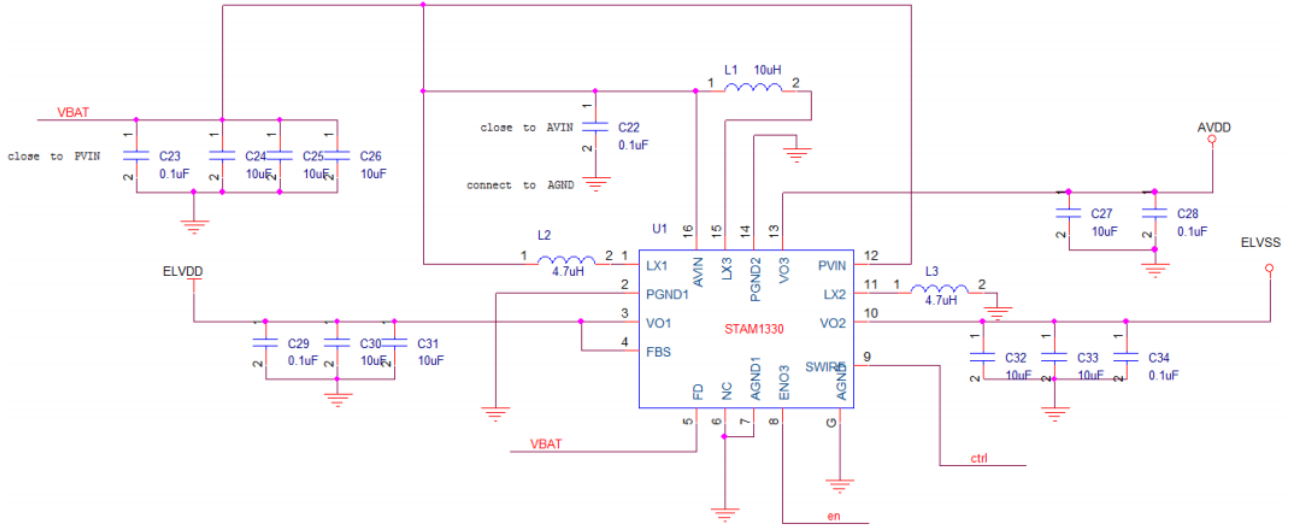
WRDISBV													
Inst/Para	R/W	Address		D15-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
		MIPI	Other										
WRDISBV	W	51h	5100h	x	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	FF





## 7 Application Circuit

ELVDD ELVSS & AVDD power supply schematic, The Triple DC/DC converter STAM1330 is recommended. The application schematics and external components are as below.



Component	Manufacturer	Part Number	Value	Size	Rating
C22 C23 C28 C29 C34	Samsung	CLO5B104KP5NNN	0.1uF	0402/1005	±10%, X7R, 10V
	Murata	GCM155R71A104KA55			
	TAIYO YUDEN	LMK105 B7104KV-F			
C24 C25 C26 C27 C30 C31 C32 C33	Samsung	CLO5A106MP5NUNC	10uF	0402/1005	±20%, X5R, 10V
	Murata	GRM155R61A106ME11			
	TDK	C1005X5R1A106MTT000E			
	TAIYO YUDEN	LDK105CB1106MVL			
L1	成育科技	ACDNR252010UP-100MT	10uH	2.5x2.0x1.0	20%, 0.65A, 570mΩ
L2 L3	成育科技	ACDNR252010UP-4R7MT	4.7uH	2.5x2.0x1.0	20%, 0.95A, 300mΩ
U1	ST	STAM1330	STAM1330	QFN16 (3.0x3.0)	



## 8 Optical Characteristics Optical Specification

Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angle	$\theta T$	CR $\geq$ 10	80	88		Degree	Note 2 Test Equipment: CS2000A
	$\theta B$		80	88			
	$\theta L$		80	88			
	$\theta R$		80	88			
Contrast Ratio	CR	$\theta=0^\circ$	10000				Note1 Note3 Test Equipment: CS2000A
Response Time	T <sub>ON</sub>	25°C				ms	Note1 Note4 Test Equipment: Admesy MSE
	T <sub>OFF</sub>				1		
Chromaticity	White	x	(0.270)	(0.300)	(0.330)	Test Equipment: CS2000A Note: Chromaticity can be modified according to customer demand	
		y	(0.280)	(0.310)	(0.340)		
	Red	x	(0.630)	(0.670)	(0.710)		
		y	(0.300)	(0.330)	(0.360)		
	Green	x	(0.170)	(0.220)	(0.270)		
		y	(0.660)	(0.710)	(0.760)		
	Blue	x	(0.110)	(0.140)	(0.170)		
		y	(0.030)	(0.060)	(0.090)		
Uniformity	U		75	80		%	Note1 Note6 luminance of center point is 350 $\pm$ 30nits Test Equipment: CS2000A
NTSC			90	100		%	Note5
Luminance	L		320	350	380	Cd/m <sup>2</sup>	Note1 Note7 Test Equipment: CS2000A
Cross-talk					3	%	Note8 L $\leq$ 350nits Test Equipment:

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							CS2000A
Gamma			1.9	2.2	2.5		Gamma=2.2±0.3 (L≤350nits) ; Gamma Self-adjustment (L>350nits) Test Equipment: CS2000A

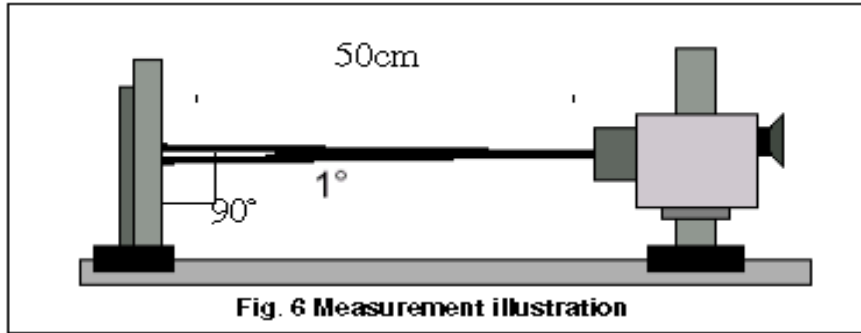
Test Conditions:

1. the ambient temperature is 25°C.
2. The test systems refer to Note1 and Note2.

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Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the AMOLED screen. All input terminals AMOLED panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

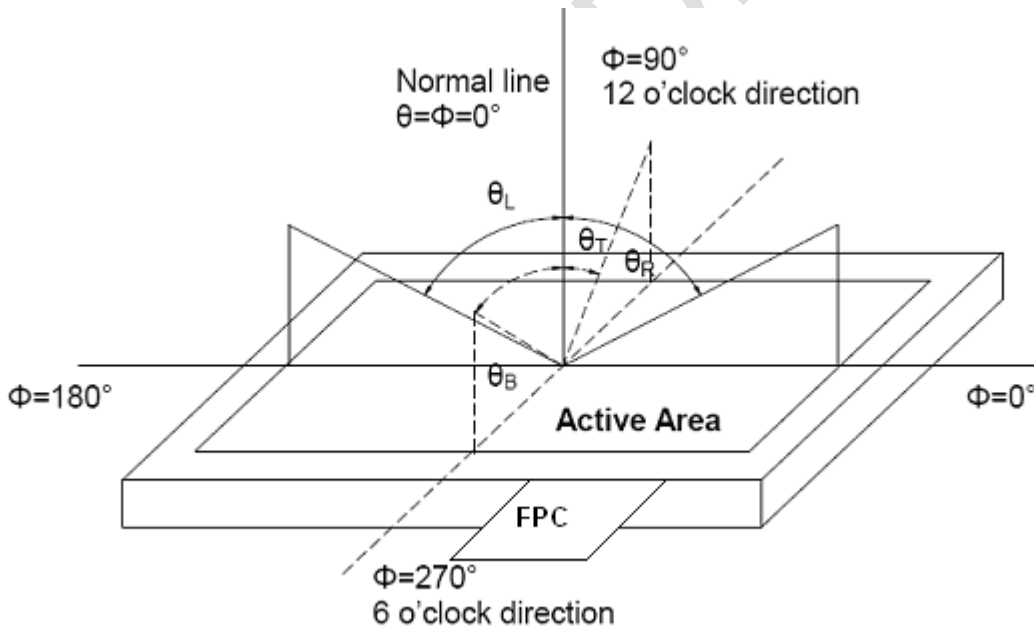


Fig. 1 Definition of viewing angle

Note 3: Definition of contrast ratio

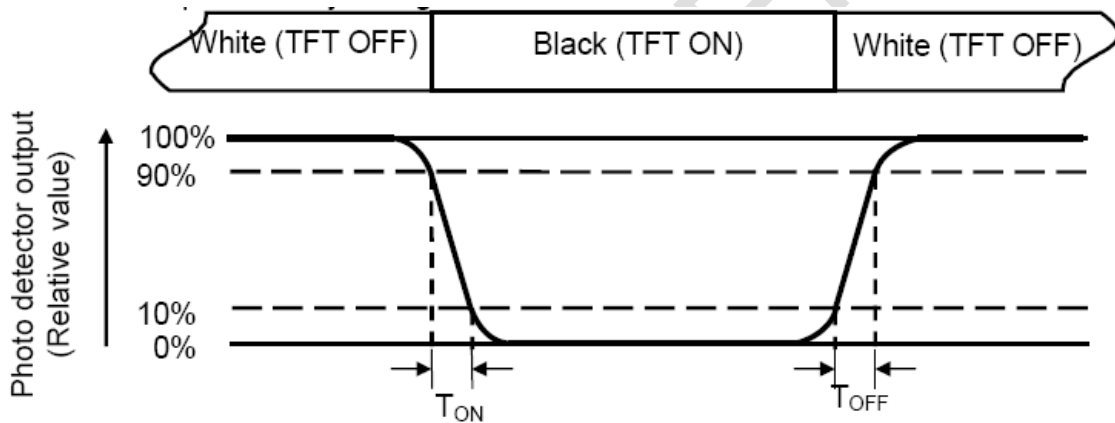
$$\text{Contrast ratio(CR)} = \frac{\text{Luminance measured when LCD is on the "white" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

“White state “: A state where the AMOLED should be driven by V<sub>white</sub>.

“Black state”: A state where the AMOLED should be driven by V<sub>black</sub>.

Note 4: Definition of response time

The response time is defined as the AMOLED optical switching time interval between “White” state and “Black” state. Rise time (T<sub>ON</sub>) is the time between photo detector output intensity changing from 90% to 10%. And fall time (T<sub>OFF</sub>) is the time between photo detector output intensity changing from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of AMOLED.

Note 6: Definition of luminance uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity}(U) = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width

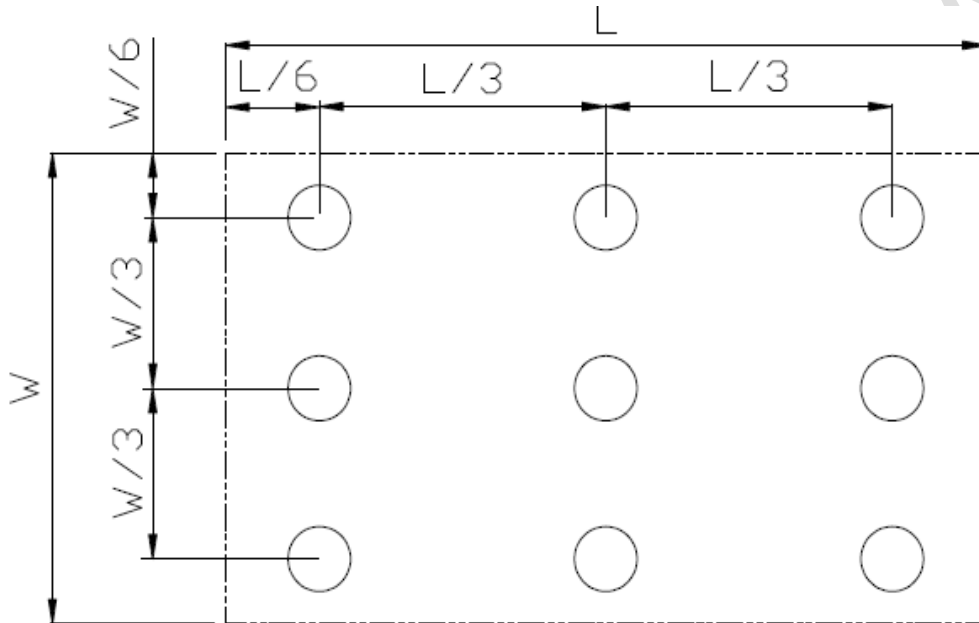


Fig. 2 Definition of uniformity

$L_{\max}$ : The measured maximum luminance of all measurement position.

$L_{\min}$ : The measured minimum luminance of all measurement position.

Note 7: Definition of luminance:

Measure the luminance of white state at center point.

Note 8: Cross Talk

A. Measure luminance at the position, P0.

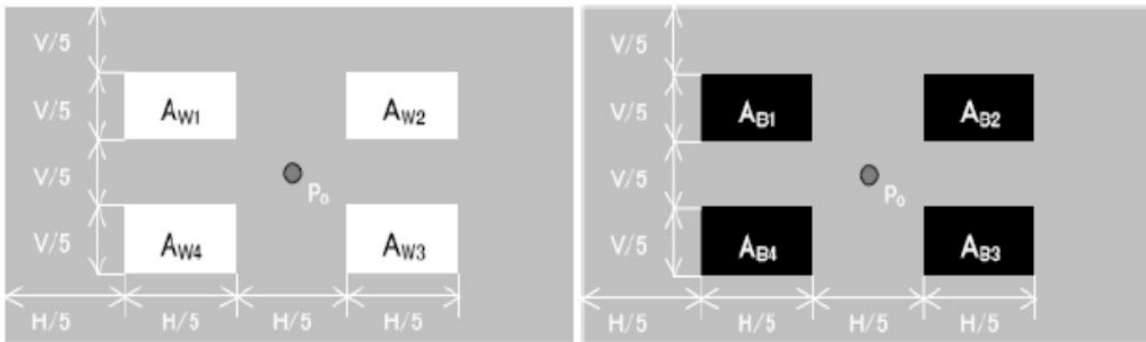
B. Calculate cross talk as below equation.

$$L_{W\_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

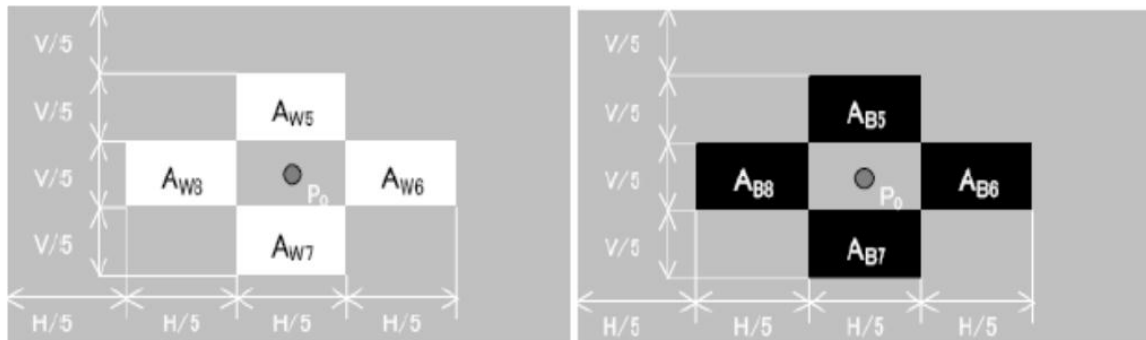
$$L_{B\_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$\text{crosstalk} = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \quad (i = 5 \text{ to } 8)$$

$$\text{crosstalk} = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \quad (i = 5 \text{ to } 8)$$

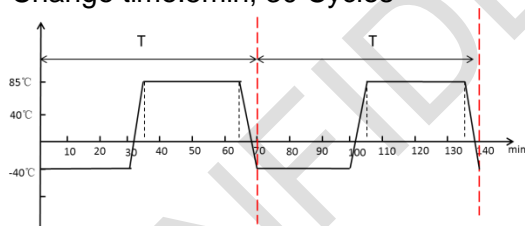
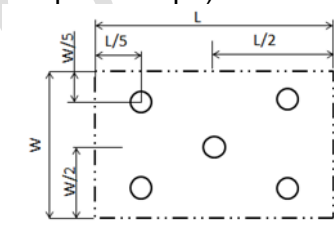


(a)  $L_{W\_OFF}$ ,  $L_{B\_OFF}$  measuring pattern



(b)  $L_{W\_ON}$ ,  $L_{B\_ON}$  measuring pattern

## 9 Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	+60°C, 120hrs	IEC60068-2-1,GB2423.2
2	Low Temperature Operation	-20°C, 120hrs	IEC60068-2-1 GB2423.1
3	High Temperature Storage	+70°C, 120hrs	IEC60068-2-1 GB2423.2
4	Low Temperature Storage	-30°C, 120hrs	IEC60068-2-1 GB2423.1
5	High Temperature & High Humidity Operation	60°C, 90% RH,120hrs	IEC60068-2-78 GB/T2423.3
6	Thermal Shock (Non-operation)	-40°C ( 30 min)~+85°C ( 30 min), Change time:5min, 30 Cycles 	Start with cold temperature, End with high temperature, IEC60068-2-14,GB2423.22
7	Electro Static Discharge (Operation)	C=150pF, R=330Ω, 5points/panel Air:±8KV, 5times; Contact:±4KV, 5 times; (Environment: 15°C~35°C, 30%~60%, 86Kpa~106Kpa). 	IEC61000-4-2 GB/T17626.2
8	Package Drop Test	1 corner, 3 edges, 6 surfaces Drop height:760mm	IEC60068-2-32 GB/T2423.8
9	Package Vibration Test	Random Vibration: 1.146Grms, 1~200Hz, Random, 30mins/(X, Y, Z)axis	IEC60068-2-34 GB/T2423.11

The above reliability verification brightness  $L \leq 350$ nits;





## 10 Quality Level

### 10.1 AMOLED Module of Characteristic Inspection

The environmental condition and visual inspection shall be conducted as below:

- (1) Ambient temperature:  $22 \pm 3^{\circ}\text{C}$
- (2) Humidity:  $55 \pm 10\% \text{RH}$
- (3) Ambient light intensity of visual inspection: 800 ~ 1200 lux
- (4) Ambient light intensity of function inspection:  $\leq 200 \text{lux}$
- (5) Viewing Distance:  $35 \pm 5 \text{cm}$
- (6) Viewing angle (tolerance): the front side  $90^{\circ} (\text{Z}) \pm 30^{\circ}$
- (7) Inspection time:  $10 \pm 2 \text{sec}$

### 10.2 Sampling Procedures for each item acceptance table

Defect type	Sampling Procedures	AQL
Major defect	GB/T2828.1-2003 Inspection level II normal inspection single sample inspection	0.65
Minor defect	GB/T2828.1-2003 Inspection level II normal inspection single sample inspection	1.0

Major defect:

Any defect may result in functional failure, or reduce the usability of product for its purpose. For example, electrical failure, deformation and etc.

Minor defect

A defect does not reduce the usability of product for its intended purpose and un-uniformity, such as dot defect and etc.

The criteria on major and/or minor judgment will be according with the classification of defects.

### 10.3 Inspection Item

No.	Item	Area	Criterion of Defect			Defect type
			Type	DS	Acceptable number	
1	Dot Defect	AA	Bright Dot	$\geq 10 \text{mm}$	0	Minor
			Dark Dot	$\geq 10 \text{mm}$	4	
			/			

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3	Abnormal Display	AA	/				Not allowed	Major
4	Normally white	AA	/				Not allowed	Major
5	Line Defect	AA	single line	Bright line		Not allowed	Major	
				Dark line		Not allowed		
			Multiple lines	Bright line		Not allowed		
				Dark line		Not allowed		
			Half-Line	Bright line		Not allowed		
				Dark line		Not allowed		
6	Mura	AA	Consulting Limit samples				Major	
7	Edge/Side breakage	OA	The following Criterion is applicable to any side (unit: mm)				Minor	
			type	Z	X	Y		
			/	$\leq T$	$\leq 2.0$	not extended to circuit Area		
						not extended to Frit		
8	Glass crack	AA、OA	/				Not allowed	Major
9	Panel Scratch	AA	W (mm)	L (mm)	DS (mm)	Acceptable number	Minor	
			$W \leq 0.03$	$L < 5.0$	$\geq 10$	Ignore		
			$0.03 < W \leq 0.05$	$L \leq 2.0$	$\geq 10$	Ignore		
				$2.0 < L \leq 5.0$	$\geq 10$	2		
			$0.05 < W$	-	0	0		
				$L > 5.0$	0	0		
		OA (not including Circuit Area)	W (mm)	L (mm)	DS (mm)	Acceptable number	Minor	
			$W \leq 0.03$	Ignore	$\geq 10$	Ignore		
			$0.03 < W \leq 0.05$	$L \leq 2.0$	$\geq 10$	Ignore		
				$2.0 < L \leq 5.0$	$\geq 10$	2		
			$0.05 < W$	-	0	0		
				$L > 5.0$	0	0		



		Circuit Area of OA	/			Not allowed	
10	Frit Encapsulation	FA	Frit width can't be less than the design width of 9/10, without bubble or breakage.				Minor
11	raised point	AA、OA	/			Not allowed	Major
12	Concave dot、Black and white dot、Polarizer Dent/Bubble	AA	Front (Encap surface)	D (mm)	DS (mm)	Acceptable number	Minor
				$D \leq 0.20$	$\geq 10$	Ignore	
				$0.20 < D \leq 0.50$	$\geq 10$	3	
			$0.50 < D$	$\geq 10$	0		
Rear (LTPS surface)	/	/	Ignore				
13	Polarizer Scratch/Fiber(Linear)	AA	W (mm)	L (mm)	DS	Acceptable number	Minor
			$W \leq 0.03$	Ignore	$\geq 10$	Ignore	
			$0.03 < W \leq 0.05$	$L \leq 2.0$	$\geq 10$	Ignore	
				$2.0 < L \leq 5.0$	$\geq 10$	3	
			$0.05 < W$	-	$\geq 10$	0	
				$L > 5.0$	$\geq 10$	0	
14	Panel dirt	AA	/	/	/	Not allowed	Minor
15	UV	Not IC side	Over coating			Not allowed	Minor
		IC side	The coating of IC side is not allowed higher than POL.				
16	Tuffy glue	IC and FPC bonding area	The coating is not allowed breakage or Bubble.				Major
		Other area	The coating is not allowed higher than POL.				Minor
			Tuffy glue is not allowed to interrupt and the diameter of Bubble is not more than 0.5mm.				
		The coating is not allowed higher than POL.					
		IC	Not allowed				
FPC	Ribbon glue: the width is not more than 1mm. Dot glue: the diameter is not more than 2mm.						
17	FPCA	FPC	The component should keep away from polarity opposition.				Major
			No wrong insertion				Major
			FPC should not have serious crease which destroy the line, prick and spots damage .Scratch is not allowed if Cu layer is exposed.				Minor



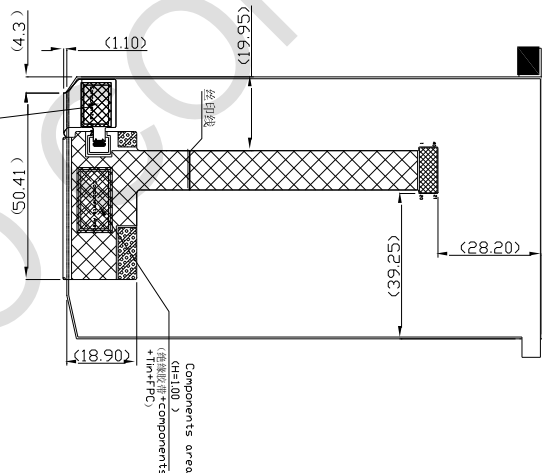
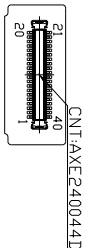
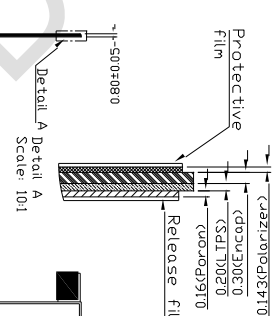
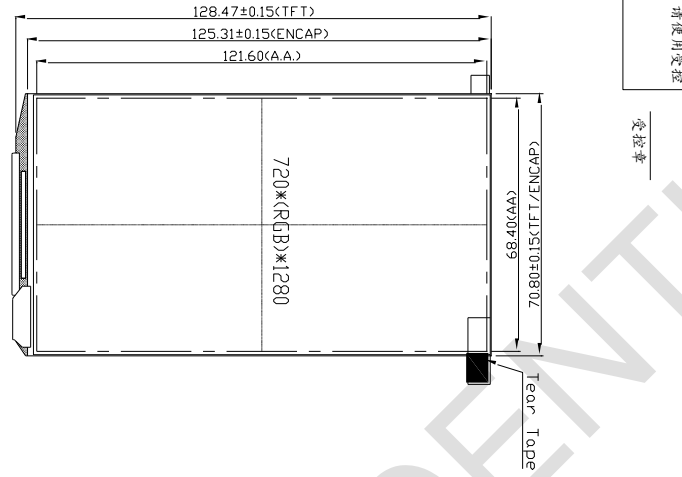
			The gold fingers should not be oxidized, scraped, folded, impressed, broken, spotted or dissymmetry.	Major
			Make sure FPC is not scalded, with its location holes not having deficiency or obviously shift.	Major
			The component of FPC should be the same as BOM list.	Major
			No remaining soldering Sn	Major
			No visual particle on the pad line	Minor
18	FPCA End Overhang	Bonding area	The size above 1/2 of soldering electrode of the parts overhang to the LAND is prohibited. (but contacting near other components is prohibited)	Major
19	FPCA Tilt Defect	Bonding area	Not allowed	Major
20	Package	other	Products should put into the anti-static trays, with non-overlapping, and the trays should be staggered placed.	Minor
			Different products cannot be mixed into the same inner package.	
			The package should not have obvious deformation, breakage, and the printing, labels type and quantity are correct.	
			The package should have QC signature. ROHS label is needed if the products under ROHS control.	



# 11 Mechanical Drawing

如本印章非红色，则表明该文件为非受控版本，不会受到控制和更新，请使用受控文件。  
分发号：

受控章



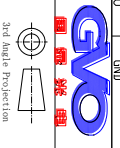
- NOTES:
1. Unspecified tolerance is ±0.2mm.
  2. Reference Dimension;
  3. \*Critical Dimension;
  4. Driver IC: RM67120;
  5. TP IC: G11151;
  6. 触控芯片需点胶 环氧树脂 黑色，高度不能超过IC;
  7. Connector type: AXE24004D;

视图B  
scale: 3:1

Rev.	Date	Notes
1	2016.02.18	Primary

Part Name	Module	Date	Rev.	Unit	Sheet
Project Code	G1549HD112GF	2016.02.18	01	mm	1/1
Part No.	G1549HD112GF-WA1-A	DES'D BY	CHK'D BY	CHK'D BY	APPROVED
		Liu renjie			

Pad No.	Pad Name
1	TP_BVDD
2	TP_AVDD
3	TP_SDA
4	TP_SCL
5	TP_INT
6	TP_RESET
7	SVREF
8	OLET1_EN
9	TE_OUT
10	VDDIO
11	AVDD_IN
12	VGI
13	RESX
14	MIP_PWR
15	LCN_I00
16	LCN_I00
17	NC
18	ELVDD
19	ELVDD
20	ELVDD
21	ELVSS
22	ELVSS
23	ELVSS
24	NC
25	GND
26	DP2
27	DP1
28	GND
29	DP2
30	DP1
31	GND
32	CGP
33	GN1
34	GND
35	DP2
36	DP1
37	GND
38	DP2
39	DP1
40	GND

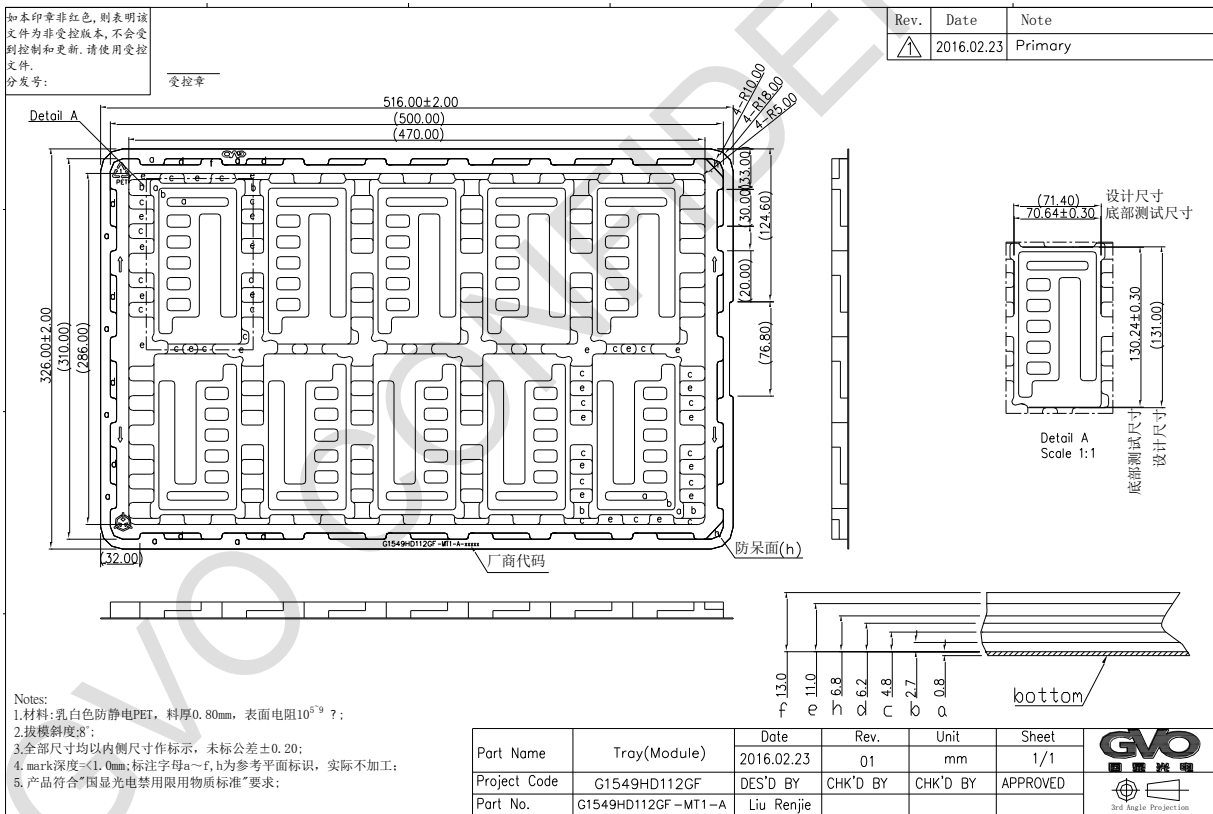


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### Packing Drawing

Packing Condition	Contents
Packing Type	TRAY + Carton packing type
TRAY material model	tray (10 <sup>5</sup> ~10 <sup>9</sup> Ω)
Tray packing type	See the picture 1
Number of panels per tray	10 pieces
Number of Tray per carton	19units (( 18 units + 1 empty)PET tray )
Number of panels per carton	180 pieces



Picture 1



## 12 Precautions for Use of AMOLED Modules

### 12.1 Handling Precautions:

- 12.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from height.
- 12.1.2 Do not press down the screen or the adjoining areas too hard because-the color tone may be shifted).
- 12.1.3 The polarizer covering the display surface of the AMOLED module is soft and easily scratched. Handle this polarizer carefully.
- 12.1.4 If the display surface is contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear, moisten the cloth with ethyl alcohol.
- 12.1.5 Solvents may damage the polarizer. Do not use water、ketone or aromatic solvents except ethyl alcohol.  
Do not attempt to disassemble the AMOLED Module.
- 12.1.6 If the logic circuit power is off, do not apply the input signals.
- 12.1.7 To prevent destruction from static electricity, be careful to maintain an optimum working environment.
- 12.1.8 Be sure to make yourself in contact with the ground when handling with the AMOLED Modules.
- 12.1.9 Tools required for assembly, such as soldering irons, must be properly ground.
- 12.1.10 To reduce the generation of static electricity, do not conduct assembly or other work under dry conditions.
- 12.1.11 To protect the display surface, the AMOLED Module is coated with a film. Be careful when peeling off this protective film, because static electricity may generate.

### 12.2 Storage Precautions:

- 12.2.1 When storing the AMOLED modules, be sure that they are not directly exposed to the sunlight or the light of fluorescent lamps.
- 12.2.2 The AMOLED modules should be stored under the storage temperature range. If the AMOLED modules will be stored for a long time, the recommended condition is:  
Temperature: 0°C~40°C Relatively humidity: ≤80%
- 12.2.3 The AMOLED modules should be stored in the room without acid, alkali or harmful gas.

### 12.3 Transportation Precautions:

- 12.3.1 The AMOLED modules should not be suffered from falling and violent shocking during transportation. Besides, excessive press, water, damp and sunshine, should be avoided.