(V) Preliminary Specifications
( ) Final Specifications

Module	**15.6" (15.55) HD 16:9 Color TFT-LCD with *LED Backlight* design**
Model Name	**G156XTN02.1**

Customer	**Date**	**Approved by**	**Date**
		Sean Lin	2018/06/30
Checked & Approved by		**Prepared by**	
		Sandy Su	2018/06/30
Customer's sign back page		General Display Business Unit / AU Optronics corporation	

2. General Description

G156XTN02.1 is a Color Active Matrix Liquid Crystal Display composed of a TFT-LCD display, a driver circuit, and LED backlight system. The screen format is intended to support 16:9 HD, 1366(H) x768(V) screen and 262k colors (RGB 6-bits data driver) with LED backlight driving circuit. All input signals are eDP (Embedded DisplayPort) interface compatible.
G156XTN02.1 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

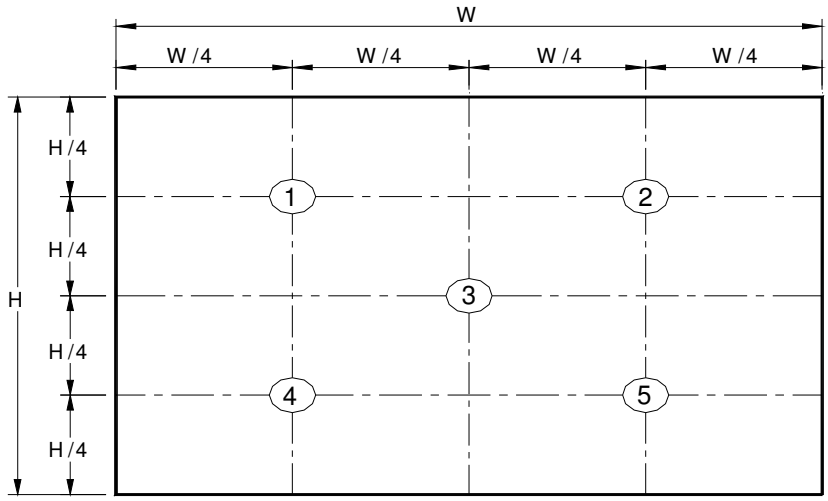
Items	Unit	Specifications
Screen Diagonal	[mm]	15.6” (15.55)
Active Area	[mm]	344.23 x193.54
Pixels H x V		1366x3(RGB) x 768
Pixel Pitch	[mm]	0.252X0.252
Pixel Format		R.G.B. Vertical Stripe
Display Mode		TN,Normally White
Nominal Input Voltage VDD	[Volt]	3.3 (Typ.)
Power Consumption	[Watt]	**3.97** (Include Logic and BLU Power) (TBD)
Weight	[Grams]	380 Max.
Physical Size	[mm]	359.5 (H)(Typ.) x 223.8 (V)(Typ.) x 3.3 (T)(Max.)(Panel)
Electrical Interface		eDP1.2
Surface Treatment		Anti Glare, hardness 3H
Color Gamut	[%]	45 (Typ.)
Support Color		262K colors (RGB 6-bit)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 0 to +50 -20 to +60
RoHS Compliance		RoHS Compliance

2.2 Optical Characteristics

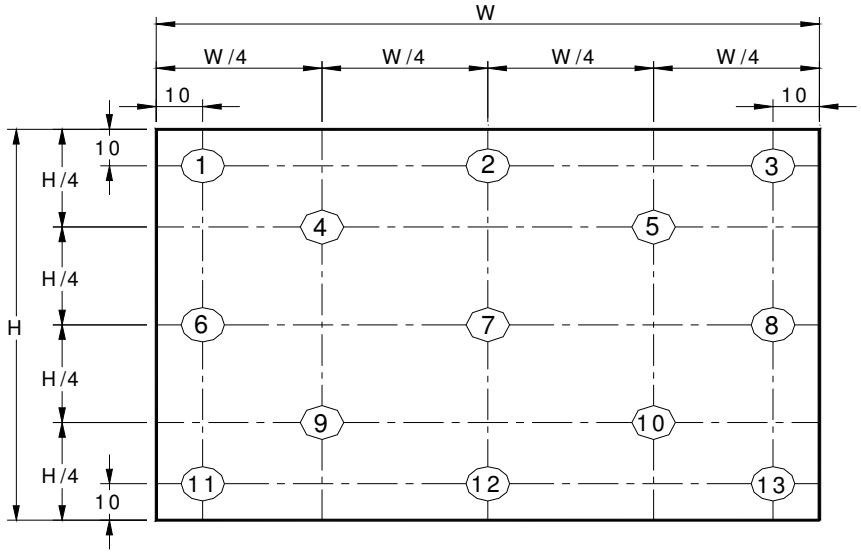
The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item		Symbol	Conditions	Min.	Typ.	Max.	Note
White Luminance		[cd/m2]	I_{LED}= 23 mA (center point)	212	250	-	1, 4, 5.
Uniformity		%	5 points	75	80		2,3
Luminance Uniformity			5 points			1.25	1, 3, 4
			13 points			1.60	2, 3, 4
Contrast Ratio				400	600	-	4,6
Response Time		[msec]	Raising + Falling	-	8	16	
Viewing Angle		[degree]	Horizontal (Right) CR = 10 (Left)	TBD TBD	80 80	- -	4,9
		[degree]	Vertical (Upper) CR = 10 (Lower)	TBD TBD	55 70	- -	
Color/ Chromaticity Coordinates	Red	Rx	(CIE 1931)	TBD	TBD	TBD	4 Note: LGP material is PMMA
		Ry		TBD	TBD	TBD	
	Green	Gx		TBD	TBD	TBD	
		Gy		TBD	TBD	TBD	
	Blue	Bx		TBD	TBD	TBD	
		By		TBD	TBD	TBD	
	White	Wx		0.255	0.285	0.315	
		Wy		0.263	0.293	0.323	

Note 1: 5 points position (Ref: Active area)



Note 2: 13 points position (Ref: Active area)



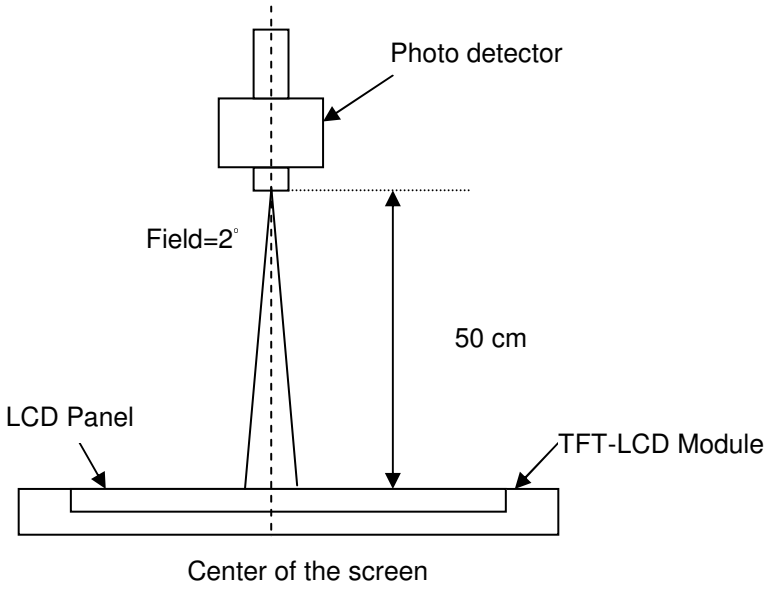
Note 3: The luminance uniformity of 5 or13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



Note 5 : Definition of Average Luminance of White (Y_L):

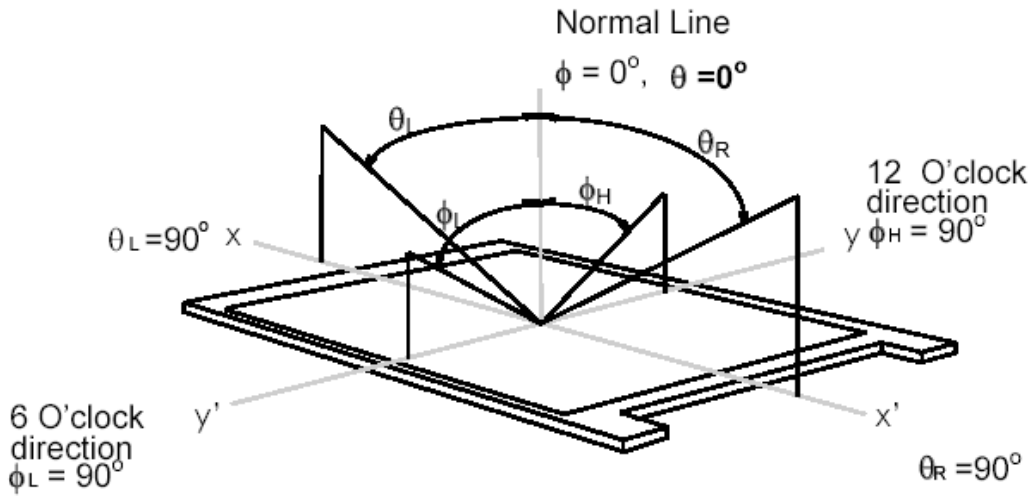
Measure the luminance of gray level 63 at 5 points，Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5
L (x) is corresponding to the luminance of the point X at Figure in Note (1).

Note 6 : Definition of contrast ratio (CR):
Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

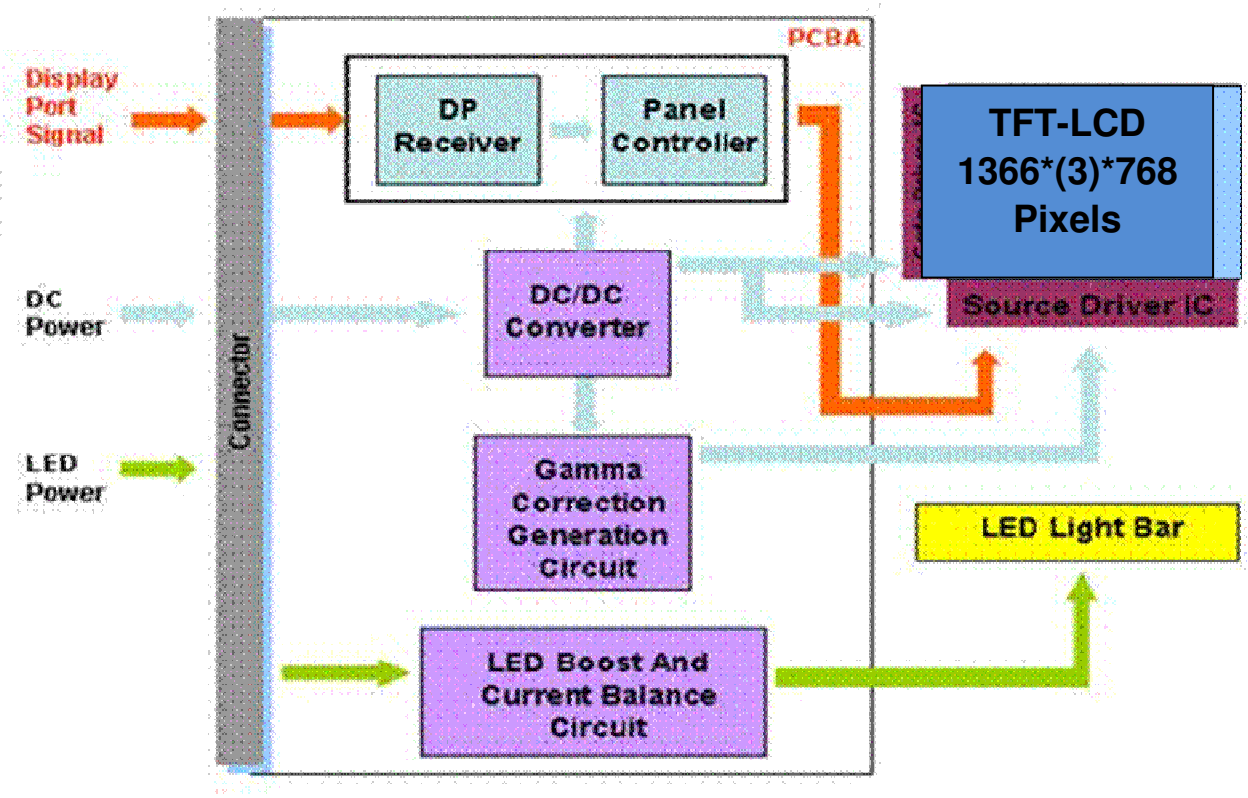
Note 7: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 15.6 inches wide Color TFT/LCD 30 Pin.



4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

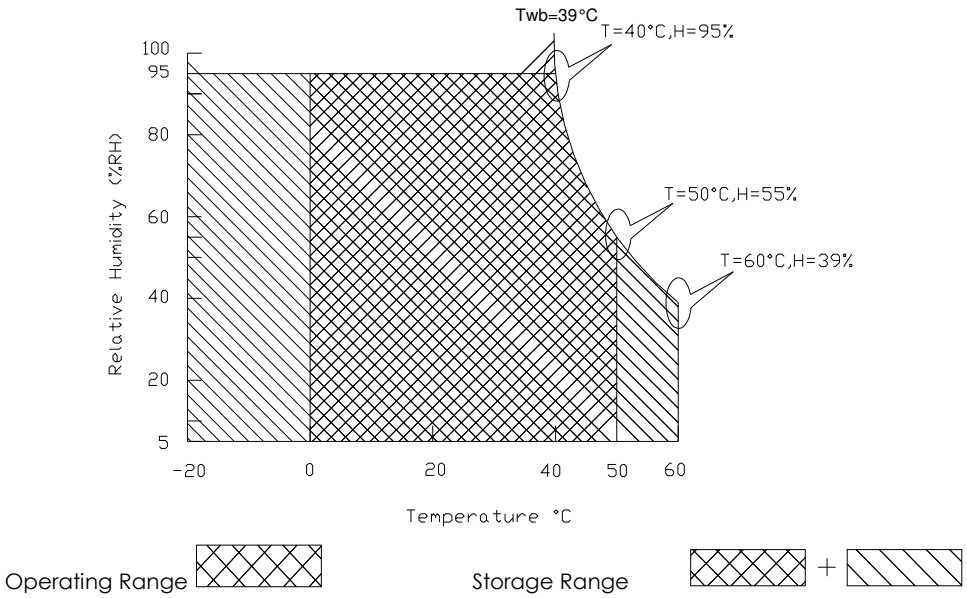
Item	Symbol	Min	Max	Unit	Conditions
Operating	TOP	0	+50	[°C]	Note 4
Storage Temperature	TST	-20	+60	[°C]	Note 4

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: LED specification refer to section 5.2

Note 4: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



5. Electrical Characteristics

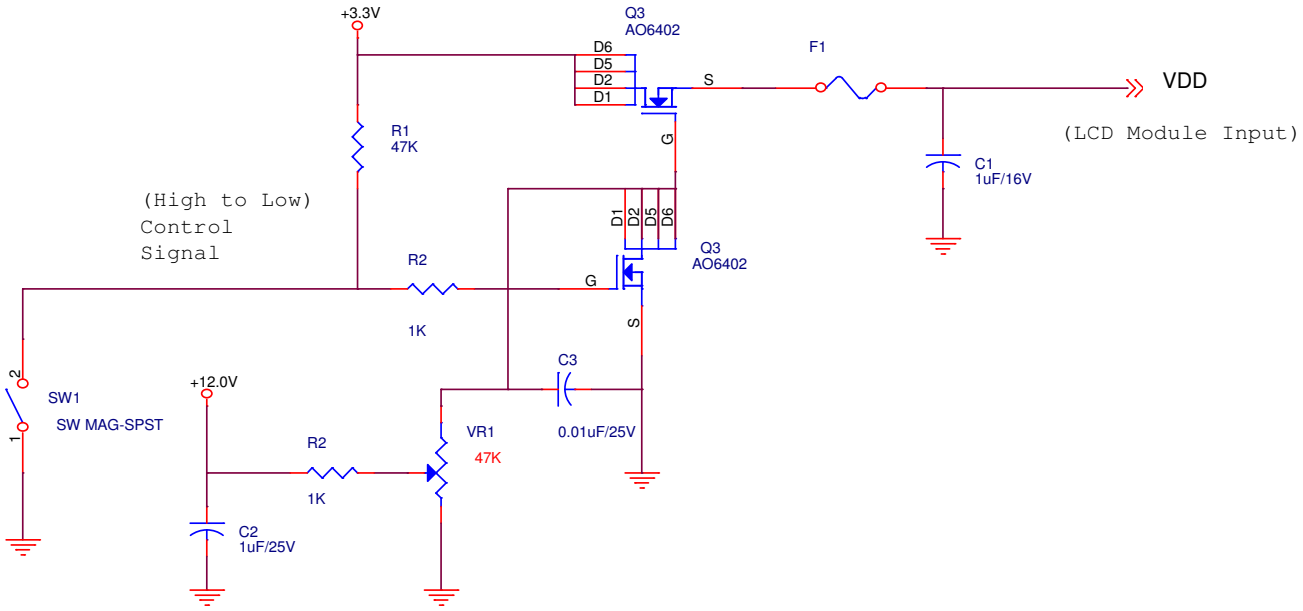
5.1 TFT LCD Module

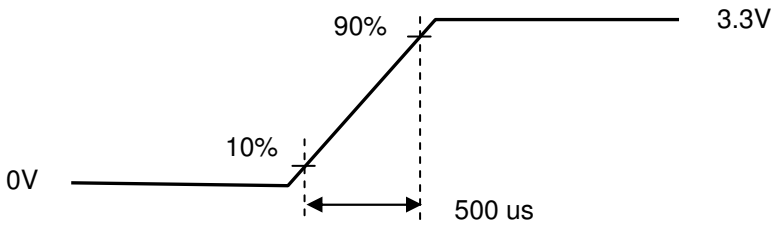
5.1.1 Power Specification

Input power specifications are as follows;
The power specification are measured under 25℃ and frame frenquency under 60Hz.

Symbol	Parameter	Min	Typ	Max	Units	Remark
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	0.85	[Watt]	Note 1
IDD	IDD Current	-	-	260	[mA]	Note 1
Irush	LCD Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：Black Pattern at 3.3V driving voltage. (Pmax=V3.3 x Iblack)
Note 2 : Measure Condition



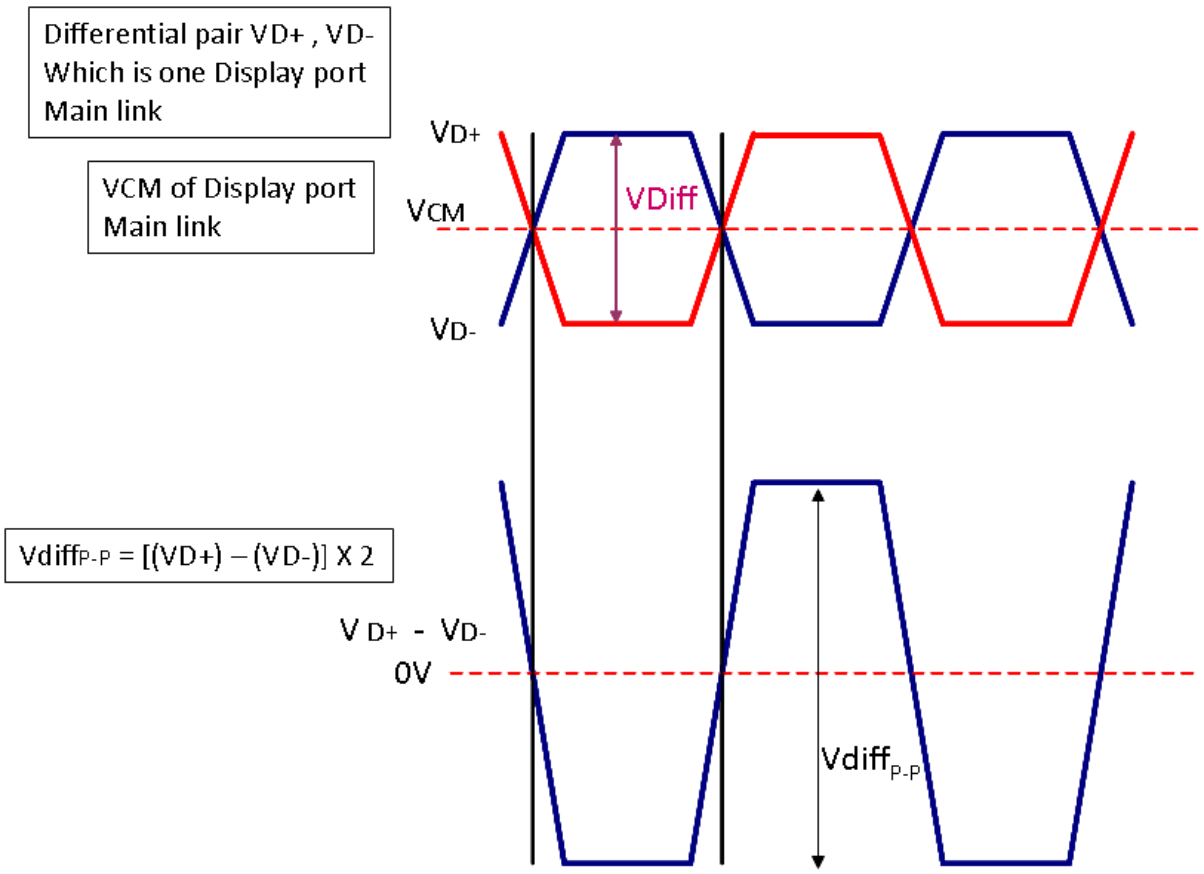


VDD rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.
Signal electrical characteristics are as follows;

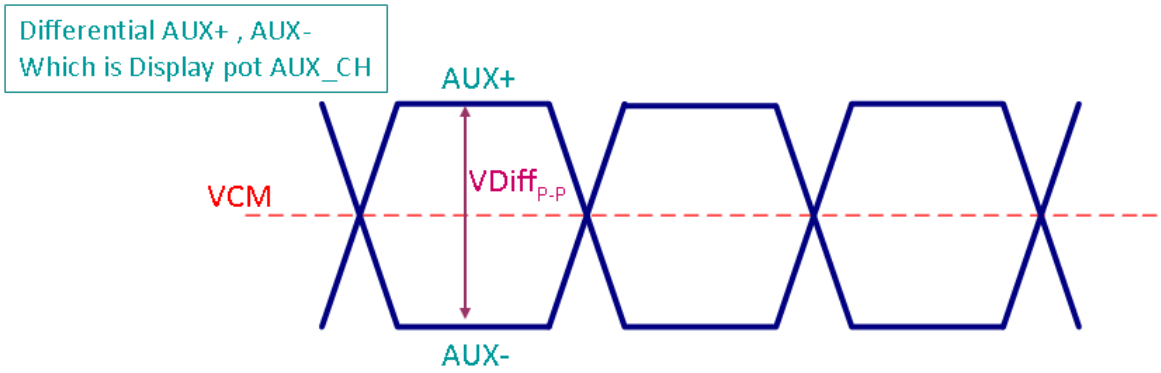
Display Port main link signal:



Display port main link					
		Min	**Typ**	**Max**	**unit**
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Folow as VESA display port standard V1.1a

Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
VDiff$_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

Follow as VESA display port standard V1.1a.

Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

Follow as VESA display port standard V1.1a.

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	3.12	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 IF= 23 mA

Note 1: Calculator value for reference PLED= VF(Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous

5.2.2 Backlight input signal characteristics

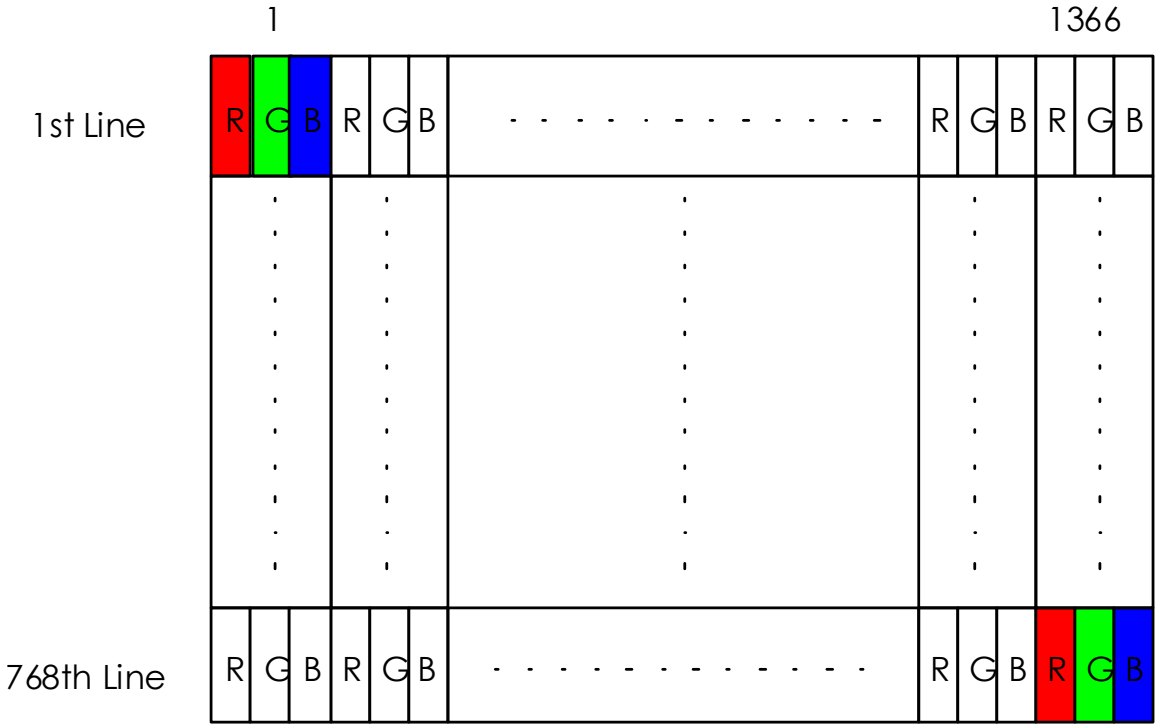
Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	5.0	12.0	21.0	[Volt]	Define as Connector Interface (Ta=25℃)
LED Enable Input High Level	VLED_EN *Note 1	2.5	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.6	[Volt]	
PWM Logic Input High Level	VPWM_EN *Note 1	2.5	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.6	[Volt]	
PWM Input Frequency	FPWM	200	1K	10k	Hz	
PWM Duty Ratio	Duty	5	--	100	%	

Note 1 : Recommanded system pull up/down resistor no bigger than 10kohm.

6. Signal Characteristic

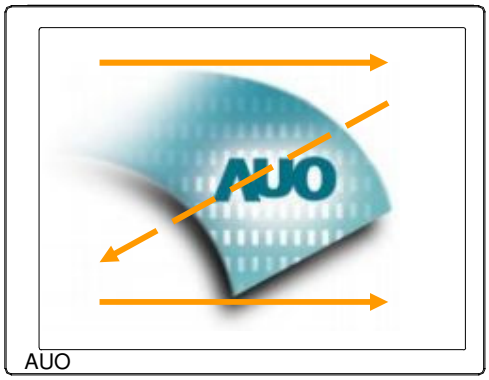
6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Scanning Direction

The following figures show the image seen from the front view. The arrow indicates the direction of scan.



6.3 Integration Interface Requirement

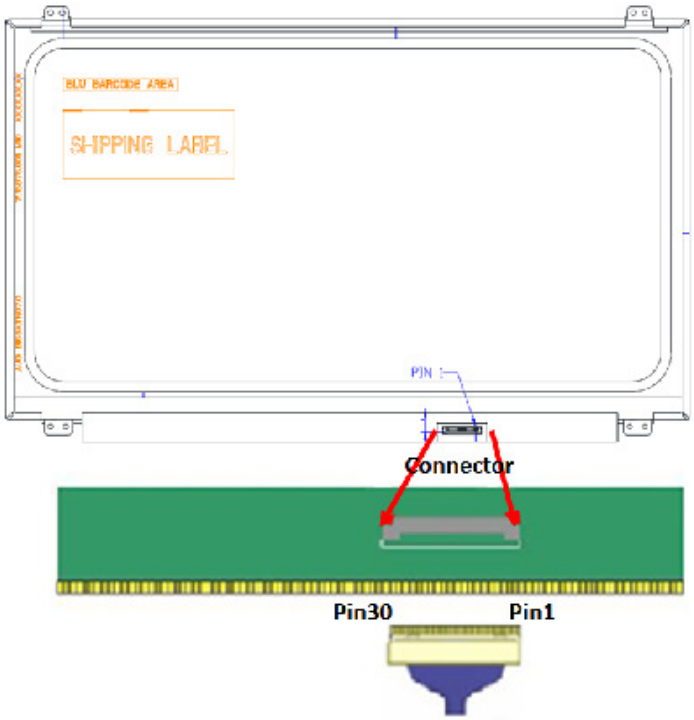
6.3.1 Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

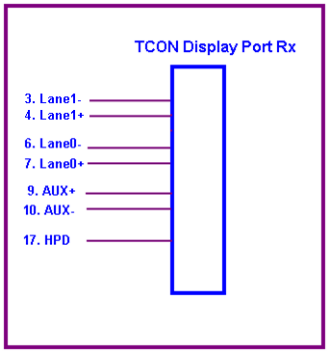
Connector Name / Designation	For Signal Connector
Manufacturer	JAE or Compatible
Type / Part Number	JAE HD2S030HA1 or Compatible
Mating Housing/Part Number	IPEX 20645-030T-01 or Compatible

6.3.2 Connector Illustration



Note1: Start from right side.

Note2: Input signals shall be low or High-impedance state when VDD is off.
Internal circuit of **eDP inputs** are as following.



6.3.4 Pin Assignment

eDP lane is a differential signal technology for LCD interface and high speed data transfer device.

PIN NO	Symbol	Function
1	NC	NC
2	H_GND	High Speed Ground
3	NC	NC
4	NC	NC
5	H_GND	High Speed Ground
6	Lane0_N	Comp Signal Link Lane 0
7	Lane0_P	True Signal Link Lane 0
8	H_GND	High Speed Ground
9	AUX_CH_P	True Signal Auxiliary Ch.
10	AUX_CH_N	Comp Signal Auxiliary Ch.
11	H_GND	High Speed Ground
12	LCD_VCC	LCD logic and driver power
13	LCD_VCC	LCD logic and driver power
14	BIST	LCD Panel Self Test Enable
15	LCD GND	LCD logic and driver ground
16	LCD GND	LCD logic and driver ground
17	HPD	HPD signal pin
18	BL_GND	Backlight ground
19	BL_GND	Backlight ground
20	BL_GND	Backlight ground
21	BL_GND	Backlight ground
22	BL_Enable	Backlight ground
23	BL PWM DIM	System PWM signal Input
24	NC	NC
25	NC	NC
26	BL_PWR	Backlight power
27	BL_PWR	Backlight power
28	BL_PWR	Backlight power
29	BL_PWR	Backlight power
30	NC	No Connect

6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1366x768 /60Hz manufacturing guide line timing.

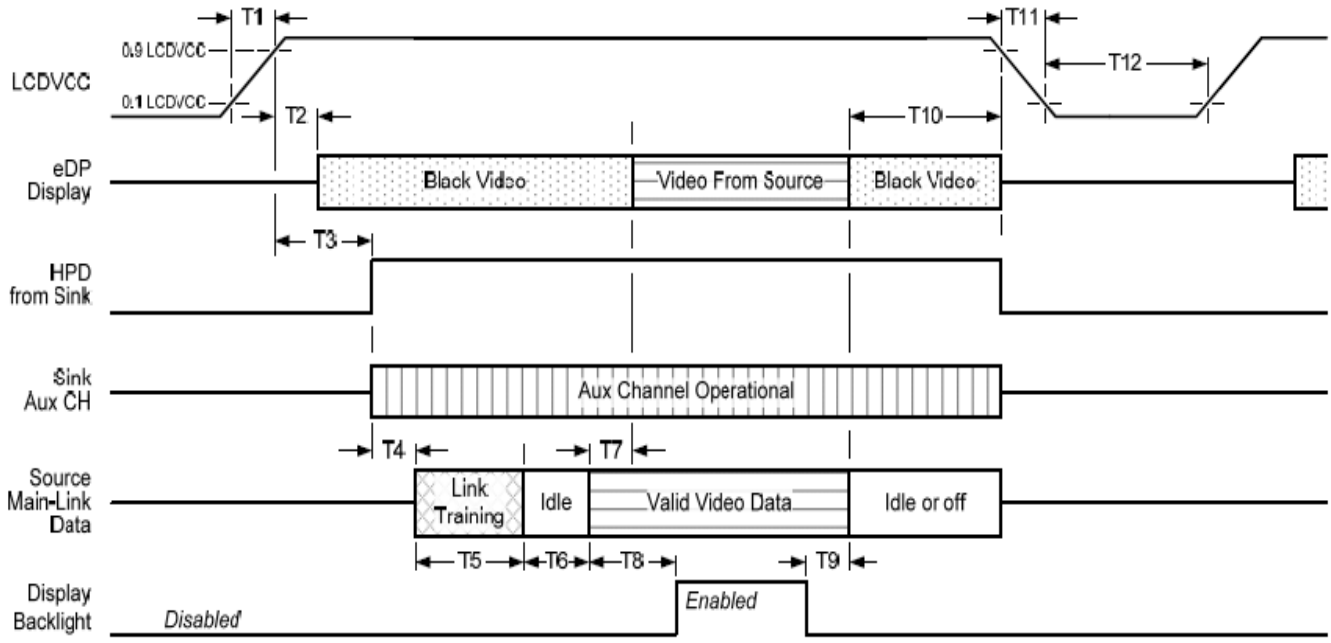
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	48	60	-	Hz
Clock frequency		$1/T_{Clock}$	65	76.3	80	MHz
Vertical Section	Period	T_V	790	816	768+A	T_{Line}
	Active	T_{VD}	768			
	Blanking	T_{VB}	22	48	A	
Horizontal Section	Period	T_H	1500	1558	1366+B	T_{Clock}
	Active	T_{HD}	1366			
	Blanking	T_{HB}	144	192	B	

Note 1 : The above is as optimized setting

Note 2 : The maximum clock frequency = (1366+B)*(768+A)*60<80MHz

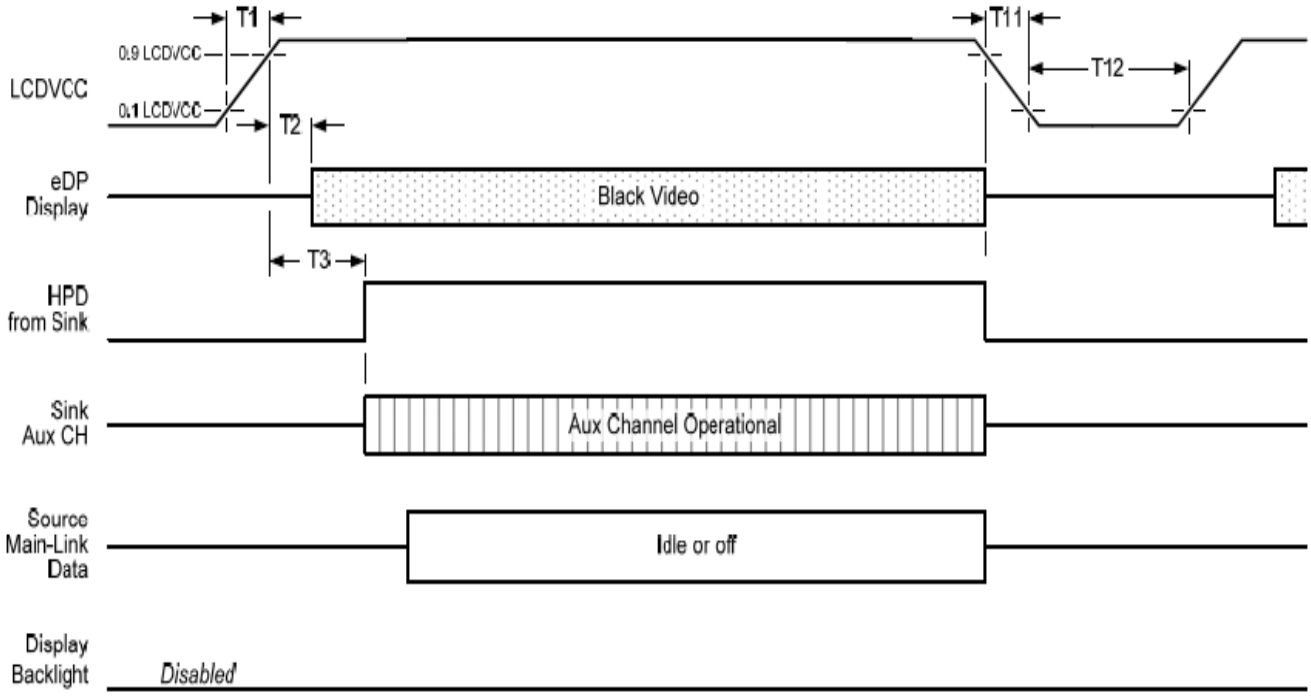
6.5 Power ON/OFF Sequence

Display Port panel power sequence:



Display port interface power up/down sequence, normal system operation

Display Port AUX_CH transaction only:



Display port interface power up/down sequence, AUX_CH transaction only

Display Port panel power sequence timing parameter:

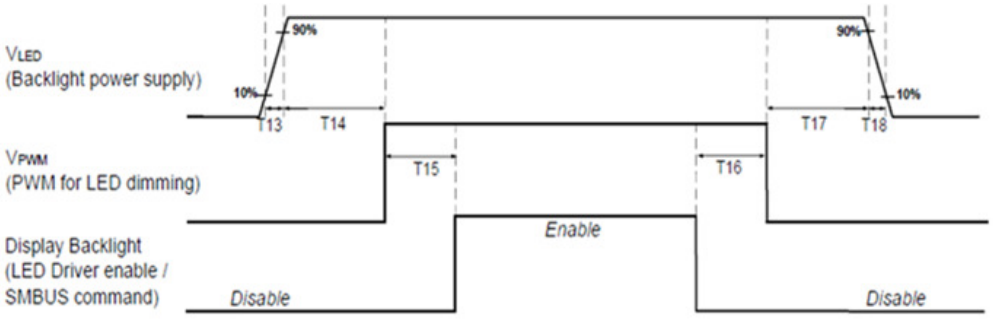
Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	300ms			sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol.
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source	100ms			source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 905 to 10%	source			10ms	
T12	power off time	source	150ms			

Note1: The sink must include the ability to generate black video autonomously. The sink must automatically enable black video under the following conditions:
-upon LCDVDD power on (with in T2 max)-when the "Novideostream_Flag" (VB-ID Bit 3) is received from the source (at the end of T9).
-when no main link data, or invalid video data, is received from the source. Black video must be displayed within 64ms (typ) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The sink may implement the ability to disable the black video function, as described in Note 1, above, for system development and debugging purpose.

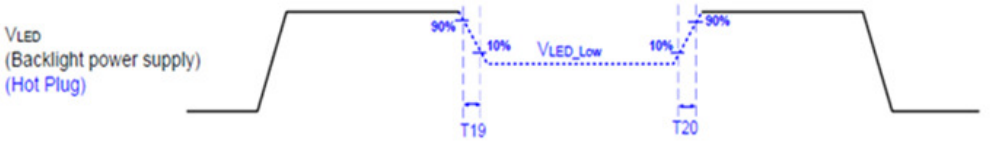
Note 3: The sink must support AUX_CH polling by the source immediately following LCDVDD power on without causing damage to the sink device (the source can re-try if the sink is not ready). The sink must be able to respond to an AUX_CH transaction with the time specified within T3 max.

Display Port panel B/L power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.



7. Reliability Test Criteria

Items	Required Condition	Note
High Temperature Operation	Ta= 50℃, Dry, 300h	
Low Temperature Operation	Ta= 0℃, 300h	
High Temperature Storage	Ta= 60℃, 35%RH, 300h	
Low Temperature Storage	Ta= -20℃, 50%RH, 250h	
Temperature Humidity Bias	Ta= 40℃, 90%RH, 300h	
Thermal Shock Test	Ta=-20℃to 60℃, Duration at 30 min, 100 cycles	
ESD	Contact Discharge = ± 8 kV, class B (R=330,C=150pF) Air Discharge = ± 15 kV, class B (R=330,C=150pF) 1sec, 9 points, 25 times/point	Note 1
Vibration Test	1.5G frequency=10～500[Hz] XYZ each direction 30min./cycle	
Shock Test	Peak acceleration 220G 2ms sign wave XYZ each direction 3sets	

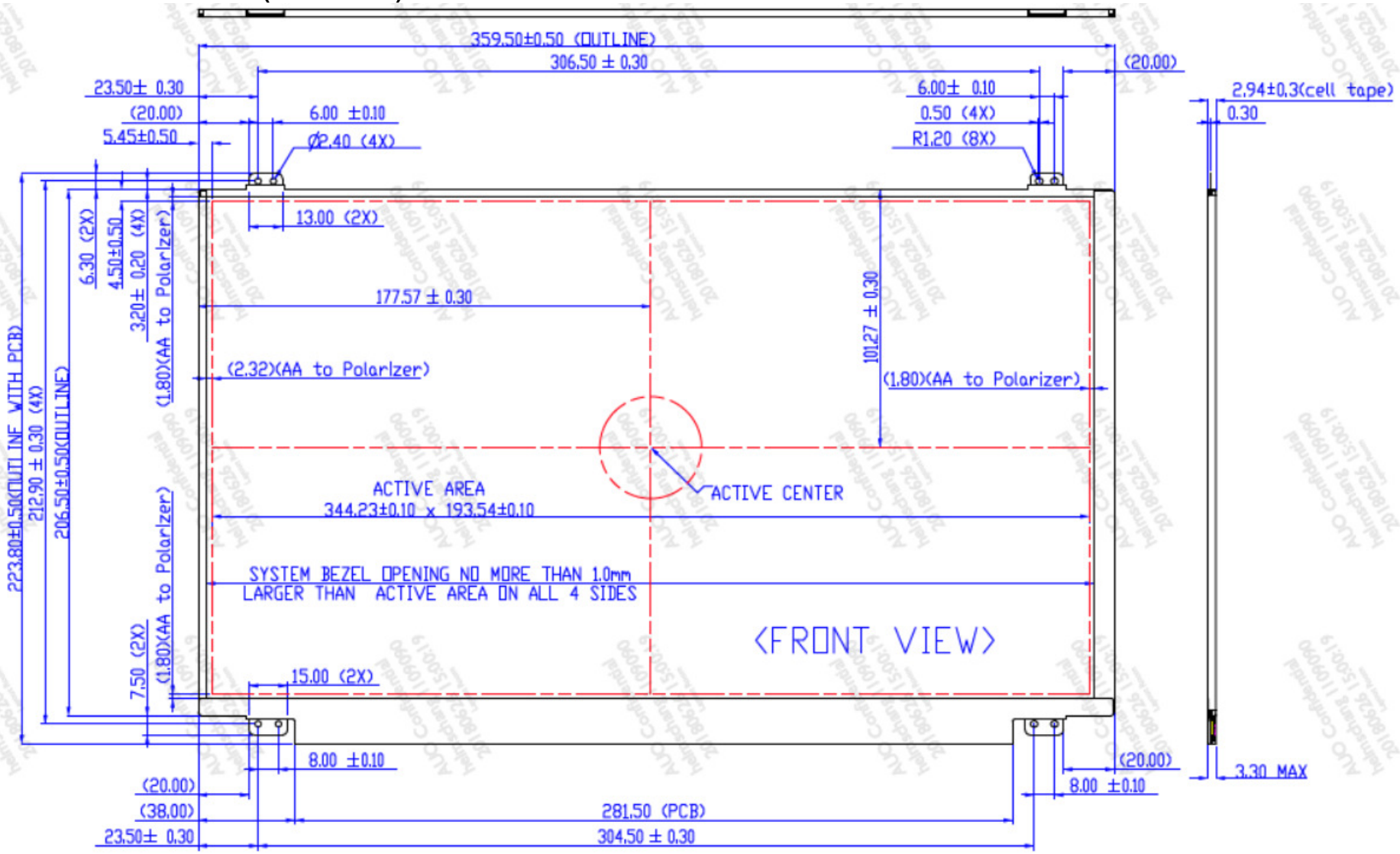
Note1: According to EN 61000-4-2, ESD class B: Some performance degradation allowed. Self-recoverable. No data lost, No hardware failures. Mura shall be ignored after high temperature reliability test.

Note2:

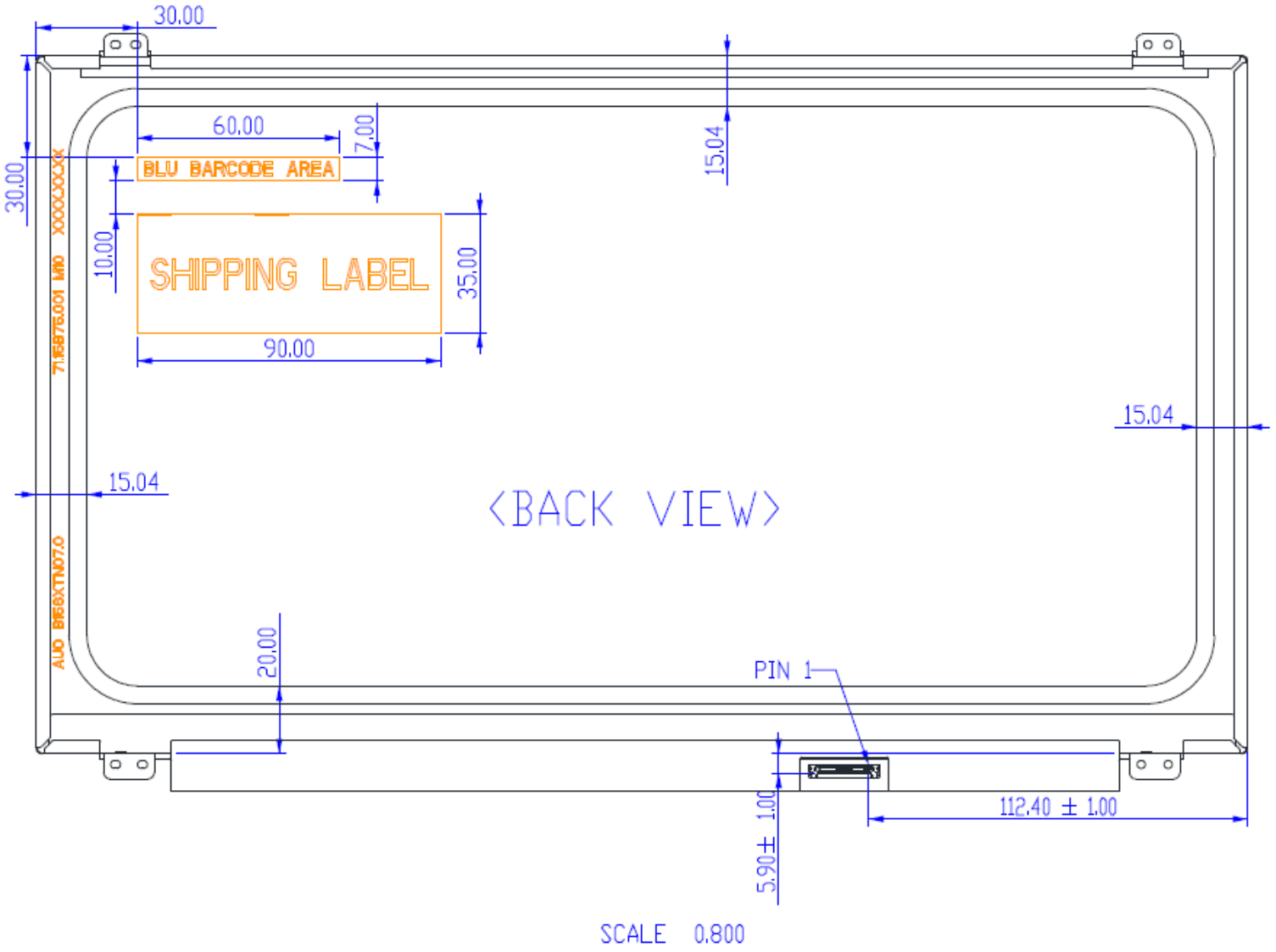
- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability. No function failure occurs. Mura shall be ignored after high temperature reliability test.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.

8. Mechanical Characteristics

8.1 LCM Outline Dimension (Front View)

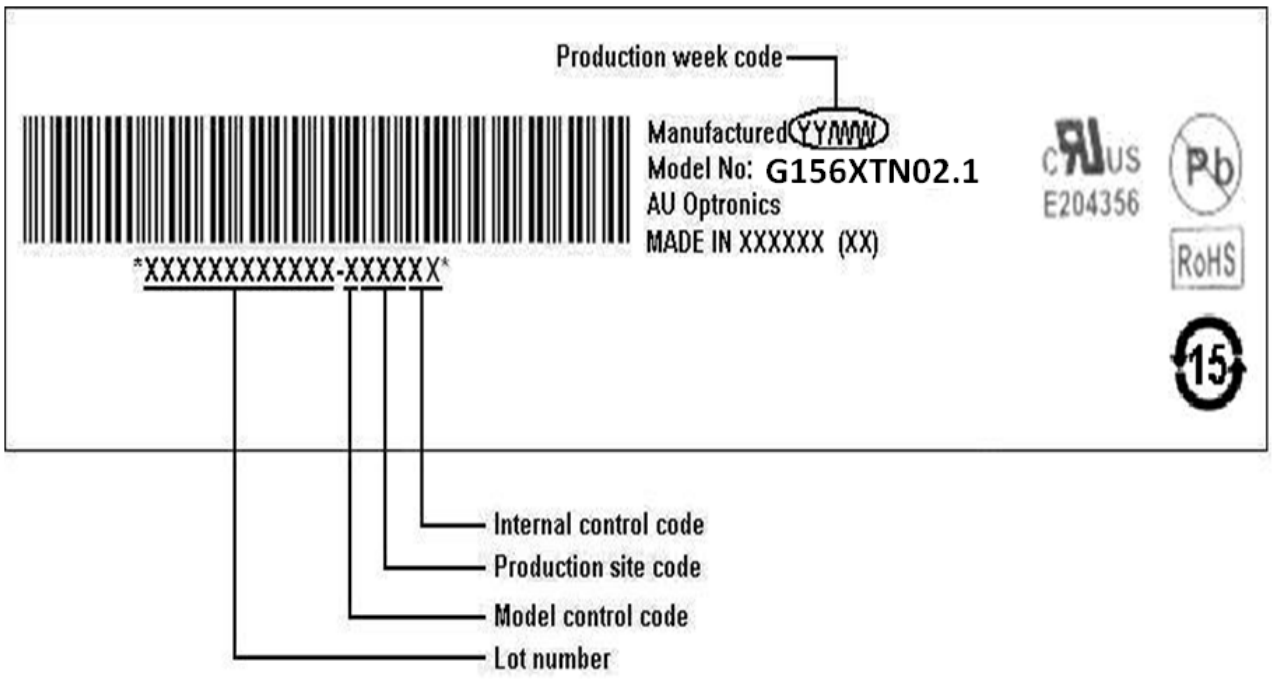


8.2 LCM Outline Dimension (Rear View)



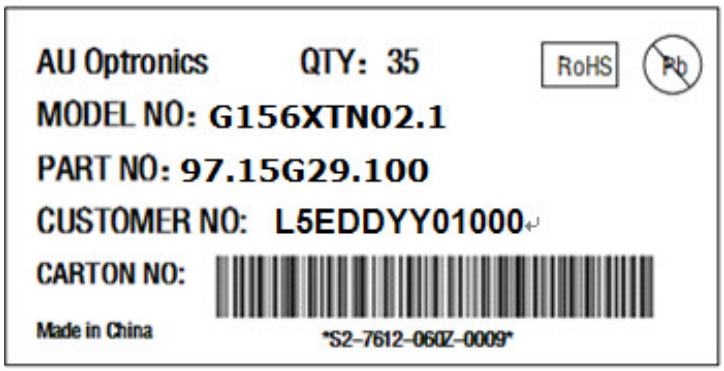
9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

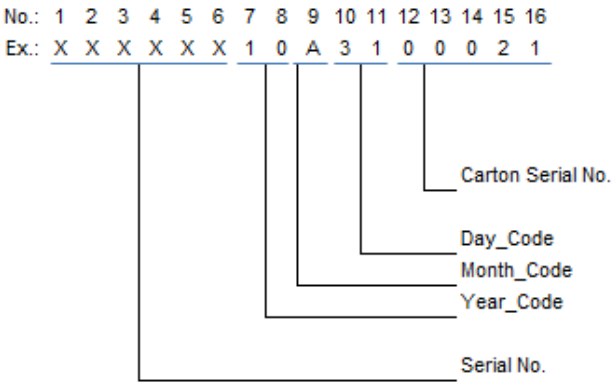


9.2 Carton Label and Package

9.2.1 Carton Label Format

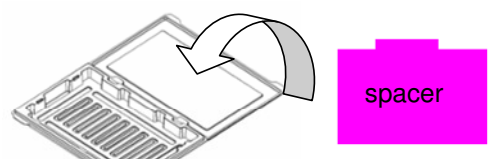


Carton number description:



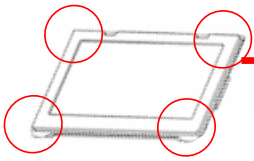
9.3 Carton Package

1. The yellow tape posted on the lower right corner.



2. Put 1Pcs EPE Spacer into Tray and put 1pcs panel on First Spacer.

1 Pcs Tray contained 6pcs Panel +6pcs Spacer



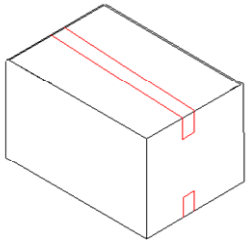
3. Cover the tray box and check corner are tight .

4. Direction according to arrow put in box

6. Cover the EPS box

7. Insert the package from the sideway of the Antistatic Bag.

8. Placing trays into carton



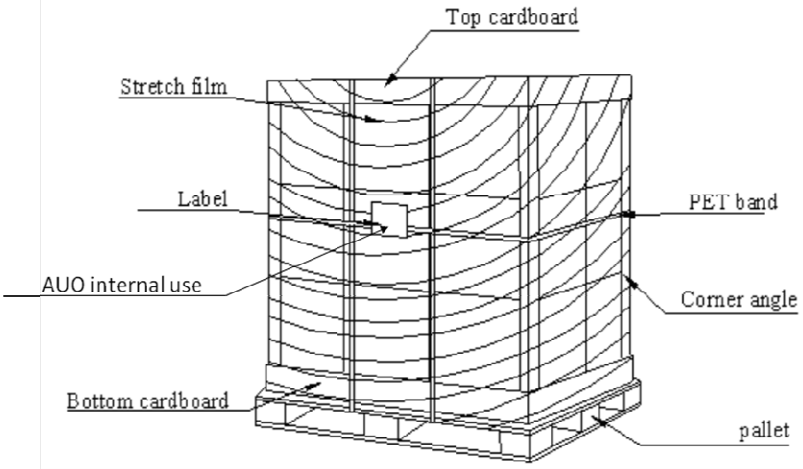
9. Sealing the carton with packing tape

9.4 Shipping Package of Palletizing Sequence

Max capacity：48pcs TFT-LCD module per carton
Max weight: 19.4 kg per carton
Outside dimension of carton: 480*370*335mm
Pallet size：1150*980*132mm

Box stacked

Module by air：(3*2) * 4 layers，one pallet put 24 boxes，total 1152 pcs module
Module by sea：(3*2) * 4 layers + (3*2) * 1 layers， two pallet put 30 boxes，total 1440 pcs module
Module by sea_HQ：(3*2) * 4 layers + (3*2) * 2 layers, two pallet put 36 boxes，total 1728 pcs module



Note: Palletizing label is AUO internal use(Internal use not for customer)

Item		Specification			Remark
		Q'ty	Dimension	Weight (Kg)	
I	Panel	I	359.5(H) × 206.5(V) × 2.94(D)	0.35	*Note I*
3	EPS Box	1	465(L)mm x 355(W)mm x 318(H)mm	0.45	without Panel & cushion *Note 1*
4	Packing Box	13 pcs/Box	480(L)mm x 370(W)mm x 335(H)mm	18.12	with panel & cushion *Note 1*
5	Pallet	1	1150(L)mm x 980 (W)mm x 132(H)mm	15	*Note 1*
6	Pallet after Packing	24boxes/pallet	1150(L)mm x 1070(W)mm x 1212(H)mm	434.8	*Note 1*

Note 1: Estimated value which is subject to change based on real measured data.

10. Safety

10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

10.2 Materials

10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

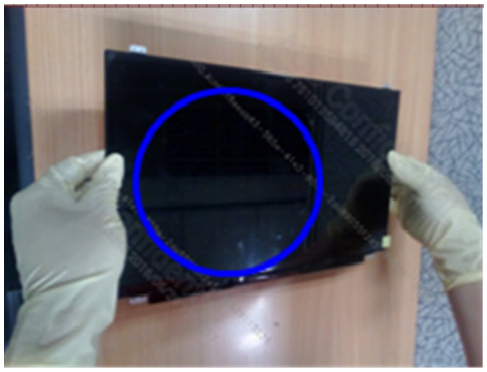
UL 60950-1, Second Edition U.S.A. Information Technology Equipment

11. Handling guide

This is a thin and slim LCD model, and please be cautious when pulling it out of package or assembling it onto platform. Careless handlings, e.g. twist, bending, pressing, or collision, will result malfunction of LCD models.

(1) Handling method notice

Do not lift and hold the panel with single hand at right or left side from Tray.



Lift and hold the panel up with both hands from tray.

(2) On the table notice

Do not press edge of panel to avoid glass broken.

Do not press the surface of the panel to avoid the glass broken or polarizer scratch.


Do not put anything or tool on the panel to avoid the glass broken or polarizer scratch.

(3) Cable assembly notice

Do not insert the connector with single hand and touching the PCBA.

Insert the connector by pushing right and left edge.

12. Appendix: EDID Description (TBD: Update after ES2)

Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	EC	11101100	236	
0B	hex, LSB first	21	00100001	33	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	00	00000000	0	
11	Year of manufacture	1C	00011100	28	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	04	00000100	4	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	95	10010101	149	
15	**Max H image size** *(rounded to cm)*	22	00100010	34	
16	**Max V image size** *(rounded to cm)*	13	00010011	19	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	02	00000010	2	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	50	01010000	80	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	25	00100101	37	
1B	Red x **(Upper 8 bits)**	93	10010011	147	
1C	Red y/ highER 8 bits	58	01011000	88	
1D	Green x	57	01010111	87	
1E	Green y	92	10010010	146	
1F	Blue x	29	00101001	41	
20	Blue y	22	00100010	34	

21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	CE	11001110	206	
37	Pixel Clock/10000 USB	1D	00011101	29	
38	Horz active **Lower 8bits**	56	01010110	86	
39	Horz blanking **Lower 8bits**	C0	11000000	192	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80	
3B	Vertical Active **Lower 8bits**	00	00000000	0	
3C	Vertical Blanking **Lower 8bits**	30	00110000	48	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48	
3E	HorzSync. Offset	08	00001000	8	
3F	HorzSync.Width	0A	00001010	10	
40	VertSync.Offset : VertSync.Width	31	00110001	49	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	58	01011000	88	
43	Vertical Image Size **Lower 8bits**	C1	11000001	193	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	

47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	
5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	

6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	47	01000111	71	G
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	35	00110101	53	5
74	Manufacture P/N	36	00110110	54	6
75	Manufacture P/N	58	01011000	88	X
76	Manufacture P/N	54	01010100	84	T
77	Manufacture P/N	4E	01001110	78	N
78	Manufacture P/N	30	00110000	48	0
79	Manufacture P/N	32	00110010	50	2
7A	Manufacture P/N	2E	00101110	46	.
7B	Manufacture P/N	31	00110001	49	1
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	60	01100000	96	