

DDR Termination Regulator

Features

- Support DDR I (1.25 V_{TT}), DDR II (0.9 V_{TT}), DDR III (0.75 V_{TT}), DDR III_L (0.675V_{TT}) and DDR IV (0.6 V_{TT}) Requirements
- VCNTL Supply Voltage: 3V to 5.5V
- Termination Supply Voltage : 1.2V to 3.6V
- Stable with Output Ceramic Capacitor
- Over Current Protection
- Thermal Shutdown Protection
- Shutdown Function for STR (S3) Mode
- Adjustable Output Voltage with Resistors
- Built-In Soft-Start
- Power MOS integrated
- SOP-8 (FD) and MSOP-8 (FD) Package
- RoHS Compliant

Applications

- DDR I/II/III/III_L/IV Memory Termination
- SSTL_3, SSTL_2, SSTL_18, SSTL_15
- Notebook/Desktop/Server
- Telecom/Datacom, GSM Base Station, LCD-TV/PDP-TV, Copier/Printer, Set-Top Box

General Description

The G2987 is a linear regulator designed to meet the JEDEC SSTL (Series Stub Termination Logic) specifications in DDR I/II/III/III_L/IV –SDRAM systems. It provides accurate and fast response with up to 1.8A source/sink ability in load transient to track reference voltage. The terminated voltage can be generated by two external resistors or programmed by forcing VREF pin at a desired voltage. Also the G2987 operate in low power consumption as low as 0.7mA and it has a shutdown function by setting VREF lower than 0.15V then the V_{TT} is turned off and discharged via an internal MOSFET. This function obtains low quiescent current as 50μA for STR mode.

Ordering Information

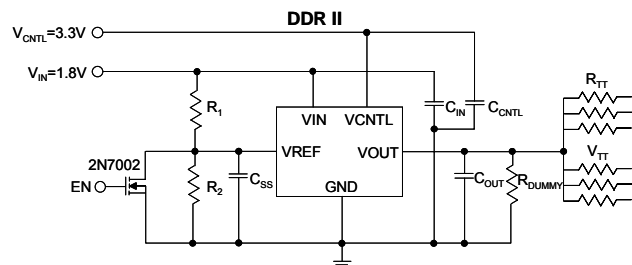
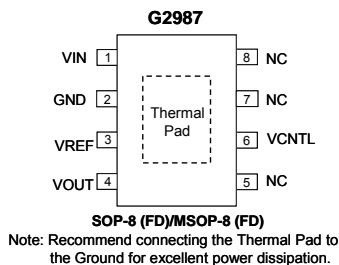
ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2987F11U	G2987	-40°C~85°C	SOP-8 (FD)
G2987F51U	G2987	-40°C~85°C	MSOP-8 (FD)

Note: F1: SOP-8 (FD) F5: MSOP-8 (FD)

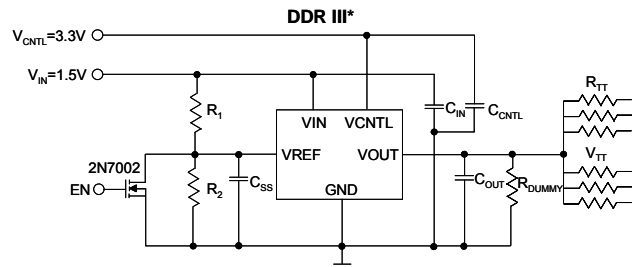
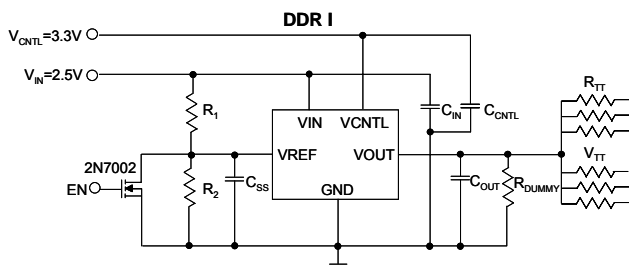
1: Bonding Code

U : Tape & Reel

Pin Configuration



Typical Application Circuit



* Recommended V_{CTRL} = 3.3V