DDR I/II Termination Regulator

Features

- **Operation Supply Voltage: 1.6V to 5.5V**
- **Low Supply Current: 280µA @ 2.5V**
- **Low Output Offset**
- **Source and Sink Current**
- **Low External Component Count**
- **No Inductor Required**
- **No external Resistors Required**
- **Thermal Shutdown Protection**
- **Suspend to RAM (STR) function**
- **SOP-8 with Power-Pad package**

Applications

- **DDR-SDRAM Termination Voltage**
- **DDR-I / DDR-II Termination Voltage**
- **SSTL-2**
- **SSTL-3**

General Description

The G2996 is a linear regulator designed to meet the JEDEC SSTL-18 ,SSTL-2 and SSTL-3 (Series Stub Termination Logic) specifications for termination of DDR-SDRAM. It contains a high-speed operational amplifier that provides excellent response to the load transients. This device can deliver 1.5A/0.9A continuous current and transient peaks up to 3A/1.8A in the application as required for DDRI/II-SDRAM termination. With an independent V_{SENSE} pin, the G2996 can provide superior load regulation. The G2996 provides a V_{REF} output as the reference for the applications of the chipset and DIMMs.

The G2996 can easily provide the accurate V_{TT} and V_{REF} voltages without external resistors that PCB areas can be reduced. The quiescent current is as low as 280µA @ 2.5V. So the power consumption can meet the low power consumption applications.

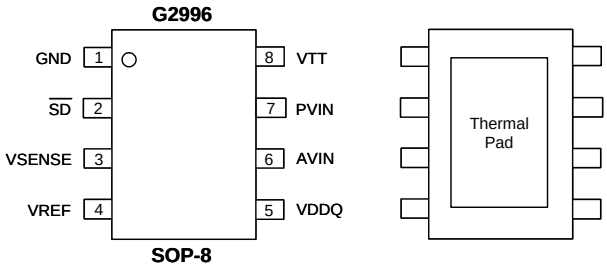
The G2996 also has an active low shutdown ($\overline{SD}$) pin that provides Suspend to RAM (STR) functionality. When $\overline{SD}$ is pulled low, the V_{TT} output will be tri-state providing a high impendence, but V_{REF} will remain active. A power saving advantage can be obtained in this mode through lowering the quiescent current to180µA @ 2.5V.

Ordering Information

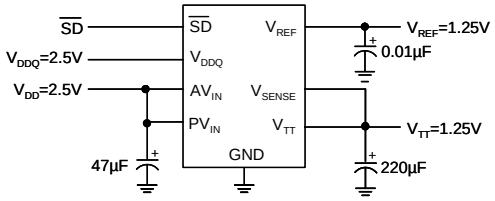
ORDER NUMBER	ORDER NUMBER (Pb free)	MARKING	TEMP. RANGE	PACKAGE
G2996P1U	G2996P1Uf	G2996	-40°C to 85°C	SOP-8
G2996F1U	G2996F1Uf	G2996	-40°C to 85°C	SOP-8 (FD)

Note: P1:SOP-8 F1:SOP-8(FD)
U: Tape & Reel (FD): Thermal Pad

Pin Configuration



Typical Application Circuit



Absolute Maximum Ratings (1)

Supply Voltage
PVIN, AVIN, VDDQ to GND . . . . . -0.3V to +6V
Operating Ambient Temperature Range
T_A . . . . . .-40°C to +125°C
Maximum Junction Temperature, T_J . . . .150°C
Storage Temperature Range, T_{STG} . . -65°C to+150°C
Reflow Temperature (soldering, 10 sec) . . . . . .260°C
Electrostatic Discharge, V_{ESD}
Human body mode . . . . . .2000V(2)
Thermal Resistance Junction to Ambient, (θ_{JA})
SOP-8 . . . . . .130°C/W
SOP-8 (FD) . . . . . 110°C/W(3)
SOP-8 (FD) . . . . . 50°C/W(4)
SOP-8 (FD) . . . . . 41°C/W(5)
Thermal Resistance Junction to Case, (θ_{JC})
SOP-8 (FD) . . . .12°C/W

Recommend Operation Range

Operating Ambient Temperature Range
T_A . . . . . .-40°C to +85°C
AVIN to GND . . . . . 1.6V to +5.5V
PVIN, SD, VDDQ to GND . . . . . 1.6V to AVIN

Note:

(1): Absolute maximum rating indicates limits beyond which damage to the device may occurs.

(2): Human body model : C = 100pF, R = 1500Ω, 3 positive pulses plus 3 negative pulses

(3): The package is placed on a 2-layer PCB (1oz/1oz) with minimum footprint.

(4): The package is placed on a 2-layer PCB (2oz/2oz) with 6 vias. Please refer the evaluation board manual (EV2996-10) for pcb layout.

(5): The package is placed on a 2-layer PCB (2oz/2oz) with 6 vias. The airflow is used. Please refer the evaluation board manual (EV2996-10) for pcb layout.

Electrical Characteristics

Specifications with standard typeface are for T_A=25°C. unless otherwise specified, AVIN=PVIN=2.5V, VDDQ=2.5V for DDR I, AVIN=PVIN=VDDQ=1.8V for DDRII.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
V_{REF} Voltage	V_{REF}	VDDQ=1.7V	0.810	0.849	0.890	V
		VDDQ=1.8V	0.860	0.898	0.940	V
		VDDQ=1.9V	0.910	0.949	0.990	V
V_{REF} Voltage	V_{REF}	VDDQ=2.3V	1.11	1.145	1.19	V
		VDDQ=2.5V	1.21	1.245	1.29	V
		VDDQ=2.7V	1.31	1.345	1.39	V
V_{REF} Output impendence	Z_{REF}	I_{REF} =-30µA to + 30µA	---	1.15	---	kΩ
V_{TT} Output voltage	V_{TT}	I_{OUT}=0A				
		VDDQ=1.7V	0.810	0.847	0.890	V
		VDDQ=1.8V	0.860	0.896	0.940	V
		VDDQ=1.9V	0.910	0.947	0.990	V
		I_{OUT}=±0.9A				
		VDDQ=1.7V	0.810	0.847	0.890	V
		VDDQ=1.8V	0.860	0.896	0.940	V
		VDDQ=1.9V	0.910	0.947	0.990	V
V_{TT} Output voltage	V_{TT}	I_{OUT}=0A				
		VDDQ=2.3V	1.11	1.152	1.19	V
		VDDQ=2.5V	1.21	1.252	1.29	V
		VDDQ=2.7V	1.31	1.352	1.39	V
		I_{OUT}=±1.5A				
		VDDQ=2.3V	1.11	1.152	1.19	V
		VDDQ=2.5V	1.21	1.252	1.29	V
		VDDQ=2.7V	1.31	1.352	1.39	V

Electrical Characteristics

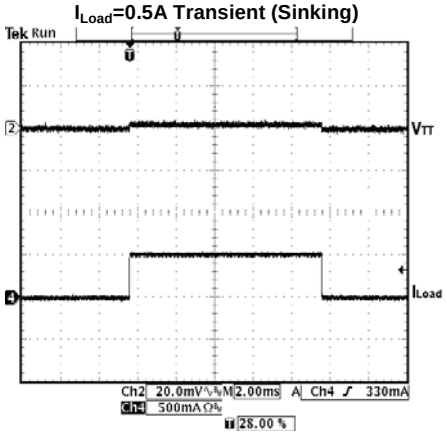
Specifications with standard typeface are for T_A=25°C. unless otherwise specified, AVIN=PVIN=2.5V, VDDQ=2.5V for DDR I, AVIN=PVIN=VDDQ=1.8V for DDRII.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
V_{TT} Output Voltage Offset (V_{REF}- V_{TT})	VOS_{Vtt}	I_{OUT}=0A	-40	0	40	mV
		I_{OUT}=-0.9A	-40	0	40	mV
		I_{OUT}=+0.9A	-40	0	40	mV
V_{TT} Output Voltage Offset (V_{REF}- V_{TT})	VOS_{Vtt}	I_{OUT}=0A	-40	0	40	mV
		I_{OUT}=-1.5A	-40	0	40	mV
		I_{OUT}=+1.5A	-40	0	40	mV
Quiescent Current	I_Q	I_{OUT}=0A	---	280	500	µA
VDDQ input Impedence	Z_{VDDQ}		---	100	---	kΩ
Quiescent Current in shutdown	I_{SD}	$\overline{SD}$ =0	---	180	300	µA
Shutdown leakage current	I_{Q_SD}		---	0.01	---	µA
V_{SENSE} input current	I_{SENSE}		---	20	---	nA
V_{TT} leakage current in shutdown	I_V	$\overline{SD}$ =0, V_{TT} =1.25V	---	0.01	---	µA
Minimum Shutdown High Level	V_{IH}		1.6	---	---	V
Maximum Shutdown Low Level	V_{IL}		---	---	0.8	V
Thermal Shutdown	T_{SD}		---	150	---	°C
Thermal Shutdown Hystersis	T_{Hsy}		---	25	---	°C

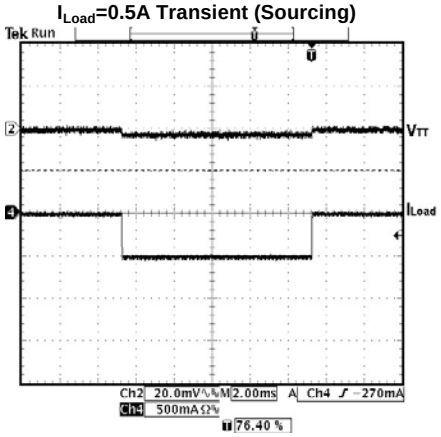
Typical Performance Characteristics

AV_{IN}=2.5V, P_{VIN}=2.5V, V_{DDQ}=2.5V, C_{AVIN}=0.1µF/Ceramic X7R/0603/6.3V/TDK, C_{PVIN}=68µF/6.3V POSCAP Series/SANYO, C_{VTT}=330µF*2/6.3V POSCAP Series/SANYO, T_A=25°C, unless otherwise noted.

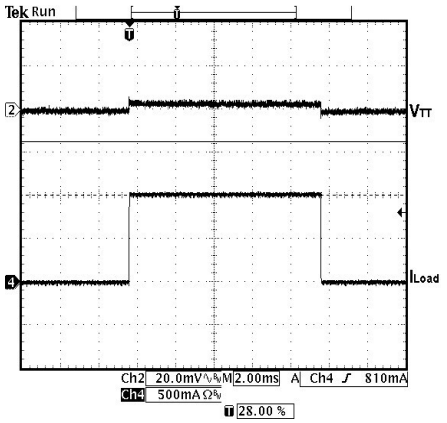
I_{Load}=0.5A Transient (Sinking)



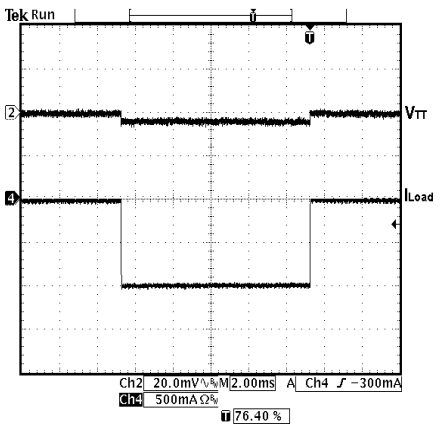
I_{Load}=0.5A Transient (Sourcing)



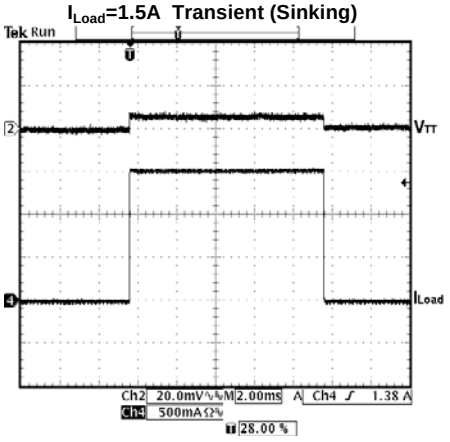
I_{Load}=1A Transient (Sinking)



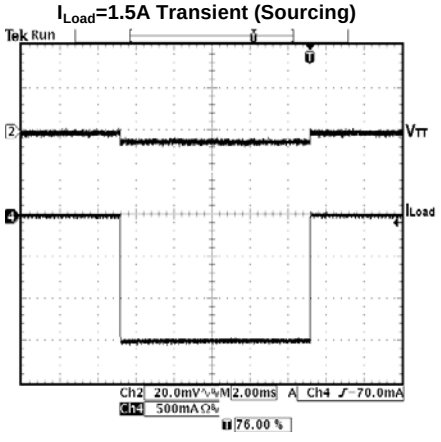
I_{Load}=1A Transient (Sourcing)



I_{Load}=1.5A Transient (Sinking)



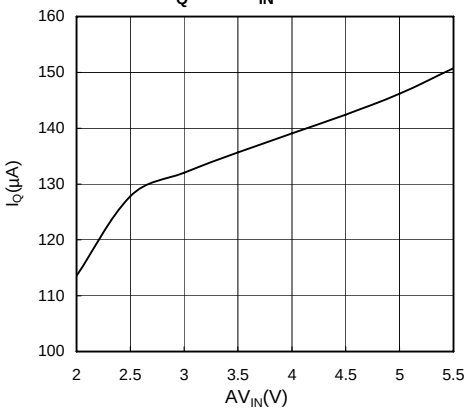
I_{Load}=1.5A Transient (Sourcing)



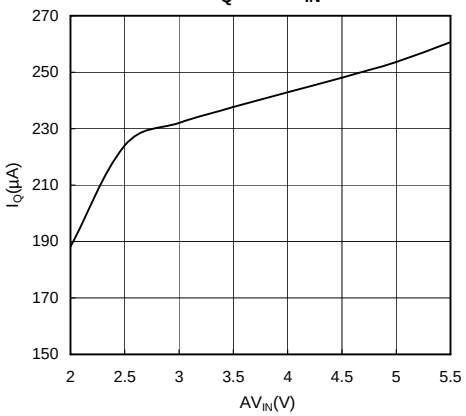
Typical Performance Characteristics

AV_{IN}=2.5V, P_{VIN}=2.5V, V_{DDQ}=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, V_{SD}=2.5V, C_{VTT}=220µF, T_A=25°C, unless otherwise noted.

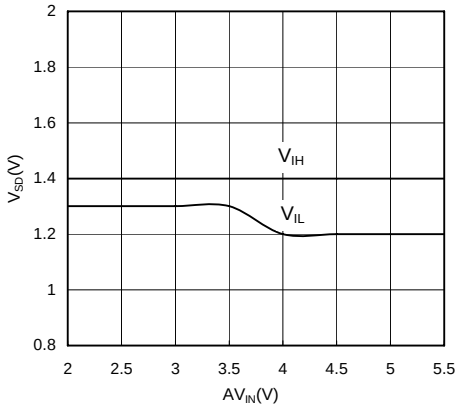
I_Q vs AV_{IN} in SD



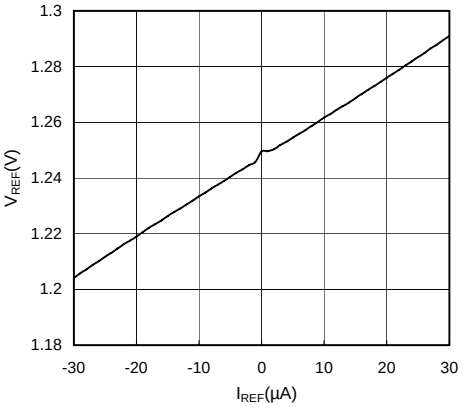
I_Q vs AV_{IN}



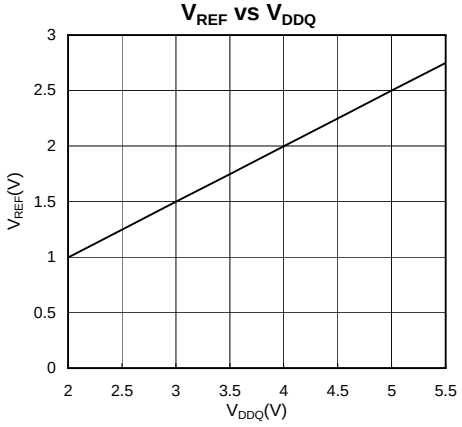
V_{IH} and V_{IL}



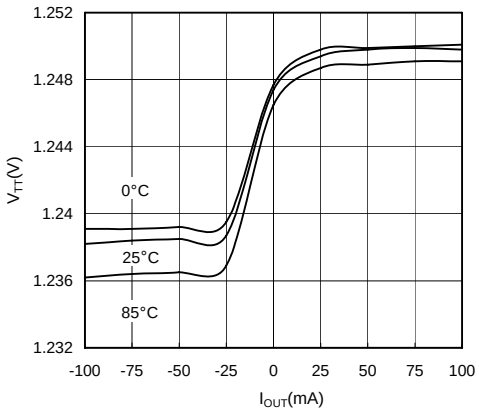
V_{REF} vs I_{REF}



V_{REF} vs V_{DDQ}



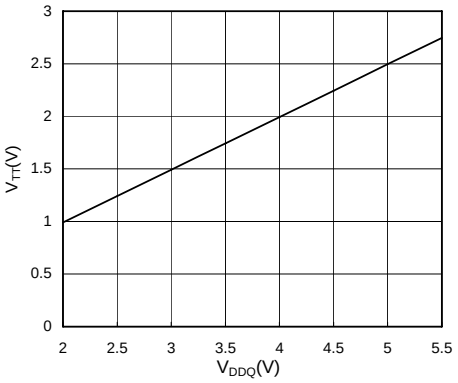
V_{TT} vs I_{OUT} Temperature



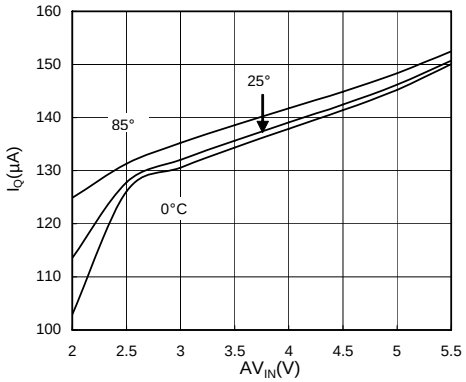
Typical Performance Characteristics (continued)

AV_{IN}=2.5V, P_{VIN}=2.5V, V_{DDQ}=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, V_{SD}=2.5V, C_{VTT}=220µF, T_A=25°C, unless otherwise noted.

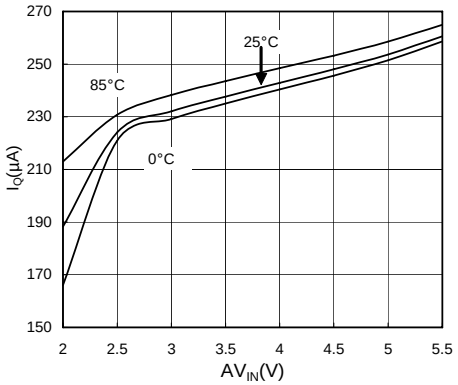
V_{TT} vs V_{DDQ}



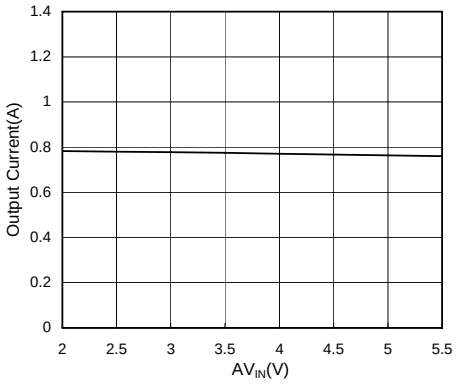
I_Q vs AV_{IN} in SD Temperature



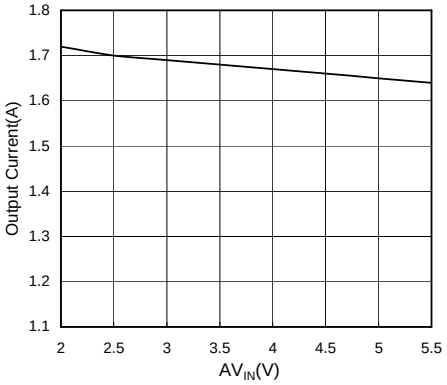
I_Q vs AV_{IN} Temperature



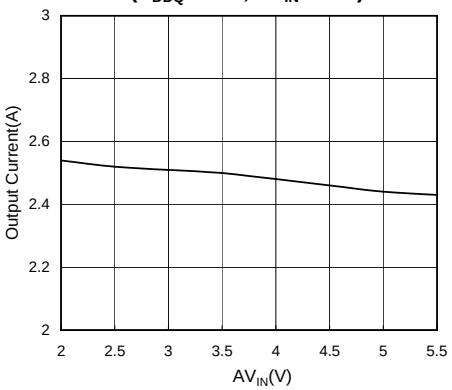
Maximum Sourcing Current vs AV_{IN} (V_{DDQ}=2.5V, PV_{IN}=1.8V)



Maximum Sourcing Current vs AV_{IN} (V_{DDQ}=2.5V, PV_{IN}=2.5V)



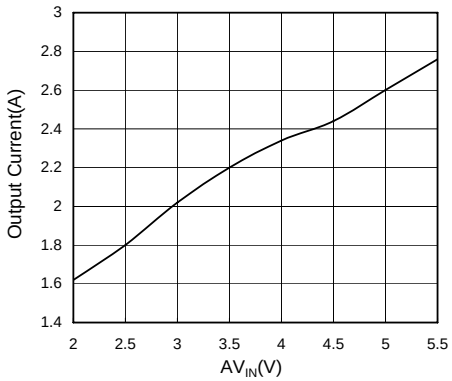
Maximum Sourcing Current vs AV_{IN} (V_{DDQ}=2.5V, PV_{IN}=3.3V)



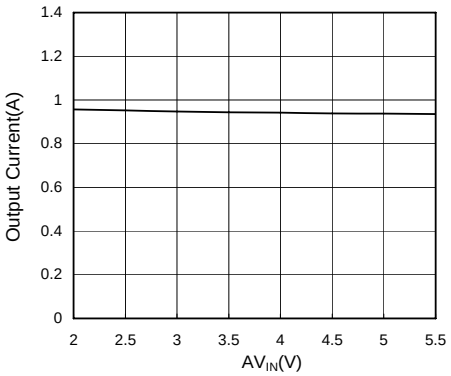
Typical Performance Characteristics (continued)

AV_{IN}=2.5V, P_{VIN}=2.5V, V_{DDQ}=2.5V, C_{AVIN}=0.1µF, C_{PVIN}=47µF, C_{VREF}=0.01µF, V_{SD}=2.5V, C_{VTT}=220µF, T_A=25°C, unless otherwise noted.

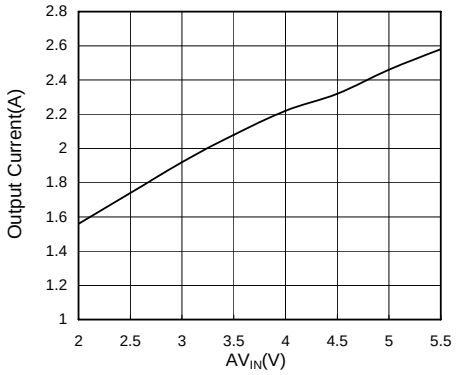
Maximum Sinking Current vs AV_{IN} (V_{DDQ}=2.5V)



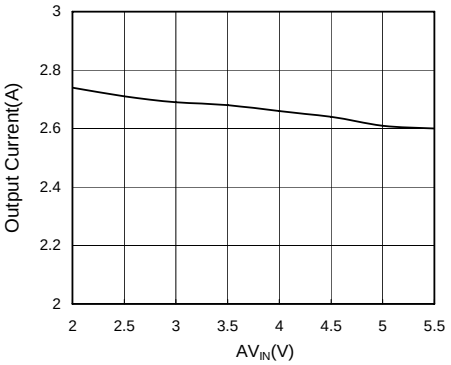
Maximum Sourcing Current vs AV_{IN} (V_{DDQ}=1.8V, PV_{IN}=1.8V)



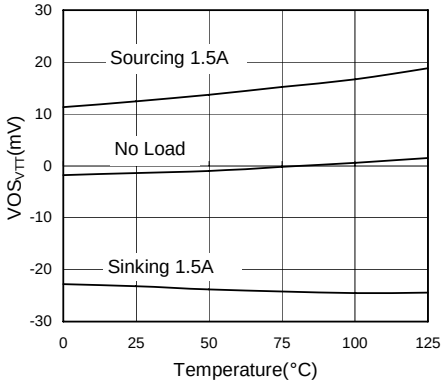
Maximum Sinking Current vs AV_{IN} (V_{DDQ}=1.8V)



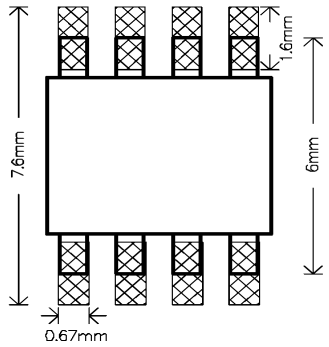
Maximum Sourcing Current vs AV_{IN} (V_{DDQ}=1.8V, PV_{IN}=3.3V)



VOS_{VTT} vs Temperature(V_{DDQ}=2.5V)



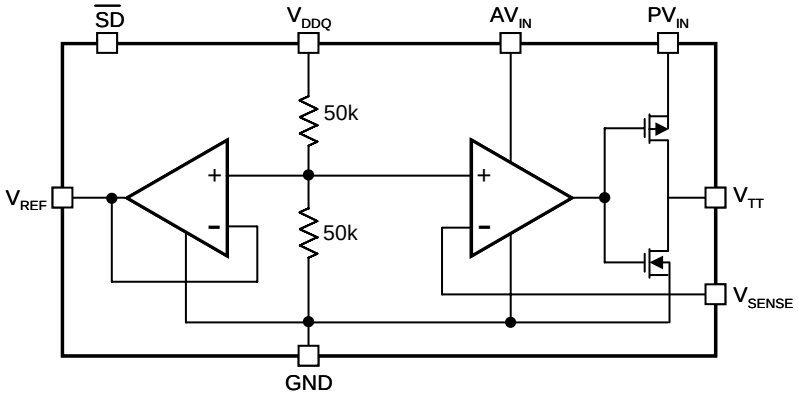
Recommended Minimum Footprint
SOP-8, SOP-8 (FD)



Pin Description

NUMBER	NAME	FUNCTION
1	GND	Ground
2	$\overline{SD}$	Active low shutdown control pin
3	VSENSE	Feedback pin for regulating V_{TT}
4	VREF	Buffered output that is a reference output of VDDQ/2
5	VDDQ	Power Input for internal reference
6	AVIN	Analog input pin
7	PVIN	Power input pin
8	VTT	Output voltage for connection to termination resistors, equal to VDDQ/2

Block Diagram



Description

The G2996 is a linear bus termination regulator designed to meet the JEDEC SSTL-2 and SSTL-3 (Series Stub Termination Logic) specifications for termination of DDR-SDRAM. The output, V_{TT}, is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ/2. The G2996 is designed to maintain the excellent load regulation and with fast response time to minimum the transition preventing shoot-through. The G2996 also incorporates two distinct power rails that separates the analog circuitry (AVIN) from the power output stage (PVIN). This power rails split can be utilized to reduce the internal power dissipation. And this also permits G2996 to provide a termination solution for the next generation of DDR-SDRAM (DDR II).

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one RS series resistor from the chipset to the memory and one RT termination resistor, both 25Ω typically. The resistors can be changed to scale the current requirements from the G2996. This implementation can be seen below in Figure 1.

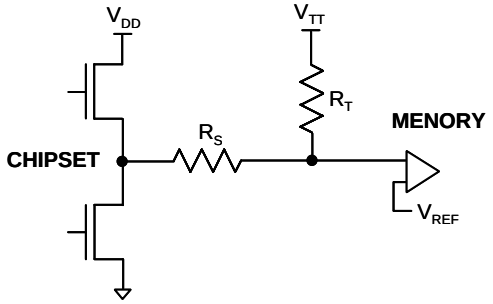


Figure 1. SSTL-Termination Scheme

AVIN, PVIN

AVIN and PVIN are two independent input supply pins for the G2996. AVIN is used to supply all the internal analog circuits. PVIN is only used to supply the output stage to create the regulated V_{TT}. To keep the regulation successfully, AVIN should be equal to or larger than PVIN. Using a higher PVIN voltage will produce a larger sourcing capability from $V_{TT.}$ But the internal power loss will also increase and then the heat increases. If the junction temperature exceeds the thermal shutdown threshold than the G2996 will enter the shutdown state that is the same as manual shutdown, where V_{TT} is tri-state and V_{REF} remains active.
For SSTL-2 applications, the AVIN and PVIN can be short together at 2.5V to minimize the PCB complexity and to reduce the bypassing capacitors for the two supply pins separately.

VDDQ

A voltage divider of two 50kΩ is connected between VDDQ and ground, to create the internal reference voltage (VDDQ/2). This guarantees that V_{TT} will track VDDQ/2 precisely. The optimal implementation of VDDQ is as a remote sensing. This can be achieved by connecting VDDQ directly to the 2.5V rail (SSTL-2 applications) at the DIMM instead of AVIN and PVIN. This will ensure that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines.

Vsense

The V_{SENSE} pin is the feedback sensing pin of the operation amplifier which regulates the V_{TT} voltage. In most motherboard applications, the termination resistors will connect V_{TT} in a long plane. If using the remote sensing pin – V_{SENSE} to the middle of the bus, the significant long-trace IR drop resulting in a termination voltage which is lower at one end than the other can be avoided. This will provide a better distribution across the entire termination bus. If the remote load regulation is not used, the V_{SENSE} pin must still be connected to V_{TT} for correct regulation. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1µF ceramic capacitor placed next to the V_{SENSE} pin can help to filter any high frequency signals and preventing errors.

V_{REF}

V_{REF} provides a buffered output of the internal reference voltage (VDDQ/2). It can support the reference voltage of Northbridge chipset and memory. This output remains active during the shutdown state and thermal shutdown events to support the suspend to RAM (STR) functionality. For better performance, using an output bypass capacitor close this pin is more helpful for the noise. A ceramic capacitor in the range of 0.1µF to 0.01µF is recommended.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors of DDR-SDRAM. It can precisely track the VDDQ/2 voltage with the sinking and sourcing current capability. The G2996 is designed to deliver 1.5A continuous current and peak current up to 3A with a fast transient response @ 2.5V supply rail. The maximum continuous current sourcing from V_{TT} is a function of PVIN. Using a higher PVIN will increase the source current from $V_{TT,}$ but it also increase the internal power dissipation and reduce the efficiency. Although the G2996 can deliver the larger current, care should be taken for the thermal dissipation when larger current is required. The G2996 is packaged with Power-Pad to increase the power dissipation capability. When driving larger current, the larger heat-sink in the PCB is strongly recommended to have a better thermal performance. The R_{DS} of MOS will increase when the junction temperature increases. If the heat is not dealt with well, the maximum output current will be degraded. When the temperature exceeds the junction temperature, the thermal shutdown protection is activated. That will drive the V_{TT} output into tri-state until the temperature returns below the hysteretic trigger point.

Capacitors

The G2996 does not require the capacitors for input stability, but it is recommended for improving the performance during large load transition to prevent the input power rail from dropping, especially for PVIN. The input capacitor for PVIN should be as close as possible. The typical recommended value is 50µF for AL electrolytic capacitors, 10µF with X5R for the ceramic capacitors. To prevent the excessive noise coupling into this device, an additional 0.1µF ceramic capacitor can be placed on the AVIN power rail for the better performance.

The output capacitor of the G2996 is suggested to use the capacitors with low ESR. Using the capacitors with low ESR (as ceramic, OS-CON, tantalum) will have the better transition performance which is with smaller voltage drop when the peak current occurring at the transition. As a general recommendation the output capacitor should be sized above 220µF with the low ESR for SSTL applications with DDR-SDRAM.

Thermal Dissipation

When the current is sinking to or sourcing from V_{TT}, the G2996 will generate internal power dissipation resulting in the heat. Care should be taken to prevent the device from damages caused by the junction temperature exceeding the maximum rating. The maximum allowable internal temperature rise (T_{RMAX}) can be calculated under the given maximum ambient temperature (T_{AMAX}) of the application and the maximum allowable junction temperature (T_{JMAX}).

$$T_{RMAX} = T_{JMAX} - T_{AMAX}$$

From this equation, the maximum power dissipation (P_{DMAX}) of the G2996 can be calculated:

$$P_{DMAX} = T_{RMAX} / \theta_{JA}$$

θ_{JA} of the G2996 will be dependent on several variables: the packages used, the thickness and size of the copper, the number of vias and the airflow. In the package, the G2996 use the SOP-8 with Power-PAD to improve the θ_{JA}. If the layout of the PCB can put a larger size of copper to contact the Power-PAD of this device, the θ_{JA} will be further improved. The better θ_{JA} is not only protecting the device well, but also increasing the maximum current capability at the same ambient temperature.

Typical Application Circuits

There are several application circuits shown in Figure 2 through 8 to illustrate some of the possible configurations of the G2996. Figure 2~4 are the SSTL-2 applications. For the majority of applications that implement the SSTL-2 termination scheme, it is recommended to connect all the input rails to 2.5V rail, as seen in Figure 2. This provides an optimal trade-off between power dissipation and component count.

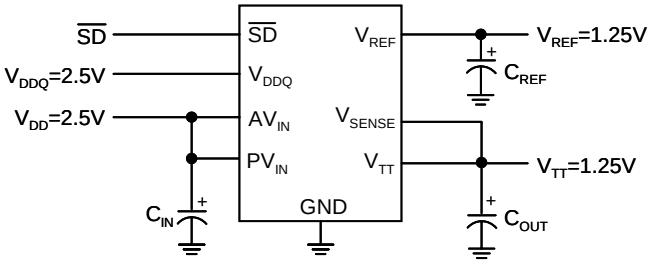


Figure 2. Recommended SSTL-2 Implementation

In Figure 3, the power rails are split. The power rail of the output stage (PVIN) can be as low as 1.8V, the power rail of the analog circuit (AVIN) is operated above 2V. The lower output stage power rail can lower the internal power dissipation when sourcing from the device and improve the efficiency, but the disadvantage is the maximum continuous current sourcing from V_{TT} is reduced. This configuration is applied when the power dissipation and efficiency are concerned.

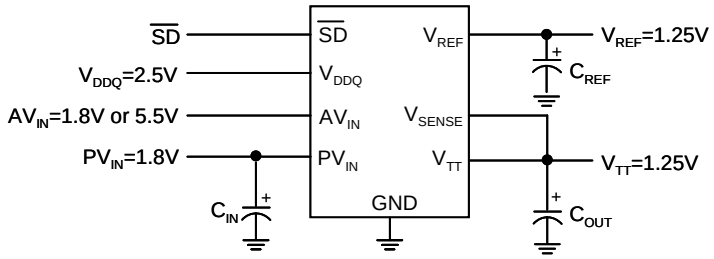


Figure 3. Lower Power Dissipation SSTL-2 Implementation

In Figure 4, the power rail of the output stage (PVIN) is connected to 3.3V to increase the maximum continuous current sourcing from V_{TT}. AVIN should be always equal to or larger than PVIN. This configuration can increase the source capability of this device, but the power dissipation increases at the same time. It should be more careful to prevent the junction temperature from exceeding the maximum rating. Because of this risk, it is not recommended to supply the output stage power rail (PVIN) with a voltage higher than a nominal 3.3V rail.

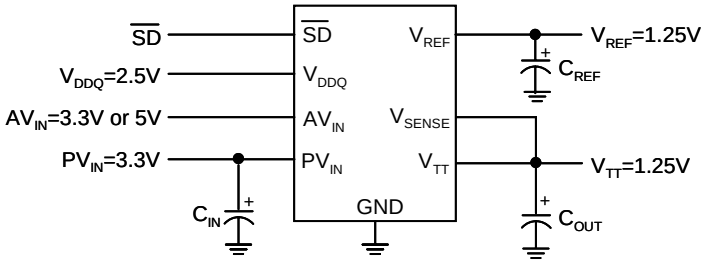


Figure 4. SSTL-2 Implementation with higher voltage rails

In Figure 5 & 6, they are the application configurations of DDR-II SDRAM bus terminations. Figure 5 is the typical application scheme of DDR-II SDRAM. With the separate VDDQ pin and an internal resistor divider, it is possible to use the G2996 in applications utilizing DDR-II memory. Figure 6 is used to increase the driving capability. The risk is the same as figure 4.

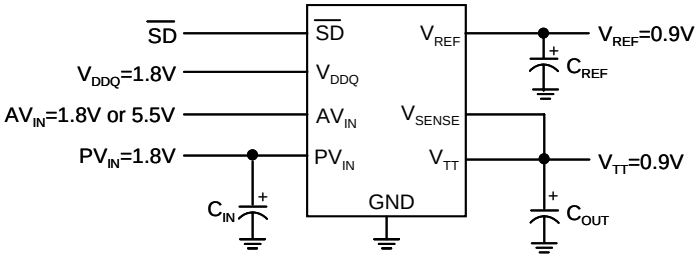


Figure 5. Recommended DDR-II Termination

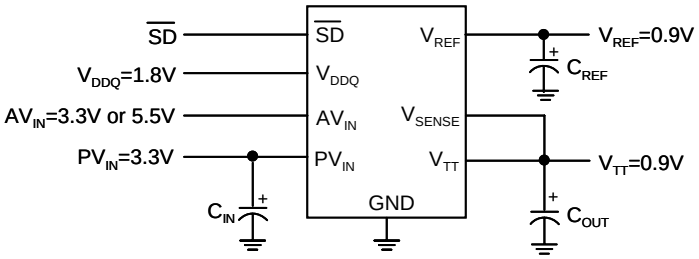


Figure 6. DDR-II Termination with higher voltage rails

Figure 7 & 8 are used to scale the V_{TT} to the wanted value when the standard voltages of SSTL-2 do not meet the requirements. Using R1 & R2, figure 7 can shift V_{TT} up to VDDQ/2 * (1+R1/R2) and figure 8 can shift V_{TT} down to VDDQ/2 * (1-R1/R2).

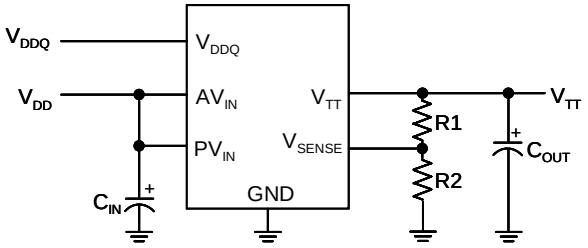


Figure 7. Increasing VTT by Level Shifting

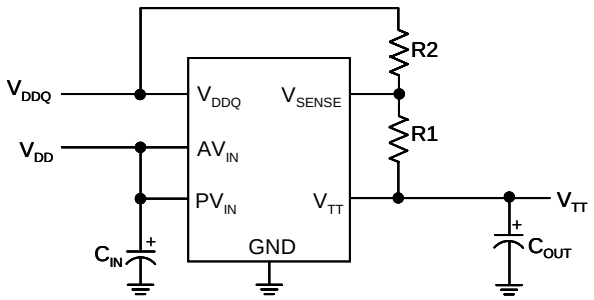
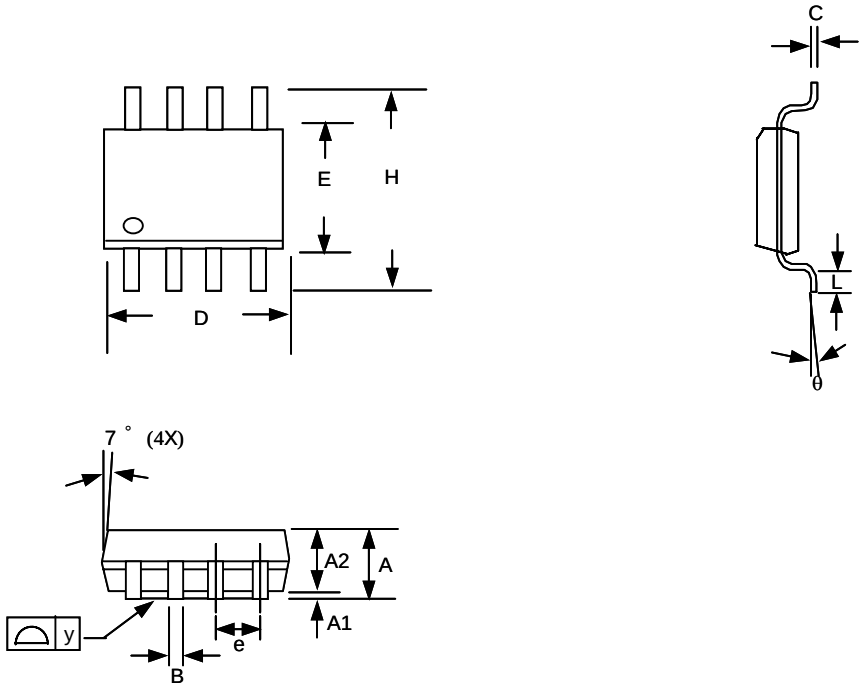


Figure 8. Decreasing VTT by Level Shifting

Package Information

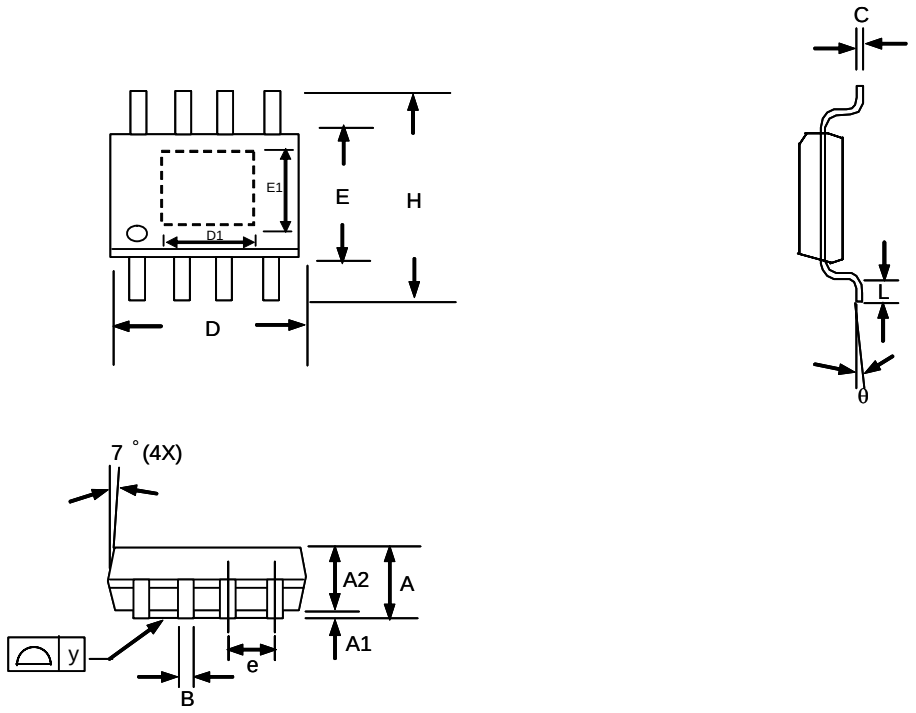


SOP-8 Package

Note:

1. Package body sizes exclude mold flash and gate burrs
2. Dimension L is measured in gage plane
3. Tolerance 0.10mm unless otherwise specified
4. Controlling dimension is millimeter converted inch dimensions are not necessarily exact.
5. Followed from JEDEC MS-012

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	0.053	0.063	0.069
A1	0.10	-----	0.25	0.004	-----	0.010
A2	-----	1.45	-----	-----	0.057	-----
B	0.33	-----	0.51	0.013	-----	0.020
C	0.19	-----	0.25	0.007	-----	0.010
D	4.80	-----	5.00	0.189	-----	0.197
E	3.80	-----	4.00	0.150	-----	0.157
e	-----	1.27	-----	-----	0.050	-----
H	5.80	-----	6.20	0.228	-----	0.244
L	0.40	-----	1.27	0.016	-----	0.050
y	-----	-----	0.10	-----	-----	0.004
θ	0°	-----	8°	0°	-----	8°



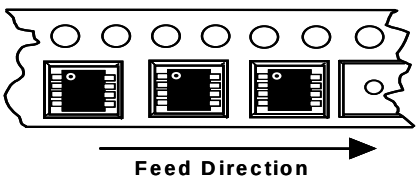
SOP- 8 (FD) Package

Note:

1. Package body sizes exclude mold flash and gate burrs
2. Dimension L is measured in gage plane
3. Tolerance 0.10mm unless otherwise specified
4. Controlling dimension is millimeter converted inch dimensions are not necessarily exact.
5. Followed from JEDEC MS-012

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.45	1.50	1.55	0.057	0.059	0.061
A1	0.00	-----	0.10	0.000	-----	0.004
A2	-----	1.45	-----	-----	0.057	-----
B	0.33	-----	0.51	0.013	-----	0.020
C	0.19	-----	0.25	0.007	-----	0.010
D	4.80	-----	5.00	0.189	-----	0.197
E	3.80	-----	4.00	0.150	-----	0.157
e	-----	1.27	-----	-----	0.050	-----
H	5.80	-----	6.20	0.228	-----	0.244
L	0.40	-----	1.27	0.016	-----	0.050
y	-----	-----	0.10	-----	-----	0.004
θ	0°	-----	8°	0°	-----	8°
D1	2.22	-----	2.60	0.087	-----	0.102
E1	2.60	-----	2.98	0.102	-----	0.117

Taping Specification



Feed Direction

Typical SOP Package Orientation

PACKAGE	Q'TY/REEL
SOP-8	2,500 ea
SOP-8 (FD)	2,500 ea