

DIGITAL PWM IC

1.0 General Description

The G5199 is a high performance AC/DC power supply controller which uses digital control technology to build peak current mode PWM flyback power supplies. The device operates in quasi-resonant mode to provide high efficiency along with a number of key built-in protection features while minimizing the external component count, simplifying EMI design and lowering the total bill of material cost. The G5199 removes the need for secondary feedback circuit while achieving excellent line and load regulation. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions. Pulse-by-pulse waveform analysis allows for a loop response that is much faster than traditional solutions, resulting in improved dynamic load response for both one-time and repetitive load transients. The built-in power limit function enables optimized transformer design in universal off-line applications and allows for a wide input voltage range. GlobalSemi's innovative proprietary technology ensures that power supplies built with the G5199 can achieve both highest average active efficiency and less than 30 mW no-load power consumption, and have fast dynamic load response in a compact form factor in typical 12 W and above applications. The active start-up scheme enables shortest possible start-up time without sacrificing no-load power loss.

Features

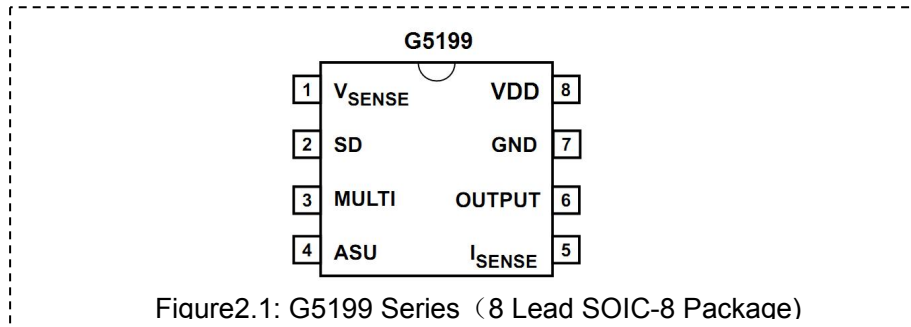
- ◆ No-load power consumption < 30 mW at 230 VAC along with fast dynamic load response and short turn-on delay time in typical 12 W compact adapter/charger applications
- ◆ Tight constant-voltage and constant-current regulation across line and load range
- ◆ Primary-side feedback eliminates opto-isolators and simplifies design
- ◆ Proprietary optimized 89 kHz maximum PWM switching frequency with quasi-resonant operation achieves best size, efficiency and common mode noise
- ◆ User-configurable 5-level cable drop compensation provides design flexibility
- ◆ Adaptive multi-mode PWM/PFM control improves efficiency
- ◆ No external loop compensation components required
- ◆ Complies with EPA 2.0 energy-efficiency specifications with ample margin
- ◆ Built-in single-point fault protection features: output short-circuit protection, output over-voltage protection, over-current protection and current-sense-resistor fault protection
- ◆ Dedicated pins for external over-temperature protection and over-voltage protection, with latch function available
- ◆ No audible noise over entire operating range

Applications

- Compact AC/DC adapter/chargers for media tablets and smart phones
- AC/DC adapters for consumer electronics

2.0 Products Information

2.1 Pin configuration



| Pin# | Name | I/O | Description |
|------|--------------------|--------------|--|
| 1 | V _{SENSE} | Analog Input | Auxiliary voltage sense (used for primary regulation). |
| 2 | SD | Analog Input | External shutdown control. Used for external over-temperature protection (OTP) by connecting an NTC resistor from this pin to Ground. |
| 3 | MULTI | Analog Input | Shared multi-function pin. Used for external cable drop compensation (CDC) configuration and supplemental over-voltage protection (OVP). |
| 4 | ASU | Output | Control signal for active start-up device (BJT or depletion mode NFET). |
| 5 | I _{SENSE} | Analog Input | Primary current sense. Used for cycle-by-cycle peak current control and limit. |
| 6 | OUTPUT | Output | Gate drive for external MOSFET switch. |
| 7 | GND | Ground | Ground. |
| 8 | VDD | Power Input | Power supply for control logic. |

2.2 Marking Information

| Part Number | Marking Information |
|-------------|---------------------|
| G5199 | HAXXX |

2.3 Series description

| Part Number | Description |
|-------------|--------------------------------|
| G5199-00 | OVP/OTP latch, no CC operation |
| G5199-01 | No OVP/OTP latch |
| G5199-03 | OVP/OTP latch |

2.4 Block diagram

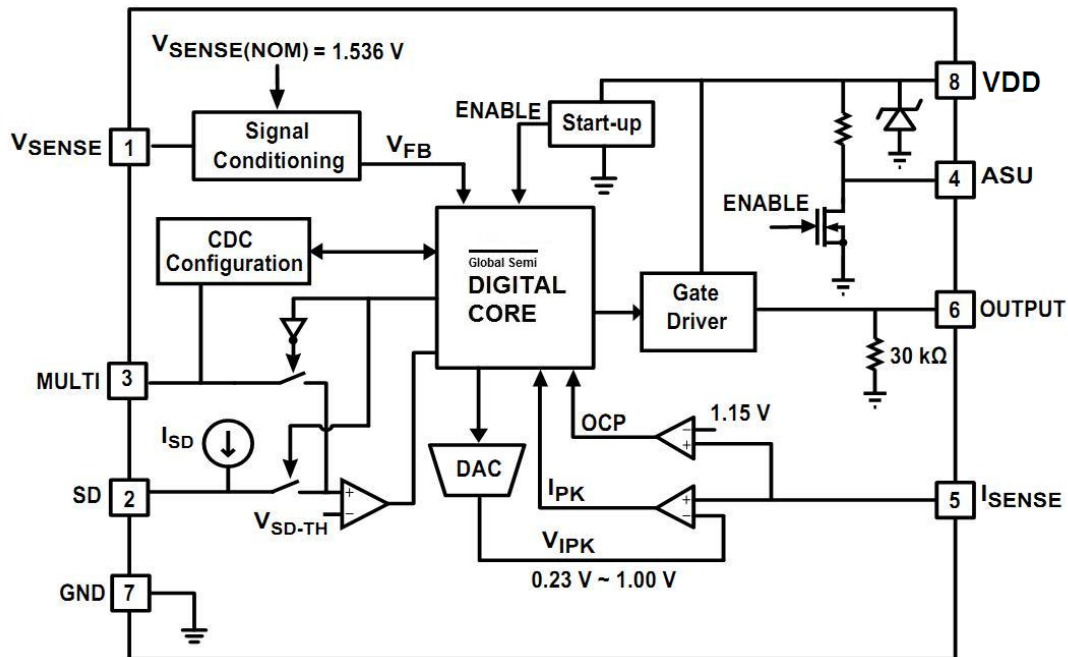


Figure2.1 G5199 Functional Block Diagram

3.0 Absolute Maximum Ratings

| Parameter | Symbol | Value | Units |
|---|---------------|--------------|-------|
| DC supply voltage range (pin 8, $I_{DD} = 20\text{mA max}$) | V_{DD} | -0.3 to 18.0 | V |
| Continuous DC supply current at V_{DD} pin ($V_{DD} = 15\text{ V}$) | I_{DD} | 20 | mA |
| ASU output (Pin 4) | | -0.3 to 18.0 | V |
| OUTPUT (Pin 6) | | -0.3 to 18.0 | V |
| V_{SENSE} input (Pin 1, $I_{VENSE} \leq 10\text{mA}$) | | -0.7 to 4.0 | V |
| I_{SENSE} input (Pin 5) | | -0.3 to 4.0 | V |
| SD (pin2) | | -0.3 to 4.0 | V |
| MULTI(Pin 3, $I_{MULTI} \leq 20\text{mA}$) | | -0.8 to 4.0 | V |
| Maximum junction temperature | T_{JMAX} | 150 | °C |
| Operating junction temperature | T_{JOPT} | -40 to 150 | °C |
| Storage temperature | T_{STG} | -65 to 150 | °C |
| Lead temperature during IR reflow for ≤ 15 seconds | T_{LEAD} | 260 | °C |
| Thermal resistance junction-to-ambient | θ_{JA} | 160 | °C/W |
| ESD rating per JEDEC JESD22-A114 | | 2,000 | V |
| Latch-up test per JEDEC 78 | | ± 100 | mA |

4.0 Typical Application

The G5199 contains a controller for a flyback circuit.

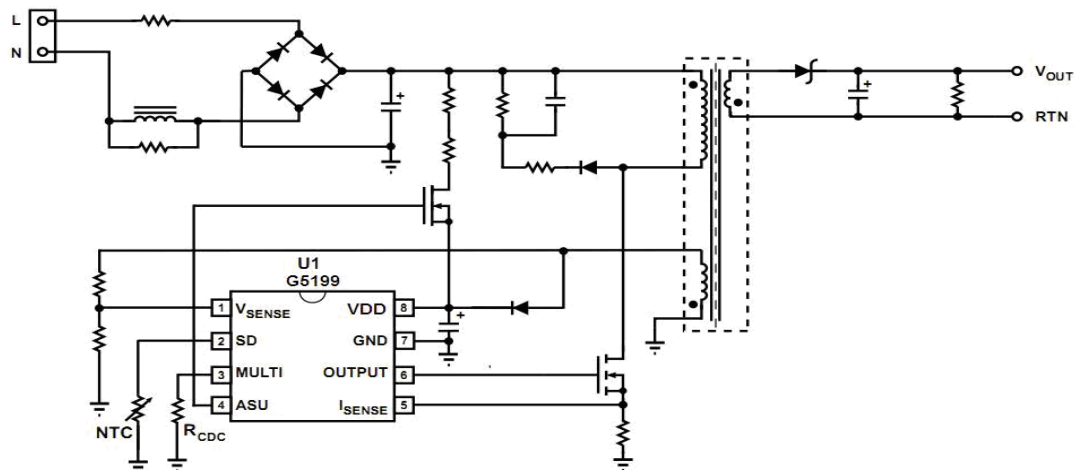


Figure4.1 G5199 Typical Application Circuit(Achieving < 30 mW No-load Power Consumption)

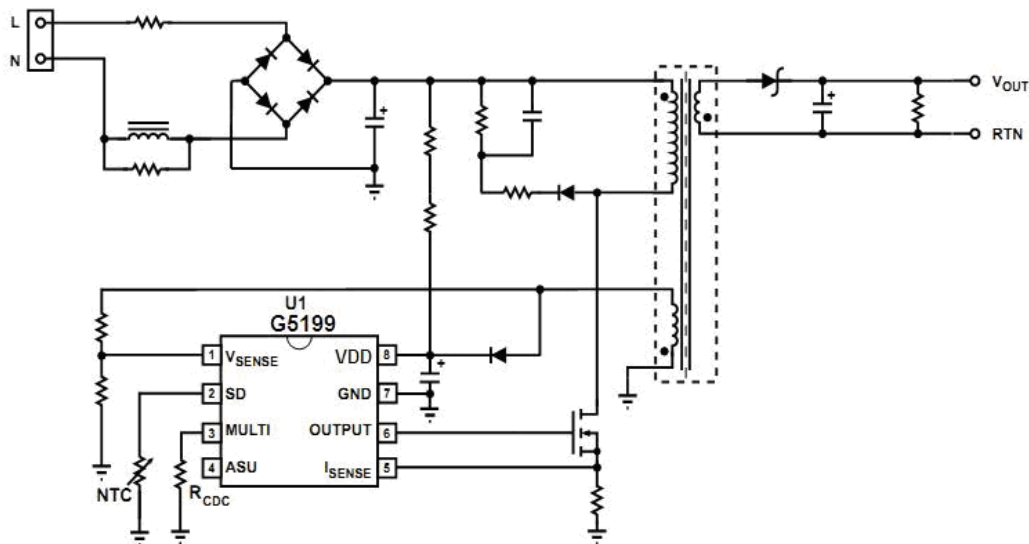


Figure4.2 G5199 Typical Application (Alternative Circuit without Using Active Start-up Device)

5.0 Electrical Characteristics

($T_A = 25^\circ\text{C}$, $V_{DD}=12\text{V}$, unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|------------------------------|--------------------------------------|--|------|-------|------|---------------|
| SD SECTION(Pin2) | | | | | | |
| $V_{SD-TH(F)}$ | Shutdown threshold (falling edge) | | 0.95 | 1.0 | 1.05 | V |
| $V_{SD-TH(ST_F)}$ | Shutdown threshold before start-up | | 1.14 | 1.2 | 1.26 | V |
| I_{SD} | Shutdown current source | | 95 | 100 | 105 | μA |
| MULTI Section (Pin3) | | | | | | |
| $V_{SD-TH(R)}$ | OVP shutdown threshold (rising edge) | | 0.96 | 1.015 | 1.07 | V |
| I_{BVSD} | Input leakage current | $V_{SD} = 1.0\text{ V}$ | | | 1 | μA |
| OUTPUT Section (Pin6) | | | | | | |
| $R_{DS(ON)PD}$ | Driver pull-down ON-resistance | $I_{SINK} = 5\text{ mA}$ | | 16 | | Ω |
| $R_{DS(ON)PU}$ | Driver pull-up ON-resistance | $I_{SOURCE} = 5\text{ mA}$ | | 125 | | Ω |
| t_R | Rise time (Note 2) | $T_A = 25^\circ\text{C}$, $C_L = 330\text{ pF}$ 10% to 90% | | 173 | | ns |
| t_F | Fall time (Note 2) | $T_A = 25^\circ\text{C}$, $C_L = 330\text{ pF}$ 90% to 10% | | 14 | | ns |
| f_{SW} | Switching frequency (Note 3) | > 50% load | | 89 | | kHz |
| VDD SECTION (Pin8) | | | | | | |
| $V_{DD(MAX)}$ | Maximum operating voltage (Note 2) | | | | 16 | V |
| $V_{DD(ST)}$ | Start-up threshold | | 11.0 | 12.0 | 13.0 | V |
| $V_{DD(UVL)}$ | Under-voltage lockout threshold | | | 5.5 | | V |
| $V_{DD(RLS)}$ | Latch release threshold | | | 4.5 | | V |
| $I_{IN(ST)}$ | Start-up current | | | 6 | | μA |
| I_{CCQ} | Quiescent current | | | 4.1 | | mA |
| V_{ZB} | Zener breakdown voltage | | 18.5 | 19.5 | 20.5 | V |
| ASU SECTION (Pin4) | | | | | | |
| $V_{ASU(MAX)}$ | Maximum operating voltage (Note 2) | | | | 16 | V |
| R_{VDD_ASU} | Resistance between VDD and ASU | | | 1100 | | k Ω |

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|--------------------------|-------|-------|-------|------|
| V_{SENSE} SECTION (Pin 1) | | | | | | |
| I _{BVS} | Input leakage current | V _{SENSE} = 2 V | | | 1 | uA |
| V _{SENSE(NOM)} | Nominal voltage threshold | TA=25°C, negative edge | 1.521 | 1.536 | 1.551 | V |
| V _{SENSE(MAX)} | V _{SENSE} -based output OVP threshold with no CDC compensation (Note 1) | TA=25°C, negative edge | | 1.838 | | V |
| I_{SENSE} SECTION (Pin 5) | | | | | | |
| V _{OCF} | Over-current threshold | | 1.11 | 1.15 | 1.19 | V |
| V _{IPK(HIGH)} | ISENSE regulation upper limit (Note 2) | | | 1.0 | | V |
| V _{IPK(LOW)} | ISENSE regulation lower limit (Note 2) | | | 0.23 | | V |

Notes:

Note 1: The V_{SENSE}-based output OVP threshold depends on the CDC setup, see Section 7.12 for more details.

Note 2: These parameters are not 100% tested, guaranteed by design and characterization.

Note 3: Operating frequency varies based on the load conditions, see Section 7.6 for more details

6. Typical Performance Characteristics

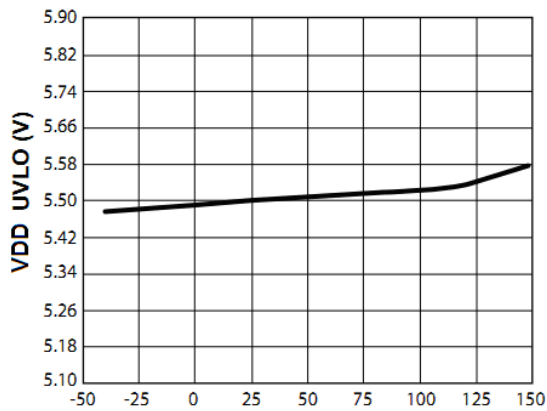


Figure 6.1 VDD UVLO vs. Temperature

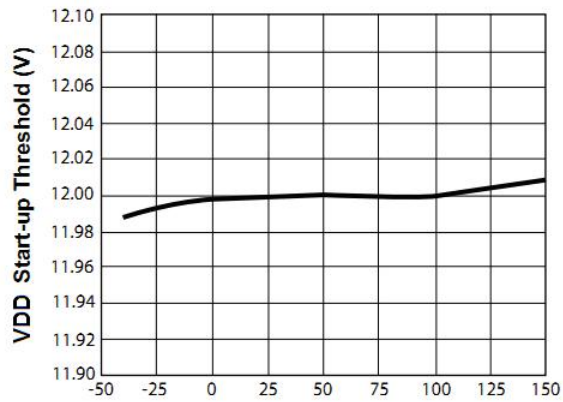


Figure 6.2 Start-Up Threshold vs. Temperature

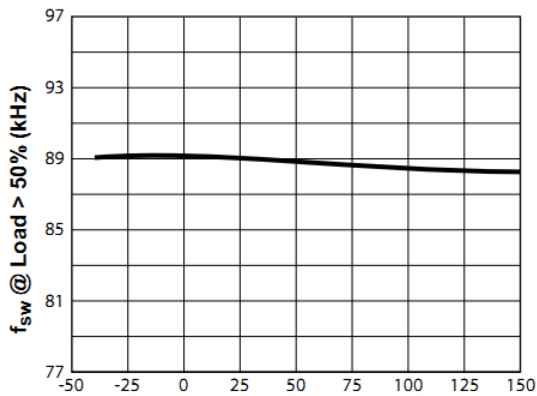


Figure 6.3 Switching Frequency vs. Temperature

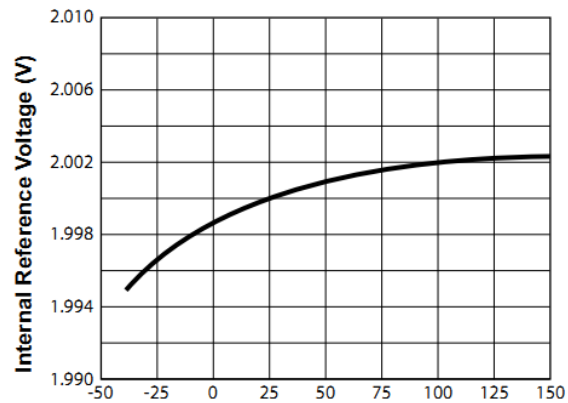


Figure 6.4 Internal Reference vs. Temperature

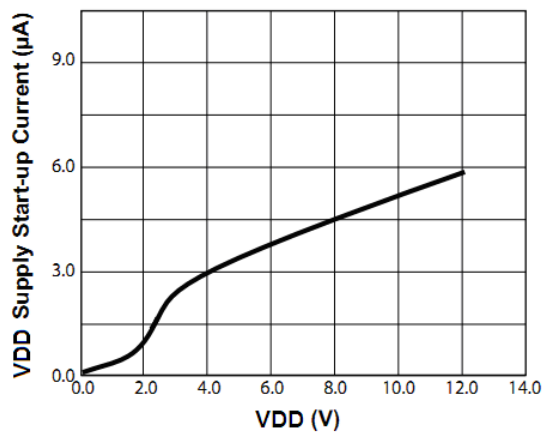


Figure 6.5 VDD vs. VDD Supply Start-up Current

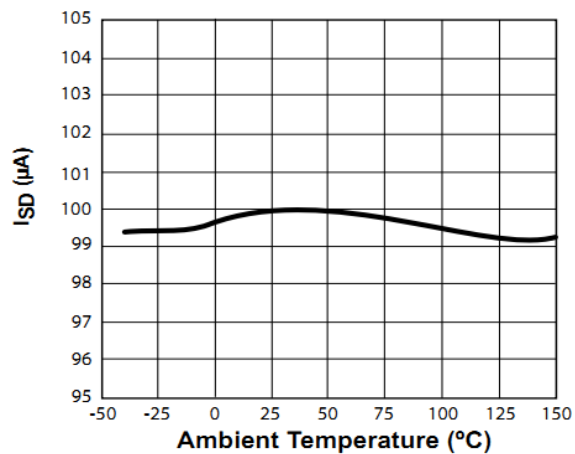


Figure 6.6 I_{SD} vs. Temperature

Notes:

Note1: Operating frequency varies based on the load conditions, see Section 7.6 for more details.

7. Theory of Operation

The G5199 is a digital controller which uses a new, proprietary primary-side control technology to eliminate the opto-isolated feedback and secondary regulation circuits required in traditional designs. This results in a low-cost solution for low power AC/DC adapters. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, GlobalSemi's digital control technology enables fast dynamic response, tight output regulation, and full featured circuit protection with primary-side control.

Referring to the block diagram in Figure 2.1, the G5199 operates in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external MOSFET gate voltage. The I_{SENSE} is an analog input configured to sense the primary current in a voltage form. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the I_{SENSE} to compare with, and it varies in the range of 0.23 V (typical) to 1.00 V (typical) under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The G5199 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant current operation is achieved without the need for any secondary-side sense and control circuits.

The G5199 uses adaptive multi-mode PWM/PFM control to dynamically change the MOSFET switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique MOSFET quasi-resonant switching to further improve efficiency and reduce EMI. Built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), and I_{SENSE} fault detection. In particular, it ensures that power supplies built with the G5199 can meet 5-star energy rating requirement and achieve fast dynamic load response in typical 12 W and above compact adapter/charger applications.

GlobalSemi's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

7.1 Pin Detail

Pin 1 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation..

Pin 2 – SD

External shutdown control. If the voltage at this pin is lower than 1.2 V (typical) at the beginning of start-up or lower than 1.0 V (typical) during normal operation, then the IC shuts down. Leave this pin unconnected if the shutdown control is not used (Refer to Section 7.14).

Pin 3 – MULTI

Multi-function pin. Used to configure external cable drop compensation (CDC) at the beginning of start-up and provide over-voltage protection during normal operation by sensing output voltage via auxiliary winding.

Pin 4 – ASU

Control signal for active startup device. This signal is pulled low after start-up is finished to cut off the active device.

Pin 5 – I_{SENSE}

Primary current sense. Used for cycle-by-cycle peak current control and limit..

Pin 6 – OUTPUT

Gate drive for the external power MOSFET switch.

Pin 7 – GND

Ground.

Pin 8 – VDD

Power supply for the controller during normal operation. The controller will start up when VDD reaches 12.0 V (typical) and will shut down when the VDD voltage drops below 5.5 V (typical). A decoupling capacitor of 0.1 μ F or so should be connected between the VDD pin and GND.

7.2 Active Start-up and Soft-start

Refer to Figure 4.1 for active start-up circuit using external depletion mode NFET. Prior to start-up, the ENABLE signal is low, and the ASU pin voltage closely follows the VDD pin voltage, as shown in Figure 7.1. Consequently, the depletion mode NFET is turned on,

allowing the start-up current to charge the VDD bypass capacitor. When the VDD bypass capacitor is charged to a voltage higher than the start-up threshold $V_{DD(ST)}$, the ENABLE signal becomes active and the G5199 begins to perform initial OTP check (See Section 7.14), followed by CDC configuration (See Section 7.12). Afterwards, the G5199 commences soft-start function. During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses will be small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator. If at any time the VDD voltage drops below under-voltage lockout (UVLO) threshold $V_{DD(UVL)}$ then the G5199 goes to shutdown. At this time ENABLE signal becomes low and the VDD capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

While the ENABLE signal initiates the soft-start process, it also pulls down the ASU pin voltage at the same time, which turns off the depletion NFET, thus minimizing the no-load standby power consumption.

In applications where active start-up is not needed, the start-up resistor can be directly connected to the VDD pin without using the active start-up device, and the ASU pin can be left unconnected. Refer to Figure 4.2 for the application circuit.

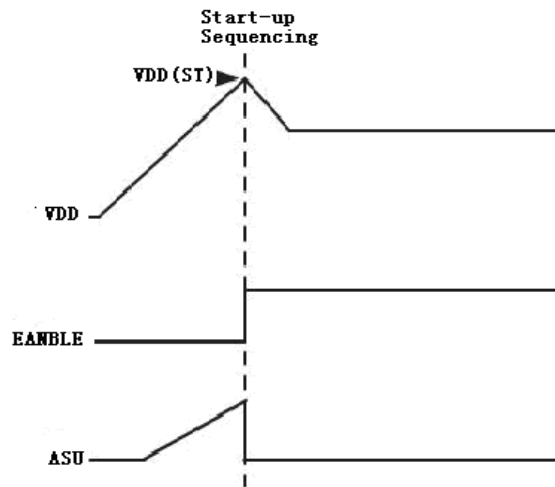


Figure 7.1: Start-up Sequencing Diagram

7.3 Understanding Primary Feedback

Figure 7.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from rectified sinusoid $v_g(t)$. The energy $E_g(t)$ is stored in the magnetizing inductance L_M . The rectifying diode D1 is reverse biased and the load current I_O is supplied by secondary capacitor C_O . When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

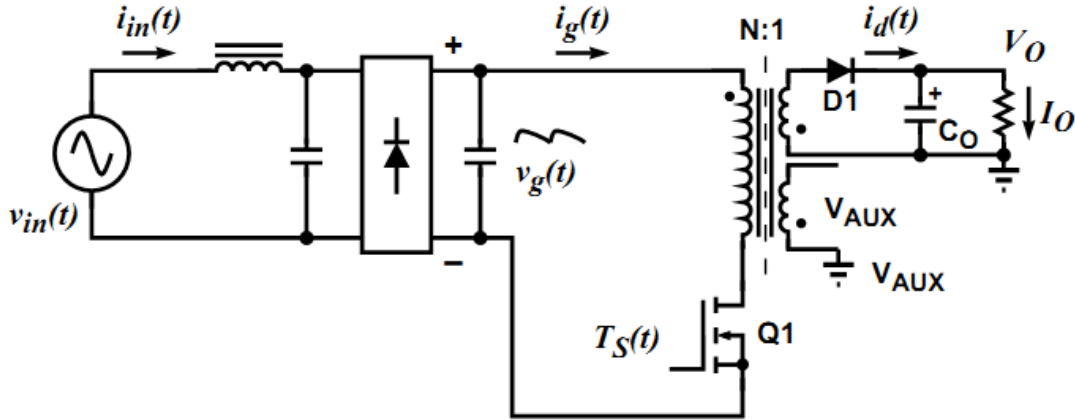


Figure 7.2: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current need to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O . The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \quad (7.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \quad (7.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g_peak}(t)^2 \quad (7.3)$$

When Q1 turns off at t_o , $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_o , the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g_peak}(t) \quad (7.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

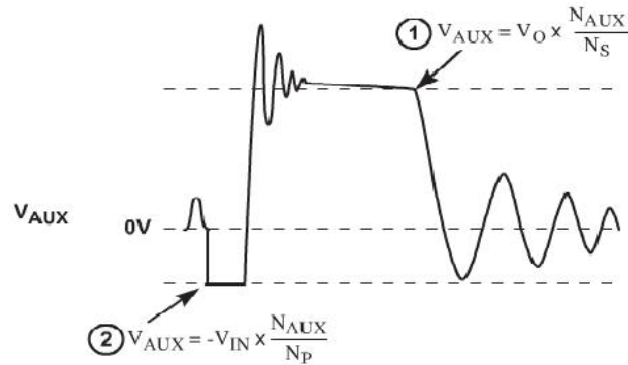


Figure 7.3: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S} (V_O + \Delta V) \quad (7.5)$$

and reflects the output voltage as shown in Figure 7.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage will be a fixed ΔV . Furthermore, if the voltage can be read when the secondary current is small, ΔV will also be small. With the G5199, ΔV can be ignored.

The real-time waveform analyzer in the G5199 reads this information cycle by cycle. The part then generates a feedback voltage V_{FB} . The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

7.4 Constant Voltage Operation

After soft-start has been completed, the digital control block measures the output conditions. It determines output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (T_{ON}) and off time (T_{OFF}) in order to meet the output voltage regulation requirements.

If no voltage is detected on V_{SENSE} it is assumed that the auxiliary winding of the transformer is either open or shorted and the G5199 shuts down.

7.5 Constant Current Operation

The constant current (CC) mode is useful in battery charging applications. During this mode of operation the G5199 will regulate the output current at a constant level regardless of the output voltage, while avoiding continuous conduction mode.

To achieve this regulation the G5199 senses the load current indirectly through the primary current. The primary current is detected by the I_{SENSE} pin through a resistor from the MOSFET source to ground.

The G5199 also provides a product option to disable the CC mode operation. If the power supply enters into the CC mode during normal operation, this product option will shut down the power supply. This feature serves as an over-load protection and can be used in certain adapter applications.

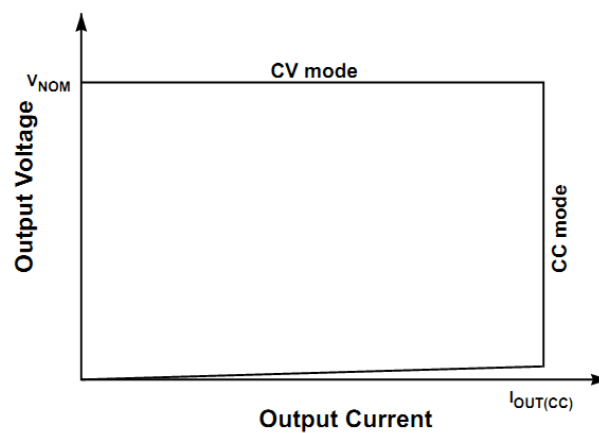


Figure 7.4: Power Envelope

7.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The G5199 uses a proprietary adaptive multi-mode PWM /PFM control to dramatically improve the light-load efficiency and thus the overall average efficiency.

During the constant voltage (CV) operation, the G5199 normally operates in a pulse-width-modulation (PWM) mode during heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time T_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. During the PFM mode, the MOSFET is turned on for a set duration under a given instantaneous rectified AC input voltage, but its off time is modulated by the load current. With a decreasing load current, the off time increases and thus the switching frequency decreases.

When the switching frequency approaches to human ear audio band, the G5199 Transitions to a second level of PWM mode, namely Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 25 kHz in order to avoid audible noise. As the load current is further reduced, the G5199 transitions to a second level of PFM mode, namely Deep PFM mode (DPFM), which can reduce the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. Therefore, the power converter practically produces no audible noise, while achieving high efficiency across varying load conditions.

As the load current reduces to very low or no-load condition, the G5199 transitions from the DPFM to the third level of PWM mode, namely Deep-Deep PWM mode (DDPWM), where the switching frequency is fixed at around 1.8 kHz. The G5199 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every PWM/PFM switching cycle, during all PFM and PWM modes and in both CV and CC operations. This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. Together these innovative digital control architecture and algorithms enable the G5199 to achieve highest overall efficiency and lowest EMI, without causing audible noise over entire operating range.

7.7 Less Than 30 mW No-Load Power with Fast Load Transient Response

The G5199 features a distinctive DDPWM control at no-load conditions to help achieve ultra-low no-load power consumption (< 30 mW for typical 12 W and above applications) and meanwhile to ensure fast dynamic load response. The power supply system designs including the pre-load resistor selection should ensure the power supply can operate in the DDPWM mode at the steady-state no-load condition. If the pre-load resistor is too small, the no-load power consumption will increase; on the other hand, if it is too large, the output voltage may increase and even cause over-voltage since the switching frequency is fixed at around 1.8 kHz. For typical designs, the pre-load resistor is in the range of 3 kW to 5 kW.

Aside from the appropriate use of pre-load resistor, the G5199 enjoys a few other features to bring down no-load power consumption as well. First, the G5199 implements an intelligent low-power management technique that achieves ultra-low chip operating current at the no-load, typically less than 350 μ A. Second, a low UVLO threshold of 5.5 V (typical) enables the power supply system design to have a low VDD voltage at the

no-load operation in order to minimize the no-load power. In addition, the active start-up scheme with depletion mode NFET eliminates the start-up resistor power consumption after the ENABLE signal becomes active. All together these features ensure lowest system cost power supplies built with the G5199 can achieve less than 30 mW no-load power consumption at 230 VAC input, and very tight constant voltage and constant current regulation over the entire operating range in typical 12 W and above compact adapter/charger applications.

While achieving ultra-low no-load power consumption, the G5199 implements innovative proprietary digital control technology to intelligently detect any load transient events, and achieve fast dynamic load response for both one-time and repetitive load transients. In particular, for load transients that are demanded in some applications from no load to full load, the G5199 can still maintain a fast enough response to meet the most stringent requirements, with the no-load operating frequency designed at around 1.8 kHz.

7.8 Variable Frequency Operation Mode

At each of the switching cycles, the falling edge of V_{SENSE} will be checked. If the falling edge of V_{SENSE} is not detected, the off-time will be extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110 μ s. When the transformer reset time reaches 110 μ s, the G5199 shuts off.

7.9 Internal Loop Compensation

The G5199 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20 dB of gain margin.

7.10 Voltage Protection Features

The secondary maximum output DC voltage is limited by the G5199. When the V_{SENSE} signal exceeds the output OVP threshold at point 1 indicated in Figure 7.3 the G5199 shuts down. For this V_{SENSE} -based OVP, latch function is available by product options given in Section 2.3.

The G5199 protects against input line under-voltage by setting a maximum T_{ON} time. Since output power is proportional to the squared $V_{IN}T_{ON}$ product, then for a given output power, as V_{IN} decreases the T_{ON} will increase. Thus by knowing when the maximum T_{ON} time occurs the G5199 detects that the minimum V_{IN} is reached, and shuts down. The maximum t_{ON} limit is set to 13.8 μ s. Also, the G5199 monitors the voltage on the VDD pin

and when the voltage on this pin is below UVLO threshold the IC shuts down immediately.

When any of these faults are met the IC remains biased to discharge the VDD supply. Once VDD drops below UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting start-up until the fault condition is removed. For the latched OVP version, the controller can only start-up when the fault is removed and input is unplugged to allow VDD to drop 1.0 V below UVLO threshold.

7.11 PCL, OCP and SRS Protection

Peak-current limit (PCL), over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built-in to the G5199. With the I_{SENSE} pin the G5199 is able to monitor the peak primary current. This allows for cycle-by-cycle peak current control and limit. When the peak primary current multiplied by the I_{SENSE} resistor is greater than 1.15 V, over-current is detected and the IC will immediately turn off the gate driver until the next cycle. The output driver will send out a switching pulse in the next cycle, and the switching pulse will continue if the OCP threshold is not reached; or, the switching pulse will turn off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the G5199 shuts down.

If the I_{SENSE} resistor is shorted there is a potential danger that over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault after start-up and shut down immediately. The VDD will be discharged since the IC remains biased. Once VDD drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to startup, but does not fully start-up until the fault condition is removed.

7.12 CDC Configuration

The G5199 incorporates an innovative approach to allow users to configure cable drop compensation (CDC) externally. This configuration is only performed once. It is completed after the initial OTP check but before the soft-start commences. During the CDC configuration, the internal digital control block senses the external resistance value between the MULTI pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

Figure 4.1 shows a simple circuit to set CDC level by connecting a resistor, R_{CDC} , from the MULTI pin to ground. The G5199 provides five levels of CDC configurations: 0, 75 mV, 150 mV, 300 mV, and 450 mV. Table 7.1 below shows the resistance range for each

of the five CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The “Cable Comp” specified in Table 7.1 refers to the voltage increment at PCB end from no-load to full-load conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the nominal output voltage of 5 V. For different output voltage, the actual voltage increment needs to be scaled accordingly. To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply by the maximum output current.

For each of the CDC levels, the internal V_{SENSE} -based OVP thresholds are different. Table 7.1 also lists the typical OVP thresholds for each CDC level.

Table 7.1 Recommended resistance range and corresponding CDC levels for 5V output

| CDC Level | 1 | 2 | 3 | 4 | 5 |
|----------------------------------|--------|-------------|-------------|-----------|-----------|
| R_{CDC} Range (k Ω) | 0-2.20 | 2.37 – 3.21 | 3.40 – 4.64 | 4.87–6.65 | 6.98 – X* |
| Cable Comp (mV) | 0 | 75 | 150 | 300 | 450 |
| V_{SENSE} -based OVP Threshold | 1.838 | 1.861 | 1.884 | 1.930 | 1.976 |

* The resistance can be as high as 100k Ω , provided MULTI pin does not float, which causes device to shut down.

7.13 External MULTI-Based OVP

In the G5199, the MULTI pin can also be used to provide the external over-voltage protection (OVP) besides fulfilling the CDC configuration. This external MULTI-based OVP serves as a supplemental or extra protection in addition to the V_{SENSE} -based OVP. The circuit implementation can be found in Figure 7.5, where two resistors R1 and R2 form a voltage divider to sense output voltage via auxiliary winding, with the tapping point connected to the MULTI pin. During the CDC configuration the G5199 does not send out any drive signal at OUTPUT pin, and the switch Q1 remains in off-state. The resistors R1 and R2 are essentially connected in parallel since the bias winding is virtually shorted. Consequently, the paralleled resistance of R1 and R2 sets the CDC level. Meanwhile, during normal operation, the MULTI pin reflects output voltage in real-time, in the similar fashion as the V_{SENSE} does at point 1 in Figure 7.3. The ratio of R1 to R2 sets the external OVP threshold.

The resistance values for the resistor divider, R1 and R2, can be derived as follows. First, for the given CDC level, the paralleled resistance of R1 and R2 should be within the

range listed in Table 7.1:

$$R_{CDC} = \frac{R_1 \times R_2}{R_1 + R_2} \quad (7.6)$$

Second, during normal operation the voltage divider, R1 and R2, sets the desired OVP threshold:

$$\left(\frac{N_{AUX}}{N_{SEC}} \right) \times V_{OVP} \times \left(\frac{R_2}{R_2 + R_1} \right) \geq V_{SD-TH(R)} \quad (7.7)$$

where N_{AUX} is the number of turns for the bias winding, N_{SEC} is the number of turns for the secondary winding, V_{OVP} is the desired OVP tripping point, and $V_{SD-TH(R)}$ is the internal comparator threshold (1.015 V typically) for OVP detection. The combination of Equations (9.6) and (9.7) leads to

$$R_1 = \left(\frac{N_{AUX}}{N_{SEC}} \right) \times R_{CDC} \times \left(\frac{V_{OVP}}{V_{SD-TH(R)}} \right)$$

$$R_2 = \left(\frac{R_1}{R_1 - R_{CDC}} \right) \times R_{CDC} \quad (7.8)$$

It is recommended the R_{CDC} value is taken as the median value of the resistance range as given in Table 7.1, and R_1 and R_2 can then be readily derived from Equation (7.8). It should be noted when the MULTI pin is used to provide external OVP, an additional constraint will be applied to the resistance range given in Table 7.1. Since for the OVP configuration in Figure 7.5, a large negative voltage may occur to the auxiliary winding (V_x in Figure 7.5) during the switch on-time, which can cause a negative current flowing out of the MULTI pin. Care needs to be taken to ensure R_1 and R_2 are large enough, so that the resulting negative current is less than the maximum allowed current, specified in Section 3.0.

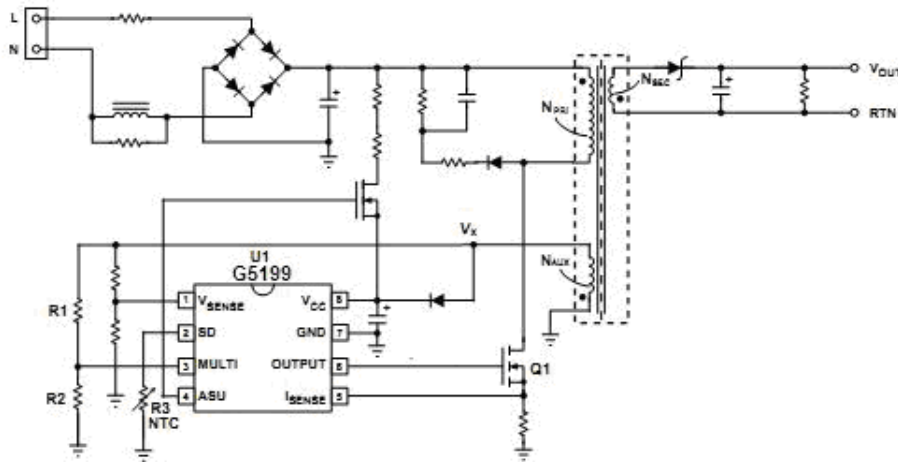


Figure 7.5: Typical Application Circuit with CDC, OVP and OTP Implemented

7.14 External OTP

The G5199 can be configured to provide external over-temperature protection (OTP) by connecting a Negative-Temperature-Coefficient (NTC) resistor from SD pin to GND. Internally, a 100 μ A current source is injected to the SD pin, which generates a voltage proportional to the NTC resistance. At high ambient temperature, the NTC resistance becomes low, which results in a low voltage at the SD pin. If the SD pin voltage drops below an internally-set threshold, then the OTP is triggered, and the G5199 shuts down. In the G5199, the external OTP has a built-in hysteresis by having two thresholds. Before start-up, the OTP is triggered if the SD pin voltage is less than 1.2 V; otherwise the device begins the CDC configuration (See Section 7.12), then followed by a normal soft-start process. During normal operation, the OTP threshold is switched to 1.0 V, and the device only shuts down when the SD pin voltage is less than 1.0 V.

During normal operation, the external OVP and OTP detections alternate every eight cycles. During the eight-cycle window of OVP detection, the voltage at the MULTI pin is fed into the internal comparator's non-inverting input. If the voltage of this pin is above 1.015 V at the instant corresponding to point 1 indicated in Figure 7.3 for consecutive several cycles, then OVP is triggered. Contrarily, during the external OTP detection window, if the voltage at SD pin is below 1.0 V for consecutive several cycles, then the OTP is triggered, and the device shuts down.

The SD pin and MULTI pin can be configured to provide different types of applications. Figure 7.6 shows four basic configurations:

In Scheme (a), the MULTI pin is directly connected to ground, which sets CDC level to be 1 (i.e. no CDC). On the other side, leaving the SD pin unconnected disables the OTP function.

In Scheme (b), CDC is set to level 1, as in Scheme (a) by grounding the MULTI pin. An NTC resistor in paralleled with a capacitor enables the external OTP protection. Note this capacitor is only for decoupling purpose. Its capacitance needs to be less than 47 pF, otherwise the voltage at this pin can be delayed too much, causing unwanted behaviors.

In Scheme (c), a resistor from the MULTI pin to ground allows to set the desired CDC level. Similarly, the NTC resistor enables the external OTP, as in Scheme (b).

In Scheme (d), the connections to the MULTI and the SD pins are complete as in Figure 7.5, allowing for any level of CDC configuration, and meanwhile enabling the external OTP and OVP.

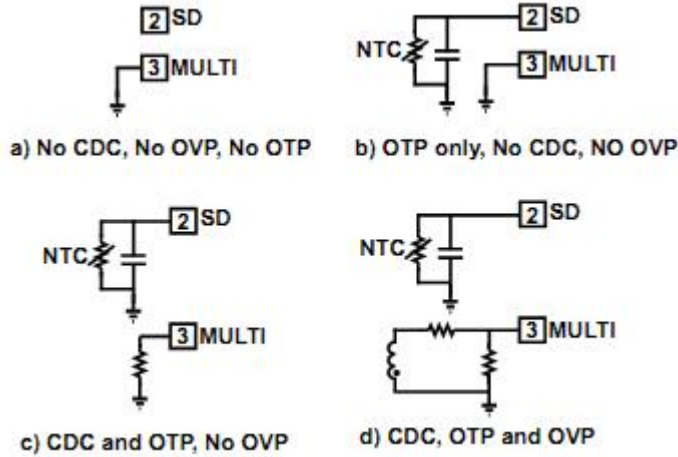


Figure 7.6: MULTI and SD Pins Configurations

7.15 Latch and Release

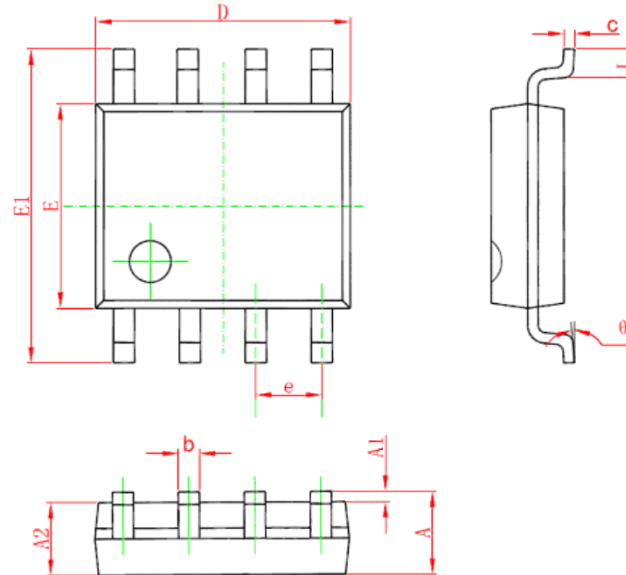
In the G5199, both OTP and OVP (including V_{SENSE} -based and the external MULTI-based OVP) can be latched whereby the G5199 does not attempt to start again even with the fault cleared. In the latch state, the controller recycles itself by periodically ramping VDD up and down between VDD(ST) and VDD(UVL), and the controller will not start up, provided the input stays connected to the AC source. To get out of the latch state, unplugging the input from the AC source is required, so that the VDD is allowed to drop 1.0 V below VDD(UVL) to release the latch.

For a fast release, VDD capacitor can be charged directly from the AC source before the diode-bridge rectifier instead of the bulk capacitor. In this way, when the input is unplugged, the VDD capacitor is immediately cut off from the bulk capacitor, allowing for much faster discharging to release the latch, and initiate a normal start-up thereafter.

8. Package Information

SOIC-8

8-Pin Plastic SOP



| Symbol | Dimension in Millimeters | | Dimensions in Inches | |
|--------|--------------------------|-------|----------------------|-------|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.050 | 0.250 | 0.002 | 0.010 |
| A2 | 1.250 | 1.650 | 0.049 | 0.065 |
| b | 0.310 | 0.510 | 0.012 | 0.020 |
| c | 0.100 | 0.250 | 0.004 | 0.010 |
| D | 4.700 | 5.150 | 0.185 | 0.203 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270(BSC) | | 0.050(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Data and specifications subject to change without notice.

This product has been designed and qualified for Industrial Level and Lead-Free.

Qualification Standards can be found on GS's Web site.

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