

Two Remote Temperature Sensors with SMBus Serial Interface and System Reset Circuit

Features

- Measures Two Remote Temperatures
 - No Calibration Required
 - SMBus 2-Wire Serial Interface
 - Programmable Under/Over-temperature Alarms
 - Programmable Thermal Shutdown Signal
 - Supports SMBus Alert Response
 - Accuracy: $\pm 5^{\circ}\text{C}$ (-40°C to $+125^{\circ}\text{C}$, remote)
 $\pm 3^{\circ}\text{C}$ ($+60^{\circ}\text{C}$ to $+100^{\circ}\text{C}$, remote)
 - 4.5V to 5.5V Supply Range
 - Precision Monitoring of 5V Power-Supply Voltage
 - 140ms Min Power-On Reset Pulse Width
- RESET Output**
- Guaranteed $\overline{\text{RESET}}$ Valid to $V_{\text{CC}}=1\text{V}$
 - Power Supply Transient Immunity
 - No External Components needed for reset function
 - Small, 16-Pin SSOP Package

Applications

- Desktop and Notebook
- Central Office Computers
- Telecom Equipment
- Smart Battery Packs
- Test and Measurement
- LAN Servers
- Multi-Chip Modules
- Industrial Controls

General Description

The G771 contains a precise digital thermometer, a system-reset circuit, and a programmable thermal shutdown signal.

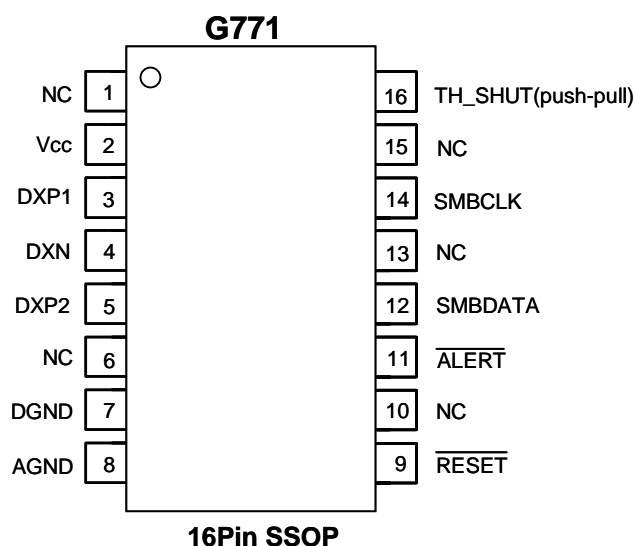
The thermometer reports the temperature of 2 remote sensors. The remote sensors are diode-connected transistors typically a low-cost, easily mounted 2N3904 NPN type that replace conventional thermistors or thermocouples. Remote accuracy is $\pm 5^{\circ}\text{C}$ for multiple transistor manufacturers, with no calibration needed. The remote channel can also measure the die temperature of other ICs, such as microprocessors, that contain an on-chip, diode-connected transistor.

The 2-wire serial interface accepts standard System Management Bus (SMBus™) Write Byte, Read Byte, Send Byte, and Receive Byte commands to program the alarm thresholds and to read temperature data. The data format is 7 bits plus sign, with each bit corresponding to 1°C , in two's-complement format. Measurements can be done automatically and autonomously, with the conversion rate programmed by the user or programmed to operate in a single-shot mode. The adjustable rate allows the user to control the supply-current drain.

Ordering Information

| PART* | TEMP. RANGE | PIN-PACKAGE |
|-------|---|-------------|
| G771 | -55°C to $+125^{\circ}\text{C}$ | 16SSOP |

Pin Configuration



The G771 also contains a microprocessor (μP) supervisory circuit used to monitor the power supplies in μP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 5V-powered circuits. This circuit asserts a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 140ms after V_{CC} has risen above the reset threshold. The G771 has an active-low $\overline{\text{RESET}}$ output. The reset comparator is designed to ignore fast transients on V_{CC} . Reset threshold of this circuit is set to 4.38V.

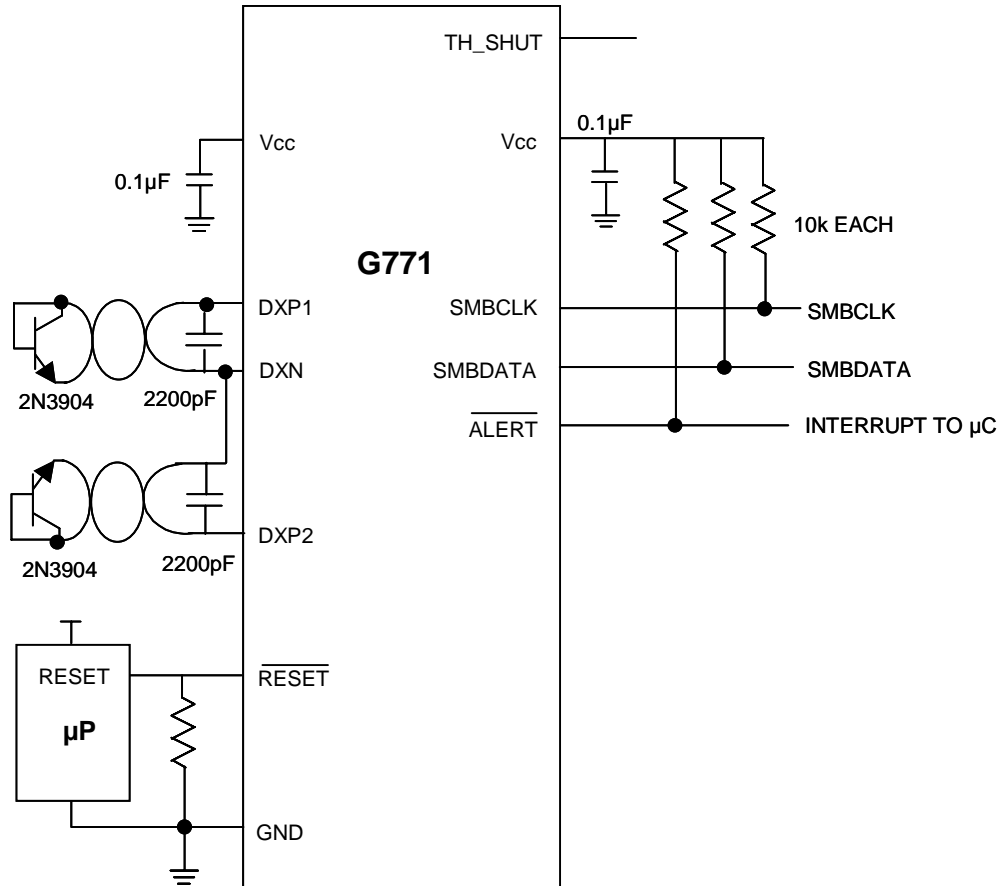
When the temperature of DX1 reaches or exceeds

the T_{crit1} (SMBus 35h) threshold consecutively for the times equal to the number of faults of the FQ_TH_SHUT registers, TH_SHUT pin becomes logic high. The same mechanism is duplicated for DX2. Therefore, either one of DX1, DX2 continuously over their respective T_{crit} , the TH_SHUT will assert logic high to indicate a thermal shutdown event.

The G771's SMBus device address is fixed to be 7Ah for write and 7Bh for read.

The G771 is available in a small, 16-pin SSOP surface-mount package.

Typical Operating Circuit



Absolute Maximum Ratings

| | |
|---|----------------------------------|
| V _{cc} to GND..... | -0.3V to +6V |
| DXP1, DXP2 to GND..... | 0.3V to (V _{cc} + 0.3V) |
| DXN to GND..... | -0.3V to +0.8V |
| SMBCLK, SMBDATA, $\overline{\text{ALERT}}$ to GND.... | -0.3V to +6V |
| SMBDATA, $\overline{\text{ALERT}}$ Current..... | -1mA to +50mA |
| DXN Current..... | ±1mA |

| | |
|--|-----------------|
| ESD Protection (human body model)..... | 2000V |
| Continuous Power Dissipation (T _A = +70°C) SSOP (de-rate 8.30mW/°C above +70°C)..... | 667mW |
| Operating Temperature Range..... | -55°C to +125°C |
| Junction Temperature..... | +150°C |
| Storage temperature Range..... | -65°C to +165°C |
| Lead Temperature (soldering, 10sec)..... | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics
(V_{cc} = + 5V, T_A = 60°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS | |
|---|--|---|-----|------|-------|----|
| Temperature Sensor | | | | | | |
| Temperature Resolution (Note 1) | Monotonicity guaranteed | 8 | | | Bits | |
| Temperature Error, Remote Diode (Notes 2 and 3) | T _R = 0°C to +125°C | -5 | | 5 | °C | |
| | T _R = 60°C to +100°C | -3 | | 3 | | |
| Temperature Error, On-chip Diode (Notes 1 and 2) | T _A = +60°C to +100°C | | ±3 | | °C | |
| Supply-Voltage Range | | 4.5 | 5 | 5.5 | V | |
| Under-voltage Lockout Threshold | V _{cc} input, disables A/D conversion, rising edge | 2.6 | 2.8 | 2.95 | V | |
| Under-voltage Lockout Hysteresis | | | 50 | | mV | |
| Power-On Reset Threshold | V _{cc} , falling edge | 1.0 | 1.7 | 2.5 | V | |
| POR Threshold Hysteresis | | | 50 | | mV | |
| Standby Supply Current | Logic inputs forced to V _{cc} or GND | SMBus static | 3 | 10 | µA | |
| | | Hardware or software standby, SMBCLK at 10kHz | 200 | | | |
| Average Operating Supply Current | Auto-convert mode, average measured over 4sec. Logic inputs forced to V _{cc} or GND | 0.25 conv/sec | 250 | 300 | µA | |
| | | 2.0 conv/sec | 300 | 350 | | |
| Conversion Time | From stop bit to conversion complete (all channels) | 94 | 125 | 156 | ms | |
| Conversion Rate Timing Error | Auto-convert mode | -25 | | 25 | % | |
| Remote-Diode Source Current | DXP forced to 1.5V | High level | 120 | 160 | 200 | µA |
| | | Low level | 15 | 20 | 25 | |
| SMBus Interface | | | | | | |
| Logic Input High Voltage | SMBCLK, SMBDATA; V _{cc} = 4.5V to 5.5V | 2.4 | | | V | |
| Logic Input Low Voltage | SMBCLK, SMBDATA; V _{cc} = 4.5V to 5.5V | | | 0.8 | V | |
| Logic Output Low Sink Current | , SMBDATA forced to 0.4V | 6 | | | mA | |
| Output High Leakage Current | forced to 5.5V | | | 1 | µA | |
| Logic Input Current | Logic inputs forced to V _{cc} or GND | -2 | | 2 | µA | |
| SMBus Input Capacitance | SMBCLK, SMBDATA | | 5 | | pF | |
| SMBus Clock Frequency | (Note 4) | DC | | 100 | KHz | |
| SMBCLK Clock Low Time | t _{LOW} , 10% to 10% points | 4.7 | | | µs | |
| SMBCLK Clock High Time | t _{HIGH} , 90% to 90% points | 4 | | | µs | |
| SMBus Start-Condition Setup Time | | 4.7 | | | µs | |
| SMBus Repeated Start-Condition Setup Time | t _{SU: STA} , 90% to 90% points | 500 | | | ns | |
| SMBus Start-Condition Hold Time | t _{HD: STA} , 10% of SMBDATA to 90% of SMBCLK | 4 | | | µs | |
| SMBus Start-Condition Setup Time | t _{SD: STO} , 90% of SMBDATA to 10% of SMBDATA | 4 | | | µs | |
| SMBus Data Valid to SMBCLK Rising-Edge Time | t _{SU: DAT} , 10% or 90% of SMBDATA to 10% of SMBCLK | 800 | | | ns | |
| SMBus Data-Hold Time | t _{HD: DAT} (Note 5) | 0 | | | µs | |
| SMBCLK Falling Edge to SMBus Data-Valid Time | Master clocking in data | | | 1 | µs | |

Electrical Characteristics (continued)
(V_{CC} =full range, T_A= 60°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------|-----------------|--|----------------------|-----|-----|-------|
| Reset Threshold | V _{TH} | | 4.2 | 4.4 | 4.5 | V |
| Reset Active Timeout Period | | | | 340 | | ms |
| Output Voltage Low | V _{OL} | V _{CC} =V _{TH} min I _{SINK} =3.2mA | | | 0.4 | V |
| RESET Output Voltage High | V _{OH} | V _{CC} >V _{TH} max, I _{SOURCE} =5.0mA | V _{CC} -1.5 | | | V |

Note 1: Guaranteed but not 100% tested.

Note 2: Quantization error is not included in specifications for temperature accuracy. For example, if the G771 device temperature is exactly +66.7°C, or +68°C (due to the quantization error plus the +1/2°C offset used for rounding up) and still be within the guaranteed ±3°C error limits for the +60°C to +100°C temperature range. See Table3.

Note 3: A remote diode is any diode-connected transistor from Table1. T_R is the junction temperature of the remote diode. See Remote Diode Selection for remote diode forward voltage requirements.

Note 4: The SMBus logic block is a static design that works with clock frequencies down to DC. While slow operation is possible, it violates the 10kHz minimum clock frequency and SMBus specifications, and may monopolize the bus.

Note 5: Note that a transition must internally provide at least a hold time in order to bridge the undefined region (300ns max) of SMBCLK's falling edge.

Pin Description

| PIN | NAME | FUNCTION |
|--------------|-----------------|---|
| 1,6,10,13,15 | NC | Not connected. |
| 2 | V _{CC} | Supply Voltage Input, 4.5V to 5.5V. Bypass to GND with a 0.1μF capacitor. |
| 3 | DXP1 | Combined Current Source and A/D Positive Input for remote-diode channel 1. Do not leave DXP1 floating; tie DXP1 to DXN if no remote diode on channel 1 is used. Place a 2200pF capacitor between DXP1 and DXN for noise filtering. |
| 4 | DXN | Combined Current Sink and A/D Negative Input. DXN is common negative node of both remote diodes on channel 1 and 2. The traces of DXP1-DXN and DXP2-DXN pairs should be routed independently. The common DXN should be connected together as close as possible to the IC. DXN is internally connected to the GND pin for signal ground use. |
| 5 | DXP2 | Combined Current Source and A/D Positive Input for remote-diode channel 2. Do not leave DXP2 floating; tie DXP2 to DXN if no remote diode on channel 2 is used. Place a 2200pF capacitor between DXP2 and DXN for noise filtering. |
| 7 | DGND | Digital Ground. |
| 8 | AGND | Analog Ground. |
| 9 | RESET | RESET Output remains low while V _{CC} is below the reset threshold, and for 240ms after V _{CC} rises above the reset threshold. |
| 11 | ALERT | SMBus Alert (interrupt) Output, open drain. |
| 12 | SMBDATA | SMBus Serial-Data Input / Output, open drain. |
| 14 | SMBCLK | SMBus Serial-Clock Input. |
| 16 | TH_SHUT | Thermal Shutdown Output, push-pull output. |

Detailed Description

The G771 (patents pending) consists of two temperature sensors, one on-chip temperature sensor and provides system-reset function.

The temperature sensor is designed to work in conjunction with an external micro-controller (μC) or other intelligence in thermostatic, process-control, or monitoring applications. The μC is typically a powermanagement or keyboard controller, generating SMBus serial commands by "bit-banging" general-purpose input-output (GPIO) pins or via a dedicated SMBus interface block.

Essentially a 12-bit serial analog-to-digital converter (ADC) with a sophisticated front end, the G771 contains a switched current source, a multiplexer, an ADC, an SMBus interface, a reset circuit and associated control logic (Figure 1).

Temperature data from the ADC is loaded into two data registers, where it is automatically compared with data previously stored in four over/under-temperature alarm registers.

ADC and Multiplexer

The ADC is an averaging type that integrates over a 60ms period (each channel, typical).

The multiplexer automatically steers bias currents through two remote diodes, measures their forward voltages, and computes their temperatures. All channels are converted automatically once the conversion process has started, either in free-running or single-shot mode. If one of the two channels is not used, the device still performs all measurements, and the user can simply ignore the results of the unused channel. If the remote diode channel is unused, tie DXPx to DXN rather than leaving the pins open.

The DXN input is internally connected to the ground node inside the chip to set up the analog to digital (A/D) inputs for a differential measurement. The worst-case DXP-DXN differential input voltage range is 0.25V to 0.95V.

Excess resistance in series with the remote diode causes about $+1/2^\circ\text{C}$ error per ohm. Likewise, $200\mu\text{V}$ of offset voltage forced on DXP-DXN causes about 1°C error.

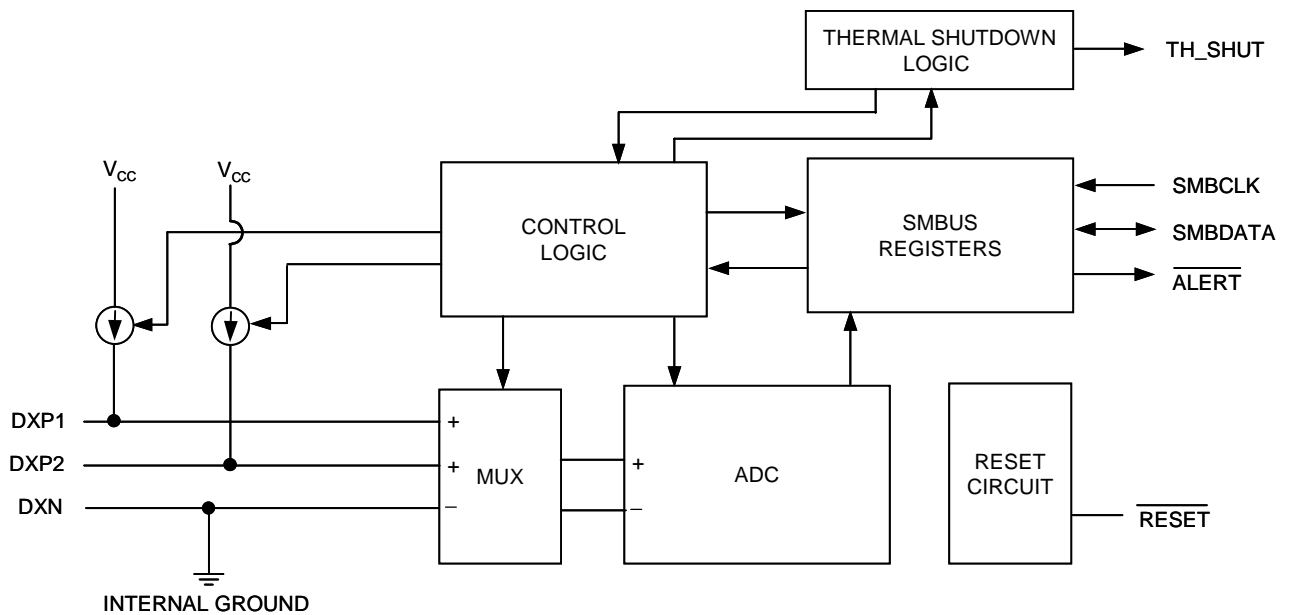


Fig 1. Functional Diagram

A/D Conversion Sequence

If a Start command is written (or generated automatically in the free-running auto-convert mode), both two channels are converted, and the results of both measurements are available after the end of conversion. A BUSY status bit in the status byte shows that the device is actually performing a new conversion; however, even if the ADC is busy, the results of the previous conversion are always available.

Remote-Diode Selection

Temperature accuracy depends on having a good-quality, diode-connected small-signal transistor. Accuracy has been experimentally verified for all of the devices listed in Table 1. The G771 can also directly measure the die temperature of CPUs and other integrated circuits having on-board temperature-sensing diodes. The transistor must be a small-signal type with a relatively high forward voltage; otherwise, the A/D input voltage range can be violated. The forward voltage must be greater than 0.25V at 10 μ A; check to ensure this is true at the highest expected temperature. The forward voltage must be less than 0.95V at 200A; check to ensure this is true at the lowest expected temperature. Large power transistors don't work at all. Also, ensure that the base resistance is less than 100 Ω . Tight specifications for forward current gain (+50 to +150, for example) indicate that the manufacturer has good process controls and that the devices have consistent VBE characteristics.

Thermal Mass and Self-Heating

Thermal mass can seriously degrade the G771's effective accuracy. The thermal time constant of the SSOP-16 package is about 140sec in still air. For the G771 junction temperature to settle to within +1 $^{\circ}$ C after a sudden +100 $^{\circ}$ C change requires about five time constants or 12 minutes. The use of smaller packages for remote sensors, such as SOT23s, improves the situation. Take care to account for thermal gradients between the heat source and the sensor, and ensure that stray air current across the sensor package do not interfere with measurement accuracy.

Table 1. Remote-Sensor Transistor Manufacturers

| MANUFACTURER | MODEL NUMBER |
|------------------------------|--------------|
| Philips | PMBS 3904 |
| Motorola (USA) | MMBT3904 |
| National Semiconductor (USA) | MMBT3904 |

Note: Transistors must be diode-connected (base shorted to collector).

ADC Noise Filtering

The ADC is an integrating type with inherently good noise rejection, especially of low-frequency signals such as 60Hz/120Hz power-supply hum. Micro-power operation places constraints on high-frequency noise rejection; therefore, careful PC board layout and

proper external noise filtering are required for high-accuracy remote measurements in electrically noisy environments.

High-frequency EMI is best filtered at DXP and DXN with an external 2200pF capacitor. This value can be increased to about 3300pF(max), including cable capacitance. Higher capacitance than 3300pF introduces errors due to the rise time of the switched current source.

Nearly all noise sources tested cause the ADC measurements to be higher than the actual temperature, typically by +1 $^{\circ}$ C to 10 $^{\circ}$ C, depending on the frequency and amplitude (see Typical Operating Characteristics).

PC Board Layout

Place the G771 as close as practical to the remote diode. In a noisy environment, such as a computer motherboard, this distance can be 4 in. to 8 in. (typical) or more as long as the worst noise sources (such as CRTs, clock generators, memory buses, and ISA/PCI buses) are avoided.

Do not route the DXP-DXN lines next to the deflection coils of a CRT. Also, do not route the traces across a fast memory bus, which can easily introduce +30 $^{\circ}$ C error, even with good filtering. Otherwise, most noise sources are fairly benign.

Route the DXP and DXN traces in parallel and in close proximity to each other, away from any high-voltage traces such as +12VDC. Leakage currents from PC board contamination must be dealt with carefully, since a 20M Ω leakage path from DXP to ground causes about +1 $^{\circ}$ C error.

Route the 2 pairs of DXP1-DXN and DXP2-DXN traces independently (Figure 2a). Connect the common DXN as close as possible to the DXN pin on IC (Figure 2a).

Connect guard traces to GND on either side of the DXP-DXN traces (Figure 2b). With guard traces in place, routing near high-voltage traces is no longer an issue.

Route through as few vias and crossunders as possible to minimize copper/solder thermocouple effects.

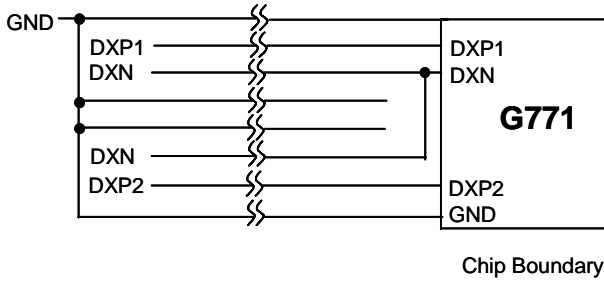
When introducing a thermocouple, make sure that both the DXP and the DXN paths have matching thermocouples. In general, PC board-induced thermocouples are not a serious problem. A copper-solder thermocouple exhibits 3 μ V/ $^{\circ}$ C, and it takes about 200 μ V of voltage error at DXP-DXN to cause a +1 $^{\circ}$ C measurement error. So, most parasitic thermocouple errors are swamped out.

Use wide traces. Narrow ones are more inductive and tend to pick up radiated noise. The 10 mil widths and spacing recommended on Figure 2 aren't absolutely necessary (as they offer only a minor improvement in leakage and noise), but try to use them where practical.

Keep in mind that copper can't be used as an EMI shield, and only ferrous materials such as steelwork will. Placing a copper ground plane between the DXP-DXN traces and traces carrying high-frequency noise signals do not help reduce EMI.

PC Board Layout Checklist

- Place the G771 close to a remote diode.
- Keep traces away from high voltages (+12V bus).
- Keep traces away from fast data buses and CRTs.
- Use recommended trace widths and spacing.
- Place a ground plane under the traces
- Use guard traces flanking DXP and DXN and connecting to GND.
- Route two DXPx-DXN pairs independently
- Connect the common DXN as close as possible to the DXN pin on IC.
- Place the noise filter and the 0.1µF V_{CC} bypass capacitors close to the G771.



- **Fig 2(a) Connect the common DXN as close as possible to the DXN pin on IC.**

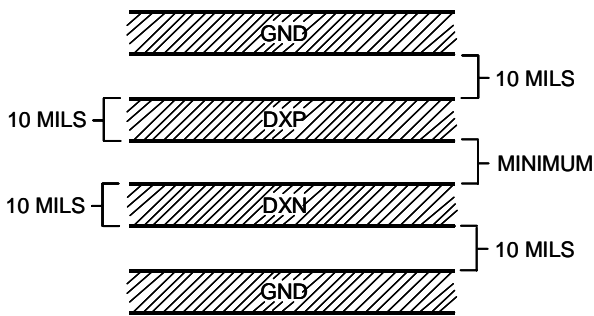


Fig 2 (b) Recommended DXP/DXN PC

Twisted Pair and Shielded Cables

For remote-sensor distances longer than 8 in., or in particularly noisy environments, a twisted pair is recommended. Its practical length is 6 feet to 12feet (typical) before noise becomes a problem, as tested in a noisy electronics laboratory. For longer distances, the best solution is a shielded twisted pair like that used for audio microphones. Connect the twisted pair to DXP and DXN and the shield to GND, and leave the shield's remote end unterminated.

Excess capacitance at DX_limits practical remote sensor distances (see Typical Operating Characteristics), For very long cable runs, the cable's parasitic capacitance often provides noise filtering, so the 2200pF capacitor can often be removed or reduced in value. Cable resistance also affects remote-sensor accuracy; 1Ω series resistance introduces about + 1°C error.

Low-Power Standby Mode

Standby mode disables the ADC and reduces the supply-current drain to less than 10µA. Enter standby mode via the RUN/STOP bit in the configuration byte register. In standby mode, all data is retained in memory, and the SMB interface is alive and listening for reads and writes. This is valid for temperature sensor only.

Standby mode is not a shutdown mode. With activity on the SMBus, extra supply current is drawn (see Typical Operating Characteristics). In software standby mode, the G771 can be forced to perform temperature measurement via the one-shot command, despite the RUN/STOP bit being high.

Supply-current drain during the 125ms conversion period is always about 500µA. Slowing down the conversion rate reduces the average supply current (see Typical Operating Characteristics). In between conversions, the instantaneous supply current is about 200µA due to the current consumed by the system resetting circuit.

Reset Immunity Negative-Going V_{CC} Transients

In addition to issuing a reset to the microprocessor (µP) during power-up, power-down, and brownout conditions, the G771 is relatively immune to short duration negative-going V_{CC} transients (glitches). Typically, for the G771, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20µs or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the G771 $\overline{\text{RESET}}$ output no longer sinks current-it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1V. However, in applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ causes any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Figure 3). R1's value is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.

Interfacing to μ Ps with Bi-directional Reset Pins

A μ P with bi-directional reset pins (such as the Motorola 68HC11 series) can connect to the G771 reset output. If, for example, the G771 $\overline{\text{RESET}}$ output is asserted high and the μ P wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7k Ω resistor between the G771 $\overline{\text{RESET}}$ output and the μ P reset I/O (Figure 4). Buffer the G771 $\overline{\text{RESET}}$ output to other system components.

Benefits of Highly Accurate Reset Threshold

Most μ P supervisor Ics have reset threshold voltages between 5% and 10% below the value of nominal supply voltages. This ensures a reset will not occur within 5% of the nominal supply, but will occur when the supply is 10% below nominal.

When using Ics rated at only the nominal supply $\pm 5\%$ this leaves a zone of uncertainty where the supply is between 5% and 10% low, and where the reset may or may not be asserted.

The G771 use highly accurate circuitry to ensure that reset is asserted close to the 5% limit, and long before the supply has declined to 10% below nominal.

SMBus Digital Interface

From a software perspective, the G771 appears as a set of byte-wide registers that contain temperature data, alarm threshold values, fan speed data, or control bits. A standard SMBus 2-wire serial interface is used to read temperature data and write control bits and alarm threshold data. Each A/D and fan control channel within the device responds to the same SMBus slave address for normal reads and writes.

The G771 employs four standard SMBus protocols: Write Byte, Read Byte, Send Byte, and Receive Byte (Figure 5). The shorter Receive Byte protocol allows quicker transfers, provided that the correct data register was previously selected by a Read Byte instruction. Use caution with the shorter protocols in multi-master systems, since a second master could over-write the command byte without informing the first master.

The temperature data format is 7bits plus sign in twos-complement form for each channel, with each data bit representing 1 $^{\circ}$ C (Table3), transmitted MSB first. Measurements are offset by +1/2 $^{\circ}$ C to minimize internal rounding errors; for example, +99.6 $^{\circ}$ C is reported as +100 $^{\circ}$ C.

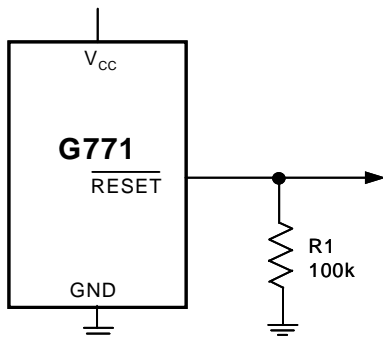


Fig 3. RESET Valid to V_{CC} = Ground Circuit

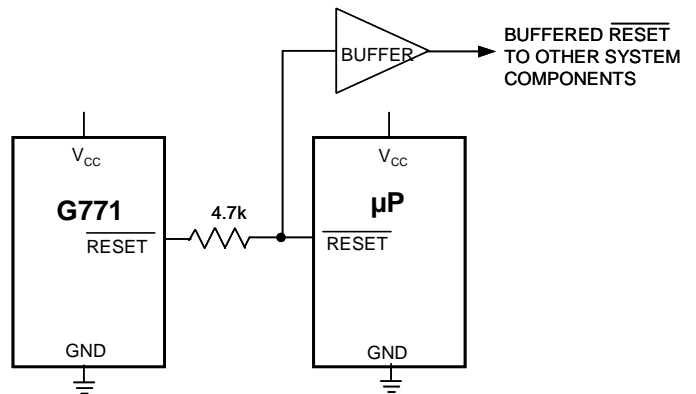


Fig 4. Interfacing to μ Ps with Bi-directional Reset I/O

Write Byte Format

| | | | | | | | | |
|----------|----------------|-----------|------------|----------------|------------|-------------|------------|----------|
| S | Address | WR | ACK | Command | ACK | DATA | ACK | P |
| | 7 bits | | | 8 bits | | 8 bits | | 1 |

Slave Address: equivalent to chip-select line of a 3-wire interface

Command Byte: selects, which register you, are writing to

Data Byte: data goes into the register set by the command byte (to set thresholds, configuration masks, and sampling rate)

Read Byte Format

| | | | | | | | | | | | | |
|----------|----------------|-----------|------------|----------------|------------|----------|----------------|-----------|------------|-------------|------------|----------|
| S | Address | WR | ACK | Command | ACK | S | Address | RD | ACK | DATA | /// | P |
| | 7 bits | | | 8 bits | | | 7 bits | | | 8 bits | | |

Slave Address: equivalent to chip- select line

Command Byte: selects, which register you, are reading from

Slave Address: repeated due to change in data-flow direction

Data byte: reads from the register set by the command byte

Send Byte Format

| | | | | | | |
|----------|----------------|-----------|------------|----------------|------------|----------|
| S | Address | WR | ACK | Command | ACK | P |
| | 7 bits | | | 8 bits | | |

Command Byte: sends command with no data usually used for one-shot command

Receive Byte Format

| | | | | | | |
|----------|----------------|-----------|------------|-------------|------------|----------|
| S | Address | RD | ACK | Data | /// | P |
| | 7 bits | | | 8 bits | | |

Data Byte: reads data from the register commanded by the last Read Byte or Write

Byte transmission; also used for SMBus Alert Response return address

S = Start condition Shaded = Slave transmission P = Stop condition /// = Not acknowledged

Fig 5. SMBus Protocols

Table 3. Data Format (Twos-Complement)

| TEMP. (°C) | ROUND TEMP. (°C) | DIGITAL OUTPUT | | |
|---------------|------------------------|----------------|-----|------|
| | | DATA BITS | | |
| | | SIGN | MSB | LSB |
| +130.00 | +127 | 0 | 111 | 1111 |
| +127.00 | +127 | 0 | 111 | 1111 |
| +126.50 | +127 | 0 | 111 | 1111 |
| +126.00 | +126 | 0 | 111 | 1110 |
| +25.25 | +25 | 0 | 001 | 1001 |
| +0.50 | +1 | 0 | 000 | 0001 |
| +0.25 | +0 | 0 | 000 | 0000 |
| +0.00 | +0 | 0 | 000 | 0000 |
| -0.25 | +0 | 0 | 000 | 0000 |
| -0.50 | +0 | 0 | 000 | 0000 |
| -0.75 | -1 | 1 | 111 | 1111 |
| -1.00 | -1 | 1 | 111 | 1111 |
| -25.00 | -25 | 1 | 110 | 0111 |
| -25.50 | -25 | 1 | 110 | 0110 |
| -54.75 | -55 | 1 | 100 | 1001 |
| -55.00 | -55 | 1 | 100 | 1001 |
| -65.00 | -65 | 1 | 011 | 1111 |
| -70.00 | -65 | 1 | 011 | 1111 |

Alarm Threshold Registers

Four registers store alarm threshold data, with high-temperature (THIGH) and low-temperature (TLOW) registers for each A/D channel. If either measured temperature equals or exceeds the corresponding alarm threshold value, an ALERT interrupt is asserted.

The power-on-reset (POR) state of both THIGH registers is full scale (0111 1111, or +127°C). The POR state of both TLOW registers is 1100 1001 or -55°C.

Diode Fault Alarm

There is a continuity fault detector at DXP that detects whether the remote diode has an open-circuit condition. At the beginning of each conversion, the diode fault is checked, and the status byte is updated. This fault detector is a simple voltage detector; if DXP rises above $V_{CC} - 1V$ (typical) due to the diode current source, a fault is detected. Note that the diode fault isn't checked until a conversion is initiated, so immediately after power-on reset the status byte indicates no fault is present, even if the diode path is broken.

If the remote channel is shorted (DXP to DXN or DXP to GND), the ADC reads 0000 0000 so as not to trip either the THIGH or TLOW alarms at their POR settings. In applications that are never subjected to 0°C in normal operation, a 0000 0000 result can be checked to indicate a fault condition in which DXP is accidentally short circuited. Similarly, if DXP is short circuited to V_{CC}, the ADC reads +127°C for both channels, and the device alarms.

ALERT Interrupts

The $\overline{\text{ALERT}}$ interrupt output signal is latched and can only be cleared by reading the Alert Response address. Interrupts are generated in response to THIGH and TLOW comparisons and when the remote diode is disconnected (for continuity fault detection). The interrupt does not halt automatic conversions; new temperature data continues to be available over the SMBus interface after $\overline{\text{ALERT}}$ is asserted. The interrupt output

rupt output pin is open-drain so that device can share a common interrupt line. The interrupt rate can never exceed the conversion rate.

The interface responds to the SMBus Alert Response address, an interrupt pointer return-address feature (see Alert Response Address section). Prior to taking corrective action, always check to ensure that an interrupt is valid by reading the current temperature.

Alert Response Address

The SMBus Alert Response interrupt pointer provides quick fault identification for simple slave devices that lack the complex, expensive logic needed to be a bus master. Upon receiving an $\overline{\text{ALERT}}$ interrupt signal, the host master can broadcast a Receive Byte transmission to the Alert Response slave address (0001 100). Then any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus.

Table 4. Command-Byte Bit Assignments

| REGISTER | COMMAND | POR STATE | FUNCTION |
|----------|---------|------------------|--|
| RRTE2 | 00h | 0000 0000b | Read 2nd remote temperature: returns latest temperature |
| RRTE1 | 01h | 0000 0000b | Read 1st remote temperature: returns latest temperature |
| RSL | 02h | N/A | Read status byte (flags, busy signal) |
| RCL | 03h | 0000 0000b | Read configuration byte |
| RCRA | 04h | 0000 0010b | Read conversion rate byte |
| RRHI2 | 05h | 0111 1111b (127) | Read 2nd remote THIGH limit |
| RRLS2 | 06h | 1100 1001b (-55) | Read 2nd remote TLOW limit |
| RRHI1 | 07h | 0111 1111b (127) | Read 1st remote THIGH limit |
| RRLS1 | 08h | 1100 1001b (-55) | Read 1st remote TLOW limit |
| WCA | 09h | N/A | Write configuration byte |
| WCRW | 0Ah | N/A | Write conversion rate byte |
| WRHA2 | 0Bh | N/A | Write 2nd remote THIGH limit |
| WRLN2 | 0Ch | N/A | Write 2nd remote TLOW limit |
| WRHA1 | 0Dh | N/A | Write 1st remote THIGH limit |
| WRLN1 | 0Eh | N/A | Write 1st remote TLOW limit |
| OSHT | 0Fh | N/A | One-shot command (use send-byte format) |
| TCRIT1 | 35h | 0110 1100b (108) | Critical temperature for 1 st remote temperature sensor |
| TCRIT2 | 36h | 0101 1000b (88) | Critical temperature for 2 nd remote temperature sensor |

The Alert Response can activate several different slave devices simultaneously, similar to the SMBus General Call. If more than one slave attempts to respond, bus arbitration rules apply, and the device with the lower address code wins. The losing device does

not generate an acknowledge and continues to hold the $\overline{\text{ALERT}}$ line low until serviced (implies that the host interrupt input is level sensitive). Successful reading of the alert response address clears the interrupt latch.

Command Byte Functions

The 8-bit command byte register (Table 4) is the master index that points to the various other registers within the G771. The register's POR state is 0000

0000, so that a Receive Byte transmission (a protocol that lacks the command byte) that occurs immediately after POR returns the current local temperature data.

The one-shot command immediately forces a new conversion cycle to begin. In software standby mode ($\overline{\text{RUN/STOP}}$ bit = high), a new conversion is begun, after which the device returns to standby mode. If a conversion is in progress when a one-shot command is received in auto-convert mode ($\overline{\text{RUN/STOP}}$ bit = low) between conversions, a new conversion begins, the conversion rate timer is reset, and the next automatic conversion takes place after a full delay elapses.

Configuration Byte Functions

The configuration byte register contents are listed in table 5. Bit 7 (MASK) is used to mask $\overline{\text{ALERT}}$ interrupt. Bit 6 ($\overline{\text{RUN/STOP}}$) is to put the device in software standby mode. Setting bit 5 (DET_FAN) with logic 1 can activate the detection of fan failure. Logic 1 in bit 4 (EN_TH_SHUT) makes thermal shutdown function valid and logic 0 disables this function and keep TH_SHUT pin low. Bit 3~0 forms thermal shutdown fault queue. The number of faults these bits decided are listed in table 6.

Thermal Status Byte Functions

The thermal status byte register (02h) (Table 6) indicates which (if any) temperature thresholds have been exceeded. This byte also indicates whether or not the ADC is converting and whether there is an open circuit

in the remote diode DXPx-DXN path. After POR, the normal state of all the flag bits is zero, assuming none of the alarm conditions are present. The status byte is cleared by any successful read of the status, unless the fault persists. Note that the $\overline{\text{ALERT}}$ interrupt latch is not automatically cleared when the status flag bit is cleared.

When reading the status byte, you must check for internal bus collisions caused by asynchronous ADC timing, or else disable the ADC prior to reading the status byte (via the $\overline{\text{RUN/STOP}}$ bit in the configuration byte). In one-shot mode, read the status byte only after the conversion is complete, which is 150ms max after the one-shot conversion is commanded.

Table 5. Configuration-Byte Bit Assignments

| BIT | NAME | POR STATE | FUNCTION |
|---------|---------------------------------------|-----------|---|
| 7 (MSB) | MASK | 0 | Masks all $\overline{\text{ALERT}}$ interrupts when high. |
| 6 | $\overline{\text{RUN}} / \text{STOP}$ | 0 | Standby mode control bit. If high, the device immediately stops converting and enters standby mode. If low, the device converts in either one-shot or timer mode. |
| 5 | DET_FAN | 0 | Should be 0. Changing this to 1 will cause $\overline{\text{ALERT}}$ function abnormal. |
| 4 | EN_TH_SHUT | 1 | Validation of the fault queue function of thermal shutdown. |
| 3-0 | FQ_TH_SHUT | 0010b | Fault Queue. Number of faults necessary to detect before setting TH_SHUT output to avoid false tripping due to noise. |

Table 6. Number of Faults assigned by FQ_TH_SHUT

| FQ_TH_SHUT | Number of Faults |
|------------|---------------------|
| 0000b | 1 |
| 0001b | 2 |
| 0010b | 3(Power-up default) |
| 0011b | 4 |
| 0100b | 5 |
| 0101b | 6 |
| 0110b | 7 |
| 0111b | 8 |

| FQ_TH_SHUT | Number of Faults |
|------------|------------------|
| 1000b | 9 |
| 1001b | 10 |
| 1010b | 11 |
| 1011b | 12 |
| 1100b | 13 |
| 1101b | 14 |
| 1110b | 15 |
| 1111b | 16 |

Table 7. Status-Byte Bit Assignments

| BIT | NAME | FUNCTION |
|--------|---------|---|
| 7(MSB) | BUSY | A high indicates that the ADC is busy converting. |
| 6 | RHIGH2* | A high indicates that the 2 nd diode high-temperature alarm has activated. |
| 5 | RLOW2* | A high indicates that the 2 nd diode low-temperature alarm has activated. |
| 4 | RHIGH1* | A high indicates that the 1 st diode high-temperature alarm has activated. |
| 3 | RLOW1* | A high indicates that the 1 st diode low-temperature alarm has activated. |
| 2 | OPEN* | A high indicates a remote-diode continuity (open-circuit) fault. |
| 1 | RFU | Reserved for future use (returns 0) |
| 0(LSB) | RFU | Reserved for future use (returns 0) |

*These flags stay high until cleared by POR, or until the status byte register is read.

Table 8. Conversion-Rate Control Byte

| DATA | CONVERSION RATE (Hz) | Temperature Sensor Average Supply Current (μ A TYP, at Vcc = 5V) |
|------------|----------------------|---|
| 00h | 0.0625 | 30 |
| 01h | 0.125 | 33 |
| 02h | 0.25 | 35 |
| 03h | 0.5 | 48 |
| 04h | 1 | 70 |
| 05h | 2 | 128 |
| 06h | 4 | 225 |
| 07h | 8 | 425 |
| 08h to FFh | RFU | - |

Table 9. RLTS and RRTE Temp Register Update Timing Chart

| OPERATING MODE | CONVERSION INITIATED BY: | NEW CONVERSION RATE (CHANGED VIA WRITE TO CRW) | TIME UNTIL RLTS AND RRTE ARE UPDATED |
|------------------|--|--|---|
| Auto-Convert | Power-on reset | N/A (0.25Hz) | 156ms max |
| Auto-Convert | 1-shot command, while idling between automatic conversions | N/A | 156ms max |
| Auto-Convert | 1-shot command that occurs during a conversion | N/A | When current conversion is complete (1-shot is ignored) |
| Auto-Convert | Rate timer | 0.0625Hz | 20sec |
| Auto-Convert | Rate timer | 0.125Hz | 10sec |
| Auto-Convert | Rate timer | 0.25Hz | 5sec |
| Auto-Convert | Rate timer | 0.5Hz | 2.5sec |
| Auto-Convert | Rate timer | 1Hz | 1.25sec |
| Auto-Convert | Rate timer | 2Hz | 625ms |
| Auto-Convert | Rate timer | 4Hz | 312.5ms |
| Auto-Convert | Rate timer | 8Hz | 237.5ms |
| Software Standby | RUN/STOP bit | N/A | 156ms |
| Software Standby | 1-shot command | N/A | 156ms |

To check for internal bus collisions, read the status byte. If the least significant seven bits are ones, discard the data and read the status byte again. The status bits LHIGH, LLOW, RHIGH, and RLOW are refreshed on the SMBus clock edge immediately following the stop condition, so there is no danger of losing temperature-related status data as a result of an internal bus collision. The OPEN status bit (diode continuity fault) is only refreshed at the beginning of a conversion, so OPEN data is lost. The $\overline{\text{ALERT}}$ interrupt latch is independent of the status byte register, so no false alerts are generated by an internal bus collision.

When auto-converting, if the THIGH and TLOW limits are close together, it's possible for both high-temp and low-temp status bits to be set, depending on the amount of time between status read operations (especially when converting at the fastest rate). In these circumstances, it's best not to rely on the status bits to indicate reversals in long-term temperature changes and instead use a current temperature reading to establish the trend direction.

Temperature Conversion Rate Byte

The conversion rate register (Table 7) programs the time interval between conversions in free running auto-convert mode. This variable rate control reduces the supply current in portable-equipment applications. The conversion rate byte's POR state is 02h (0.25Hz). The G771 looks only at the 3 LSB bits of this register, so the upper 5 bits are "don't care" bits, which should be set to zero. The conversion rate tolerance is $\pm 25\%$ at any rate setting.

Valid A/D conversion results for all channels are available one total conversion time (125ms nominal, 156ms

156ms maximum) after initiating a conversion, whether conversion is initiated via the RUN/STOP bit, one-shot command, or initial power-up. Changing the conversion rate can also affect the delay until new results are available. See Table 8.

Slave Addresses

The G771 appears to the SMBus as one device having a common address for all the ADC and fan control channels. The device address is fixed to be 7Ah for write and 7Bh for read.

The G771 also responds to the SMBus Alert Response slave address (see the Alert Response Address section).

POR and UVLO

The G771 has a volatile memory. To prevent ambiguous power-supply conditions from corrupting the data in memory and causing erratic behavior, a POR voltage detector monitors Vcc and clears the memory if Vcc falls below 1.7V (typical, see Electrical Characteristics table). When power is first applied and Vcc rises above 1.75V (typical), the logic blocks begin operating, although reads and writes at Vcc levels below 3V are not recommended. A second Vcc comparator, the ADC UVLO comparator, prevents the ADC from converting until there is sufficient headroom (Vcc = 2.8V typical).

Power-Up Defaults:

- Interrupt latch is cleared.
- ADC begins auto /converting at a 0.25Hz rate.
- Command byte is set to 00h to facilitate quick remote Receive Byte queries.
- THIGH and TLOW registers are set to max and min limits, respectively

Thermal Shutdown Signal

When the temperature of DX1 reaches or exceeds the Tcrit1 threshold consecutively for the times equal to the number of faults of the FQ_TH_SHUT registers, TH_SHUT pin becomes logic high. The

same mechanism is duplicated for DX2. There fore, either one of DX1, DX2 continuously over their respective Tcrit, the TH_SHUT will assert logic high to indicate a thermal shutdown event.

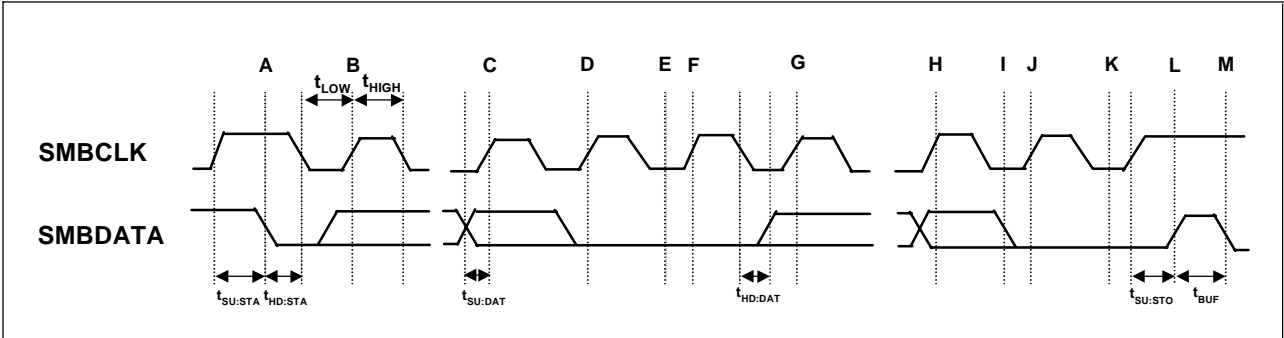


Figure 6. SMBus Write Timing Diagram

A = start condition

B = MSB of address clocked into slave

C = LSB of address clocked into slave

D = R / W bit clocked into slave

E = slave pulls SMB Data line low

F = acknowledge bit clocked into master

G = MSB of data clocked into slave

H = LSB of data clocked into slave

I = slave pulls SMBDATA line low

J = acknowledge clocked into master

K = acknowledge clocked pulse

L = stop condition data executed by slave

M = new start condition

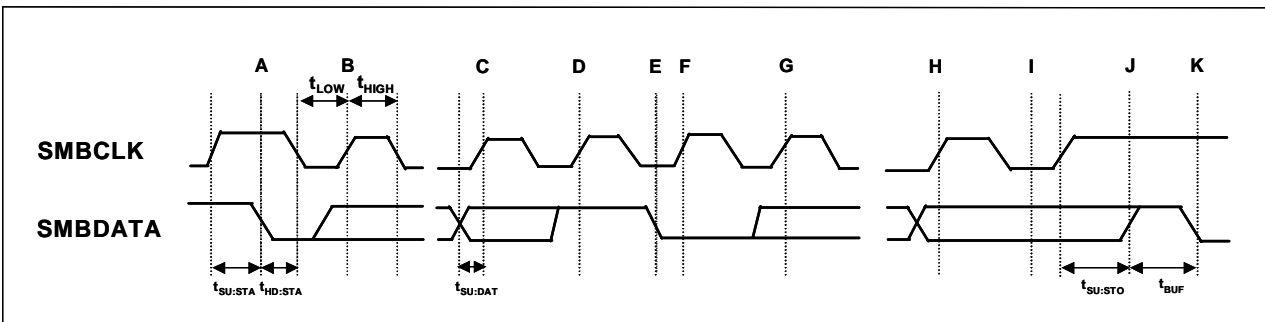


Figure 7. SMBus Read Timing Diagram

A = start condition

B = MSB of address clocked into slave

C = LSB of address clocked into slave

D = R / W bit clocked into slave

E = slave pulls SMBDATA line low

F = acknowledge bit clocked into master

G = MSB of data clocked into master

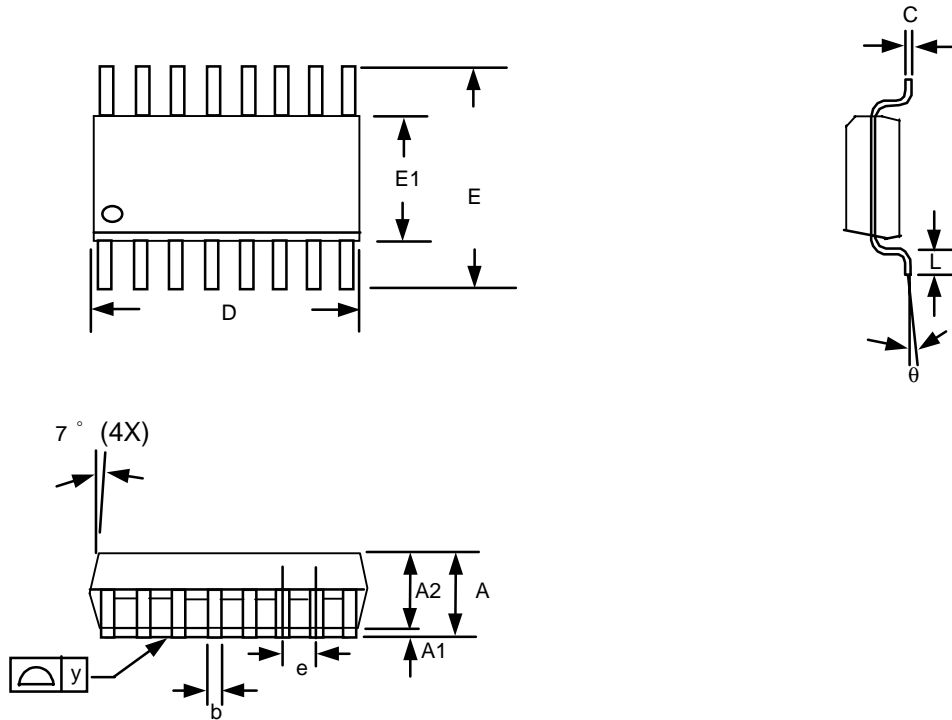
H = LSB of data clocked into master

I = acknowledge clocked pulse

J = stop condition

K = new start condition

Package Information



Note:

1. Package body sizes exclude mold flash and gate burrs
2. Dimension L is measured in gage plane
3. Tolerance 0.10mm unless other wise specified
4. Controlling dimension is millimeter converted inch dimensions are not necessarily exact.

| SYMBOLS | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|----------|-----------------|-------|-------|-------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.35 | 1.60 | 1.75 | 0.053 | 0.064 | 0.069 |
| A1 | 0.10 | ----- | 0.25 | 0.004 | ----- | 0.010 |
| A2 | ----- | 1.45 | ----- | ----- | 0.057 | ----- |
| b | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| C | 0.19 | ----- | 0.25 | 0.007 | ----- | 0.010 |
| D | 4.80 | ----- | 5.00 | 0.189 | ----- | 0.197 |
| E | 5.80 | ----- | 6.20 | 0.228 | ----- | 0.244 |
| E1 | 3.80 | ----- | 4.00 | 0.150 | ----- | 0.157 |
| e | ----- | 0.64 | ----- | ----- | 0.25 | ----- |
| L | 0.40 | ----- | 1.27 | 0.016 | ----- | 0.050 |
| y | ----- | ----- | 0.10 | ----- | ----- | 0.004 |
| θ | 0° | ----- | 8° | 0° | ----- | 8° |

Taping Specification

