

Description

The G80N04 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

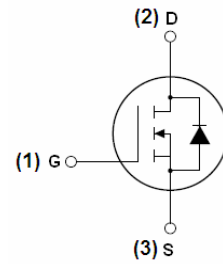
General Features

VDSS	RDS(ON) @10V (typ)	RDS(ON) @4.5V (typ)	ID
40V	3.2 m Ω	5.5 m Ω	90A

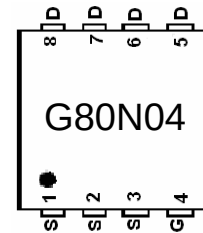
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability
- RoHS Compliant

Application

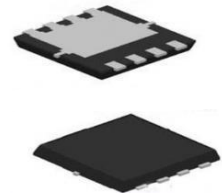
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



DFN5X6-8L

Ordering Information

Part Number	Marking	Case	Packaging
G80N04	G80N04	DFN5*6-8L	2500pcs/Reel

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	90	A
Drain Current-Continuous($T_C=100^{\circ}\text{C}$)	$I_D(100^{\circ}\text{C})$	63.5	A
Pulsed Drain Current	I_{DM}	330	A
Maximum Power Dissipation	P_D	65	W
Derating factor		0.43	W/ $^{\circ}\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^{\circ}\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.3	$^{\circ}\text{C}/\text{W}$
--	-----------------	-----	-----------------------------

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

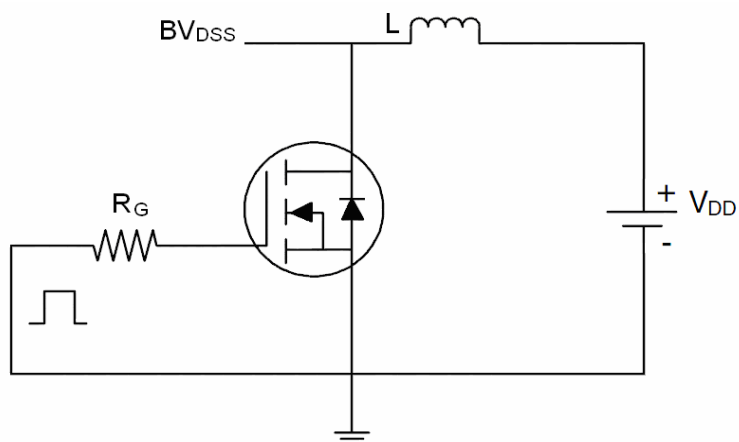
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	40	45	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	1.2	1.9	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.2	4.0	mΩ
		V _{GS} =4.5V, I _D =10A	-	5.5	7.0	
Forward Transconductance	g _{FS}	V _{DS} =10V,I _D =20A	26	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =20V,V _{GS} =0V, F=1.0MHz	4600	5000	5400	PF
Output Capacitance	C _{oss}		826	898	970	PF
Reverse Transfer Capacitance	C _{rss}		324	351	380	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =20V,I _D =20A,R _L =1Ω V _{GS} =10V,R _G =3Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	18	-	nS
Turn-Off Delay Time	t _{d(off)}		-	52	-	nS
Turn-Off Fall Time	t _f		-	23	-	nS
Total Gate Charge	Q _g	V _{DS} =20V,I _D =20A, V _{GS} =10V	-	90	-	nC
Gate-Source Charge	Q _{gs}		-	14	-	nC
Gate-Drain Charge	Q _{gd}		-	22	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	90	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs ^(Note3)	-	42	-	nS
Reverse Recovery Charge	Q _{rr}		-	45	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

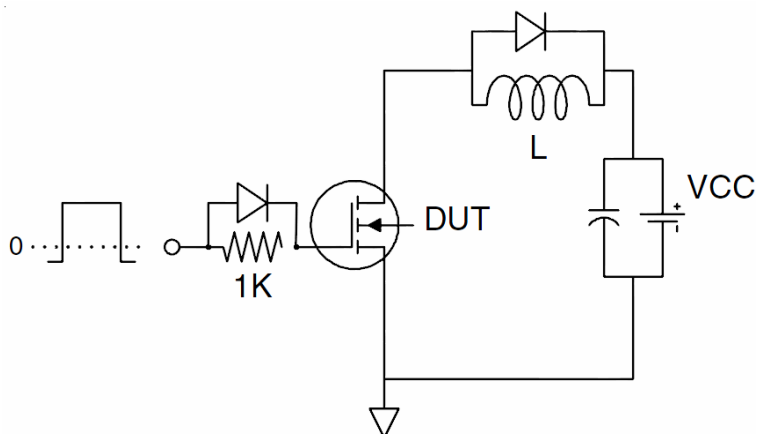
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

Test circuit

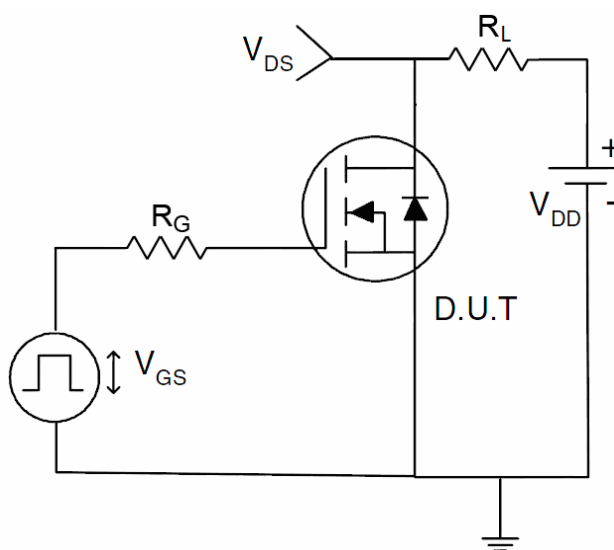
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

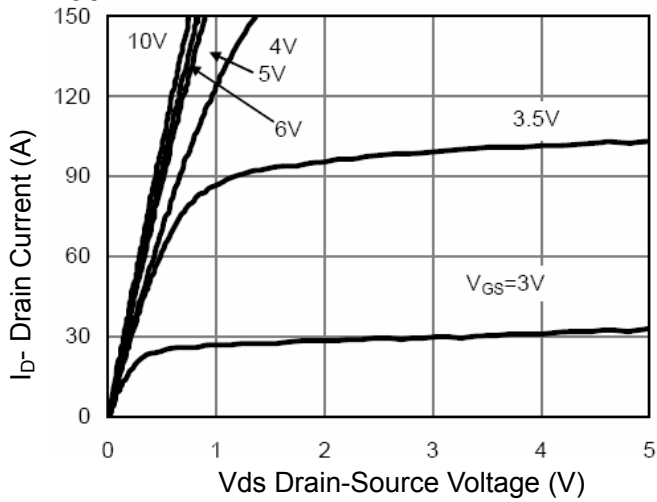


Figure 1 Output Characteristics

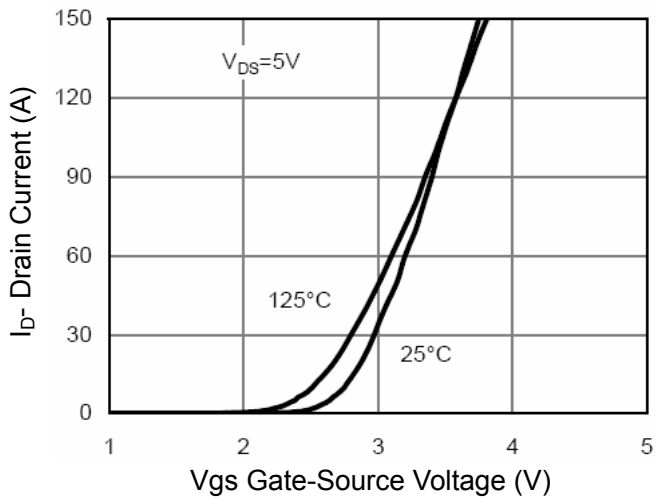


Figure 2 Transfer Characteristics

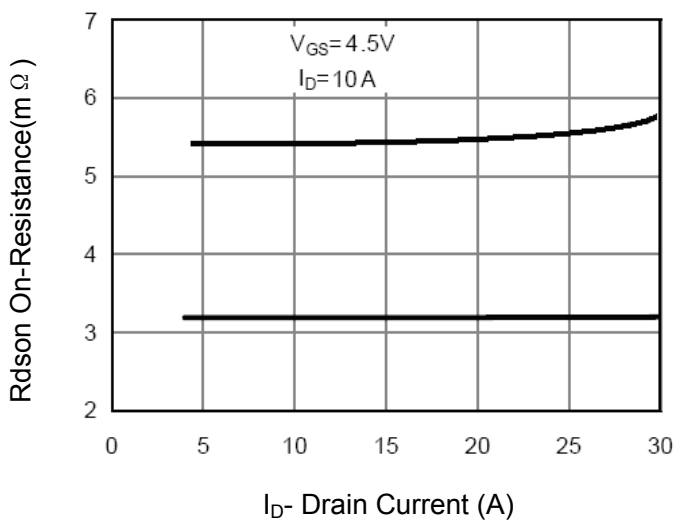


Figure 3 $R_{DS(on)}$ - Drain Current

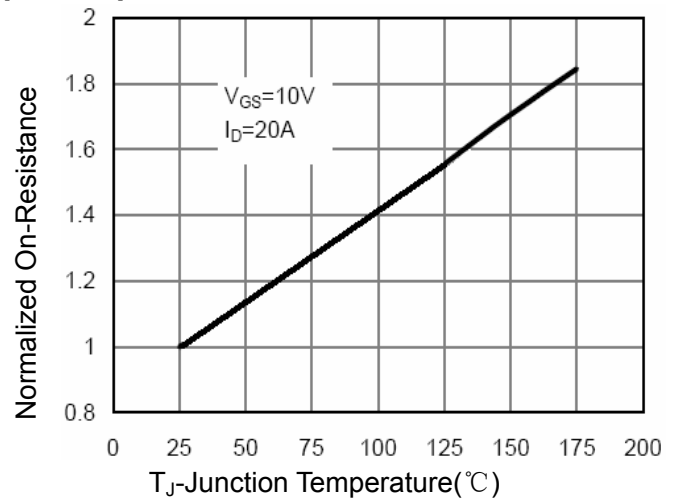


Figure 4 $R_{DS(on)}$ -Junction Temperature

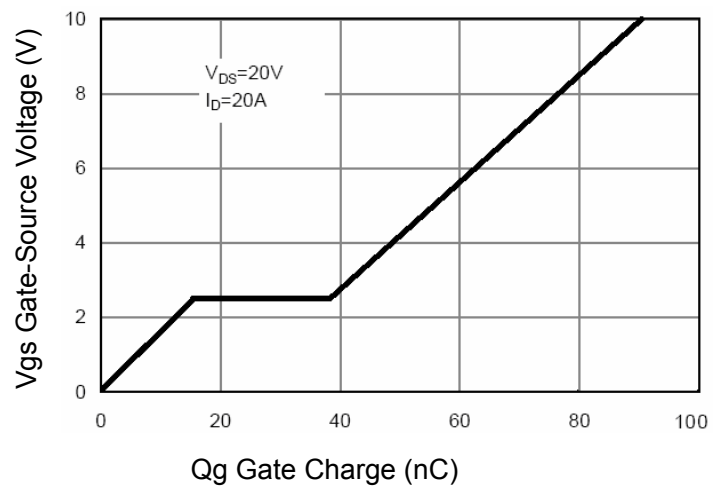


Figure 5 Gate Charge

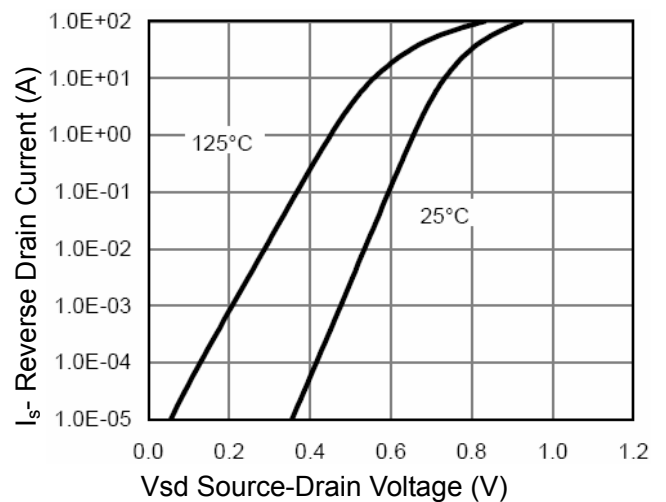


Figure 6 Source- Drain Diode Forward

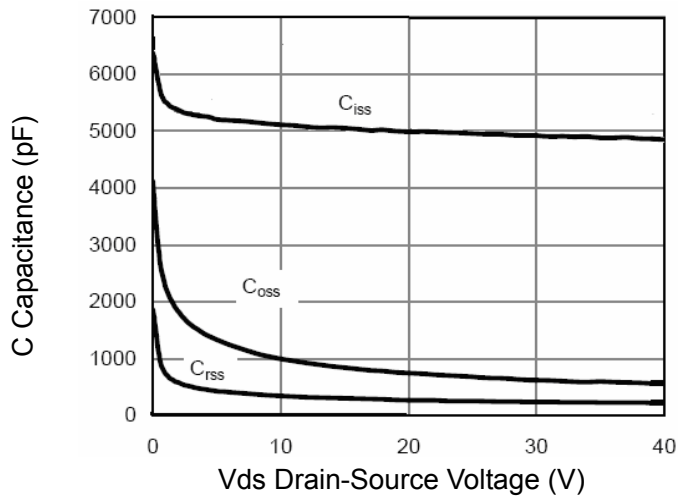


Figure 7 Capacitance vs Vds

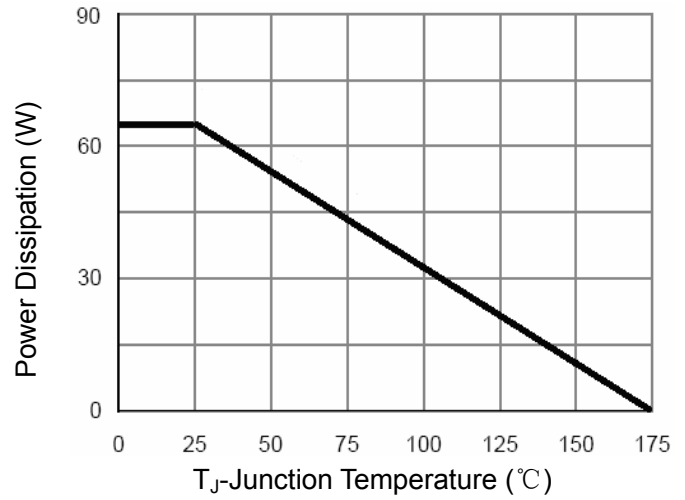


Figure 9 Power De-rating

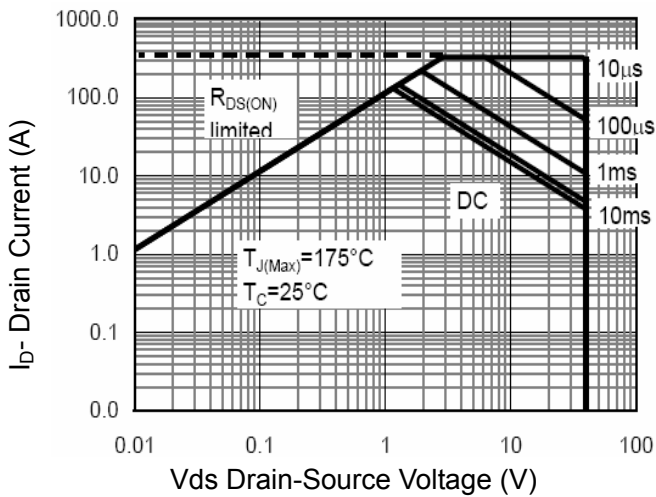


Figure 8 Safe Operation Area

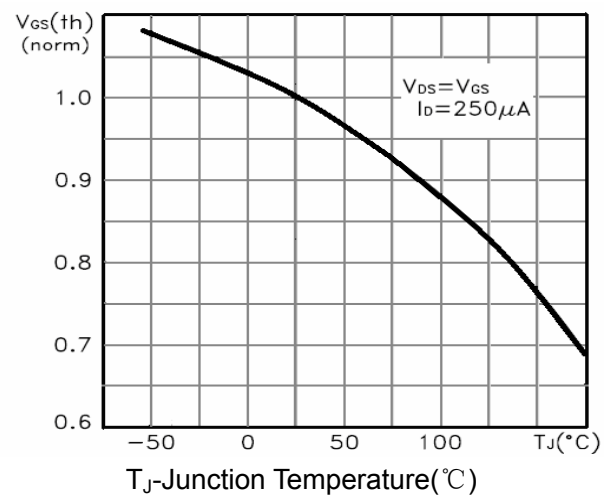


Figure 10 $V_{GS(th)}$ vs Junction Temperature

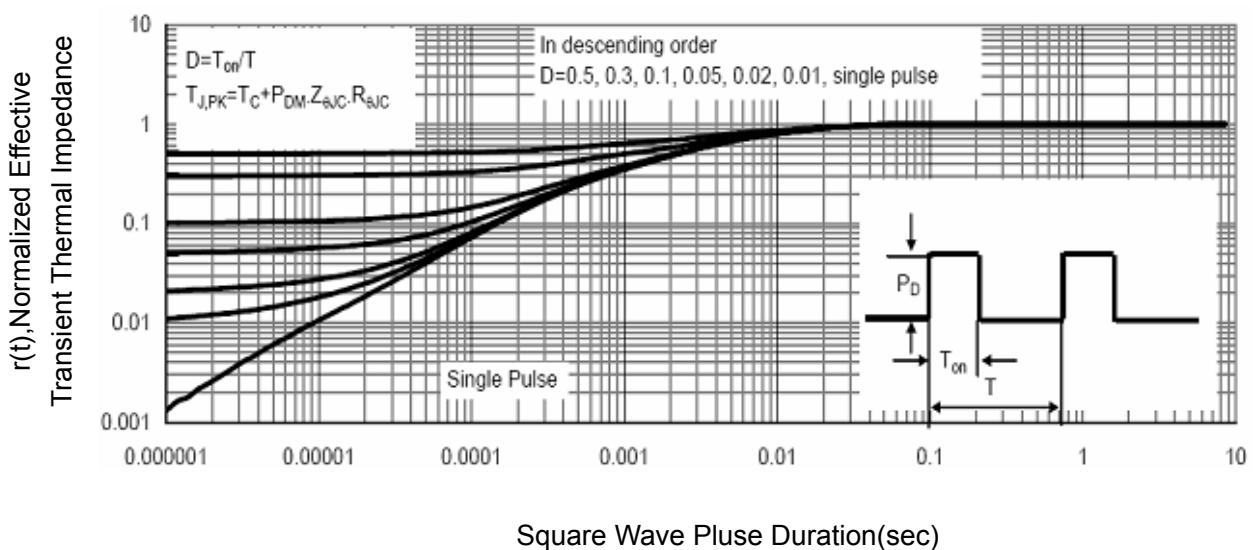
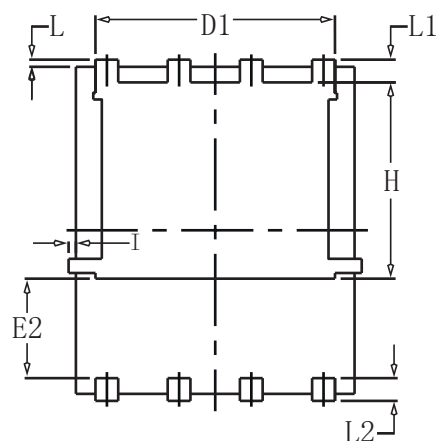
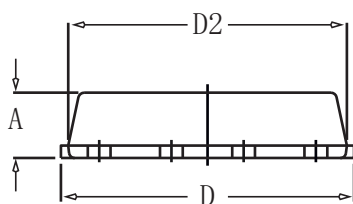
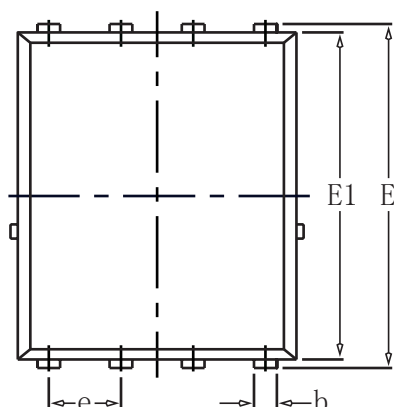


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package information



SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.59	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070