GA05JT01-46

Normally – OFF Silicon Carbide Junction Transistor

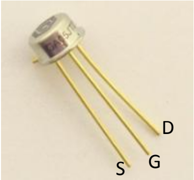
V_{DS} = 100 V
$R_{DS(ON)}$ = 240 mΩ
I_D (T_c = 25°C) = 9 A
h_{FE} (T_c = 25°C) = 110

Features

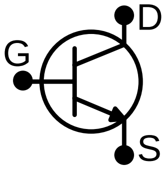
- 225°C maximum operating temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Compatible with 5 V TTL Gate Drive
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package

- RoHS Compliant



TO-46



Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 µs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling
- Geothermal Instrumentation
- Solenoid Actuators
- General Purpose High-Temperature Switching
- Amplifiers
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	100	V	
Continuous Drain Current	I_D	T_J = 225°C, T_C = 25°C	5.8	A	Fig. 21
Continuous Gate Current	I_{GM}		0.5	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 225°C, I_G = 0.5 A, Clamped Inductive Load	$I_{D,max}$ = 9 @ $V_{DS} \leq V_{DSmax}$	A	Fig. 19
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 225°C, I_G = 0.5 A, V_{DS} = 70 V, Non Repetitive	>20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Power Dissipation	P_{tot}	T_J = 225°C, T_C = 25°C	20	W	Fig. 16
Operating and Storage Temperature	T_{stg}		-55 to 225	°C	

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: On State							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 5 A, T_j = 25 °C I_D = 5 A, T_j = 125 °C I_D = 5 A, T_j = 175 °C I_D = 5 A, T_j = 225 °C		240 368 455 620		mΩ	Fig. 5
Gate – Source Saturation Voltage	$V_{GS,sat}$	I_D = 5 A, I_D/I_G = 40, T_j = 25 °C I_D = 5 A, I_D/I_G = 30, T_j = 175 °C		3.45 3.22		V	Fig. 7
DC Current Gain	h_{FE}	V_{DS} = 5 V, I_D = 5 A, T_j = 25 °C V_{DS} = 5 V, I_D = 5 A, T_j = 125 °C V_{DS} = 5 V, I_D = 5 A, T_j = 175 °C V_{DS} = 5 V, I_D = 5 A, T_j = 225 °C		113 79 72 69		–	Fig. 5
B: Off State							
Drain Leakage Current	I_{DSS}	V_R = 100 V, V_{GS} = 0 V, T_j = 25 °C V_R = 100 V, V_{GS} = 0 V, T_j = 125 °C V_R = 100 V, V_{GS} = 0 V, T_j = 225 °C		10 50 100	100 500 1000	µA	Fig. 6
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	
C: Thermal							
Thermal resistance, junction - case	R_{thJC}	Assumes thermal conduction through baseplate only actual value may be lower		9.86		°C/W	Fig. 17

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: Capacitance and Gate Charge							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 100 V, *f* = 1 MHz		547		pF	Fig. 7
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_D = 100 V, *f* = 1 MHz		45		pF	Fig. 7
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_D = 100 V, *f* = 1 MHz		0.2		µJ	Fig. 8
Effective Output Capacitance, time related	$C_{oss,tr}$	I_D = constant, V_{GS} = 0 V, V_{DS} = 0…70 V		83		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	V_{GS} = 0 V, V_{DS} = 0…70 V		67		pF	
Gate-Source Charge	Q_{GS}	V_{GS} = -5…3 V		3.7		nC	
Gate-Drain Charge	Q_{GD}	V_{GS} = 0 V, V_{DS} = 0…70 V		5.8		nC	
Gate Charge - Total	Q_G			9.5		nC	
B: Switching[1]							
Internal Gate Resistance – zero bias	$R_{G(INT-ZERO)}$	*f* = 1 MHz, V_{AC} = 50 mV, V_{DS} = V_{GS} = 0 V , T_j = 225 ºC		14.5		Ω	
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	V_{GS} > 2.5 V, V_{DS} = 0 V, T_j = 225 ºC		0.37		Ω	
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 70 V, I_D = 5 A, Resistive Load Refer to Section V: for additional driving information		8.0		ns	
Fall Time, V_{DS}	t_f			7.4		ns	Fig. 11, 13
Turn Off Delay Time	$t_{d(off)}$			14.0		ns	
Rise Time, V_{DS}	t_r			4.2		ns	Fig. 12, 14
Turn On Delay Time	$t_{d(on)}$	T_j = 225 ºC, V_{DS} = 70 V, I_D = 5 A, Resistive Load Refer to Section V: for additional driving information		8.0		ns	
Fall Time, V_{DS}	t_f			7.8		ns	Fig. 11
Turn Off Delay Time	$t_{d(off)}$			28.0		ns	
Rise Time, V_{DS}	t_r			2.3		ns	Fig. 12
Turn-On Energy Per Pulse	E_{on}	T_j = 25 ºC, V_{DS} = 70 V, I_D = 5 A, Inductive Load		3.6		µJ	Fig. 11, 13
Turn-Off Energy Per Pulse	E_{off}			0.4		µJ	Fig. 12, 14
Total Switching Energy	E_{tot}			4.0		µJ	
Turn-On Energy Per Pulse	E_{on}	T_j = 225 ºC, V_{DS} = 70 V, I_D = 5 A, Inductive Load		3.6		µJ	Fig. 11
Turn-Off Energy Per Pulse	E_{off}			0.5		µJ	Fig. 12
Total Switching Energy	E_{tot}			4.1		µJ	

[1] – All times are relative to the Drain-Source Voltage V_{DS}

Section IV: Figures

A: Static Characteristics

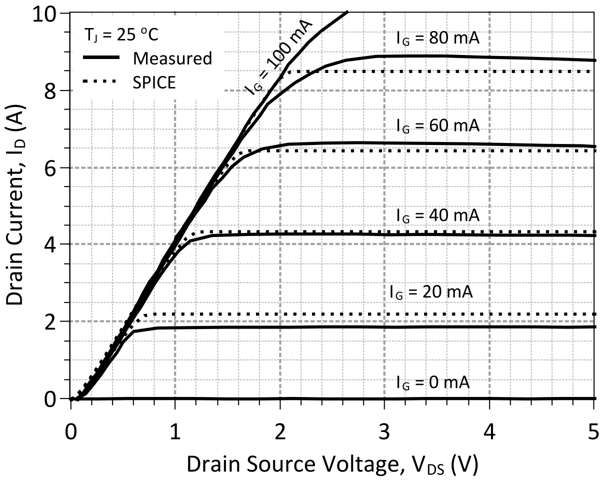


Figure 1: Typical Output Characteristics at 25 °C

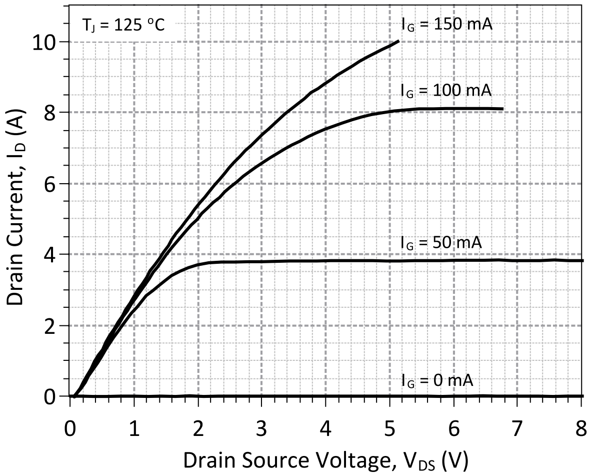


Figure 2: Typical Output Characteristics at 125 °C

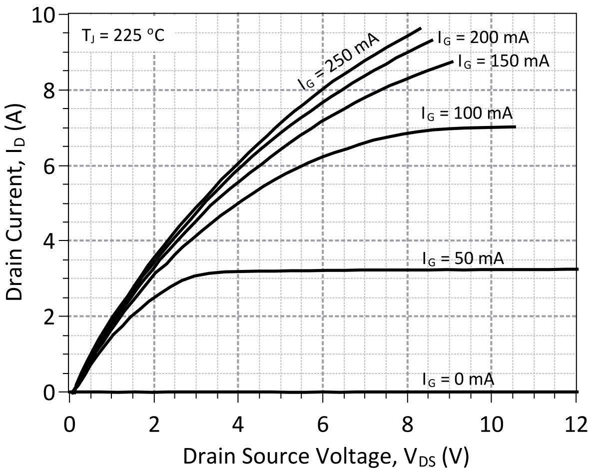


Figure 3: Typical Output Characteristics at 225 °C

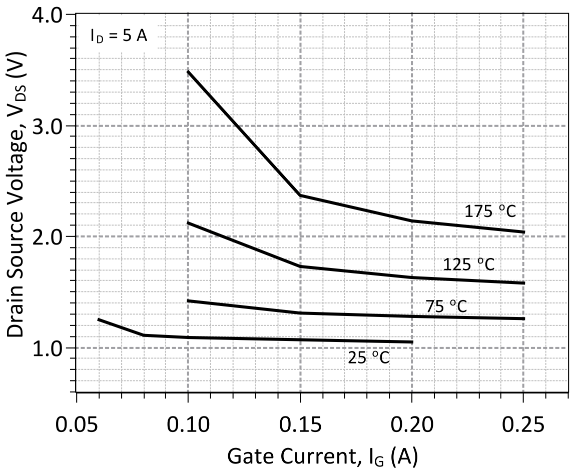


Figure 4: Drain-Source Voltage vs. Gate Current

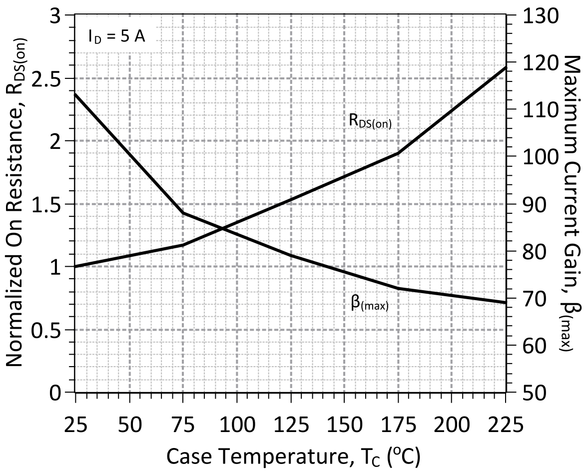


Figure 5: DC Current Gain and Normalized On-Resistance vs. Temperature

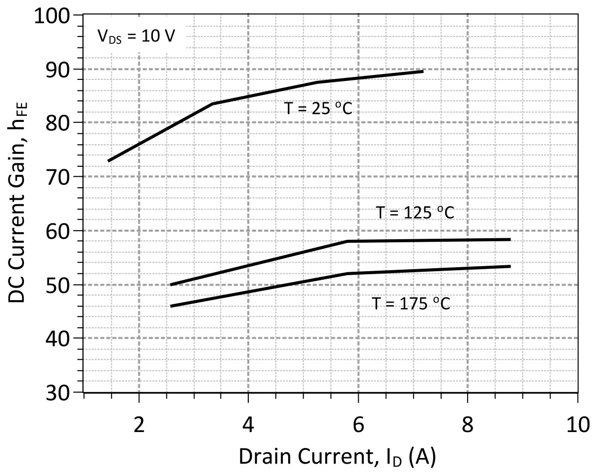


Figure 6: DC Current Gain vs. Drain Current

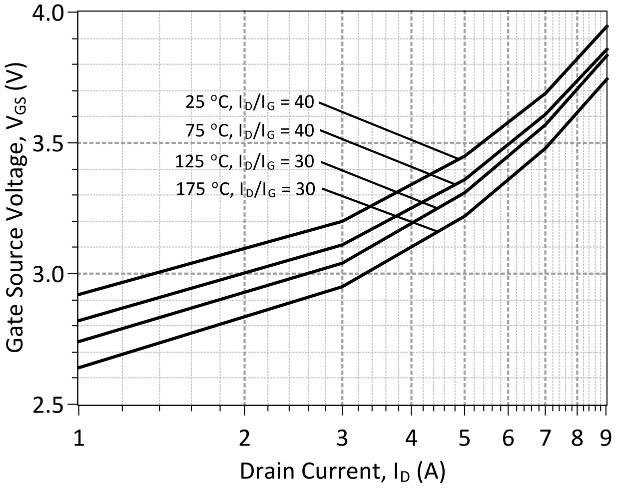


Figure 7: Typical Gate – Source Saturation Voltage

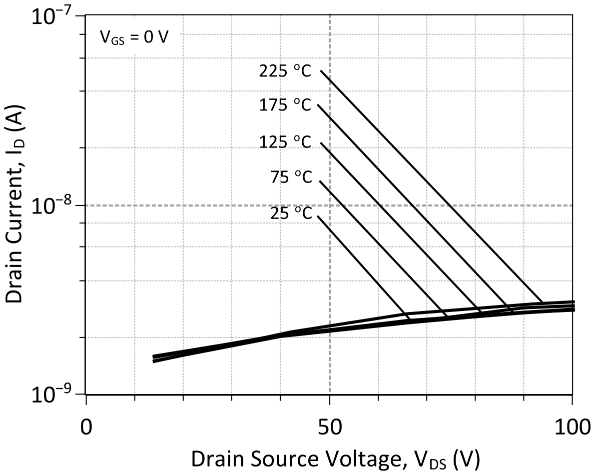


Figure 8: Typical Blocking Characteristics

B: Dynamic Characteristics

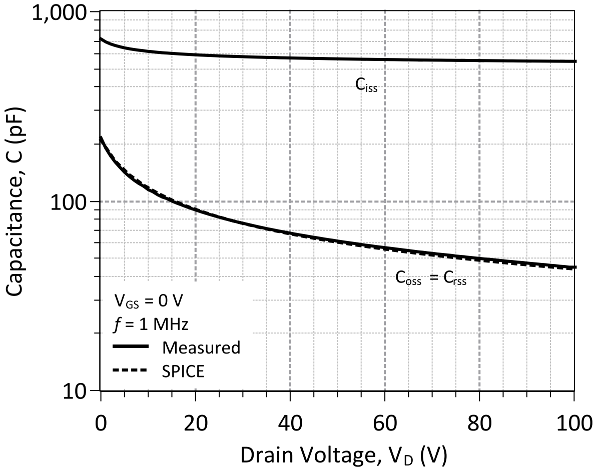


Figure 9: Input, Output, and Reverse Transfer Capacitance

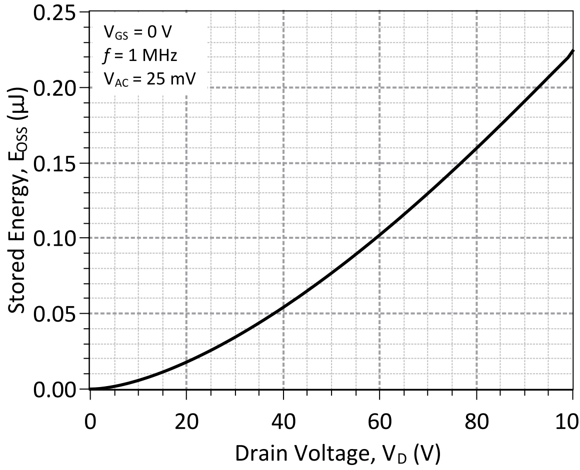


Figure 10: Energy stored in Output Capacitance

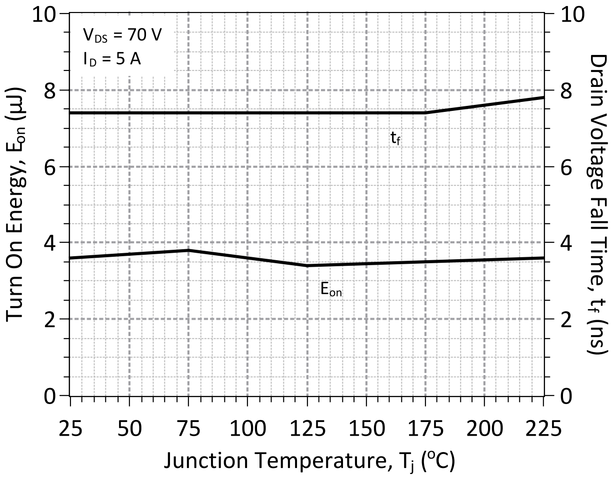


Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

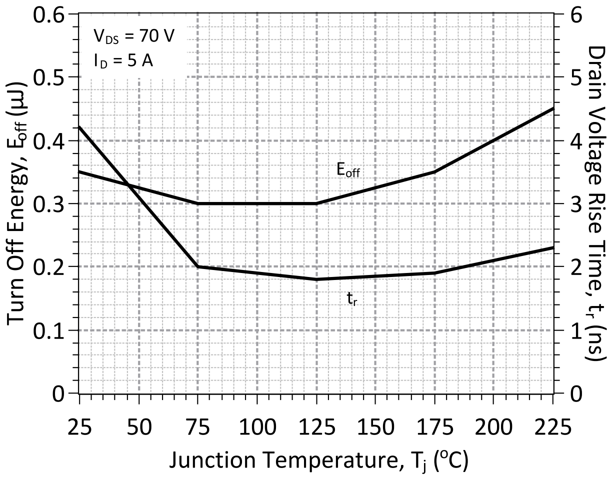


Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

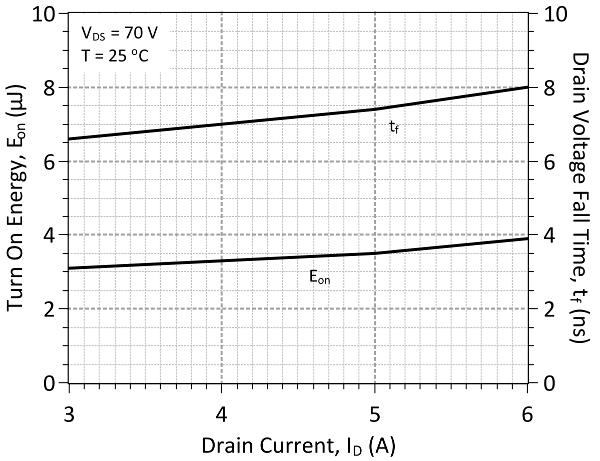


Figure 13: Typical Turn On Energy Losses and Switching Times vs. Drain Current

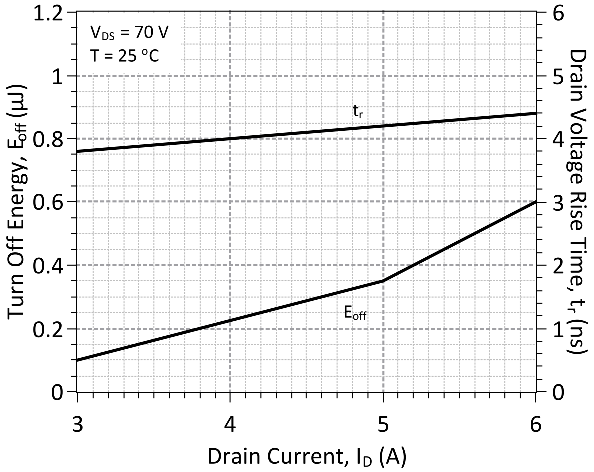


Figure 14: Typical Turn Off Energy Losses and Switching Times vs. Drain Current

C: Current and Power Derating

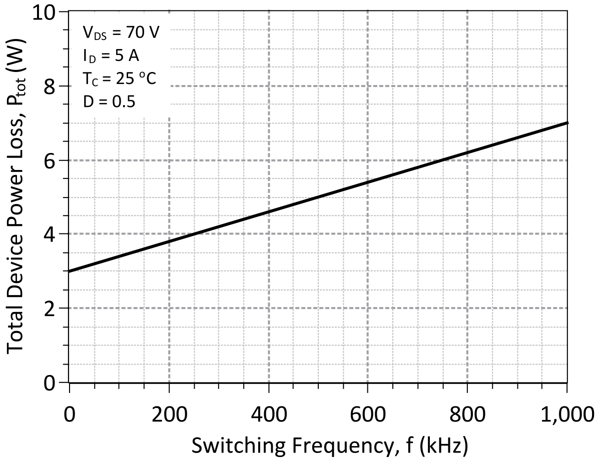


Figure 15: Typical Hard Switched Device Power Loss vs. Switching Frequency [2]

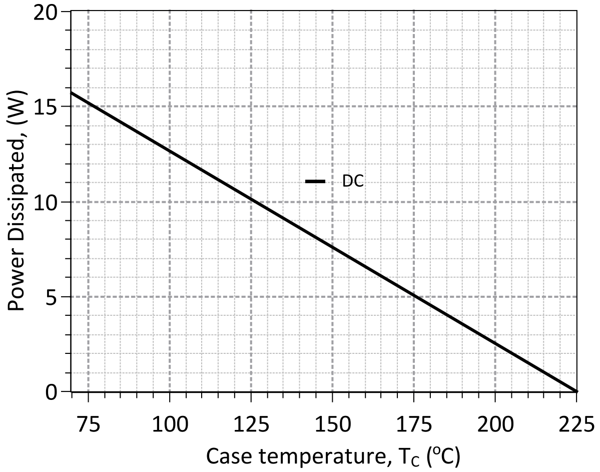


Figure 16: Power Derating Curve

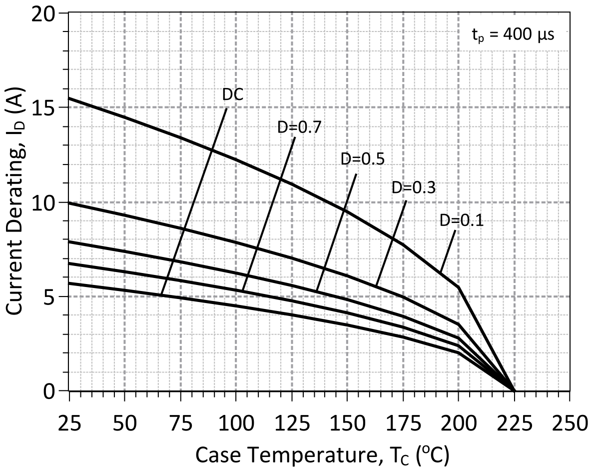


Figure 17: Drain Current Derating vs. Temperature

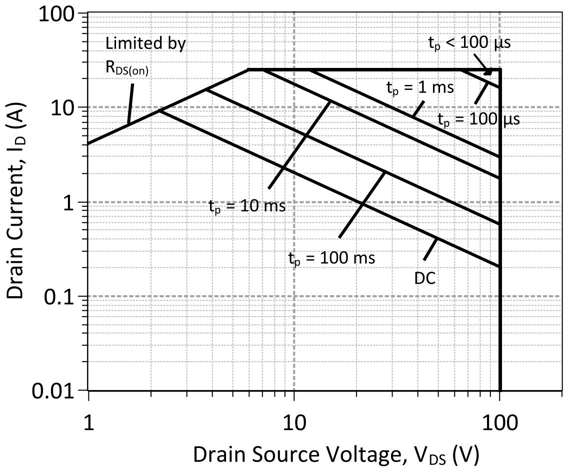


Figure 18: Forward Bias Safe Operating Area at T_c= 25 °C

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[2] – Representative values based on device conduction and switching loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

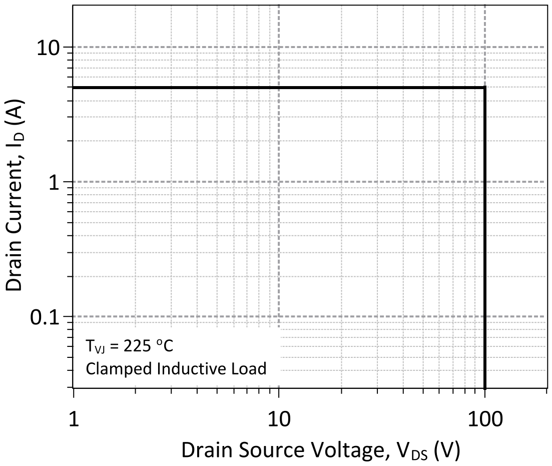

Figure 19: Turn-Off Safe Operating Area

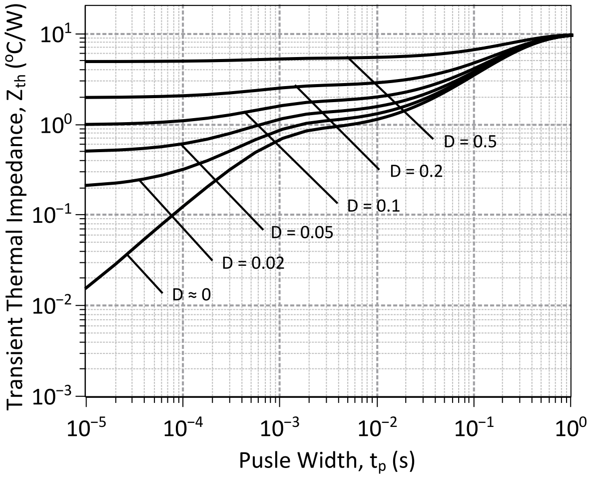

Figure 20: Transient Thermal Impedance

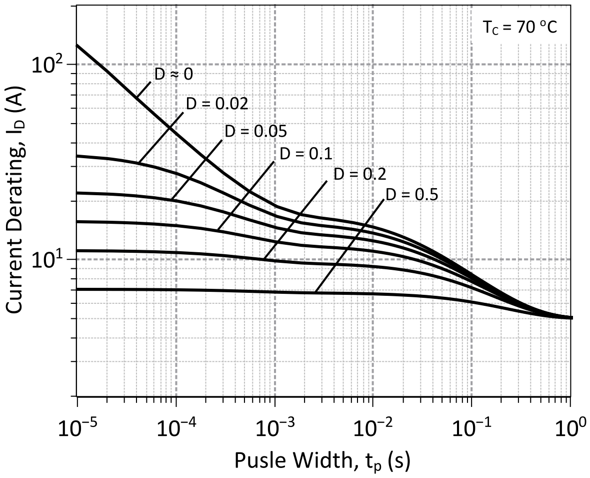

Figure 21: Drain Current Derating vs. Pulse Width

Section V: Driving the GA05JT01-46

The GA05JT01-46 is a current controlled SiC transistor which requires a positive gate current for turn-on and to remain in on-state. It may be driven by different drive topologies depending on the intended application.

Table 1: Estimated Power Consumption and switching frequencies for various Gate Drive topologies.

Drive Topology	Gate Drive Power Consumption	Switching Frequency
Simple TTL	High	Low
Constant Current	Medium	Medium
High Speed – Boost Capacitor	Medium	High
High Speed – Boost Inductor	Low	High
Proportional	Lowest	Medium
Pulsed Power	Medium	N/A

A: Simple TTL Drive

The GA05JT01-46 may be driven by 5 V TTL logic by using a simple current amplification stage. The current amplifier output current must meet or exceed the steady state gate current, $I_{G,steady}$, required to operate the GA05JT01-46. An external gate resistor R_G, shown in the Figure 22 topology, sets $I_{G,steady}$ to the required level which is dependent on the SJT drain current I_D and DC current gain h_{FE}, R_G may be calculated from the equation below. The values of h_{FE} and $V_{GS,sat}$ may be read from Figure 6 and Figure 7, respectively. $V_{EC,sat}$ can be taken from the PNP datasheet, a partial list of high-temperature PNP and NPN transistors options is given below. High-temperature MOSFETs may also be used in the topology.

$$R_{G,max} = \frac{\left(5.0\,V - V_{EC,sat}(PNP) - V_{GS,sat}(SJT)\right) * h_{FE}(T, I_D)}{I_D * 1.5}$$

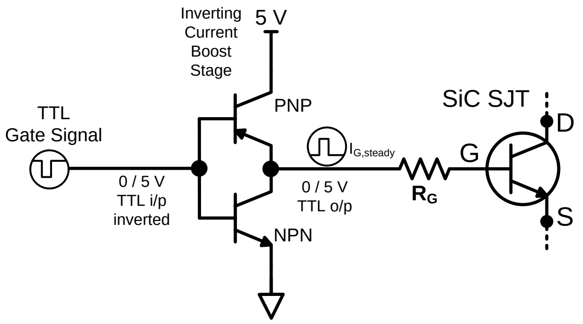

Figure 22: Simple TTL Gate Drive Topology

Table 2: Partial List of High-Temperature BJTs for TTL Gate Driving

BJT Part Number	Type	$T_{j,max}$ (°C)
PHPT60603PY	PNP	175
PHPT60603NY	NPN	175
2N2222	NPN	200
2N6730	PNP	200
2N2905	PNP	200
2N5883	PNP	200
2N5885	NPN	200

B: High Speed Driving

For ultra high speed GA05JT01-46 switching (t_r, t_f < 20 ns) while maintaining low gate drive losses the supplied gate current should include a positive current peak during turn-on, a negative voltage peak during turn-off, and continuous gate current I_G to remain on.

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge for turn-on, Q_G, is supplied by a burst of high gate current until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged. Ideally, the burst should terminate when the drain voltage has fallen to its on-state value in order to avoid unnecessary drive losses. A negative voltage peak is recommended for the turn-off transition in order to ensure that the gate current is not being supplied under high dV/dt due to the Miller effect. While satisfactory turn off can be achieved with $V_{GS} = 0$ V, a negative V_{GS} value may be used in order to speed up the turn-off transition.

B:1: High Speed, Low Loss Drive with Boost Capacitor

The GA05JT01-46 may be driven using a High Speed, Low Loss Drive with Boost Capacitor topology in which multiple voltage levels, a gate resistor, and a gate capacitor are used to provide current peaks at turn-on and turn-off for fast switching and a continuous gate current while in on-state. As shown in Figure 23, in this topology two gate driver ICs are utilized. An external gate resistor R_G is driven by a low voltage driver to supply the continuous gate current throughout on-state.and a gate capacitor C_G is driven at a higher voltage level to supply a high current peak at turn-on and turn-off. A 3 kV isolated evaluation gate drive board (GA03IDDJT30-FR4) from GeneSiC Semiconductor utilizing this topology is commercially available for high and low-side driving, its datasheet provides additional details about this drive topology.

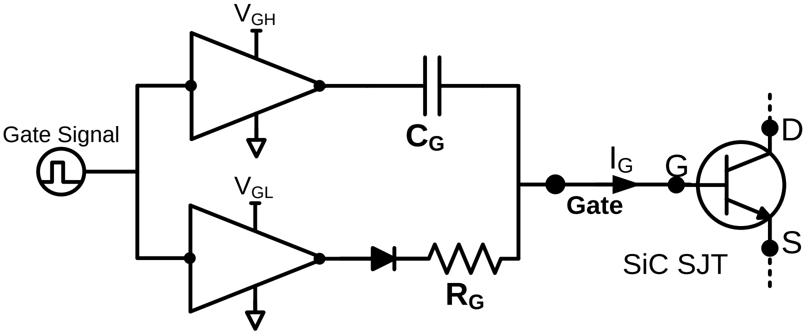

Figure 23: High Speed, Low Loss Drive with Boost Capacitor Topology

B:2: High Speed, Low Loss Drive with Boost Inductor

A High Speed, Low-Loss Driver with Boost Inductor is also capable of driving the GA05JT01-46 at high-speed. It utilizes a gate drive inductor instead of a capacitor to provide the high-current gate current pulses $I_{G,on}$ and $I_{G,off}$. During operation, inductor L is charged to a specified $I_{G,on}$ current value then made to discharge I_L into the SJT gate pin using logic control of S_1, S_2, S_3, and S_4, as shown in Figure 24. After turn on, while the device remains on the necessary steady state gate current $I_{G,steady}$ is supplied from source V_{CC} through R_G. Please refer to the article "A current-source concept for fast and efficient driving of silicon carbide transistors" by Dr. Jacek Rąbkowski for additional information on this driving topology.[3]

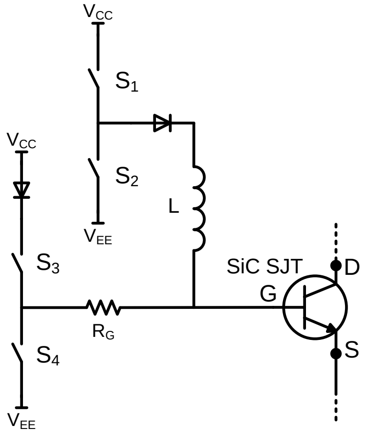

Figure 24: High Speed, Low-Loss Driver with Boost Inductor Topology

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[3] – Archives of Electrical Engineering. Volume 62, Issue 2, Pages 333–343, ISSN (Print) 0004-0746, DOI: 10.2478/aee-2013-0026, June 2013

C: Proportional Gate Current Driving

A proportional gate drive topology may be beneficial for applications in which the GA05JT01-46 will operate over a wide range of drain current conditions to lower the gate drive power consumption. A proportional gate driver relies on instantaneous drain current I_D feedback to vary the steady state gate current $I_{G,steady}$ supplied to the GA05JT01-46.

C:1: Voltage Controlled Proportional Driver

A voltage controlled proportional driver relies on a gate drive integrated circuit to detect the GA05JT01-46 drain-source voltage V_{DS} during on-state to sense I_D. The integrated circuit will then increase or decrease I_G in response to I_D. This allows I_G and gate drive power consumption to reduce while I_D is low or for I_G to increase when I_D increases. A high voltage diode connected between the drain and sense protects the integrated circuit from high-voltage when blocking. A simplified version of this topology is shown in Figure 25. Additional information will be available in the future at http://www.genesicsemi.com/references/product-notes/.

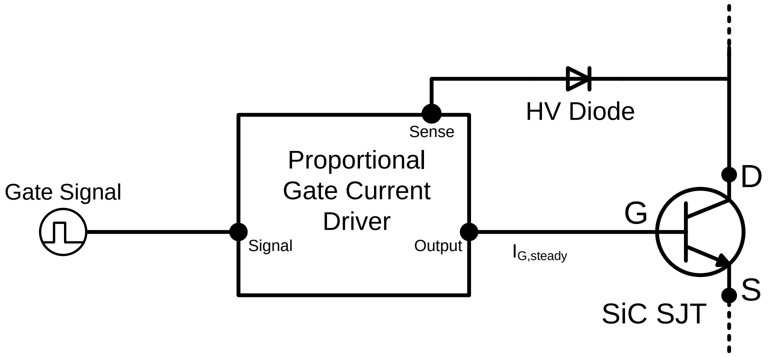


Figure 25: Simplified Voltage Controlled Proportional Driver

C:2: Current Controlled Proportional Driver

The current controlled proportional driver relies on a low-loss transformer in the drain or source path to provide feedback of the GA05JT01-46 drain current during on-state to supply $I_{G,steady}$ into the gate. $I_{G,steady}$ will increase or decrease in response to I_D at a fixed forced current gain which is set be the turns ratio of the transformer, $h_{force} = I_D / I_G = N_2 / N_1$. GA05JT01-46 is initially tuned-on using a gate current pulse supplied into an RC drive circuit to allow I_D current to begin flowing. This topology allows $I_{G,steady}$ and the gate drive power consumption to reduce while I_D is relatively low or for $I_{G,steady}$ to increase when I_D increases. A simplified version of this topology is shown in Figure 26. Additional information will be available in the future at http://www.genesicsemi.com/references/product-notes/.

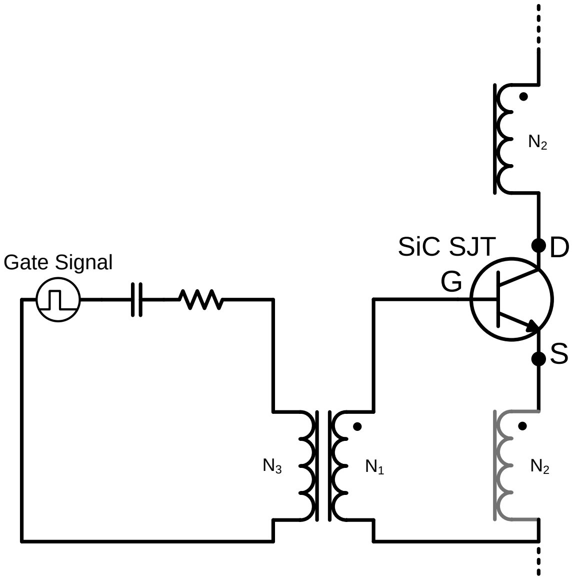
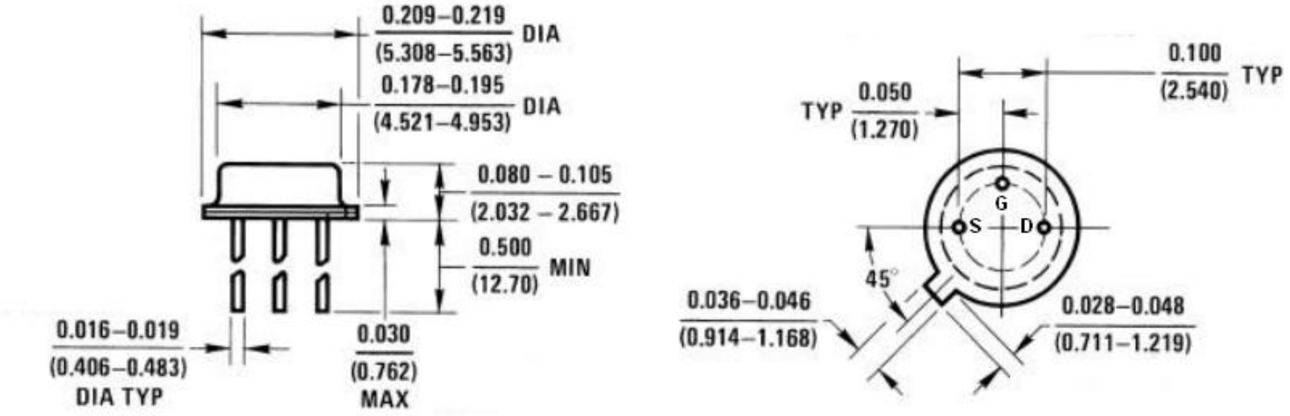


Figure 26: Simplified Current Controlled Proportional Driver

Section VI: Package Dimensions

TO-46 PACKAGE OUTLINE



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History

Date	Revision	Comments	Supersedes
2014/12/12	1	Updated Electrical Characteristics	
2014/08/25	0	Initial release	

Published by
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Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.

Section VII: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/sjt/GA05JT01-46_SPICE.pdf into LTSPICE (version 4) software for simulation of the GA05JT01-46.

```
*       MODEL OF GeneSiC Semiconductor Inc.
*
*       $Revision:   1.0              $
*       $Date:   12-DEC-2014          $
*
*       GeneSiC Semiconductor Inc.
*       43670 Trade Center Place Ste. 155
*       Dulles, VA 20166
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* IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA05JT01 NPN
+ IS            9.8338E-48
+ ISE           1.0733E-26
+ EG            3.23
+ BF            135
+ BR            0.55
+ IKF           200
+ NF            1
+ NE            2.
+ RB            14.5
+ IRB           0.002
+ RBM           0.37
+ RE            0.01
+ RC            0.23
+ CJC           2.16E-10
+ VJC           3.656
+ MJC           0.4717
+ CJE           5.021E-10
+ VJE           2.95
+ MJE           0.4867
+ XTI           3
+ XTB           -1.0
+ TRC1          1.050E-2
+ VCEO          100
+ ICRATING      9
+ MFG           GeneSiC_Semiconductor
*
* End of GA05JT01 SPICE Model
```