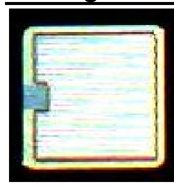
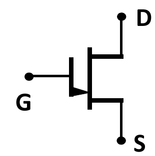
Normally – OFF Silicon Carbide Junction Transistor

V_{DS}	=	1200 V
$R_{DS(ON)}$	=	120 mΩ
$I_{D\ (Tc\ =\ 25°C)}$	=	25 A
$h_{FE\ (Tc\ =\ 25°C)}$	=	80

Features

- 250 °C Maximum Operating Temperature
- Gate Oxide Free SiC Switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Coefficient of $R_{DS,ON}$
- Suitable for Connecting an Anti-parallel Diode

Package

Advantages

- Compatible with Si MOSFET/IGBT Gate Drive ICs
- > 20 μs Short-Circuit Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Table of Contents

Section I: Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V	
Continuous Drain Current	I_D	T_C = 25°C	25	A	
Continuous Drain Current	I_D	T_C = 155°C	10	A	
Continuous Gate Current	I_G		1.3	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 250 °C, Clamped Inductive Load	$I_{D,max}$ = 10 @ $V_{DS} \leq V_{DSmax}$	A	
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 250 °C, I_G = 1 A, V_{DS} = 800 V, Non Repetitive	>20	μs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Power Dissipation	P_{tot}	T_C = 25 °C / 155 °C, t_p > 100 ms	170 / 22	W	
Storage Temperature	T_{stg}		-55 to 250	°C	

Section II: Static Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
A: On State							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 10 A, T_j = 25 °C I_D = 10 A, T_j = 125 °C I_D = 10 A, T_j = 175 °C		120 164 208		mΩ	Fig. 5
Gate On Voltage	$V_{GS,ON}$	I_D = 10 A, V_{DS} = 30 V, T_j = 25 °C I_D = 10 A, V_{DS} = 30 V, T_j = 175 °C		3.5 3.2		V	Fig. 4
DC Current Gain	h_{FE}	V_{DS} = 5 V, I_D = 10 A, T_j = 25 °C V_{DS} = 5 V, I_D = 10 A, T_j = 125 °C V_{DS} = 5 V, I_D = 10 A, T_j = 175 °C		80 56 50		–	Fig. 5
B: Off State							
Drain Leakage Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 25 °C V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 125 °C V_{DS} = 1200 V, V_{GS} = 0 V, T_j = 175 °C		1 1 10		μA	Fig. 6
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	

Section III: Dynamic Electrical Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz		1403		pF	Fig. 9
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_{DS} = 800 V, f = 1 MHz		30		pF	Fig. 9
Output Capacitance Stored Energy	E_{OSS}	V_{GS} = 0 V, V_{DS} = 800 V, f = 1 MHz		9		μJ	Fig. 10
Effective Output Capacitance, time related	$C_{oss,tr}$	I_D = constant, V_{GS} = 0 V, V_{DS} = 0…800 V		55		pF	
Effective Output Capacitance, energy related	$C_{oss,er}$	V_{GS} = 0 V, V_{DS} = 0…800 V		40		pF	
Gate-Source Charge	Q_{GS}	V_{GS} = -5…3 V		11		nC	
Gate-Drain Charge	Q_{GD}	V_{GS} = 0 V, V_{DS} = 0…800 V		44		nC	
Gate Charge - Total	Q_G			55		nC	
Internal Gate Resistance – zero bias	$R_{G(INT-ZERO)}$	f = 1 MHz, V_{AC} = 50 mV, V_{DS} = 0 V, V_{GS} = 0 V, T_j = 175 ºC		2.6		Ω	
Internal Gate Resistance – ON	$R_{G(INT-ON)}$	V_{GS} > 2.5 V, V_{DS} = 0 V, T_j = 175 ºC		0.19		Ω	

Section IV: Figures

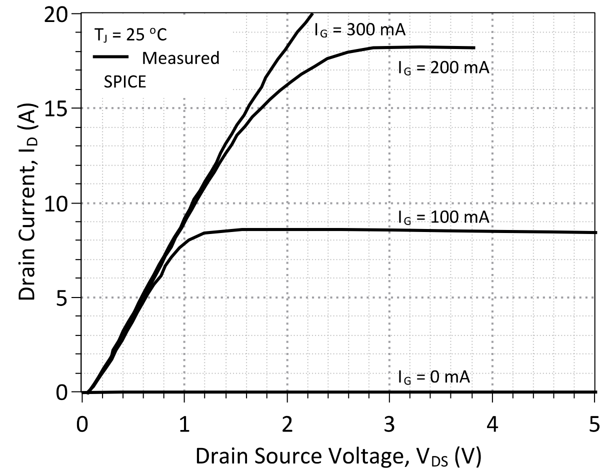


Figure 1: Typical Output Characteristics at 25 °C

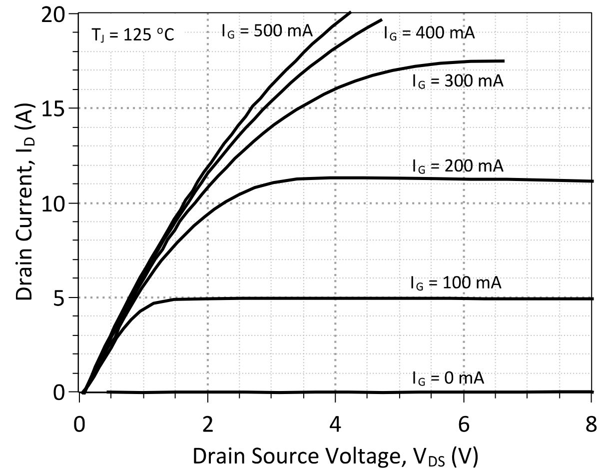


Figure 2: Typical Output Characteristics at 125 °C

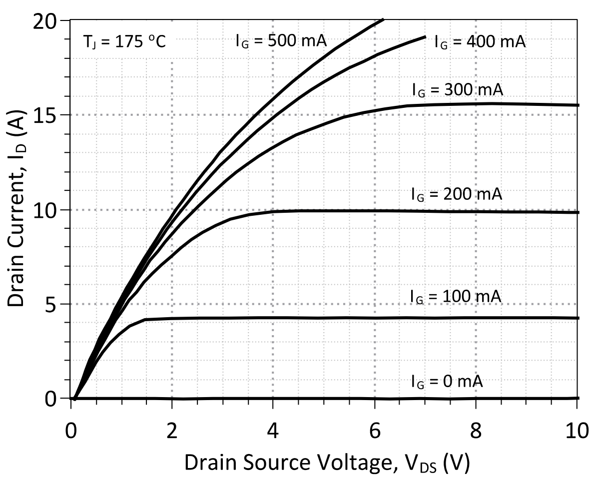


Figure 3: Typical Output Characteristics at 175 °C

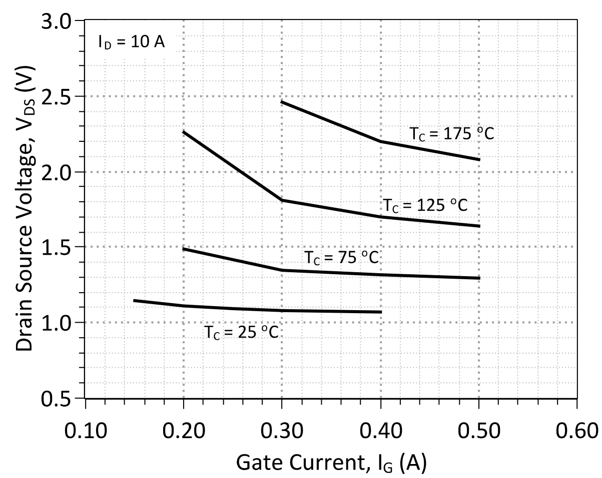


Figure 4: Drain-Source Voltage vs. Gate Current

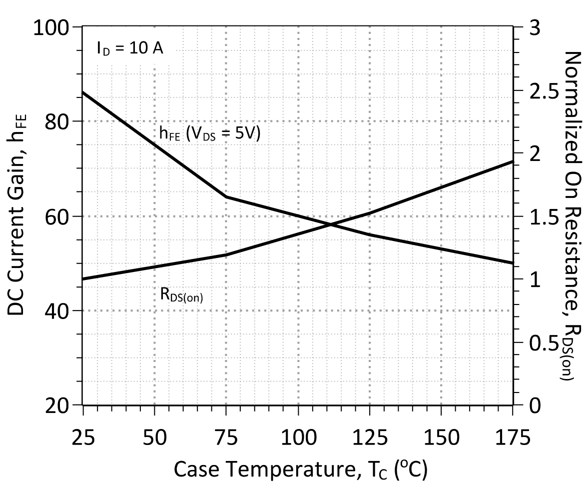


Figure 5: DC Current Gain and Normalized On-Resistance vs. Temperature

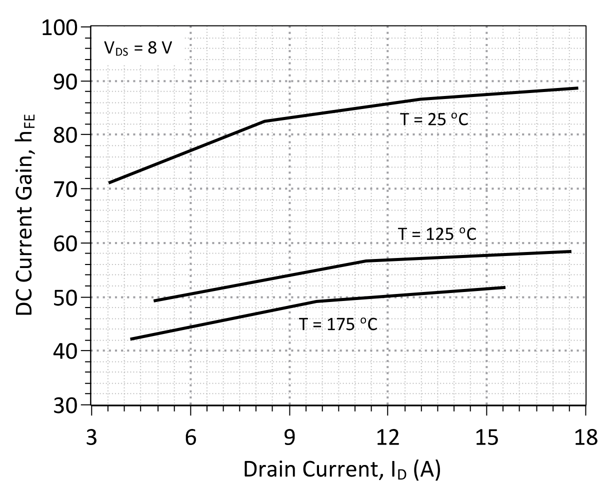


Figure 6: DC Current Gain vs. Drain Current

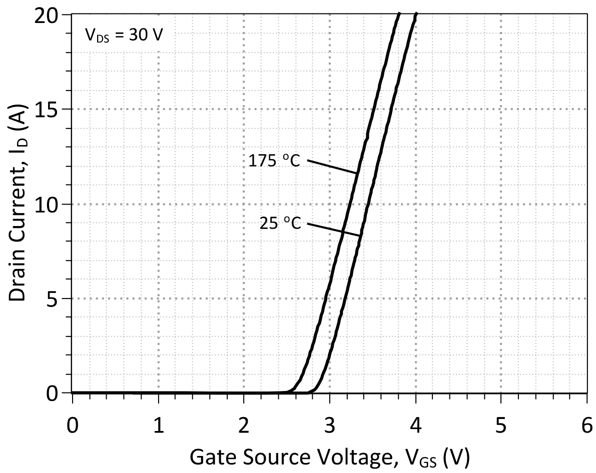


Figure 7: Typical Transfer Characteristics

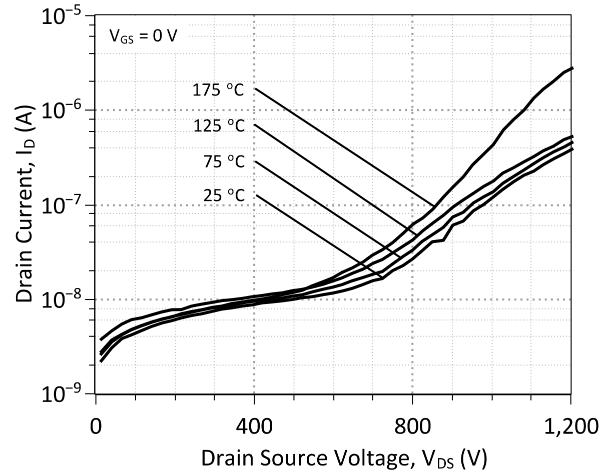


Figure 8: Typical Blocking Characteristics

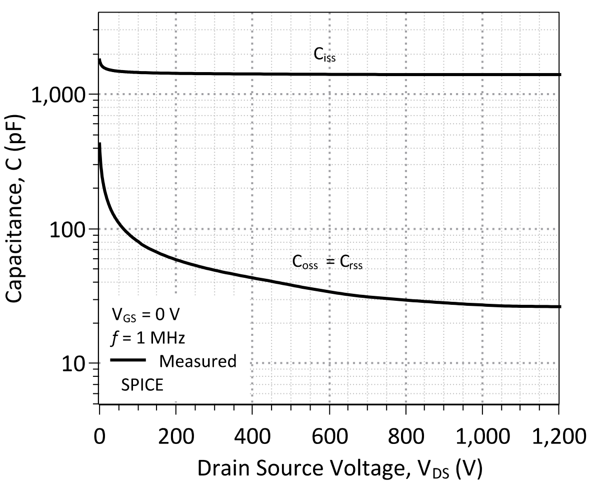


Figure 9: Input, Output, and Reverse Transfer Capacitance

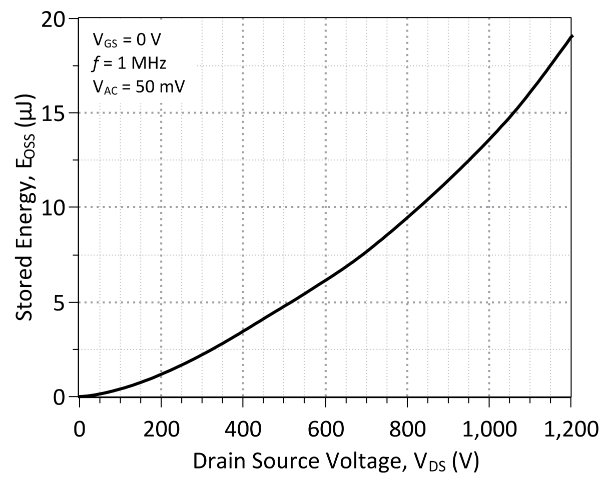


Figure 10: Output Capacitance Stored Energy

Section V: GA10JT12-CAL Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 11.

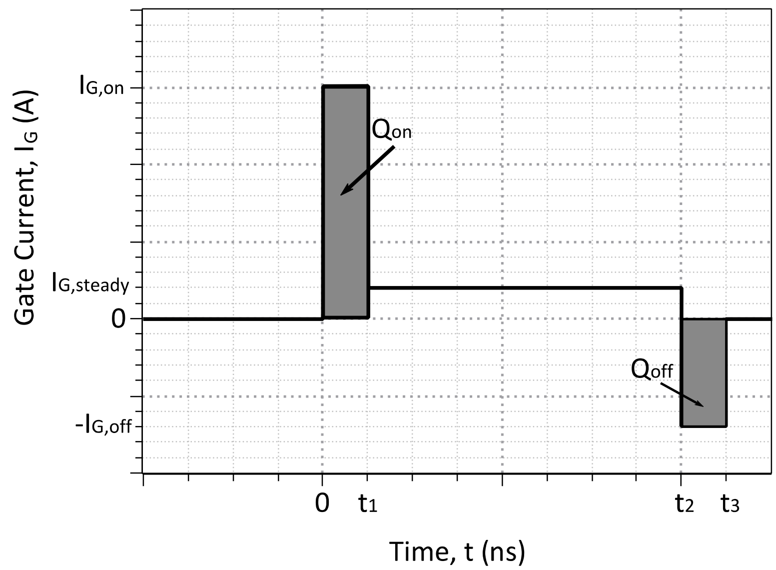


Figure 11: Idealized Gate Current Waveform

A: Gate Currents, $I_{G,pk}$/-$I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

As an example, an $I_{G,pon}$ ≥ 2.5 A is required to achieve a 18 ns V_{DS} fall time for a 800 V switching transition, due to the gate-drain charge, Q_{GD} of 44 nC for the GA10JT12-CAL. The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the TO-247 package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ (see Figure 7) level to counter these effects.

A high negative peak current, -$I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

B: Steady On-State

After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device from Figures 5 and 6.

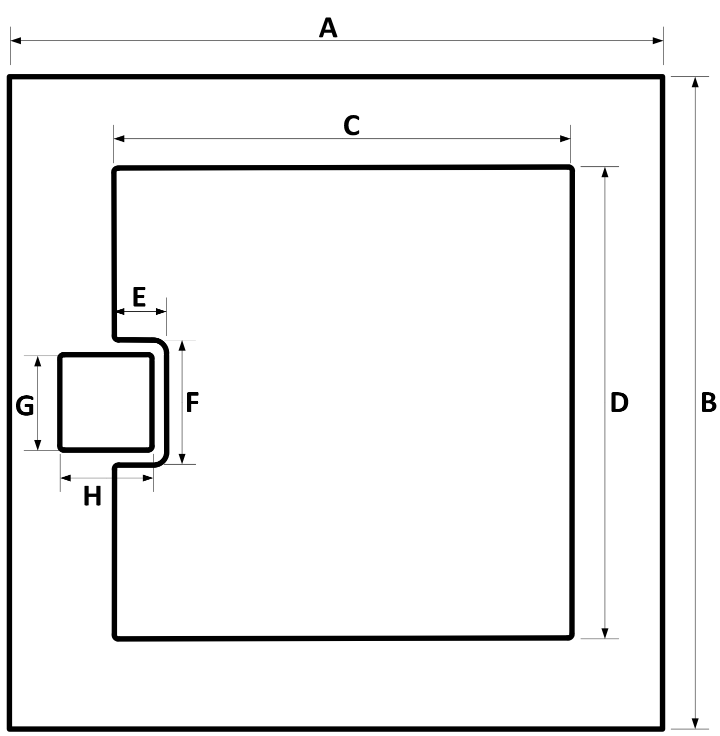
The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Section VI: Mechanical Parameters

Raster Size	2.10 x 2.10	mm^2	83 x 83	mil^2
Area total / active	4.41/3.31	mm^2	6836/5134	mil^2
Thickness	360	µm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Passivation frontside	Polyimide			
Pad Metal (Anode)	4000 nm Al			
Backside Metal (Cathode)	400 nm Ni + 200 nm Au -system			
Die Bond	Electrically conductive glue or solder			
Wire Bond	Al ≤ 10 mil (Source) Al ≤ 3 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

Section VII: Chip Dimensions



		mm	mil
DIE	A	2.10	83
	B	2.10	83
SOURCE WIREBONDABLE	C	1.47	58
	D	1.52	60
	E	0.17	7
	F	0.40	16
GATE WIREBONDABLE	G	0.30	12
	H	0.30	12

NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2014/09/12	0	Initial release	

Published by
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43670 Trade Center Place Suite 155
Dulles, VA 20166

Section VIII: SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/sjt/GA10JT12-CAL_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA10JT12-CAL.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   2.0           $
*     $Date:   12-SEP-2014       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
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*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA10JT12 NPN
+ IS       5.00E-47
+ ISE      1.26E-28
+ EG       3.23
+ BF       85
+ BR       0.55
+ IKF      5000
+ NF       1
+ NE       2
+ RB       4.67
+ IRB      0.001
+ RBM      0.16
+ RE       0.005
+ RC       0.099
+ CJC      427.39E-12
+ VJC      3.1004
+ MJC      0.4752
+ CJE      1373E-12
+ VJE      10.6442
+ MJE      0.21376
+ XTI      3
+ XTB      -1.27
+ TRC1     6.8E-3
+ VCEO     1200
+ ICRATING 10
+ MFG      GeneSiC_Semiconductor
*
* End of GA10JT12 SPICE Model
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