Gate Driver for SiC SJT with Signal Isolation

$V_{ISO,SIG}$	=	5000 V
P_{DRIVE}	=	27 W
f_{max}	=	350 kHz

Features

- Requires single 12 V voltage supply
- Pin Out compatible with MOSFET driver boards
- Multiple internal voltage level topology for low drive losses
- Point-of-load (POL), non-isolated design
- 5000 V Signal Isolation (up to 10 s)
- Capable of high gate currents with 27 W maximum power
- RoHS Compliant

Product Image

Section I: Introduction

The GA15IDDJT22-FR4 provides an optimized gate drive solution for 10 and 20 mΩ SiC Junction Transistors (SJT). The board utilizes DC/DC converters and FOD3182 signal opto-isolation as well as totem-pole gate driver ICs providing fast switching and customizable continuous gate currents necessary for any SJT device. Its footprint and 12 V supply voltage make it a plug-in replacement for existing SiC MOSFET gate drive solutions.

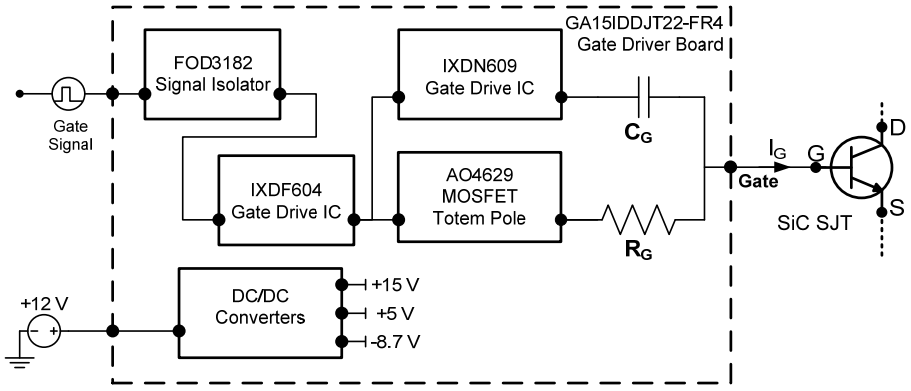


Figure 1: Simplified GA15IDDJT22-FR4 Gate Drive Board Block Diagram

Section II: Compatibility with SiC SJTs

The GA15IDDJT22-FR4 has an installed gate resistance (R_G) of 0.7 Ω on-board which may need to be modified by the user for safe operation of certain SJT parts. Please see the table below and Section VI for more information.

Table 1: GA15IDDJT22-FR4 – SiC SJT Compatibility Information Table

SJT Part Number	Compatible	Notes
GA03JT12-247	Yes	Driver GA03IDDJT30-FR4 Recommended
GA05JT12-247/263	Yes	Driver GA03IDDJT30-FR4 Recommended
GA06JT12-247	Yes	Driver GA03IDDJT30-FR4 Recommended
GA10JT12-247/263	Yes	Driver GA03IDDJT30-FR4 Recommended
GA20JT12-247/263	Yes	Driver GA03IDDJT30-FR4 Recommended
GA50JT12-247	Yes	
GA100JT12-227	Yes	Reduction of RG values recommended (Section VI)
GA04JT17-247	Yes	Driver GA03IDDJT30-FR4 Recommended
GA16JT17-247	Yes	Driver GA03IDDJT30-FR4 Recommended
GA50JT17-247	Yes	
GA100JT17-227	Yes	Reduction of RG values recommended (Section VI)
GA50SICP12-227	Yes	
GA100SICP12-227	Yes	Reduction of RG values recommended (Section VI)

Section III: Operational Characteristics

Parameter	Symbol	Conditions	Value			Unit	Notes
			Min.	Typical	Max.		
Input Supply Voltage	V_{CC}	V_{CC} High, V_{CC} Low	10.8	12	13.2	V	
Input Signal Voltage, Off	$V_{sig, OFF}$		-5	0	0.8	V	
Input Signal Voltage, On	$V_{sig, ON}$		3.2	5.0	6.4	V	
Input Signal Current, On	$I_{sig, ON}$		20	36	50	mA	
Propagation Delay, Signal Turn On	$t_{d,ON}$			160	270	ns	
Propagation Delay, Signal Turn Off	$t_{d,OFF}$			187	270	ns	
Output Gate Current, Peak	$I_{G,ON}$			7	15	A	
Output Gate Current, Continuous	$I_{G,steady}$	f < 350 kHz		2.0	5	A	
Output Gate Voltage Rise Time	t_r	C_{load} = 50 nF		40	70	ns	
Output Gate Voltage Fall Time	t_f	C_{load} = 50 nF		25	60	ns	
Operating Frequency	f_{sw}	Dependant on installed CG values			350	kHz	
Power Dissipation	P_{tot}	25.0 W (V_{GL}) + 2.0 W (V_{GH} + V_{EE})			27.0	W	
SJT Drain – Source Voltage	V_{DS}	On driven power transistor			1700	V	
Isolation Voltage, Signal	$V_{ISO-SIG}$				±5000	V	
Storage Temperature	T		-55		100	°C	
Product Weight				30		g	

Section IV: Pin Out Description

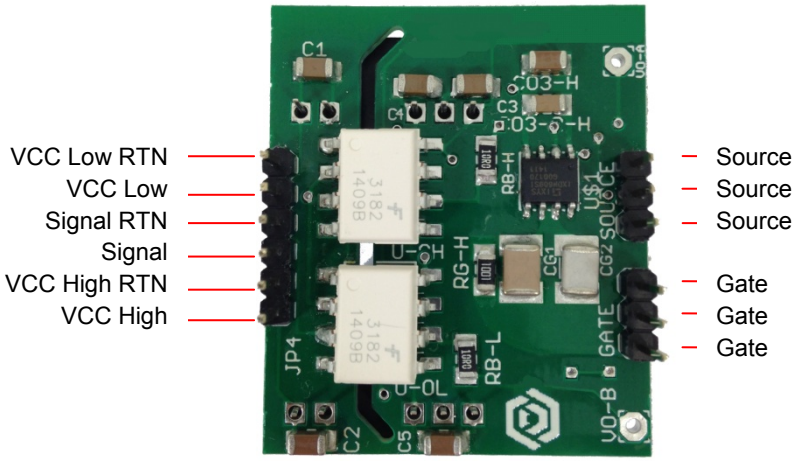


Figure 2: Gate Drive Board Top View

Table 2: GA15IDDJT22-FR4 Pin Out Connections

Header	Pin Label	Suggested Connection
JP1	VCC High	+ 12 V, > 30 W Supply
JP1	VCC High RTN	Analog Ground
JP1	Signal	Gate Drive Control Signal
JP1	Signal RTN	Analog Ground
JP1	VCC Low	+ 12 V, > 30 W Supply
JP1	VCC Low RTN	Analog Ground
Gate	Gate	SJT Gate Pin
Gate	Gate	SJT Gate Pin
Gate	Gate	SJT Gate Pin
Source	Source	SJT Source/GR Pin
Source	Source	SJT Source/GR Pin
Source	Source	SJT Source/GR Pin

Section V: SJT Gate Driving Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 3. This is similar to what the GA15IDDJT22-FR4 provides.

An SJT is rapidly switched on when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$Q_{on} = I_{G,on} * t_1$$

$$Q_{on} \geq Q_{gs} + Q_{gd}$$

The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the device package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

After the SJT is turned on, I_G may be lowered to $I_{G,steady}$ for reducing unnecessary gate drive power losses. The minimum $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device from its datasheet. The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

For SJT turn -off, a high negative peak current, $-I_{G,off}$ at the start of the turn-off transition rapidly sweeps out charge from the gate. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition. The GA15IDDJT22-FR4 provides a negative bias of -8.7 V during off state.

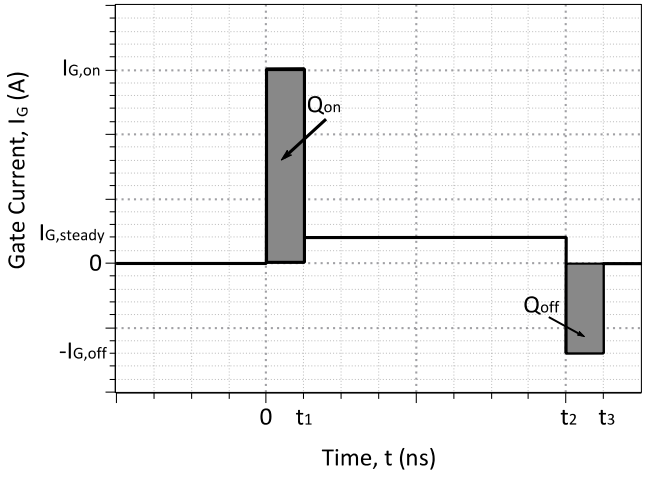


Figure 3: Idealized SJT Gate Current Waveform

Section VI: Gate Driver Implementation

The GA15IDDJT22-FR4 is a gate driver circuit which can be used to drive an SJT transistor by supplying the required gate drive current I_G in a low-power gate drive solution. This configuration features a gate capacitor C_G (CG1 and CG2 in parallel) which creates a brief current peak $I_{G,ON}$ during device turn-on and $I_{G,OFF}$ during turn-off for fast switching and a gate resistor R_G (RG1 and RG2 in parallel) to set the continuous gate current $I_{G,steady}$ required for an SJT to operate. This configuration is shown in the Figure 6 circuit diagram as well as in Figure 4 below with further details provided below. This section provides detail on selecting optimal C_G and R_G values based on the SJT, drain current, and temperature.

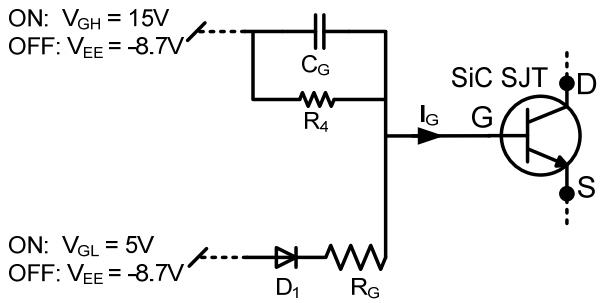


Figure 4: Primary gate drive circuit passive components with series gate resistance Schottky rectifier.

Table 3: Passive Output Component List

Symbol	Parameter	Values		
		Range	Default	Units
R_G	Gate Resistor, On Board	0 – 2.0	0.7	Ω
C_G	Gate Capacitor, On Board	5 – 50	22	nF
R_4	Charging Resistor	500 – 10k	1k	Ω
D_1	Schottky Diode of Gate Resistor	--	--	

A: Gate Resistor R_G Modification

The GA15IDDJT22-FR4 on board gate resistors R_G (RGx) control the continuous current $I_{G,steady}$ during steady on-state. The gate current is determined according to:

$$I_{G,steady} = \frac{V_{GL} - V_{GS,sat} - V_D}{R_G + 0.04\Omega}$$

$$I_{G,steady} = \frac{4.5\ V - V_{GS,sat}}{R_G + 0.04\Omega}$$

Where V_{GL} is the internal, low-level drive voltage (5 V), $V_{GS,sat}$ is the driven SJT saturated gate-source voltage obtained from the individual device datasheets, V_D is the Schottky diode voltage drop (approximately 0.5 V), and 0.04 Ω is added from internal GA15IDDJT22-FR4 drive components.

It is necessary for the user to reduce R_G from its pre-install value of 0.7 Ω for several SiC SJTs for safe operation with the GA15IDDJT22-FR4 under high drain current conditions. The location of RG on the circuit board is shown in Figure 5. The maximum allowable value of R_G for each device across all rated drain currents can be found in the Gate Drive section of each individual device datasheets. R_G may also be calculated from the following equation, where h_{FE} is the SJT DC current gain and $V_{GS,sat}$ is the gate-source saturation voltage. Both of these values may be taken from individual device datasheets.

$$R_{G,max} = \frac{\left(4.5V - V_{GS,sat}\right) * h_{FE}(T, I_D)}{I_D * 1.5} - 0.04\Omega$$

For some devices and drain currents it may be desired for the user to install a very low value of R_G or to short R_G (R_G = 0 Ω) to increase the gate current output. This is acceptable, but may limit the duty cycle D during operation. Please see section VII:B for more information.

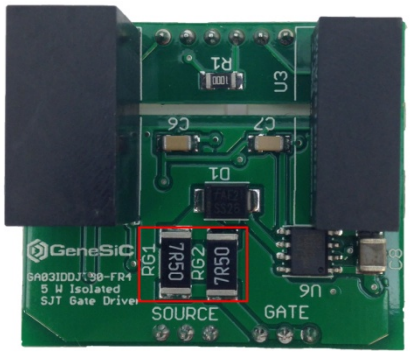


Figure 5: Location of R_G (RG1 and RG2 in parallel) on GA15IDDJT22-FR4 driver for substitution

B: Gate Capacitor C_G Modification

An external gate capacitor C_G connected directly to the device gate pin delivers the positive current peak $I_{G,ON}$ during device turn-on and the negative current peak $I_{G,OFF}$ during turn-off. A high value resistor R_4 in parallel with C_G sets the SJT gate pin to a defined potential $-V_{EE}$ (-8.7 V) during steady off-state.

At device turn-on, C_G is pulled to the GA15IDDJT22-FR4 internal voltage level V_{GH} (15 V) which produces a transient peak of gate voltage and current. This current peak rapidly charges the internal SJT C_{GS} and C_{GD} capacitances. A Schottky diode, D1, in series with R_G blocks any C_G induced current from draining out through R_G and ensures that all of the charge within C_G flows only into the device gate, allowing for an ultra-fast device turn-on. During steady on-state, a potential of V_{GH} - V_{GS} = V_{GH} – 3 V is across C_G. When the device is turned off, C_G is pulled to negative V_{EE} and V_{GS} is pulled to a transient peak of $V_{GS,turn-off} = V_{EE} – (V_{GH} – 3\ V)$, this induces the negative current peak $I_{G,off}$ out of the gate which discharges the SJT internal capacitances.

C: Voltage Supply Selection

The GA15IDDJT22-FR4 gate drive design features three internal supply voltages V_{GH}, V_{GL}, and V_{EE} (listed in Table 4) supplied through two DC/DC converters. During device turn-on, V_{GH} charges the capacitor C_G thereby delivering the narrow width, high current pulse $I_{G,ON}$ to the SJT gate and charges the SJT's internal terminal capacitances C_{GD} and C_{GS}. For a given level of parasitic inductance in the gate circuit and SJT package, the rise time of $I_{G,ON}$ is controlled by the value of V_{GH} and C_G. During the steady on-state, V_{GL} in combination with the internal and external gate resistances provides a continuous gate current for the SJT to remain on. The V_{EE} supply controls the gate negative voltage during turn-off and steady off-state for faster switching and to avoid spurious turn-on which may be caused by external circuit noise. The power rating of the provided voltage supplies are adequate to meet the gate drive power requirements as determined by

$$P_{min,VGH} = \frac{1}{2}\, C_G\, V_{GH}^2\, f_{sw}$$

$$P_{min,VEE} = \frac{1}{2}\, C_G\, V_{EE}^2\, f_{sw}$$

$$P_{min,VGL} = V_{GL} I_{G,steady}\, D$$

Table 4: GA15IDDJT22-FR4 Gate Drive Voltage Supply Component List

Symbol	Parameter	Values	
		Range	Default
V_{GH}	Supply Voltage, Gate Capacitor	13 – 20	+ 15.0
V_{GL}	Supply Voltage, Gate Resistor	4.5 – 6.0	+ 5.0
V_{EE}	Negative Supply Voltage	-10 – GND	- 8.7

D: Signal Isolation

The gate supply signal is suggested to be isolated to twice the working V_{DS} on the SJT during off-state to provide adequate protection to circuitry external to the gate drive circuit. This may be done using opto or galvanic isolation techniques.

Section VII: Detailed Schematic and Bill of Materials

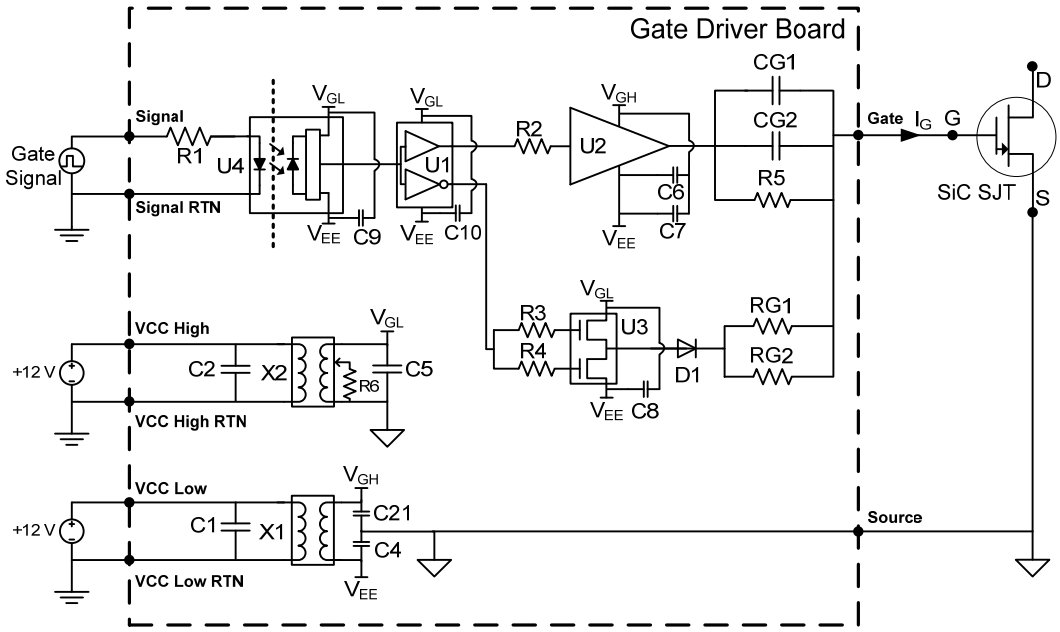


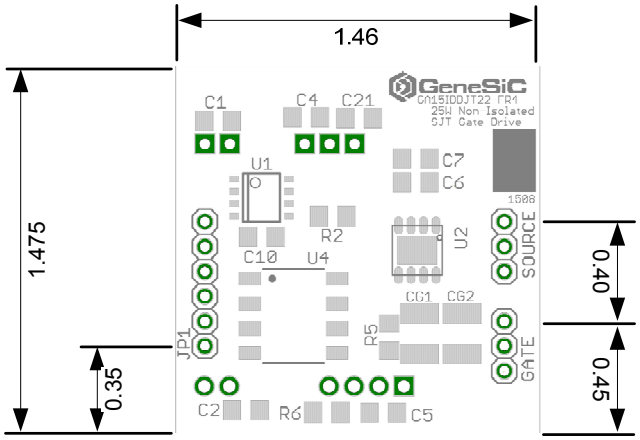
Figure 6: Gate Drive Board Detailed Block Diagram

Table 5: Gate Drive Board Bill of Materials

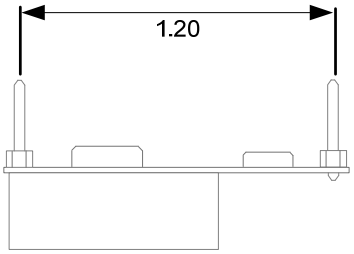
# ITEM	Designator	Description	Package (Metric)	Manufacturer	Manufacturer Part Number	Quantity /Board
1	CAP CER 0.1UF 50V 10% X7R 1206	C6, C9, C10	3216	Murata	GRM319R71H104KA01D	3
2	CAP CER 22UF 25V 10% X5R 1206	C1, C2, C7	3216	Murata	GRM31CR61E226KE15L	3
3	CAP CER 47UF 25V 20% X5R 1206	C4, C5, C21	3216	TDK	C3216X5R1E476M160AC	3
4	CAP CER 100UF 16V 20% X5R 1210	C8	3225	Taiyo Yuden	EMK325ABJ107MM-T	1
5	RES 100 OHM 1/4W 1% 1206 SMD	R1	3216	Yageo	RC1206FR-07100RL	1
6	RES SMD 10 OHM 1% 1/4W 1206	R2	3216	Panasonic	ERJ-8ENF10R0V	1
7	RES SMD 7.5 OHM 5% 1/4W 1206	R3	3216	Yageo	RC1206JR-077R5L	1
8	RES SMD 3.3 OHM 5% 1/4W 1206	R4	3216	Yageo	RC1206JR-073R3L	1
9	RES SMD 1K OHM 1/4W 1% 1206	R5	3216	Yageo	RC1206FR-071KL	1
10	RES SMD 1.47K R 0.1% 1/4W 1206	R6	3216	Panasonic	ERA-8AEB1471V	1
11	CONN HDR BRKWAY .100 3POS VERT	GATE, SOURCE	3POS HEADER	TE Connectivity	5-146274-3	2
12	CONN HEADER VERT 6POS .100 TIN	JP1	6POS HEADER	TE Connectivity	3-644456-6	1
13	DIODE SCHOTTKY 40V 4A DO214AA	D1	SMB	Micro Commercial	SK44BL-TP	1
14	IC GATE DVR 4A DIFF 8-SOIC	U1	8-SOIC	IXYS	IXDF604SIA	1
15	IC GATE DVR 9A NON-INV 8-SOIC	U2	8-SOIC	IXYS	IXDN609SI	1
16	MOSFET N/P-CH 30V 6A/5.5A 8SOIC	U3	8-SOIC	Alpha & Omega	AO4629	1
17	OPTOISO 5KV GATE DRIVER 8SMT	U4	8-SMT	Fairchild	FOD3182S	1
18	DC/DC CONVERTER 15V -8.7V 2W	X1	7-SIP	CUI	VQA-S12-D15-SIP	1

19	DC-DC CONVRT 0.7525-5.5V 5A 5SIP	X2	7-SIP	Murata	OKX-T/5-D12N-C	1
20	CAP CER 0.022UF 200V X7R 1812	CG1	4532	Kemet	C1812C223K2RACTU	1
21	RES SMD 2.2 OHM 5% 2W 2512	RG1	6332	Bourns	CRM2512-JW-2R2ELF	1
22	RES SMD 1 OHM 5% 2W 2512	RG2	6332	Bourns	CRM2512-JW-1R0ELF	1

Section VIII: Mechanical Drawing

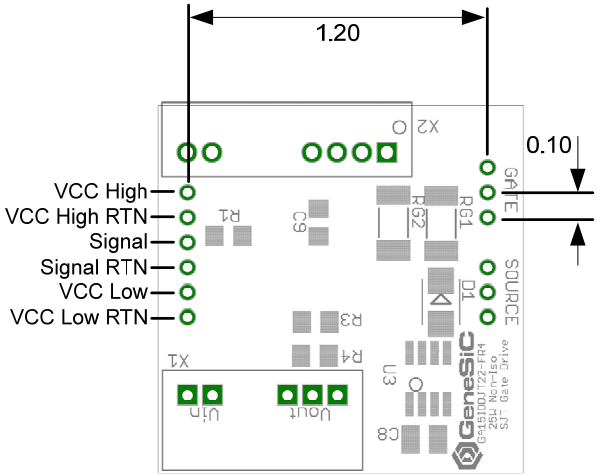


Top



Front

Note: Header Pins JP1, GATE, and SOURCE extend from “Top” face



Bottom

All units inches

Figure 7: Gate Drive Board Mechanical Drawing

Revision History			
Date	Revision	Comments	Supersedes
2014/09/09	0	Initial release	

Published by
GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155
Dulles, VA 20166