# GC5325 Wideband Digital Predistortion Transmit Processor

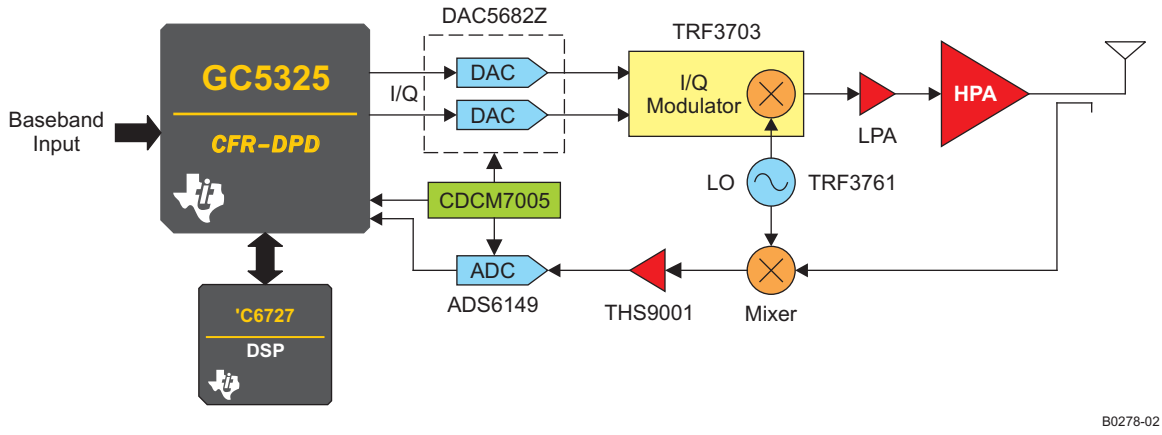
## FEATURES

- Integrated CFR and DPD Functions
- Up to 20-MHz Combined Signal Bandwidth
- CFR: Typically Meets 3GPP TS 25.141 <6.5 dB PAR, <8 dB PAR for 802.16e Signals
- DPD: Memory Compensation, Typical ACLR Improvement of 20 dB to 30 dB or More
- Transmit- and Feedback-Channel Equalizers
- 352-Ball S-PBGA Package, 27 mm × 27 mm
- 1.2-V Core, 3.3-V I/O
- Typical Power Consumption = 1.9 W
- Flexible DSP Algorithm Supports Existing and Emerging Wireless Standards
- Supports Direct Interface to TI High-Speed Data Converters

## APPLICATIONS

- 3GPP (W-CDMA, TD-SCDMA) Base Stations
- 3GPP2 (CDMA2000) Base Stations
- WiMAX and WiBRO (OFDMA) Base Stations
- Multicarrier Power Amplifiers (MCPAs)

## SYSTEM BLOCK DIAGRAM




## DESCRIPTION

The GC5325 is a wideband digital predistortion transmit processor that includes a crest factor reduction (CFR) block and a digital predistortion (DPD) block with its associated feedback chain and capture buffers. The GC5325 processes composite input bandwidths of up to 20 MHz and processes DPD sample rates of up to 140 MHz. The GC5325 accepts a composite signal over an interleaved parallel interface at a data rate of up to 140 MSPS. The GC5325 CFR block reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I/Q) format, such as those used in third-generation (3G) code division multiple access (CDMA) wireless and orthogonal frequency division multiple access (OFDMA) applications. The GC5325 DPD block reduces adjacent-channel leakage ratio (ACLR), or out-of-band energy, by 20 dB to 30 dB or more. The efficiency of follow-on power amplifiers (PAs) is substantially improved by reducing the PAR and ACLR of digital signals. The digital-to-RF conversion can be further simplified by the fractional interpolator between the CFR and the DPD blocks, and a bulk upconverter (BUC) in the final stage of the GC5325. This feature typically eliminates the need for superheterodyne (dual-stage) upconversion architectures. Transmit and feedback NCO/mixers provide additional flexibility in the system frequency planning.

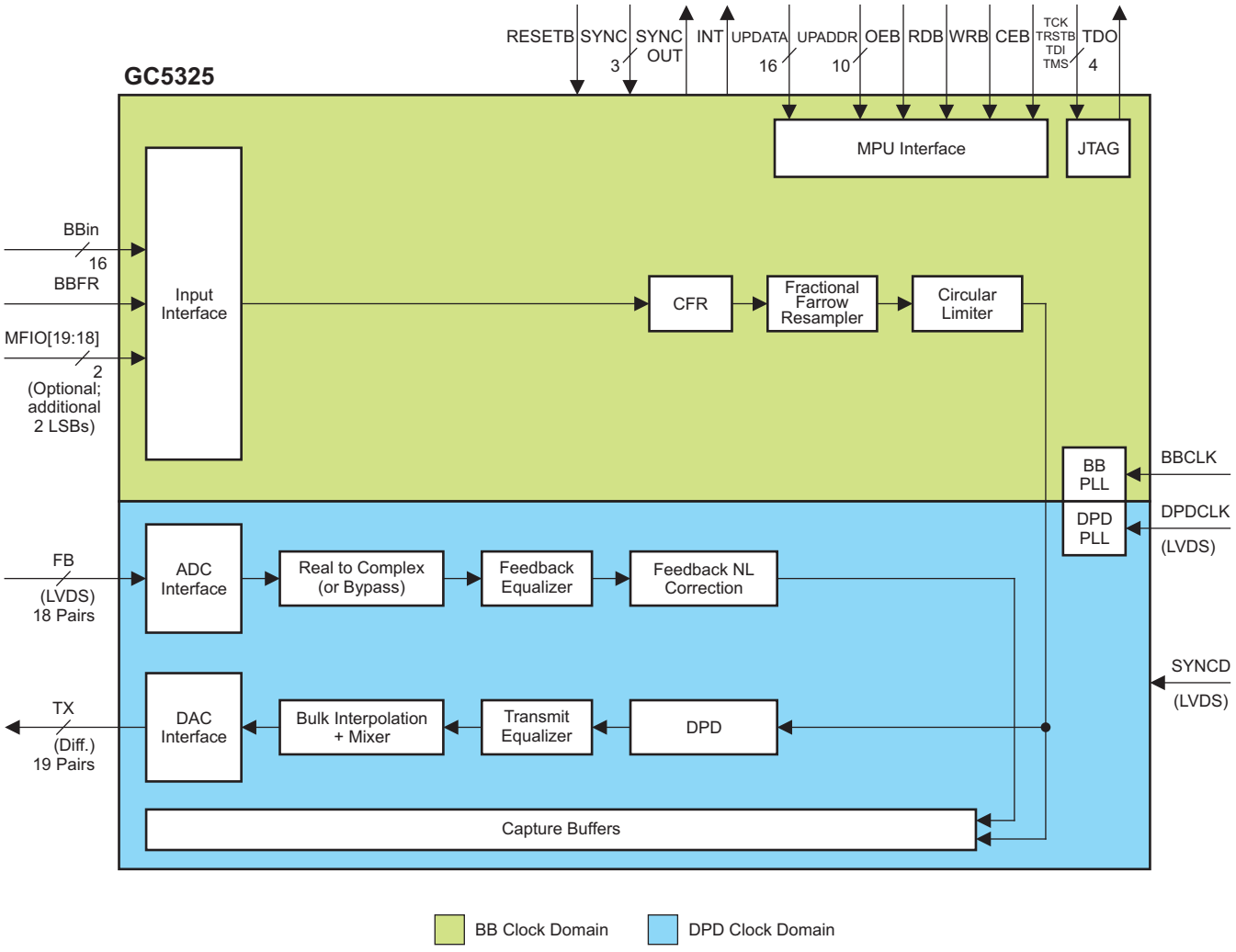
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTIONS

| $T_C$ | PACKAGED DEVICE(1) |
|---|---|
| | 352-ball S-PBGA package, 27 mm × 27 mm |
| –40°C to 85°C | GC5325IZND |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## GC5325 FUNCTIONAL BLOCK DIAGRAM



# DETAILED DESCRIPTION

## GC5325 Introduction

The GC5325 is a flexible transmit sector processor that includes a crest factor reduction (CFR) block and a digital predistortion (DPD) block and its associated feedback chain. The GC5325 processes composite input bandwidths of up to 40 MHz and processes DPD expansion bandwidths of up to 140 MHz (actual performance may vary for signal bandwidths exceeding 23 MHz). By reducing both the peak-to-average ratio (PAR) of the input signals using the CFR block and linearizing the power amplifier (PA) using the DPD block, the GC5325 reduces the costs of multicarrier PAs (MCPA) for wireless infrastructure applications. The GC5325 applies CFR and DPD while a separate microprocessor (a Texas Instruments TMS320C6727 DSP) is used to optimize performance levels and maintain target PA performance levels.

By including the GC5325 in their system architecture, manufacturers of BTS equipment can realize significant savings on power amplifier bill of materials (BOM) and overall operational costs due to the PA efficiency improvement. The GC5325 meets multicarrier 3G performance standards (PCDE, composite EVM, and ACLR) at PAR levels down to 6.5 dB and improves the ACLR, at the PA output, by 20 dB to 30 dB or more. The GC5325 integrates easily into the transmit signal chain between baseband processors such as the Texas Instruments TMS320C64x™ DSP family and their high-performance data converters.

A typical GC5325 system application would include the following transmit-chain components:

- TMS320C6727 digital signal processor (DSP)
- DAC5682 16-bit, 1-GSPS DAC (transmit path)
- CDCM7005 clock generator
- TRF3761 integrated VCO/PLL synthesizer
- TRF3703 quadrature modulator
- ADS5517 11-bit 200-MSPS or ADS6149 14-bit, 250-MSPS ADC (feedback path)
- AMC7823 analog monitoring and control circuit with GPIO and SPI

## Baseband Interface

The GC5325 BB interface block accepts baseband signals over an interleaved parallel interface at a data rate of up to 140 MHz. The input interface supports up to 12 separate baseband carriers. The GC5325 input interface can be programmed in a wideband mode in which users are required to channelize the data using an external processor.

## Gain/Pilot Insertion/AntCal Insertion/Power Meter

Baseband gain can be applied on a per-carrier basis to accurately control the individual channel power through the system. Also present is the functionality for adding pilot codes to the data stream for antenna calibration applications. Independent programmable RMS power meters for up to 12 channels are also included in this block of the device.

## Crest Factor Reduction (CFR)

The GC5325 CFR block selectively reduces the peak-to-average ratio (PAR) of wideband digital signals provided in quadrature (I and Q) format, such as those used in third-generation (3G) code division multiple access (CDMA) wireless applications. The CFR block can reduce the PAR of W-CDMA Test Model 1 and Test Model 3 signals down to 6.5 dB output PAR while still meeting all 3GPP requirements for ACLR, composite EVM, and peak code domain error (PCDE). The CFR block accepts input sampling rates up to 140 MSPS complex from the input interface.

## Fractional Farrow Resampler (FR)

The CFR block output signal bandwidth is up to 40 MHz wide, sampled at up to 70 MSPS. However; the DPD block provides PA compensation over an expansion bandwidth of up to 140 MHz, using a complex sampling rate of up to 140 MSPS. To provide the requisite sampling rate of up to 140 MSPS at the input to DPD, the output of the CFR block must be resampled. The GC5325 performs this (nominally 2×) upsampling function using a Farrow filter resampler. The user-programmable Farrow resampler supports upsampling rates from 1× to 64×, with 16-bit precision on the interpolation ratio. It marks the transition of the input clock domain (driven by the input interface clock) to the transmit domain (driven by the DAC sampling clock).

## Digital Predistortion (DPD)

The DPD block provides predistortion for up to Nth-order nonlinearities, and can correct multiple orders and lengths of PA memory effects. The predistortion correction terms are computed by an external processor (for example, TI TMS320C6727 DSP) based on PA feedback data captured in the GC5325. The external processor reads the captured data buffers from the GC5325 and writes back the newly computed DPD correction terms on a continuous basis. TI provides a base delivery of 'C6727 software to GC5325 customers that achieves a typical ACLR improvement of 20 dB to 30 dB or more when compared to a PA without DPD. The standard EMIF bus allows the user to provide an alternate DPD adaptation algorithm and DSP embodiment, if desired.

## Bulk Upconverter (BUC)

The bulk upconverter block can interpolate the DPD block output by 1.5×, 2×, 3× with a complex output, or 6× with a real output. The complex-to-real converter block optionally modifies the DPD complex output stream into a real output stream. The bulk upconverter has flexible mixing options between its various interpolation stages. When used in combination, the bulk upconverter and the complex-to-real functions allow the GC5325 to output a 16-bit real signal at up to 840 MSPS, or a complex signal at up to 420 MSPS. Next-generation data converters can accept sampling rates as high as 1 GSPS and sample widths of 16 bits. In a typical application, the bulk upconverter outputs a 737.28-MSPS real sampling rate (16 bits/sample) directly to the DAC on a modified center frequency of 184.32 MHz (1/4 of the 737.28-MSPS sampling rate). The bulk upconverter has multiple high-speed, low-voltage, single-ended/differential output interfaces to existing and future TI DACs.

## Feedback Path (FB)

The feedback block accepts an external A/D converter input that represents the PA output signal. This feedback signal is processed by a feedback path that adjusts for gain, frequency, and phase anomalies in the RF-to-IF downconversion chain. The feedback path includes an 8-tap complex receive equalizer and lookup tables that can compensate for the nonlinearities in the RF-to-IF part of the feedback chain. The block also includes a real-to-complex conversion to facilitate signal processing. The GC5325 connects directly to the ADS5444, ADS5545, ADS5546, and ADS5517 among others, without requiring external components. The GC5325 simplifies timing by providing a FIFO for each ADC port, sampling the input data using the ADC data-ready signal.

## Microprocessor Interface (MPU)

The MPU interface is designed to interface with external memory interface (EMIF) ports on TI DSPs operating in asynchronous mode. It consists of a 16-bit bidirectional data bus, a 10-bit address bus, and RDB, WRB, OEB, and CEB control signals. The interface fully supports TI C55x™, C64x™ DSPs and, with minimal effort, supports the low-cost 'C6727 floating-point DSP.

## Smart Capture Buffers (SCB)

The GC5325 has two capture buffers, each 4096 complex words deep, which are periodically read by the external coefficient update controller (DSP) in order to optimize the DPD coefficients. The first capture buffer can be used to capture:

- The output of the Farrow resampler; this is also called the reference signal.
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(31:16)

The second capture buffer can be used to provide:

- The output of the Farrow resampler; this is also called the reference signal.
- The feedback output; this represents the waveform as seen by the PA.
- The error output
- Testbus(15:0)

The reference and feedback buffers are time-aligned by the GC5325, because there may be a delay of tens or even hundreds of samples between the transmitted signal and the feedback signal from the PA output. The capture controller can trigger a capture on several different metrics, including an above-threshold peak count or an average signal power value.

## Input and Output Syncs

The GC5325 features multiple-user programmable input syncs. These are typically used as trigger mechanisms to activate features within the device. These triggers can be provided internally or through externally provided inputs. The input syncs can be used to trigger:

- Power measurements
- Initializing/loading the feedback, equalizer, LUTs, etc.
- Flush out data within the processing blocks of the device
- Feedback path tuner alignment
- Capturing and sourcing of data through SCBs

## Programmable Power Meters

There are three power meter locations/functions within the GC5325. The first is a channel RMS power meter. The second power meter is located at the output of the CFR block, and the final power detector is similar to the CFR output power detector and is located at the Farrow resampler output. This power meter can measure RMS power integrated up to a million samples at the DPD sample rate.

## Pin Assignment and Descriptions

**GND Package**
**(Bottom View)**

| | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS1 | VSS1 | VSS1 | VSS1 | FB1 | FB5 | FB9 | FB11 | FB15 | FB17 | FB21 | FB25 | FB27 | VDD SHV | FB31 | FB35 | VSSA2 | SYNCC | BB15 | BB11 | BB7 | BB3 | BB0 | VSS1 | VSS1 | VSS1 |
| B | VDD1 | VSS1 | VSS1 | VSS1 | FB0 | FB4 | FB8 | FB10 | FB14 | FB16 | FB20 | FB24 | FB26 | VDD SHV | FB30 | FB34 | VDDA2 | SYNCB | BBFR | BB12 | BB8 | BB4 | BB1 | VSS1 | VSS1 | VDD1 |
| C | VSS1 | VDD1 | VSS1 | VSS1 | NC | FB3 | FB7 | VDD1 | FB13 | ADC IREF | FB19 | FB23 | VDD1 | VDD SHV | FB29 | FB33 | VDD1 | SYNCA | BBCLK | BB13 | BB9 | BB5 | BB2 | VSS1 | VDD1 | VSS1 |
| D | VSS1 | VSS1 | VDD1 | VSS1 | NC | FB2 | FB6 | VDD1 | FB12 | ADC VREF | FB18 | FB22 | VDD1 | VDD SHV | FB28 | FB32 | VSS1 | SYNC OUT | VDD1 | BB14 | BB10 | BB6 | VSS1 | VDD1 | VSS1 | VSS1 |
| E | VSS1 | VSS1 | VSS1 | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VSS1 | VSS1 | VSS1 |
| F | VSS1 | VSS1 | VSS1 | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VDD1 | VSS1 | VSS1 |
| G | VSS1 | VSS1 | VSS1 | VDD SHV | | | | | | | | | | | | | | | | | | | VDD SHV | VSS1 | VSS1 | VSS1 |
| H | NC | NC | VPP1 | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP ADDR2 | UP ADDR1 | UP ADDR0 |
| J | VPP1 | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP ADDR5 | UP ADDR4 | UP ADDR3 |
| K | NC | NC | VDD SHV | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP ADDR8 | UP ADDR7 | UP ADDR6 |
| L | NC | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VDD SHV | WRB | UP ADDR9 |
| M | NC | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | OEB | CEB | RDB |
| N | NC | NC | VDD SHV | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP DATA2 | UP DATA1 | UP DATA0 |
| P | NC | NC | MFIO18 | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VDD SHV | VSS1 | VSS1 |
| R | MFIO19 | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP DATA5 | UP DATA4 | UP DATA3 |
| T | NC | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VDD SHV | VPP2 | UP DATA6 |
| U | NC | NC | VDD SHV | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP DATA8 | UP DATA7 | VPP2 |
| V | NC | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP DATA11 | UP DATA10 | UP DATA9 |
| W | NC | NC | NC | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | UP DATA14 | UP DATA13 | UP DATA12 |
| Y | NC | VSS1 | VSS1 | VDD1 | | | | | | | | | | | | | | | | | | | VDD SHV | VSS1 | VSS1 | UP DATA15 |
| AA | VSS1 | VSS1 | VSS1 | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VSS1 | VSS1 | VSS1 |
| AB | VSS1 | VSS1 | VSS1 | VDD1 | | | | | | | | | | | | | | | | | | | VDD1 | VDD1 | VSS1 | VSS1 |
| AC | VSS1 | VSS1 | VDD1 | RESET B | VDD SHV | DPD CLK | VSS1 | VDD1 | TX2 | TX6 | TX10 | TX14 | VDDS | VSS1 | DAC REFP | TX25 | TX29 | TX33 | TX37 | VSS1 | VDD1 | VDD2 | VSS1 | VDD1 | VSS1 | VSS1 |
| AD | VSS1 | VDD1 | VSS1 | VSS1 | DPD IREF | DPD CLKC | VSS1 | VDDA1 | TX3 | TX7 | TX11 | TX15 | VDDS | VSS1 | DAC REFN | TX24 | TX28 | TX32 | TX36 | VDD SHV | VDD1 | VSS2 | VSS1 | VSS1 | VDD1 | VSS1 |
| AE | VDD1 | VSS1 | VSS1 | VSS1 | DPD VREF | SYNCD | VDD SHV | TX0 | TX4 | TX8 | TX12 | TX16 | VDDS | TX19 | TX21 | TX23 | TX27 | TX31 | TX35 | TRSTB | TDI | INTER-RUPT | VSS1 | VSS1 | VSS1 | VDD1 |
| AF | VSS1 | VSS1 | VSS1 | VSS1 | VSS1 | SYNC DC | VSSA1 | TX1 | TX5 | TX9 | TX13 | TX17 | VSS1 | TX18 | TX20 | TX22 | TX26 | TX30 | TX34 | TMS | TCK | TDO | TEST MODE | VSS1 | VSS1 | VSS1 |

= Baseband Input
= Transmit Ouput
= Feedback Input
= Microprocessor Interface
= Miscellaneous
= Multi-Function Input/Output
= Power and Biasing
= JTAG Interface
= NC

P0077-01

## Table 1. TERMINAL FUNCTIONS

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **MICROPROCESSOR INTERFACE** | | | |
| OEB | M3 | I | Output enable |
| CEB | M2 | I | Chip enable |
| RDB | M1 | I | Read |
| WRB | L2 | I | Write |
| UPADDR[9:0] | L1, K3, K2, K1, J3, J2, J1, H3, H2, H1 | I | Microprocessor address |
| UPDATA[15:0] | Y1, W3, W2, W1, V3, V2, V1, U3, U2, T1, R3, R2, R1, N3, N2, N1 | I/O | Microprocessor data |
| INTERRUPT | AE5 | O | Microprocessor interrupt |
| **POWER AND BIASING** | | | |
| VDD1 | B1, B26, C2, C10, C14, C19, C25, D3, D8, D14, D19, D24, E4, E23, F3, F4, F23, H4, H23, J4, J23, K4, K23, L4, L23, M4, M23, N4, N23, P4, P23, R4, R23, T4, T23, U4, U23, V4, V23, W4, W23, Y23, AA4, AA23, AB3, AB4, AB23, AC3, AC6, AC19, AC24, AD2, AD6, AD25, AE1, AE26 | PWR | 1.2-V supply |
| VSS1 | A1, A2, A3, A23, A24, A25, A26, B2, B3, B23, B24, B25, C1, C3, C23, C24, C26, D1, D2, D4, D10, D23, D25, D26, E1, E2, E3, E24, E25, E26, F1, F2, F24, F25, F26, G1, G2, G3, G24, G25, G26, P1, P2, Y2, Y3, Y24, Y25, AA1, AA2, AA3, AA24, AA25, AA26, AB1, AB2, AB24, AB25, AB26, AC1, AC2, AC4, AC7, AC13, AC20, AC25, AC26, AD1, AD3, AD4, AD13, AD20, AD23, AD24, AD26, AE2, AE3, AE4, AE23, AE24, AE25, AF1, AF2, AF3, AF14, AF22, AF23, AF24, AF25, AF26 | PWR | Ground |
| VDD2 | AC5 | NC | Do not connect |
| VSS2 | AD5 | NC | Do not connect |
| VDDS | AC14, AD14, AE14 | PWR | 1.8-V supply |
| VDDSHV | A13, B13, C13, D13, G4, G23, K24, L3, N24, P3, T3, U24, Y4, AC22, AD7, AE20 | PWR | 3.3-V supply |
| VDDA1 | AD19 | PWR | 1.2-V supply (requires filtering) |
| VSSA1 | AF20 | PWR | Ground (requires filtering) |
| VDDA2 | B10 | PWR | 1.2-V supply (requires filtering) |
| VSSA2 | A10 | PWR | Ground (requires filtering) |
| VPP1 | H24, J26 | PWR | 1.2-V supply |
| VPP2 | T2, U1 | PWR | 1.2-V supply |
| DPDIREF | AD22 | PWR | DPD bias 1 kΩ to VSS |
| DPDVREF | AE22 | PWR | DPD bias to VDD |
| DACREFP | AC12 | PWR | DAC bias 50-Ω to VSS |
| DACREFN | AD12 | PWR | DAC bias 50-Ω to VDDS |
| ADCIREF | C17 | PWR | ADC bias 1 kΩ to VSS |
| ADCVREF | D17 | PWR | ADC bias to VDD |
| **BASEBAND INPUT** | | | |
| BB[15:0] | A8, D7, C7, B7, A7, D6, C6, B6, A6, D5, C5, B5, A5, C4, B4, A4 | I | Baseband input signal |
| BBCLK | C8 | I | Baseband input clock |
| BBFR | B8 | I | Baseband frame for sample and channel timing |
| MFIO[19:18] | R26, P24 | I | LSBs for 18-bit baseband input signal [-2, -1] |
| **MISCELLANEOUS** | | | |
| RESETB | AC23 | I | Chip reset (active-low .Required.) |

**Table 1. TERMINAL FUNCTIONS (continued)**

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SYNCA | C9 | I | Programmable general-purpose sync |
| SYNCB | B9 | I | Programmable general-purpose sync |
| SYNCC | A9 | I | Programmable general-purpose sync |
| SYNCD | AE21 | I | Programmable general-purpose sync |
| SYNCDC | AF21 | I | Complementary of SYNCD |
| SYNCOUT | D9 | O | Programmable general-purpose sync output |
| DPDCLK | AC21 | I | Clock to DPD |
| DPDCLKC | AD21 | I | Complementary clock to DPD |
| TESTMODE | AF4 | I | Tie to ground |
| **JTAG INTERFACE** | | | |
| TCK | AF6 | I | JTAG clock |
| TDI | AE6 | I | JTAG data in |
| TDO | AF5 | O | JTAG data out |
| TRSTB | AE7 | I | JTAG reset (active-low); pull down if JTAG is not used. |
| TMS | AF7 | I | JTAG mode select |
| **SIGNALS (See mode selection guide for pin assignment)** | | | |
| TX[37:0] | AC8, AD8, AE8, AF8, AC9, AD9, AE9, AF9, AC10, AD10, AE10, AF10, AC11, AD11, AE11, AF11, AE12, AF12, AE13, AF13, AF15, AE15, AD15, AC15, AF16, AE16, AD16, AC16, AF17, AE17, AD17, AC17, AF18, AE18, AD18, AC18, AF19, AE19 | O | Transmit to DAC(s) |
| FB[35:0] | A11, B11, C11, D11, A12, B12, C12, D12, A14, B14, A15, B15, C15, D15, A16, B16, C16, D16, A17, B17, A18, B18, C18, D18, A19, B19, A20, B20, C20, D20, A21, B21, C21, D21, A22, B22 | I | Feedback from ADC(s) |
| NC | Y26, W24, W25, W26, V24, V25, V26, U25, U26, T24, T25, T26, R24, R25, P25, P26, N25, N26, M24, M25, M26, L24, L25, L26, K25, K26, J24, J25, H25, H26, D22, C22 | – | No connect |

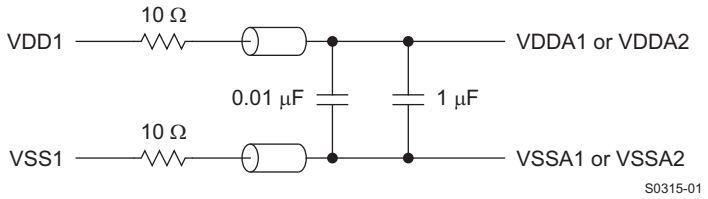



**Figure 1. GC5325 PLL Power Supply Filter**

The two PLLs require an analog supply. These can be generated by filtering the core digital supply (Vdd). A representative filter is shown in Figure 1. The two PLLs should have separate filters and be located as close as reasonable to their respective pins (especially the bypass capacitors). The ferrite beads should be series 50R (similar to Murata P/N: BLM31P500SPT Description: IND FB BLM31P500SPT 50R 1206). In particular, supply VDDA1 must be less than or equal to VDD1 when VDD1 is at the low end of the required range. The series resistor assures this condition is met.

**Table 2. GC5325 TX Interface Options**

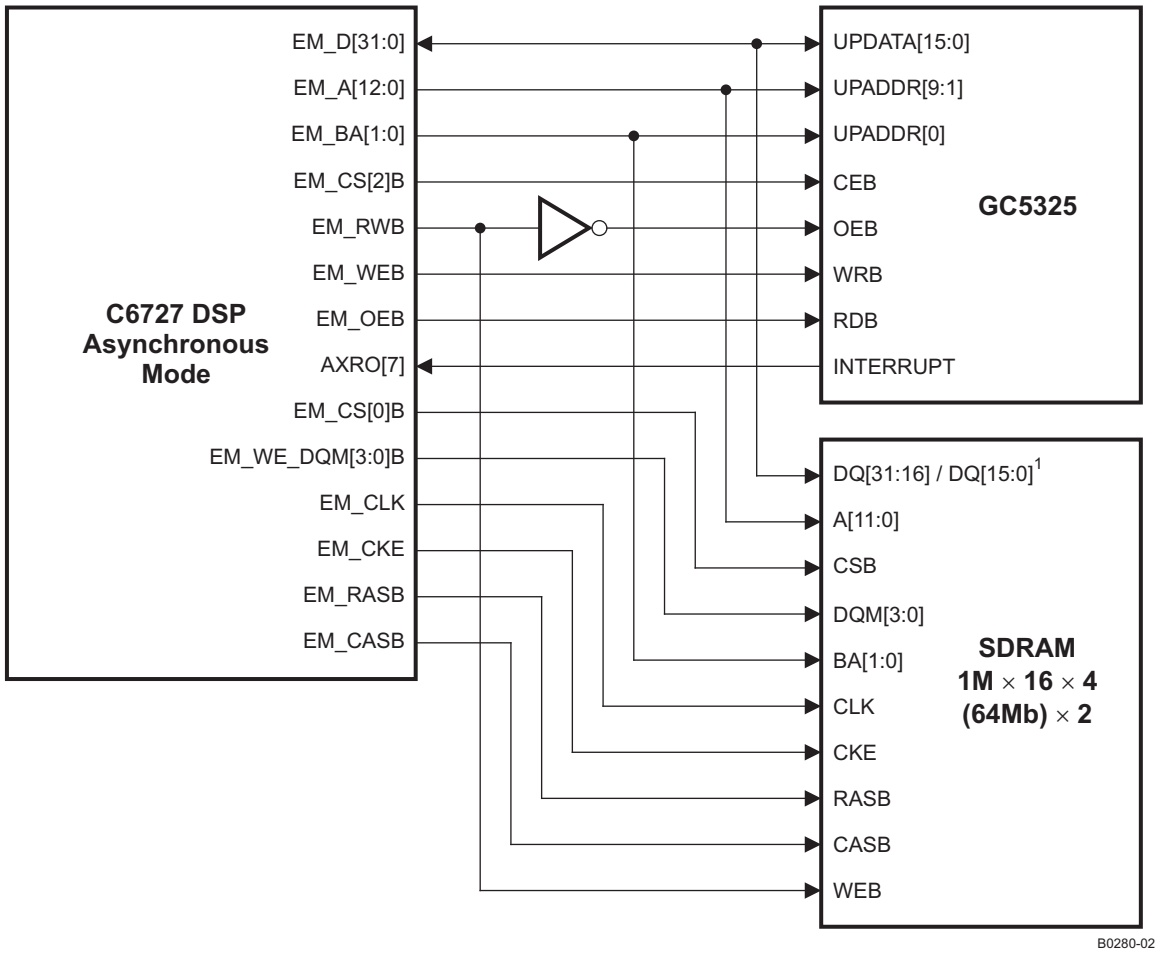
| PIN FUNCTION | PIN NAME | I/O | DESCRIPTION |
|---|---|---|---|
| **TX (Single-Channel HSTL)** | | | |
| DAC[15:0]P | TX10, TX6, TX2, TX0, TX4, TX8, TX12, TX16, TX23, TX27, TX31, TX35, TX32, TX36, TX29, TX25 | O | DAC positive output |
| DAC[15:0]N | TX11, TX7, TX3, TX1, TX5, TX9, TX13, TX17, TX22, TX26, TX30, TX34, TX33, TX37, TX28, TX24 | O | DAC negative output |
| DACCLK | TX21 | O | Clock to DAC |
| DACCLKC | TX20 | O | Complementary clock to DAC |
| DACSYNCP | TX14 | O | Positive output data sync |
| DACSYNCN | TX15 | O | Negative output data sync |

**Table 3. GC5325 FB Interface Options**

| PIN FUNCTION | PIN NAME | I/O | DESCRIPTION |
|---|---|---|---|
| **Feedback (Single-Channel SDR LVDS or DDR LVDS)** | | | |
| ADC[15:0]P | FB2, FB4, FB6, FB8, FB10, FB12, FB14, FB16, FB20, FB22, FB24, FB26, FB28, FB30, FB32, FB34 | I | ADC positive feedback from PA output |
| ADC[15:0]N | FB3, FB5, FB7, FB9, FB11, FB13, FB15, FB17, FB21, FB23, FB25, FB27, FB29, FB31, FB33, FB35 | I | ADC negative feedback from PA output |
| ADCCLK | FB0 | I | Clock from ADC |
| ADCLKC | FB1 | I | Complementary clock from ADC |
| **Feedback (Single- or Dual-Channel DDR LVDS)** | | | |
| ADCA[7:0]P | FB2, FB4, FB6, FB8, FB10, FB12, FB14, FB16 | I | ADC-A positive feedback from PA output |
| ADCA[7:0]N | FB3, FB5, FB7, FB9, FB11, FB13, FB15, FB17 | I | ADC-A negative feedback from PA output |
| ADCACLK | FB0 | I | Clock from ADC-A |
| ADCACLKC | FB1 | I | Complementary clock from ADC-A |
| ADCB[7:0]P | FB20, FB22, FB24, FB26, FB28, FB30, FB32, FB34 | I | ADC-B positive feedback from PA output |
| ADCB[7:0]N | FB21, FB23, FB25, FB27, FB29, FB31, FB33, FB35 | I | ADC-B negative feedback from PA output |
| ADCBCLK | FB18 | I | Clock from ADC-B |
| ADCBCLKC | FB19 | I | Complementary clock from ADC-B |

## MPU Interface Guidelines

The following section describes the hardware interface between the recommended microprocessor, external memory, and the GC5325. Users may select a microprocessor that meets their specific system requirements. Although the hardware can support multiple options, the recommended TMS320C6727 DSP is also fully supported with host control and adaptation software. Figure 2 illustrates the hardware interface between the DSP to GC5325 and SDRAM. The external memory is required to accommodate the computational efforts of the adaptation algorithm. Although the system evaluation kit suggests dual parallel 64-Mb/PC133 (128-Mb) memory modules provided by Samsung (K4S641632H-TC(L)75), other memory alternatives are available. The processing speed or convergence time of the adaptation algorithm is not strictly limited by the external memory speed rating. The use of an external inverter, with minimal propagation delay, is required for OEB of the GC5325; this device is necessary when using a TMS320C6727 DSP. Additional documentation for the hardware interface is available in the *Hardware Designer's Resource Guide* application report (SPRAA87) and *TMS320C672x DSP External Memory Interface (EMIF)* user's guide (SPRU711).




NOTE: Dual SDRAM modules are used, upper and lower EMIF data lines are split to access each respective memory module.

**Figure 2. DSP to GC5325/SDRAM Interface Specifications**

In a typical implementation, the system configuration software resides locally (in nonvolatile memory) to ensure proper operation at power up. The adaptation algorithm should also reside in the same location; at power up, the host should transfer/load the software from the nonvolatile memory (FLASH) to the 'C6727 DSP. The size of the software required to support the GC5325 and 'C6727 should be no more than 128 Mb (16 MB); however, this allocation is subject to change pending algorithm improvements. The suggested host-to-DSP interface is through the UHPI port. See Chapter 0.

The port can be configured into multiple modes of data transfer; the *Multiplexed Host Address/Data Dual Halfword Mode* is suggested for this application.

Additional specifications and documents for the TMS320C6727 DSP are available from Texas Instruments at:

http://focus.ti.com/docs/prod/folders/print/tms320c6727b.html.

## Typical Baseband Interface

The GC5325 baseband interface receives time-interleaved I and Q data for each channel over the 16- or 18-bit input bus. The BB[15..0] bus is the 16-bit interface or the top 16 bits of the 18-bit interface. The frame strobe BBFS signal is used to identify the first channel I data. The data is input in channel order, I then Q. The baseband clock is used to register the interleaved IQ data and frame strobe.

The hardware sync signals SyncA, SyncB, and SyncC are used to time-align internal GC5325 operations. A 0-to-1 transition clocked by BBClock is an active sync signal.

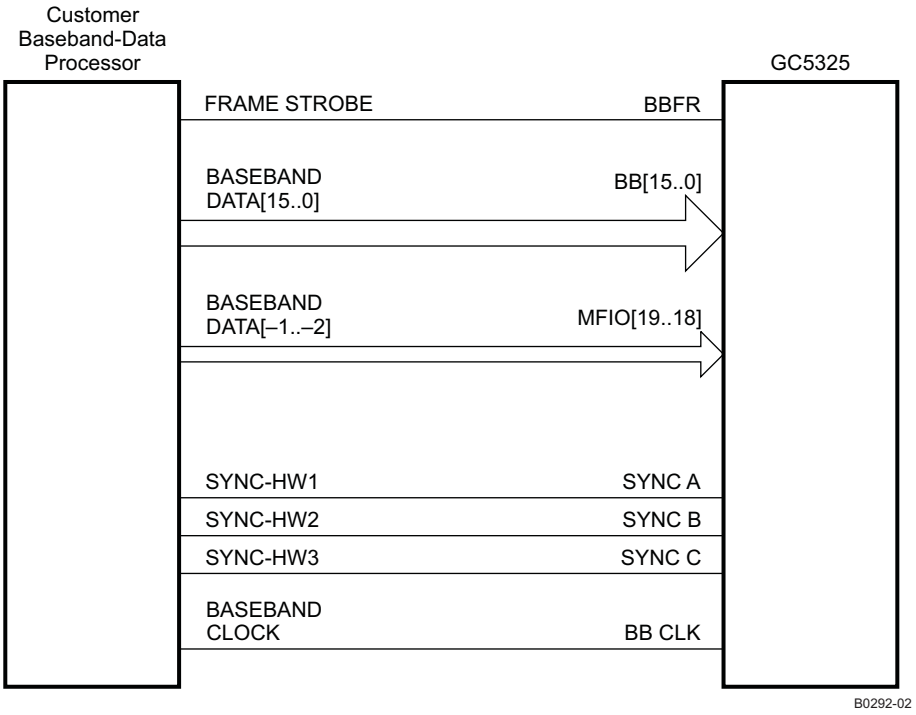



**Figure 3. Typical Baseband Interface**

## GENERAL SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{DD}$, $V_{DDA}$ | Core supply voltage | –0.3 to 1.32 | V |
| $V_{DDS}$ | Digital supply voltage for TX | –0.3 to 2 | V |
| $V_{DDSHV}$ | Digital supply voltage | –0.3 to 3.6 | V |
| $V_{IN}$ | Input voltage (under/overshoot) | –0.5 to $V_{DDSHV}$ + 0.5 | V |
| | Clamp current for an input/output | –20 to 20 | mA |
| $T_{stg}$ | Storage temperature | –65 to 150 | °C |
| | Lead soldering temperature, 10 seconds | 300 | °C |
| | ESD Classification Class 2 (Required 2-kV HBM, 500-V CDM) (Passed 2.5-kV HBM, 500-V CDM, 200-V MM) | | |
| | Moisture sensitivity Class 3 (1 week floor life at 30°C/60% H) | | |
| | Reflow conditions JEDEC standard | 260 | = C |

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$, $V_{DDA2}$, $V_{PP}$ | Core supply voltages. Note $V_{DDA2} \le V_{DD}$ | | 1.14 | 1.2 | 1.26 | V |
| $V_{DDA1}$ | Analog supply for DPD PLL | See (1) | 1 | 1.1 | VDD | V |
| $V_{DDS}$ | Digital supply voltage for TX | | 1.71 | 1.8 | 1.89 | V |
| $V_{DDSHV}$ | Digital supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $I_{DD}$, $I_{DDA1}$, $I_{DDA2}$, $I_{PP}$ | Combined supply current for Vdd, Vdda1, Vdda2, and $V_{PP}$ | | | | 3 | A |
| $I_{DDS}$ | Digital supply current for TX | | | | 0.25 | A |
| $I_{DDSHV}$ | Digital supply current | | | | 0.3 | A |
| $T_C$ | Case temperature | See (2) | -40 | 30 | 85 | °C |
| $T_J$ | Junction temperature | See (3) | | | 105 | °C |

(1) VDDA1 must be less than VDD1 when VDD1 is low. See recommended filtering circuit in Figure 1. Maximum observed current on VDDA1 is 8 mA.
(2) Chip specifications in are production tested to 90°C case temperature. QA tests are performed at 85°C.
(3) Thermal management may be required for full-rate operation. Sustained operation at elevated temperatures reduces long-term reliability. Lifetime calculations based on maximum junction temperature of 105°C.

## THERMAL CHARACTERISTICS

| PARAMETER | | 352 BGA at 4 W | UNITS |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient (still air) | 15 | °C/W |
| $R_{\theta JMA1}$ | Theta junction to ambient (1 m/s) | 11.8 | °C/W |
| $R_{\theta JC}$ | Thermal resistance, junction-to-case | 0.92 | °C/W |
| $R_{\theta JB}$ | Thermal resistance, junction-to-board | 5.3 | °C/W |

## GENERAL ELECTRICAL CHARACTERISTICS

Describes the electrical characteristics for the baseband interface, multifunction I/O (MFIO), DPD clock and fast sync, MPU and JTAG interfaces over recommended operating conditions. Device is production tested at 90 = C for the given specification and characterized at –40 = C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CMOS INTERFACE** | | | | | | |
| $V_{IL}$ | CMOS voltage input, low | | | | 0.8 | V |
| $V_{IH}$ | CMOS voltage input, high | | 2 | | $V_{DDSHV}$ | V |
| $V_{OL}$ | CMOS voltage output, low | $I_{OL}$ = 2 mA | | | 0.5 | V |
| $V_{OH}$ | CMOS voltage output, high | $I_{OH}$ = –2 mA | 2.4 | | $V_{DDSHV}$ | V |
| $\|I_{PU}\|$ | Pullup current | $V_{IN}$ = 0 V | 40 | 100 | 200 | µA |
| $\|I_{IN}\|$ | Leakage current | $V_{IN}$ = 0 or $V_{IN}$ = $V_{DDSHV}$ | | | 5 | µA |
| **DAC INTERFACE (DAC P/N[15:0])** | | | | | | |
| $V_{O(diff)}$ | Output differential swing, $\| V_{O(diff)} \| = \| V_{OH} - V_{OL} \|$ | (1) | 250 | | | mV |
| $V_{(COMM)}$ | Common mode voltage, $(V_{OH} + V_{OL})/2$ | (1) | 1000 | | | mV |
| **LVDS INTERFACE (FB[35:0], DPDCLK/C, SYNCD/C)** | | | | | | |
| $V_i$ | Input voltage range | | 0 | | 2000 | mV |
| $V_{i(diff)}$ | Input differential voltage, \|Vpos – Vneg\| | 0 < $V_i$ < 2000 mV | 250 | | | mV |
| | | 1000 mV < $V_i$ < 1400 mV, FB[35:0] only | 90 | | | |
| $R_{IN}$ | Input differential impedance | | 80 | | 120 | Ω |
| **POWER SUPPLY** | | | | | | |
| Idyn | Core current | See (2) | | | 2.2 | A |

(1) HSTL output levels are measured at 675 Mb/s delay and with 100-Ω load from P to N. Drive strength set to 0x360. Contact TI for operations above 675 Mb/s.
(2) Operating at 280 MHz core, 840 TX port, maximum filtering, nominal supplies

## GENERAL SWITCHING CHARACTERISTICS

Describes the electrical characteristics for the baseband interface, MFIO, Fast Sync, and MPU interfaces over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| **BASEBAND INTERFACE** | | | | | |
| $f_{CLK(BB)}$ | Baseband input clock frequency | | 25 | 140 | MHz |
| $t_{su(BB)}$ | Input data setup time before BBCLK↑ | BB[15:0], BBFR, SYNCA, SYNCB, and SYNCC; MFIO18/19 | 1.3 | | ns |
| $t_{h(BB)}$ | Input data hold time after BBCLK↑ | BB[15:0], BBFR, SYNCA, SYNCB, and SYNCC; MFIO18/19 | 1.5 | | ns |
| $t_{h(SYNCA, -B, -C)}$ | Input data hold time after BBCLK↑ | Valid for SYNCA, SYNCB, and SYNCC | 2 | | ns |
| $Duty_{CLK(BB)}$ | Duty cycle | | 30% | 70% | |
| $t_{jCLK(BB)}$ | Baseband input clock cycle-to-cycle jitter(1) | | –2.5% | 2.5% | |

(1) Percent of baseband PLL clock period. The baseband PLL clock is typically 2×–4× the baseband clock frequency.

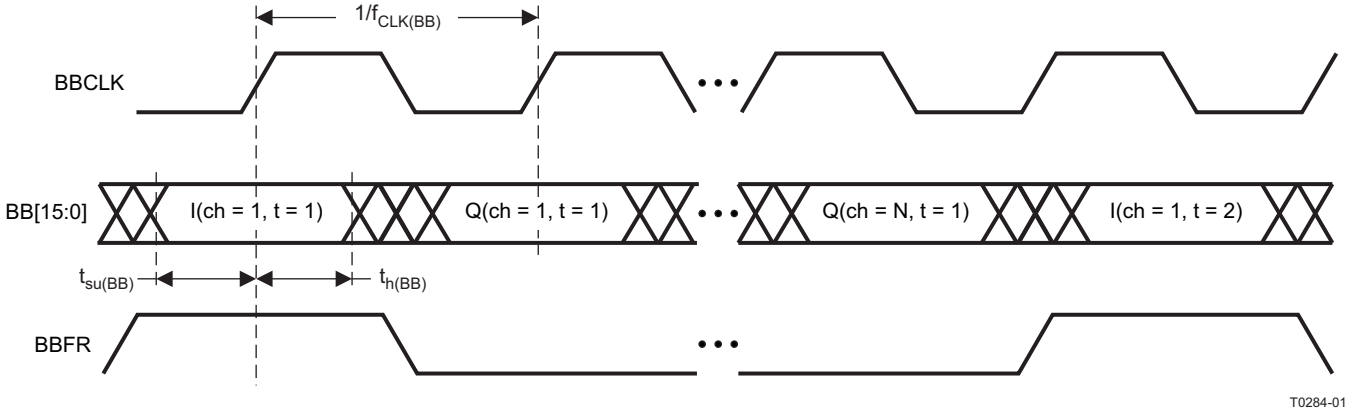



**Figure 4. Baseband Timing Specifications (ex. Four Interleaved I/Q Channels)**

## Table 12. DPD CLOCK AND FAST SYNC SWITCHING CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{CLK(DPD)}$ | DPD input clock frequency | | 100 | 280 | MHz |
| $Duty_{CLK(DPD)}$ | DPD input clock duty cycle | | 30% | 70% | |
| $t_{h(SYNCD)}$ | Input hold time after DPDCLK↑ | See (1) | 0.2 | | ns |
| $t_{su(SYNCD)}$ | Input setup time after DPDCLK↑ | See (1) | 0.4 | | ns |
| $t_{h(SYNCA, -B, -C)}$ | Input hold time after DPDCLK↑ | | 2 | | ns |
| $t_{su(SYNCA, -B, -C)}$ | Input setup time after DPDCLK↑ | | 0.4 | | ns |
| $t_{jCLK(DPD)}$ | DPD clock cycle-to-cycle jitter | | –2.5% | 2.5% | |

(1) SYNCD is the preferred sync for DPD clock and clock domain.

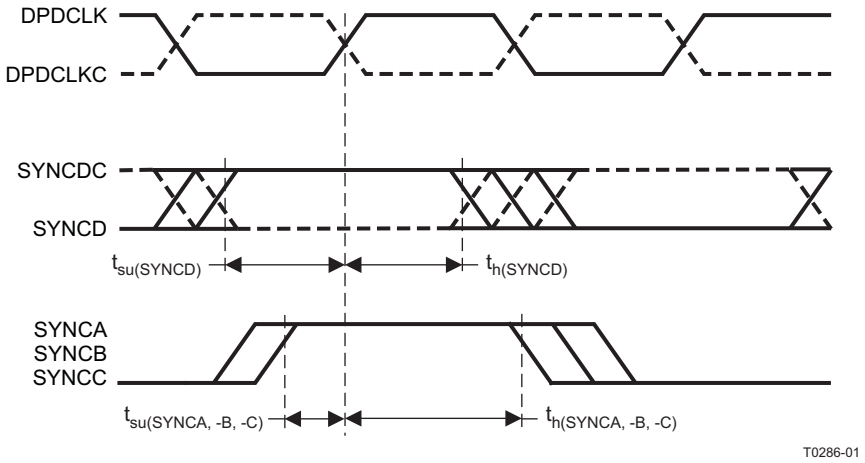



**Figure 5. DPD Clock and Fast Sync Timing Specifications**

## MPU SWITCHING CHARACTERISTICS (READ)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su(AD)}$ | ADDR setup time to RDB↓ | WRB is HIGH. | 5 | | ns |
| $t_{su(CEB)}$ | CEB setup time to RDB↓ | WRB is HIGH. | 7 | | ns |
| $t_{su(OEB)}$ | OEB setup time to RDB↓ | WRB is HIGH. | 2 | | ns |
| $t_{d(RD)}$ | DATA valid time after RDB↓ | WRB is HIGH. | | 14 | ns |
| $t_{h(RD)}$ | ADDR hold time to RDB↑ | WRB is HIGH. | 2 | | ns |
| | OEB, CEB hold time to RDB↑ | | 0 | | |
| | OEB hold time to RDB↑ | | 2 | | |
| $t_{HIGH(RD)}$ | Time RDB must remain HIGH between READs. | WRB is HIGH(1). | 7 | | ns |
| $t_{Z(RD)}$ | DATA goes high-impedance after OEB↑ or RDB↑. | WRB is HIGH(1). | | 7 | ns |

(1) Controlled by design and process and not directly tested

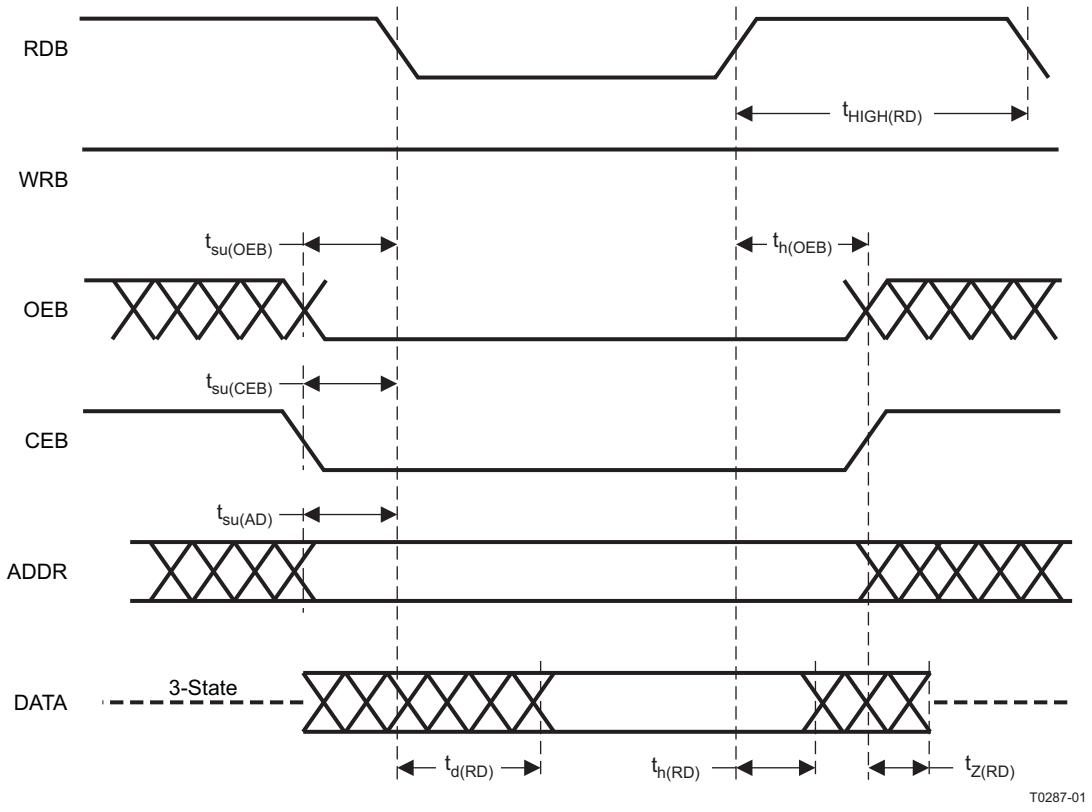



**Figure 6. MPU READ Timing Specifications**

## MPU SWITCHING CHARACTERISTICS (WRITE)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{su(WR)}$ | DATA and ADDR setup time to WRB↓ | OEB and RDB are HIGH. | 5 | | ns |
| | CEB setup time to WRB↓ | | 7 | | |
| | OEB setup time to WRB↓ | | 2 | | |
| $t_{h(WR)}$ | DATA and ADDR hold time after WRB↑ | OEB and RDB are HIGH. | 2 | | ns |
| | OEB and CEB hold time after WRB↑ | | 0 | | |
| $t_{low(WR)}$ | Time WRB and CEB must remain simultaneously LOW | OEB and RDB are HIGH. | 15 | | ns |
| $t_{high(WR)}$ | Time CEB or WRB must remain HIGH between WRITEs. | OEB and RDB are HIGH. | 10 | | ns |

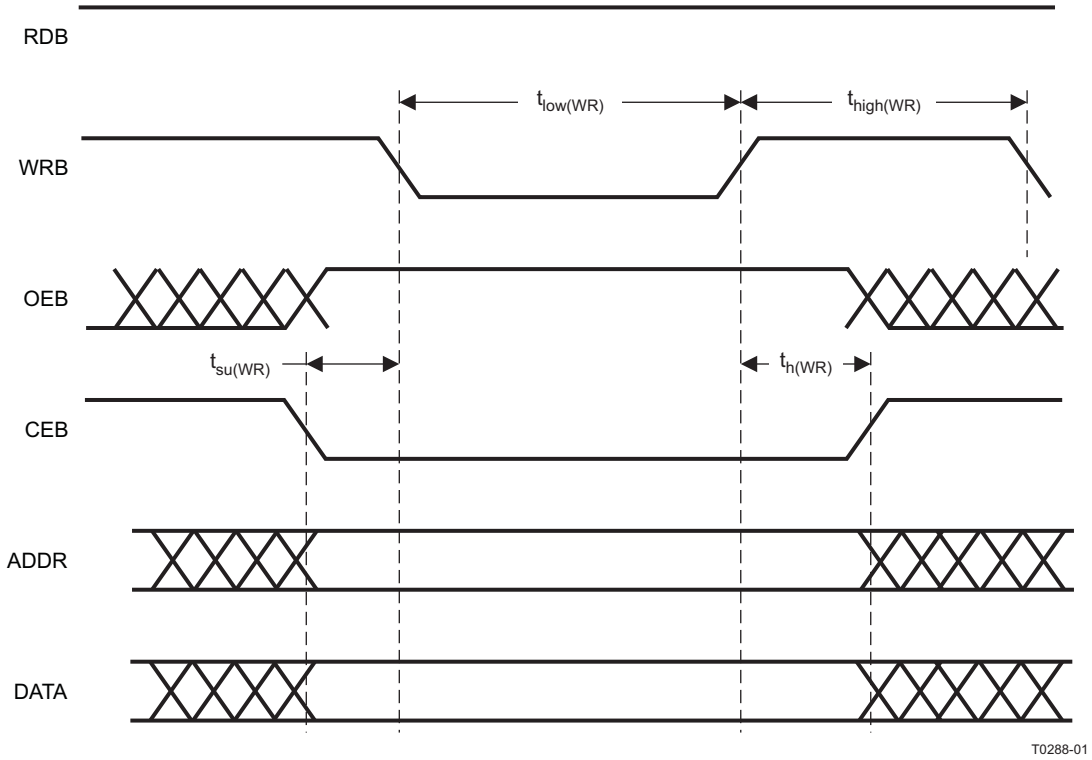



**Figure 7. MPU WRITE Timing Specifications**

## JTAG SWITCHING CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{TCK}$ | JTAG clock frequency | | | 50 | MHz |
| $t_{p(TCKL)}$ | JTAG clock low period | | 10 | | ns |
| $t_{p(TCKH)}$ | JTAG clock high period | | 10 | | ns |
| $t_{su(TDI)}$ | Input data setup time before TCK↑ | Valid for TDI and TMS | 1 | | ns |
| $t_{h(TDI)}$ | Input data hold time after TCK↑ | Valid for TDI and TMS | 6 | | ns |
| $t_{d(TDO)}$ | Output data delay from TCK↓ | | | 8 | ns |

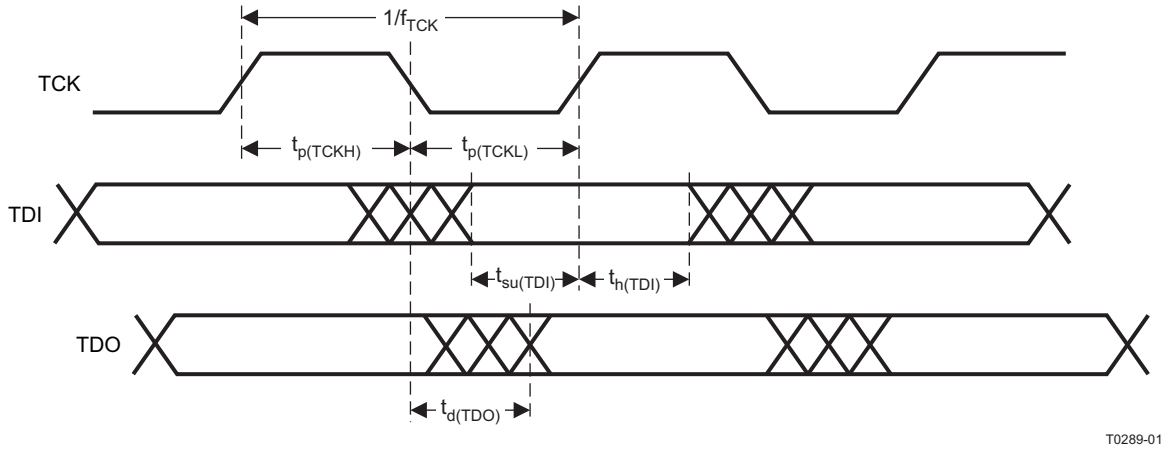



**Figure 8. JTAG Timing Specifications**

## ELECTRICAL CHARACTERISTICS

## TX SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **HSTL MODE – DDR ex. DAC5682** | | | | | | |
| $f_{CLK(DAC)}$ | DAC output clock frequency | $R_L$ = 100 Ω (1) | | | 420 | MHz |

(1) Because the output clock is DDR, this represents 840 MSPS real or 420 MSPS complex.

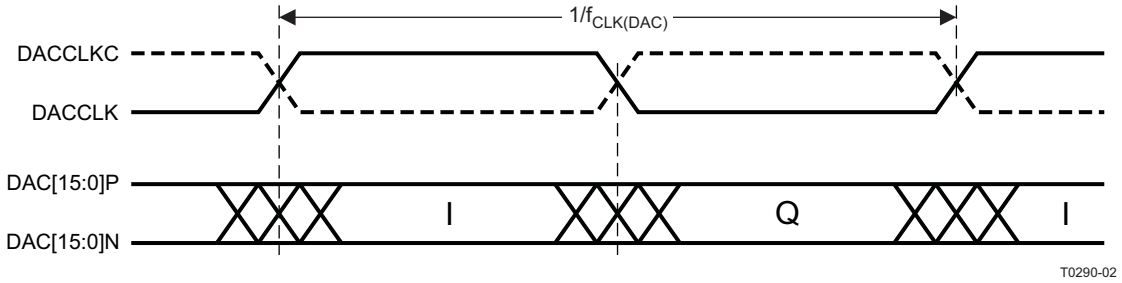



**Figure 9. TX Timing Specifications (HSTL – DDR)**

## LVDS SWITCHING CHARACTERISTICS

Over recommended operating conditions (unless otherwise noted). The following table uses a shorthand nomenclature, NxM. N means the number of differential pairs used to transmit data from one ADC and M means the number of bits sent serially down each LVDS pair. Thus, 8x2 means 8 LVDS pairs each containing 2 bits of information sent serially.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **16x1 SDR LVDS MODE ex. ADS5444** | | | | | | |
| $f_{CLK(ADC)}$ | ADC interface clock frequency | See (1) | | | 280 | MHz |
| $t_{su(ADC[\#]P)}$ | Input data setup time before CLK↑ | See (1) (2) | 300 | | | ps |
| $t_{h(ADC[\#]P)}$ | Input data hold time after CLK↑ | See (1) (2) | 600 | | | ps |
| **16x1 DDR LVDS MODE ex. ADS5463** | | | | | | |
| $f_{CLK(ADC)}$ | ADC interface clock frequency | See (1) | | | 140 | MHz |
| $t_{su(ADC[\#]P)}$ | Input data setup time before CLK↑↓ | See (1) (2) | 100 | | | ps |
| $t_{h(ADC[\#]P)}$ | Input data hold time after CLK↑↓ | See (1) (2) | 1200 | | | ps |
| **8x2 DDR LVDS MODE ex. ADS5545** | | | | | | |
| $f_{CLK(ADCA)}$ | ADCA interface clock frequency | See (1) | | | 280 | MHz |
| $t_{su(ADCA[\#/2]P)}$ | Input data setup time before CLK↑↓ | See (1) (3). For port A | 430 | | | ps |
| $t_{h(ADCA[\#/2]P)}$ | Input data hold time after CLK↑↓ | See (1) (3). For port A | 260 | | | ps |
| $f_{CLK(ADCB)}$ | ADCB interface clock frequency | See (1) | | | 280 | MHz |
| $t_{su(ADCB[\#/2]P)}$ | Input data setup time before CLK↑↓ | See (1) (4). For port B | 800 | | | ps |
| $t_{h(ADCB[\#/2]P)}$ | Input data hold time after CLK↑↓ | See (1) (4). For port B | 400 | | | ps |

(1) Specifications are limited by GC5325 performance and may exceed the example ADC capabilities for the given interface.
(2) Setup and hold measured for ADC[15:0]P, ADC[15:0]N valid for ($V_{OD}$ > 250 mV) to/from ADCCLK and ADCCLKC clock crossing ($V_{OD}$ = 0).
(3) Setup and hold measured for ADCA[7:0]P, ADCA[7:0]N valid for ($V_{OD}$ > 250 mV) to/from ADCACLK and ADCACLKC clock crossing ($V_{OD}$ = 0).
(4) Setup and hold measured for ADCB[7:0]P, ADCB[7:0]N valid for ($V_{OD}$ > 250 mV) to/from ADCBCLK and ADCBCLKC clock crossing ($V_{OD}$ = 0).

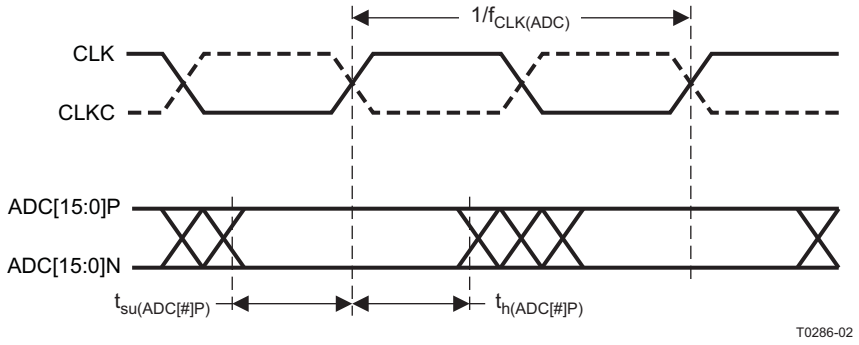



**Figure 10. LVDS Timing Specifications (16 × 1 SDR LVDS)**

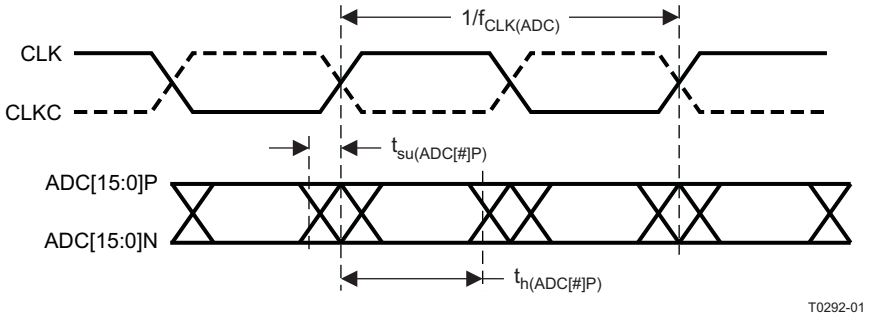



**Figure 11. LVDS Timing Specifications (16 × 1 DDR LVDS)**

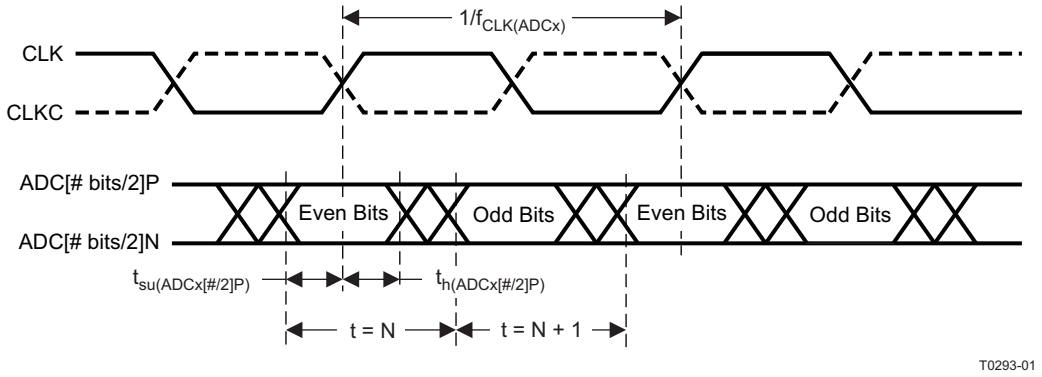
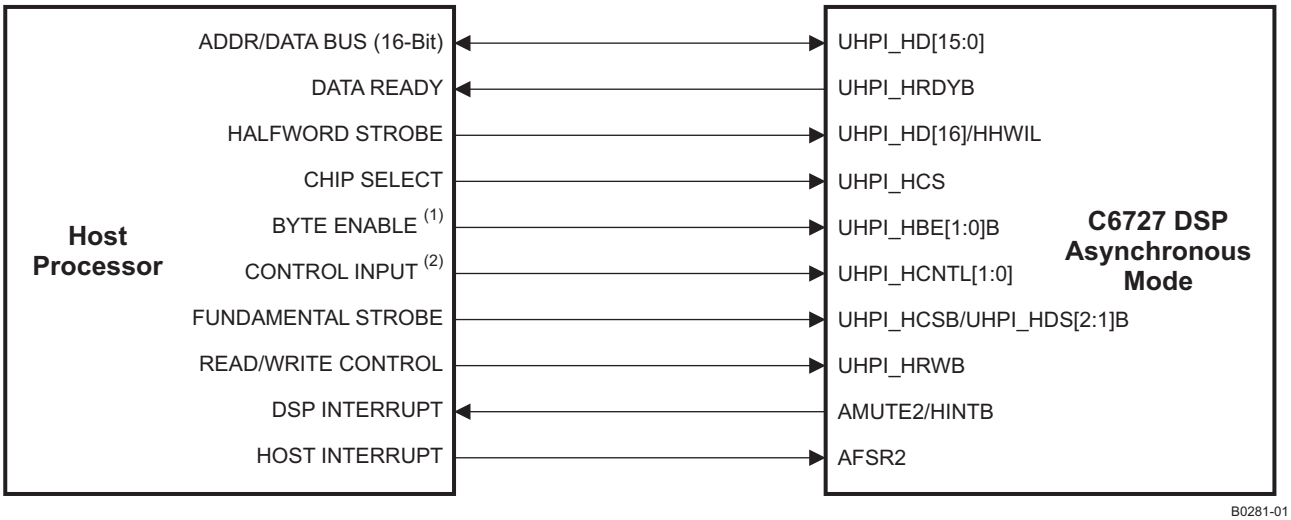



**Figure 12. LVDS Timing Specifications (8 × 2 DDR LVDS)**

## APPENDIX A

See the *TMS320C672x DSP Universal Host Port Interface (UHPI)* reference guide (SPRU719).




(1) Byte enables are aplicable to single HPID accesses. All byte enables must be active during HPID with post-increment (burst) UHPI accesses.

(2) Control inputs selecting between HPIA, HPIC, HPID, and HPID with post-increment accesses.

**Figure 13. Host-to-DSP Interface (Multiplexed Host Address/Data Dual Halfword)**

## GLOSSARY OF TERMS

| | |
|---|---|
| 3G | Third generation (refers to next-generation wideband cellular systems that use CDMA) |
| 3GPP | Third generation partnership project (W-CDMA specification, www.3gpp.org) |
| 3GPP2 | Third generation partnership project 2 (cdma2000 specification, www.3gpp2.org) |
| ACLR | Adjacent channel leakage ratio (measure of out-of-band energy from one CDMA carrier) |
| ACPR | Adjacent channel power ratio |
| ADC | Analog-to-digital converter |
| BW | Bandwidth |

| | |
|---|---|
| CCDF | Complementary cumulative distribution function |
| CDMA | Code division multiple access (spread spectrum) |
| CEVM | Composite error vector magnitude |
| CFR | Crest factor reduction |
| CMOS | Complementary metal oxide semiconductor |
| DAC | Digital-to-analog converter |
| dB | Decibels |
| dBm | Decibels relative to 1 mW (30 dBm = 1 W) |
| DDR | Dual data rate (ADC output format) |
| DSP | Digital signal processing or digital signal processor |
| EVM | Error vector magnitude |
| FIR | Finite impulse response (type of digital filter) |
| I/Q | In-phase and quadrature (signal representation) |
| IF | Intermediate frequency |
| IIR | Infinite impulse response (type of digital filter) |
| JTAG | Joint Test Action Group (chip debug and test standard 1149.1) |
| LO | Local oscillator |
| LSB | Least-significant bit |
| Mb | Megabits (divide by 8 for megabytes MB) |
| MSB | Most-significant bit |
| MSPS | Megasamples per second ($1\times10^6$ samples/s) |
| PA | Power amplifier |
| PAR | Peak-to-average ratio |
| PCDE | Peak code domain error |
| PDC | Peak detection and cancellation (stage) |
| PDF | Probability density function |
| RF | Radio frequency |
| RMS | Root mean square (method to quantify error) |
| SDR | Single data rate (ADC output format) |
| SEM | Spectrum emission mask |
| SNR | Signal-to-noise ratio (usually measured in dB or dBm) |
| UMTS | Universal mobile telephone service |
| W-CDMA | Wideband code division multiple access (synonymous with 3GPP) |
| WiBRO | Wireless broadband (Korean initiative IEEE 802.16e) |
| WiMAX | Worldwide Interoperability of Microwave Access (IEEE 802.16e) |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| GC5325IZND | LIFEBUY | BGA | ZND | 352 | 40 | Pb-Free (RoHS) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | GC5325IZND | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

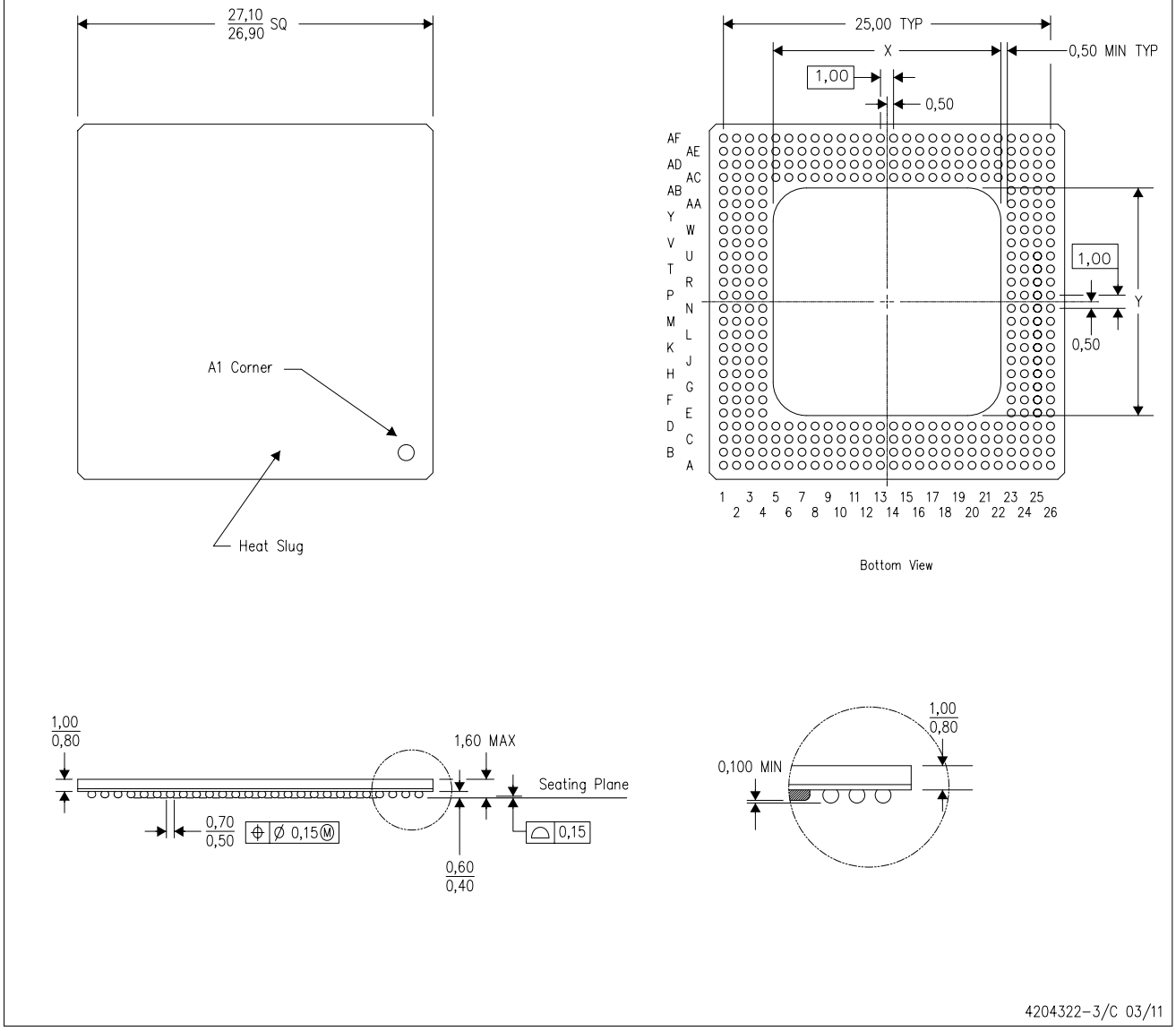
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ZND (S–PBGA–N352) PLASTIC BALL GRID ARRAY (CAVITY DOWN)




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Thermally enhanced plastic package with heat slug (HSL).
D. The encapsulation size (X,Y) will vary with cavity size. The distance from bond finger edge to encapsulation shall be min 0.5mm
E. This is a Pb–free solder ball design.

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