1/13’’ QVGA CMOS Image Sensor

GC6103

DataSheet
V1.0

2011-03-28

GalaxyCore Inc.

Content

1. Sensor Overview

1.1 General Description

GC6103 is GalaxyCore's lastest low cost QVGA sensor, it can work with GC6113 and provide the customer very low cost dual camera solution.

1.2 Features

- Standard optical format of 1/13 inch
- Output format: Raw Bayer
- Support Windowing
- Horizontal /Vertical mirror
- Package type: CSP
- GC SPI interface support

1.3 Technical Specifications

Parameter	Typical value
Optical Format	1/13 inch
Pixel Size	3.23um x 3.23um
Active pixel array	248 x328
Max Frame rate	30fps@24MHz,QVGA
Power Supply	AVDD28 : 2.8V IOVDD : 1.7~3.0V
Power Consumption	30mW
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃

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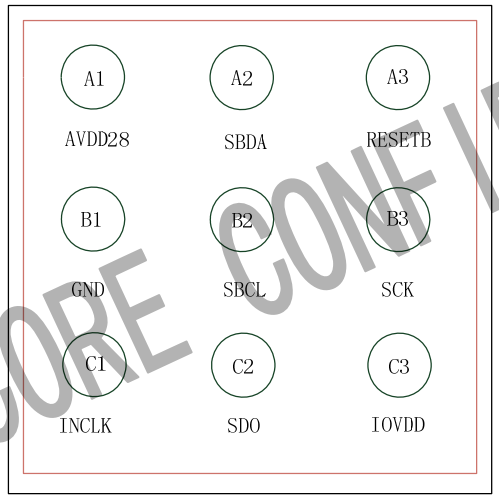
Optical lens chief ray angle(CRA)	23 degree(linear)
Package type	CSP

1.4 Signal descriptions

Pin	Name	Pin Type	Description
A1	**AVDD28**	POWER	Power for analog circuit/sensor array
A2	**SBDA**	I/O	SCCB data
A3	**RESETB**	Input	reset (active high)
B1	**GND**	Power	Ground for analog
B2	**SBCL**	Input	SCCB input clock
B3	**SCK**	Output	SPI master SCK，or SPI slave mode SCK
C1	**INCLK**	Input	System master clock
C2	**SDO**	Output	SPI data output
C3	**IOVDD**	Power	Power Supply for I/O circuits，1.7~3.0V

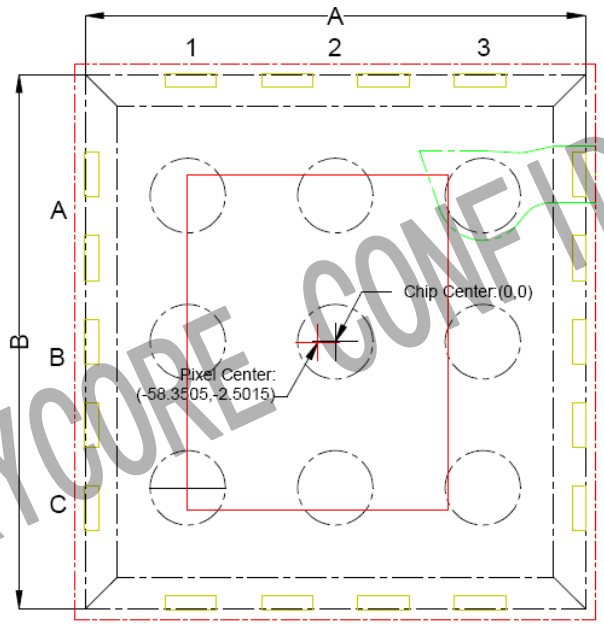
1.5 Pin Diagram



Top view

2. Optical specifications

2.1 Sensor array center



Top View

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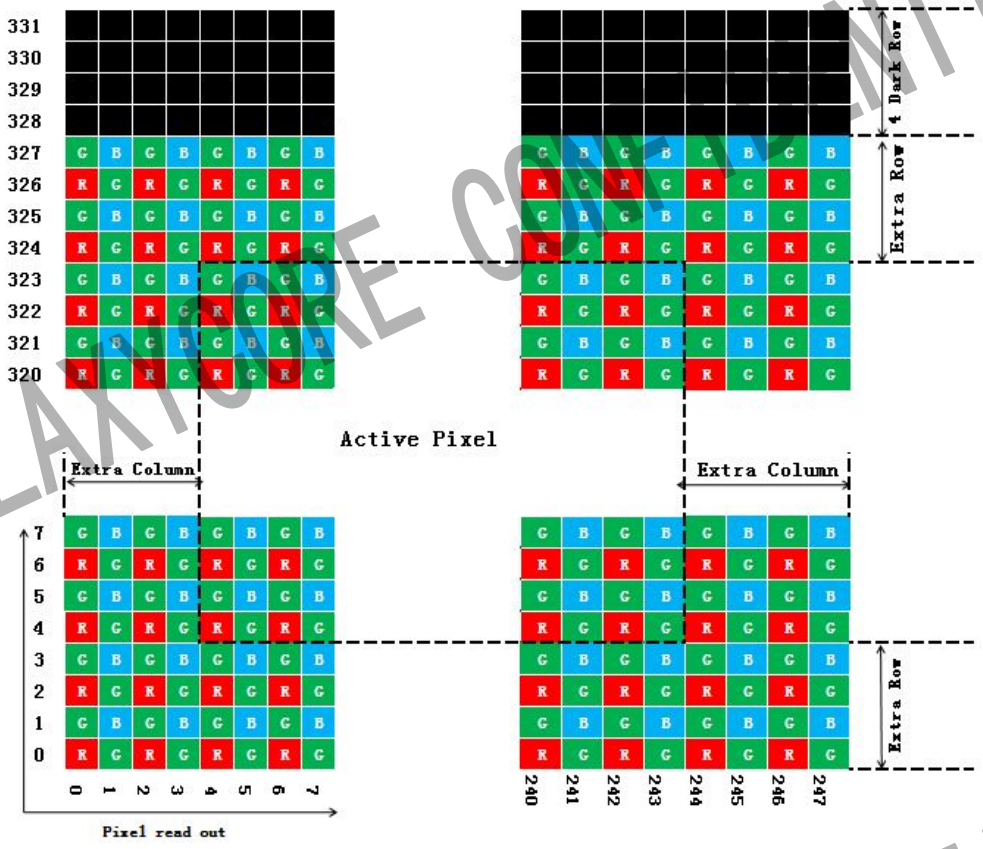
2.2 Pixel Array Structure



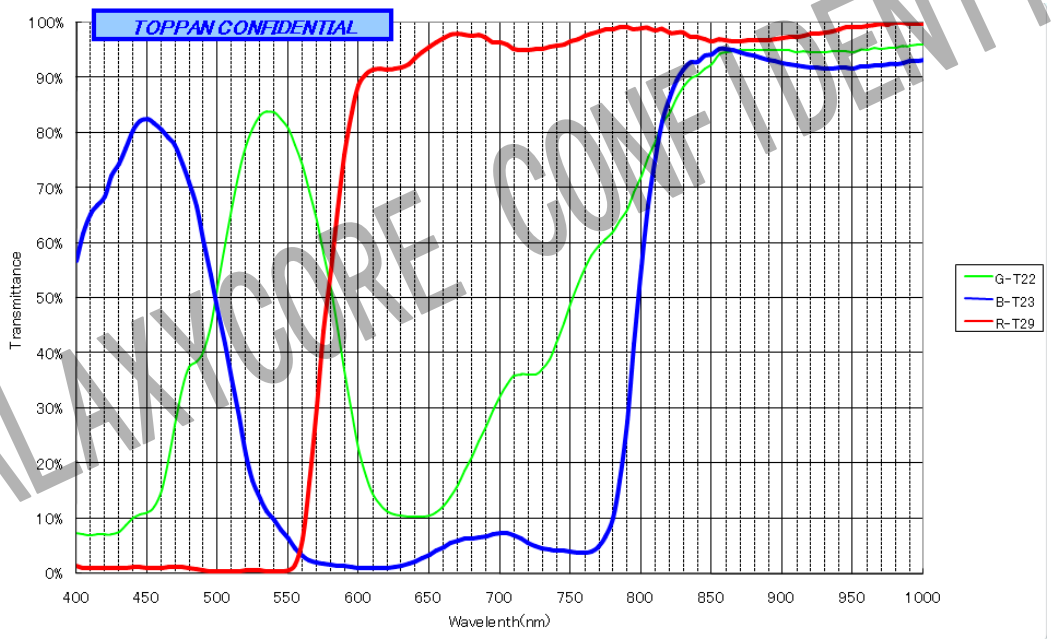
Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 247. If flip in column, column is read out from 247 to 0.

If no flip in row, row is read out from 0 to 327. If flip in row, row is read out from 327 to 0.

2.3 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



3. Two-wire Serial Bus Communication

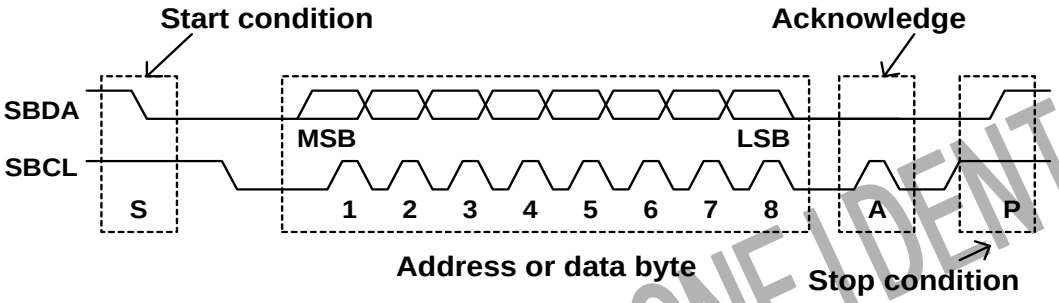
GC6103 Device Address:

Serial bus write address = 0x42, serial bus read address = 0x43

3.1 Protocol

The host must perform the role of a communications master and GC6103 acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	A	P

Incremental Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data(1)	A	……	Data(N)	A	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

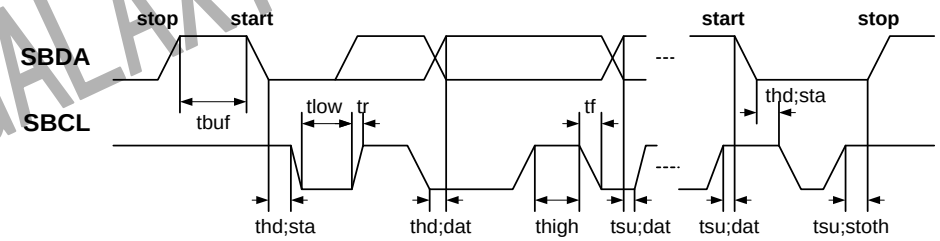
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor registers value

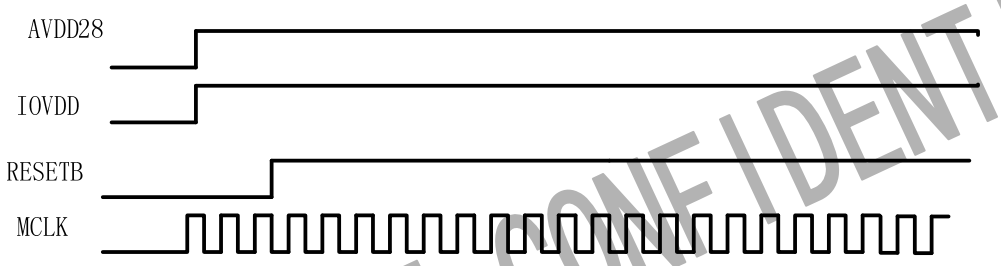
3.2 Serial Bus Timing



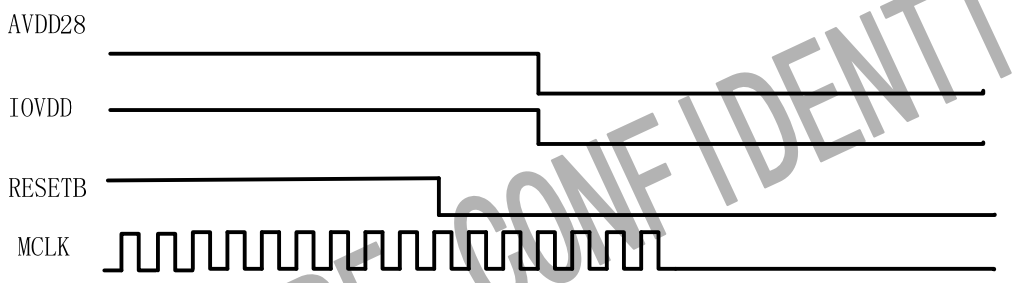
Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	µs
Hold time for a repeated start	thd;sta	1.0	*	µs
LOW period of SBCL	tlow	1.2	*	µs
HIGH period of SBCL	thigh	1.0	*	µs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns
Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	µs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

3.3 Power on/off sequence

3.3.1 Power On Sequence



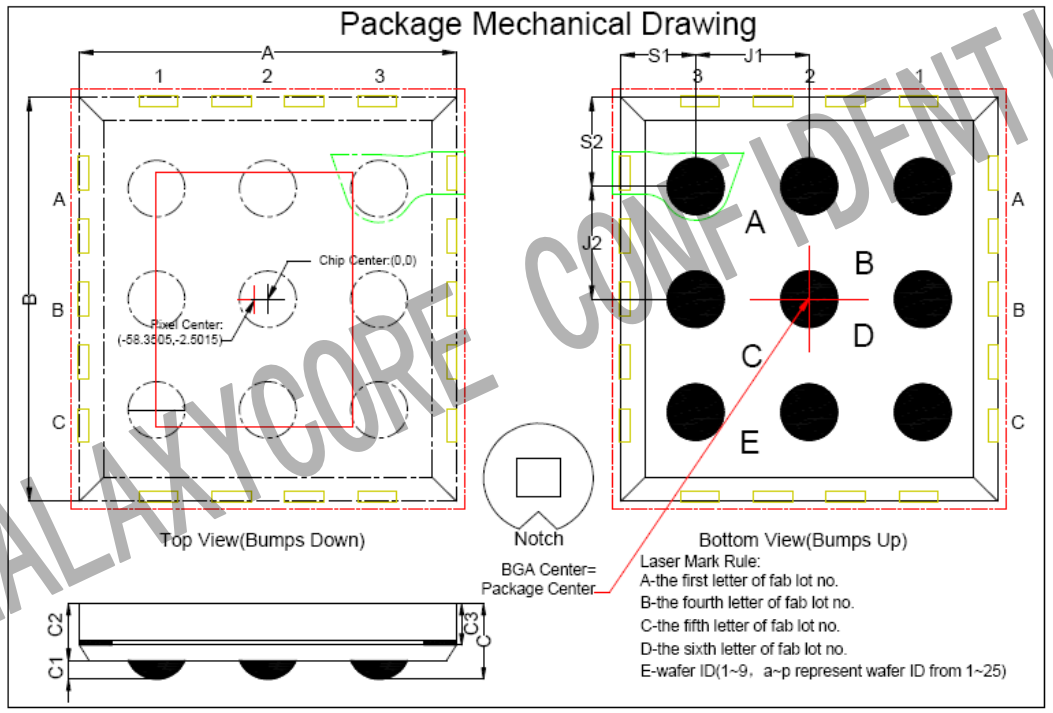
3.3.2 Power Off Sequence



3.4 DC characteristics (-20 ^{O}C < T_A <70^{O}C)

Symbol		Parameter	Min	Typ	Max	Unit
Supply						
V_{AVDD28}		Power supply	2.7	2.8	3.0	V
V_{IOVDD}		Supply voltage(digital I/O)	1.7	2.8	3.0	V
I_{AVDD28}		Active(operating) current		8	10	mA
I_{IOVDD}	1.8V			3	5	mA
	2.8V			2.5	5	mA
I_{DDS_PWD}		Standby Current	10	20	40	uA
Digital Input(Typical conditions: AVDD28 = 2.8V,IOVDD = 2.8V)						
V_{IH}		Input voltage HIGH	1.4			V
V_{IL}		Input voltage LOW			1.6	V
Digital Output(AVDD28 = 2.8V,standard Loading 25PF ,IOVDD = 1.8V)						
V_{OH}		Output voltage HIGH	1.6			V
V_{OL}		Output voltage LOW			0.2	V

4. Package specifications



Package dimensions

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	1.660	1.635	1.685
Package Body Dimension Y	B	1.790	1.765	1.815
Package Height	C	0.745	0.685	0.805
Ball Height	C1	0.130	0.100	0.160
Package Body Thickness	C2	0.615	0.580	0.650
Thickness from top glass surface to wafer	C3	0.435	0.415	0.455
Ball Diameter	D	0.250	0.220	0.280
Total Ball Count	N	9		
Ball Count X axis	N1	3		
Ball Count Y axis	N2	3		
Pins Pitch X axis	J1	0.500		
Pins Pitch Y axis	J2	0.500		
Edge to Pin Center Distance along X	S1	0.330	0.300	0.360
Edge to Pin Center Distance along Y	S2	0.395	0.365	0.425

5. Register List

5.1 System Register

Address	Name	Width	Default Value	R/W	Description
0xf8	Pad_updn	5	0x00	RW	[4]pwd_dnb 0: power down, sensor power down pin control. 1: normal work [3:2] SCK output updn 00: no pull up 01: pull down 10: pull up 11: illegal [1:0] SDO output updn 00: no pull up 01: pull down 10: pull up 11: illegal
0xf9	Output_en	2	0x00	RW	[1] SCK output enable [0] SDO output enable
0xfa	Clk_div_mode	8	0x00	RW	[6:4] represent the frequency division number (1/(N+1)). [2:0] represent the high level in one pulse after frequency division.
0xfb	I2c_device_id	8	0x00	RO	[7:1]i2c_device_id，only can write once [0]NA
0xfc	Clk_enabel Analog_pwd	6	0x00	RW	[7:5]NA [4] Digital clock enable [3:2]NA [1] DAC18 enable [0] analog power down
0xfe	Soft_reset	8	0x00	RW	[7]soft reset enable [6]NA [5]SPI soft reset [4]CISCTL reset enable [3:0]NA

5.2 Analog Register

Pin	Name	Width	Default Value	R/W	Description
P0:0x00	**Chip_ID**	**8**	**0xB0**	**RO**	**Chip version ID**
P0:0x01	Hb[8:0]	8	0x1a	RW	Horizontal blanking, unit pixel clock
P0:0x02	Vb[8:0]	8	0x2f	RW	Vertical blanking, if current exposure < (Vb + window Height) , frame rate will be (Vb + window Height); otherwise frame rate will be determined by exposure
P0:0x03	Exposure Time High Bit	4	0x00	RW	[7:4] NA [3:0] exposure[11:8]，use line processing time as the unit.
P0:0x04	Exposure Time Low Bit	8	0x06	RW	Exposure[7:0], controlled by AEC, if AEC is in on ,Exposure time is controlled by AEC, Read Only ; if AEC is off , you can change it ,
P0:0x05	Row start High bit	1	0x00	RW	Defines the starting row of the pixel array, Bit[0]
P0:0x06	Row start Low Bit	8	0x00	RW	starting row of the pixel array, Bit[7:0]
P0:0x07	Column start High Bit	2	0x00	RW	Defines the starting column of the pixel array, bit[9:8]
P0:0x08	Column start Low Bit	8	0x02	RW	starting column of the pixel array, bit[7:0]
P0:0x09	Window Height High Bit	1	0x01	RW	Defines image height, bit[8]
P0:0x0a	Window Height Low Bit	8	0x48	RW	image height, bit[7:0]
P0:0x0b	Window width High Bit	2	0x00	RW	Defines image width , bit[9:8]
P0:0x0c	Window width Low Bit	8	0xf8	RW	image width, bit[7:0]
P0:0x0d	vs_st	8	0x02	RW	[7:0] number of Row time from frame start to first HSYNC valid
P0:0x0e	vs_et	8	0x08	RW	[7:0] number of Row time from last HSYNC valid to frame end Notice the relation with VB, VB > vs_st+vs_et
P0:0x0f	Vb[11:8] Hb[11:8]	8	0x05	RW	[7:4] Vb high 4 bits [3:0] Hb high 4 bits
P0:0x10	Rsh_width	8	0x22	RW	[7:4] restg_width，X2,

					[3:0] sh_width，X2,
P0:0x11	Tsp_width	8	0x0d	RW	[7:2] tx_width [1:0] space width x2
P0:0x12	Sh_delay	8	0x2a	RW	Sample-hold delay time after row finish
P0:0x13	Row_tail_width	4	0x00	RW	[7:4] NA [3:0] Row_tail_width, generate more hsync for special application
P0:0x14	CISCTL_Mode1	8	0x10	RW	[7] hsync_always 1: hsync always on 0: hsync output at active output [6] NA [5:4] CFA sequence, determined once color filter is determined [3:2] NA [1] upside down [0] mirror
P0:0x15	CISCTL_mode2	8	0x0a	RW	[7:6] NA [5] Double pixel reset mode. 1: on 0: off [4] Reset off for testing. 1:on 0: off [3:2] sdark_mode 0 0: sdark off 0 1: sdark on each Rows for test 1 0: sdark on 4 dark Rows only on even frame 1 1: sdark on 4 dark Rows on each frame [1] exposure mode 1: new exposure 0: normal /bad frame [0] badframe_en, do NOT output bad frame when exposure mode is 0
P0:0x16	CISCTL_mode3	8	0x06	RW	[7:5] NA [4] capture_ad_data_edge 1: use positive edge to sample data 0: use negative edge to sample data [3:0] Number of A/D pipe stages
P0:0x17	CISCTL_mode4	8	0x00	RW	[7:6] tx_mode 00 normal 10 tx all off 11 tx all on [5] coltest_en

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					[4] ad_test enable [3] ad_off_en [2:0]NA
P0:0x18	Rsgg_rsh2	8	0x00	RW	[7:4] rowsg_gap The gap of twice rowsg. [3:0]shw2_width
P0:0x19	NA				
P0:0x1a	Analog mode 1	8	0x23	RW	[7] rsv1, reserved register #1 [6] rsv0, reserved register #0 [5:3] coln_r:col bias current 3'b111 8.5uA 3'b110 7.5uA 3'b101 6.5uA 3'b100 5.5uA 3'b011 4.5uA 3'b010 3.5uA 3'b001 2.5uA 3'b000 1.5uA [2:1] ref_r :AD input range 2'b11 110uA 2'b10 100uA(default) 2'b01 90uA 2'b00 80uA [0] clk_delay_en 1: delay about 5ns 0: delay about 3.6 ns
P0:0x1b	Analog mode 2	8	0x70	RW	[7:4]NA [3]rowclk_mode: clks used for row read synchronized by in_clk or in_clk_dg 0: In_clk 1: In_clk_dg [2]adclk_mode：clk for AD produced by using in_clk or in_clk_dg to sample DG_pclk_b 0: in_clk 1: in_clk_dg [1:0]comv_r: PGA input vcm 2'b11: 1.04 2'b10: 0.86 2'b01: 0.6 2'b00: 0.6(default)
P0:0x1c	Hrst_rsg_v18	8	0xb1	RW	[7] hrst enable, Pixel hard reset

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	Da_rsg Txhigh_en Da18_r				1: pixel hard reset enable 0: normal pixel reset [6:4] da_rsg: row select gate low output voltage 3'b000 0.175V 3'b001 0.35V 3'b010 0.524V 3.b011 0.7V 3'b100 0.874V（default） 3'b101 1.05V 3'b110 1.23V 3'b111 1.4V [3] tx high enable [2] NA [1:0] da15_r, set internal D15 voltage 11: 1.74V 10: 1.67V 01: 1.54V(default) 00: 1.4
P0:0x1d	Vref_v25	8	0xba	RW	[7] vref_en, use internal reference voltage 1: use internal Vref 0: use external reference voltage supplied via the PAD [6:4] da_vref, set internal reference voltage 000: 3.00V 001: 3.2 V 010: 3.36V 011: 3.52V（default） 100: 3.68V 101: 3.84V 110: 4.00V 111: 4.16V [3:0] NA
P0:0x1e	ADC_r	8	0x11	RW	[7] NA [6:5] opa_r, ADC's bias current 2'b11: 24.5uA 2'b10: 20uA 2'b01: 17uA 2'b00: 12.5uA [4:2] NA [1:0] sref_r AD VCM 2'b00 1.4V

					2’b01 1.3V (Default) 2’b10 1.2V 2’b11 1.1V
P0:0x1f	PAD_drv	8	0x15	RW	[7:6] NA [5:4]sck driver current 2’b00: 4mA 2’b01: 8mA 2’b10: 12mA 2’b11: 16mA [3:2]sdo driver current 2’b00: 4mA 2’b01: 6mA 2’b10: 10mA 2’b11: 12mA [1:0] sda driver current 2’b00: 2mA 2’b01: 4mA 2’b10: 8mA 2’b11: 10mA

5.3 ISP Related

Pin	Name	Width	Default Value	R/W	Description
P0:0x20	Block_enable1	8	0x83	RW	[7] normal data output [6] dark data output valid [5:4] byte select from 10 bit data 00: data bit[6:0] x2 01: data bit[7:0] 10: data bit[8:1] 11: data bit[9:2] [3] data valid bit select 1: select from 0x20[5:4] 0: data bit[9:2] [2] NA [1] Gamma enable [0] Lens-shading correction enable
P0:0x2a	Clock_gating_en	8	0x84	RW	[7] ISP quiet mode，in SH time, clock ISP's AAA clock [6:3]NA [2]Divider clock gate enable [1:0]NA

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P0:0x2d	Debug_mode1	8	0x08	RW	[7:4] NA [3:2] pipe gate mode 00: all the time allow clk to pipeline 01: only no clk in SH quiet time 10: provide pipeline clock during pipeline time 11: provide pipeline clk both on real HSYNC and dummy HSYNC for even power consumption of D18 [1:0] NA
P0:0x2e	Debug_mode2	8	0x10	RW	[5] INBF_en [4] update_gain_mode 1: update gains 0: update exposure [3:2]NA [1] LSC_test_image,test image before SRAM [0] NA

BLK

Pin	Name	Width	Default Value	R/W	Description
P0:0x30	Blk_mode	8	0x27	RW	[7] dark current mode 1: use exp_ rated_ dark_c 0: use measured dark current, should set [1]=1 [6:4] BLK smooth speed [3:2] BLK Row select mode 00: Row 12 01: Row 23 10: Row 34 11: Row 1234 [1] dark current measure enable [0] offset enable
P0:0x31	Blk_limit_value	7	0x40	RW	[7] NA [6:0] Blk value limit
P0:0x32	Global_offset	7	0x00	RW	[7] NA [6:0] X2, global offset value
P0:0x33	Current_R_offset	6	0x25	RO	[7] NA [6:0] Current_R_offset
P0:0x34	Current_G_offse	6	0x24	RO	[7] NA

	t				[6:0] Current_G_offset
P0:0x35	Current_B_offset	6	0x25	RO	[7] NA [6:0] Current_B_offset
P0:0x36	Current_R_dark_current	6	0x1a	RO	[7] NA [6:0] Current_R_dark_current
P0:0x37	Current_G_dark_current	7	0x28	RO	[7] NA [6:0] Current_G_dark_current
P0:0x38	Current_B_dark_current	8	0x2e	RO	[7] NA [6:0] Current_B_dark_current
P0:0x39	Exp_rate_darkc	8	0x04	RW	Low 8 bits of 0.12; 4 means when exp=1024, dark current portion is 4
P0:0x3a	offset_submode, offset_ratio	8	0x20	RW	[7:6] offset sub mode 0 0 channel will be adjusted respectively 0 1 change will be adjusted by the average of 4 channels 1 0 G and RB channels will be adjusted separately 1 1 switch RB and G channels [5:0] offset ratio, 1.5 bits
P0:0x3b	darkc_submode, dark_current_ratio	8	0x10	RW	[7:6] dark current sub mode 0 0 channel will be adjusted respectively 0 1 change will be adjusted by the average of 4 channels 1 0 G and RB channels will be adjusted separately 1 1 switch RB and G channels [5:0] dark current ratio, 1.5 bits
P0:0x3c	Manual_G1_offset	6	0x00	RW	[7:6] NA [5:0] manual_G1_offset , S5, aligned to lower 8 of 11 bits data
P0:0x3d	Manual_R1_offset	6	0x00	RW	[7:6] NA [5:0] manual_R2_offset , S5, aligned to lower 8 of 11 bits data
P0:0x3e	manual_B2_offset	6	0x00	RW	[7:6] NA [5:0] manual_B2_offset , S5, aligned to lower 8 of 11 bits data
P0:0x3f	manual_G2_offset	6	0x00	RW	[7:6] NA [5:0] manual_G2_offset , S5, aligned to lower 8 of 11 bits data

PREGAIN

Pin	Name	Width	Default Value	R/W	Description
P0:0x50	Global_gain	6	0x12	RW	[7:6] NA [5:0] global_gain, 2.4bits, 0x10 is 1.0x
P0:0x51	Auto_pregain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC
P0:0x52	NA				
P0:0x53	Channel_gain_G1	8	0x80	RW	1.7 bits, G1 channel pre gain
P0:0x54	Channel_gain_R	8	0x80	RW	1.7 bits, R channel pre gain
P0:0x55	Channel_gain_B	8	0x80	RW	1.7 bits, B channel pre gain
P0:0x56	Channel_gain_G2	8	0x80	RW	1.7 bits, G2 channel pre gain

SPI module

Pin	Name	Width	Default Value	R/W	Description
P0:0x60	SPI_mode	6	0x06	RW	[7] sck_manual_oen [6] sdo_manual_oen [5] sck_manual_set [4] sdo_manual_set [3] spi_manual_pause [2]reset_line_flag [1]reset_frame_flag [0]spi_enable
P0:0x61	Spi_config	8	0x50	RW	[7] spi_hold, pause as spi_hold_set(0x65) setting [6]FF_FE_valid [5]spi_CPHA [4] mab_first [3:0] sck_freq_div
P0:0x62	Spi_data_width[7:0]	8	0xf8	RW	Image width sent
P0:0x63	Spi_data_width[8]	1	0x00	RW	
P0:0x64	Spi_fifo_wdiv	4	0x01	RW	Must set as clk_div_mode（0xfa） [6:4]×2+1
P0:0x65	Spi_hold_set	8	0x42	RW	[7:4] SPI pause time , x16 [3:0] SPI work time , x16
P0:0x66	Spi_data_change_valid	2	0x03	RW	[1]remove zero [0]remove ff

P0:0x70	Test_config	2	0x00	RW	[1] SRam amend enable [0] SRam test enable
P0:0x71	ram test finish	5	0x00	RO	[7:5]NA [4]sram test finish [3]NA [2:0]error cnt locked
P0:0x72	Error0_addr	8	0xff	RO	
P0:0x73	Error1_addr	8	0xff	RO	
P0:0x74	Error2_addr	8	0xff	RO	
P0:0x75	Error3_addr	8	0xff	RO	

LSC

Pin	Name	Width	Default Value	R/W	Description
P0:0x8b	LSC red b2	8	0x40	RW	Square coefficient for R channel
P0:0x8c	LSC green b2	8	0x40	RW	Square coefficient for G channel
P0:0x8d	LSC blue b2	8	0x40	RW	Square coefficient for B channel
P0:0x8e	LSC red b4	8	0x30	RW	Quadra coefficient for R channel
P0:0x8f	LSC green b4	8	0x30	RW	Quadra coefficient for G channel
P0:0x90	LSC blue b4	8	0x30	RW	Quadra coefficient for B channel
P0:0x91	Signed b4	1	0x00	RW	[0] controls the sign of quadric coefficient, default 0
P0:0x92	LSC row center	8	0x3e	RW	Row center for LSC correction X4
P0:0x93	LSC column center	8	0x52	RW	Column center for LSC correction X4

Gamma

Pin	Name	Width	Default Value	R/W	Description
P0:0x9f	Gamma_out0	8	0x07	RW	Each out value of knee_i. Knee0=0
P0:0xa0	Gamma_out1	8	0x1b	RW	Knee1=8
P0:0xa1	Gamma_out2	8	0x35	RW	Knee2=16
P0:0xa2	Gamma_out3	8	0x4e	RW	Knee3=24
P0:0xa3	Gamma_out4	8	0x67	RW	Knee4=32
P0:0xa4	Gamma_out5	8	0x7e	RW	Knee5=40
P0:0xa5	Gamma_out6	8	0x94	RW	Knee6=48
P0:0xa6	Gamma_out7	8	0xa7	RW	Knee7=64
P0:0xa7	Gamma_out8	8	0xb7	RW	Knee8=80

P0:0xa8	Gamma_out9	8	0xc6	RW	Knee9=96
P0:0xa9	Gamma_out10	8	0xd4	RW	Knee10=112
P0:0xaa	Gamma_out11	8	0xe9	RW	Knee11=128
P0:0xab	Gamma_out12	8	0xff	RW	Knee12=144

Measure Window

Pin	Name	Width	Default Value	R/W	Description
P0:0xC0	Big_win_x0	6	0x04	RW	Measure big window left column number, X4
P0:0xC1	Big_win_y0	6	0x02	RW	Measure big window left row number, X4
P0:0xC2	Big_win_x1	8	0x76	RW	Measure big window right column number, X4
P0:0xC3	Big_win_y1	8	0x4e	RW	Measure big window right row number, X4

AEC

Pin	Name	Width	Default Value	R/W	Description
P0:0xd0	AEC_mode1	8	0x0a	RW	[7] ignore mode [6:5] ignore mode select 00: continues ignore in high and low rang 01: interval ignore in high and low rang 1x: interval 1:2 ignore in high and low rang [4] ignore same pixel THD 0: Same TH is 4 1: same Th is 7 [2] measure point 1: before RGB gamma 0: after Y gamma [1:0]div_sel [1]: Y_average X 4 [0]: Y_average X 2 [1:0] = 2'b00 Y_average
P0:0xd1	AEC_mode2	8	0x00	RW	[7]NA [6:4] AEC take action every N frame [3:2] close frame number to eliminate bad

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					frame [1] change exp_gain_mode: only effect when exp change 2 steps(up or down) [0] dead_zone_mode: 1: AEC stop margin use smaller margin 0: AEC converging mode use two criteria
P0:0xd2	AEC_mode3	8	0x40	RW	[7] AEC_en [6:4] low range , x4 [3:0] high range, x16 + 15
P0:0xd3	AEC_target_Y	8	0x50	RW	expected luminance value
P0:0xd4	Y_average	8	0xac	RO	Y_average
P0:0xdb	AEC_slow_margin AEC_slow_speed	8	0x91	RW	[7:4] AEC slow margin, X4 [3] NA [2:0] AEC slow speed
P0:0xdc	AEC_fast_margin AEC_fast_speed	8	0x96	RW	[7:4] AEC fast margin, X4 [3] NA [2:0] AEC fast speed
P0:0xdd	AEC_exp_change _gain_ratio	8	0x96	RW	Gain change criteria, float 1.7, default use 1.2x
P0:0xde	AEC_step2_sunlight	8	0x02	RW	AEC_step2_sunlight
P0:0xdf	AEC_D_ratio	6	0x03	RW	[7:4] NA [3:0] differential coefficient in AEC control algorithm
P0:0xe0	AEC_I_stop_L_margin	7	0x07	RW	[7] NA [6:0] x2, Will be used as AEC convergence margin when P0:0xd1[0]=0
P0:0xe1	AEC_I_stop_margin AEC_I_ratio	8	0x61	RW	[7:4] AEC adjust stop margin [3:0] integration coefficient
P0:0xe2	Anti_flicker_step [11:8]	4	0x00	RW	[3:0] flicker step
P0:0xe3	Anti_flicker_step [7:0]	8	0x96	RW	
P0:0xe4	exp level_1 high	4	0x01	RW	Exposure level 1
P0:0xe5	exp level_1 low	8	0x2c	RW	
P0:0xe6	exp level_2 high	4	0x02	RW	Exposure level 2
P0:0xe7	exp level_2 low	8	0x58	RW	
P0:0xe8	exp_level_3 high	4	0x03	RW	Exposure level 3

P0:0xe9	exp_level_3 low	8	0x84	RW	
P0:0xea	exp_level_4 high	4	0x05	RW	Exposure level 4
P0:0xeb	exp_level_4 low	8	0xdc	RW	
P0:0xec	Max_exp_level Exp_min_l[11:8]	6	0x20	RW	[7:6] NA [5:4] max exposure levels can be applied by AEC [3:0] minimum exposure level high 4 bits
P0:0xed	Exp_min_l[7:0]	8	0x04	RW	minimum exposure level lower 8 bits
P0:0xef	AEC_max_pre_dg_gain	8	0x00	RW	Digital pre gain limit, float 2.6, X1.5