GC87C510A0-SP8IP
(8-bit Turbo Microcontroller)
Approval Sheet

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Confirmed by CTO, Victor Nam	

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Contents :

1. Product Feature

1.1 Overview

- 8-bit turbo 80C52 architecture (X3)
- 4 clock cycles/1 machine cycle
- Instruction level compatible with Intel 80C52
- 4Kbyte OTP ROM (EPROM)
- 128byte Internal Data RAM
- Supply Voltage: 2.4V ~ 5.5V
- On-chip Oscillator Circuitry Using External Crystal
  - ✓ Max. 20MHz @ 4.5 ~ 5.5V
  - ✓ Max. 10MHz @ 2.4 ~ 3.3V
- Operating Temperature: -20 ℃ ~ 85 ℃
- 6 Programmable I/O pins
- Low Voltage Detector (LVD)
- 16-bit Programmable Watchdog Timer (WDT)
- Two 16-bit Timer/Counters
- Full-Duplex UART
  - ✓ Automatic address recognition
- 1-channel 8-bit High Speed Pulse Width Modulator (PWM)
- 2-channel 10-bit Analog to Digital Converter (ADC)
  - ✓ Max. 100K SPS (samples per second) @ 8MHz
  - ✓ Programmable input clock frequency
- 9 Interrupt Sources including 3 External
  - ✓ Timer 0/1, UART, ADC, PWM, WDT, and four External
  - ✓ Two-level interrupt priority
- Reset scheme
  - ✓ On-chip Rower-On-Reset (POR)
  - ✓ External Reset
  - ✓ Low Voltage Detector Reset
  - ✓ Watchdog Timer Reset
- Power consumption
  - ✓ Active current: Max 10mA @ 5V, 20MHz
  - ✓ Stop current: Max 1uA
- ESD protection up to 2,000V

- Latch-up protection up to ±200mA

1.2 Electrical Spec

Absolute Maximum Ratings

Items	Conditions	Ranges
Voltage on any pin relative to Ground	-	-0.5 V to (V_{DD}+0.5V)
Voltage in V_{DD} relative to Ground	-	-0.5V to 6.5V
Output Voltage	-	-0.5 V to (V_{DD}+0.5V)
Output Current High	One I/O pin active	-25mA
	All I/O pin active	-100mA
Output Current Low	One I/O pin active	+30mA
	All I/O pin active	+150mA
Operating Temperature	-	-40 ^{o}C to 85 ^{o}C
Storage Temperature	-	-65 ^{o}C to +150 ^{o}C
Soldering Temperature	-	160 ^{o}C for 10 seconds

General DC Characteristics

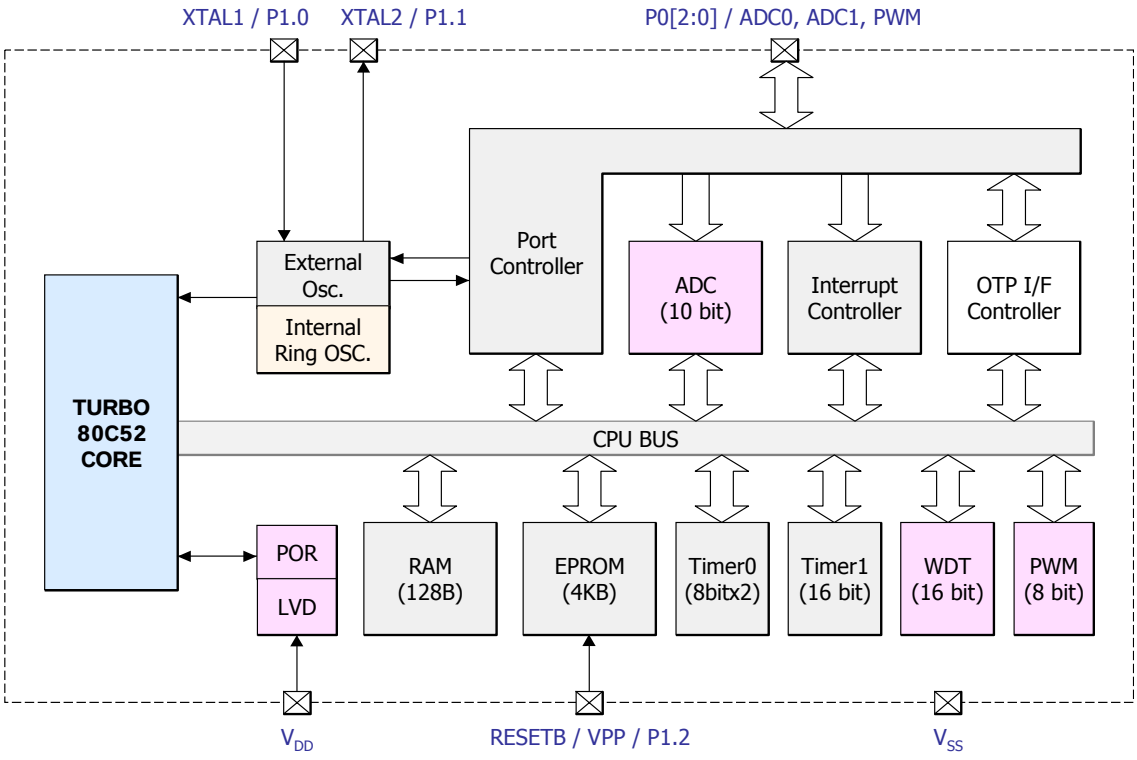
(T_A = -20°C ~ + 85°C, V_{DD}=2.4V ~ 5.5V unless otherwise specified)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min.	Typ.	Max.	
Input Low Voltage	V_{IL1}	P0, P2	V_{DD} = 2.4V ~ 5.5V	-0.5	-	$0.2V_{DD}$-0.1	V
	V_{IL2}	XTAL1, XTAL2, RESETB		-0.5	-	$0.3V_{DD}$	V
Input High Voltage	V_{IH1}	P0, P2	V_{DD} = 2.4V ~ 5.5V	$0.2V_{DD}$+1.0	-	V_{DD}+0.5	V
	V_{IH2}	XTAL1, XTAL2, RESETB		$0.7V_{DD}$	-	V_{DD}+0.5	V
Output Low Voltage	V_{OL1}	XTAL1, XTLA2, P0, P2	I_{OL}=20mA @V_{DD}=5V (I_{OL}=5mA @V_{DD}=2.6V)	-	-	$0.3V_{DD}$	V
	V_{OL2}	RESETB	I_{OL}=10mA @V_{DD}=5V (I_{OL}=2.5mA @V_{DD}=2.6V)	-	-	$0.3V_{DD}$	V
Output High Voltage	V_{OH}	XTAL, XTAL2, P0, P2	I_{OL}=-15mA @V_{DD}=5V (I_{OL}=2.5mA @V_{DD}=2.6V)	$0.7V_{DD}$	-	-	V
	V_{OH1}	P0, P2 (Pull-up R Only)	I_{OL}=-140uA @V_{DD}=5V (I_{OL}=-20uA @V_{DD}=2.6V)	$0.7V_{DD}$	-	-	V
	V_{OH2}	XTAL1, XTAL2 (Pull-up R Only)	I_{OL}=-10uA @V_{DD}=5V (I_{OL}=1.5mA @V_{DD}=2.6V)	$0.7V_{DD}$	-	-	V
Input Leakage Current	I_{IL}	All pins except XTAL1 and XTAL2	V_{IN} = V_{IH} or V_{IL}	-	-	±1.0	uA
Pin Capacitance	C_{IO}	All pins	V_{DD} = 5V	-	10	-	pF

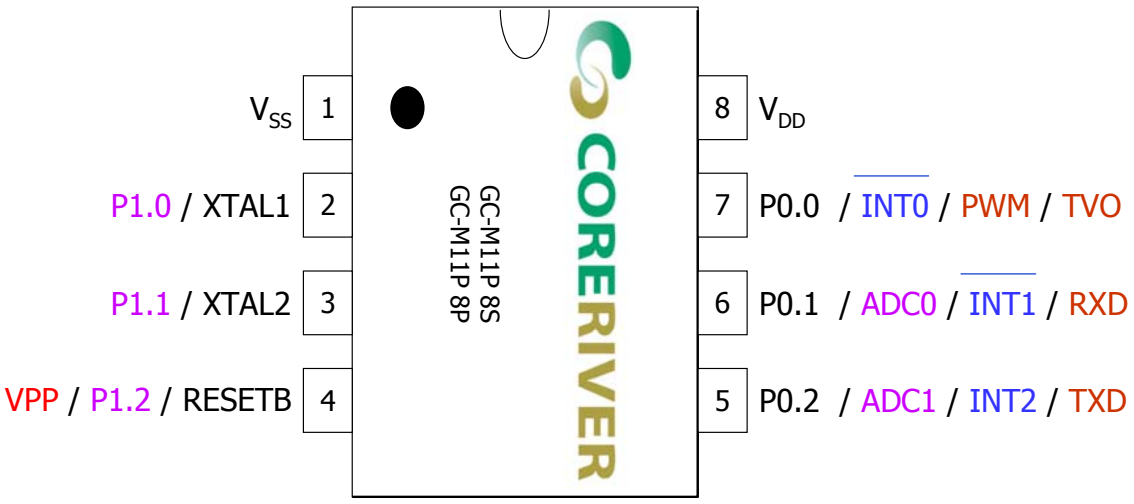
ADC Specifications

Parameter		Symbol	Conditions	Value			Unit
				Min.	Typ.	Max.	
Supply Voltage		V_{DDADC}	-	2.4	-	5.5	V
Input Voltage		V_{INADC}	-	V_{SS}	-	V_{DD}	V
Resolution		RES_{ADC}	-	-	10	-	Bit
Operating Frequency		F_{ADC}	V_{DD} = 4.5V ~ 5.5V V_{DD} = 2.4 ~ 3.3V	-	-	10 5	MHz
Conversion Time		t_{ADC}	-	-	96/F_{ADC}	-	sec
Overall Accuracy		OA_{ADC}	V_{DD} = 5V, F_{ADC} = 10MHz V_{DD} = 3V, F_{ADC} = 5MHz	-	±2.0	±4.0	LSB
Integral Nonlinearity		INL_{ADC}	V_{DD} = 5V, F_{ADC} = 10MHz V_{DD} = 3V, F_{ADC} = 5MHz	-	±2.0	±4.0	LSB
Differential Nonlinearity		DNL_{ADC}	V_{DD} = 5V, F_{ADC} = 10MHz V_{DD} = 3V, F_{ADC} = 5MHz	-	±0.5	±1.0	LSB
Zero Input Error		ZIE_{ADC}	V_{DD} = 5V, F_{ADC} = 10MHz V_{DD} = 3V, F_{ADC} = 5MHz	-	±2.0	±4.0	LSB
Full Scale Error		FSE_{ADC}	V_{DD} = 5V, F_{ADC} = 10MHz V_{DD} = 3V, F_{ADC} = 5MHz	-	±2.0	±4.0	LSB
Analog Input Capacitance		C_{INADC}	-	-	10	15	pF
ADC Current	Active	I_{ADC}	V_{DD} = 5V, F_{ADC} = 10MHz	-	1.0	2.0	mA
			V_{DD} = 3V, F_{ADC} = 5MHz	-	0.3	0.6	mA
	Power-down		V_{DD} = 5V	-	-	100	nA

2. Block Diagram



3. Pin List & Description

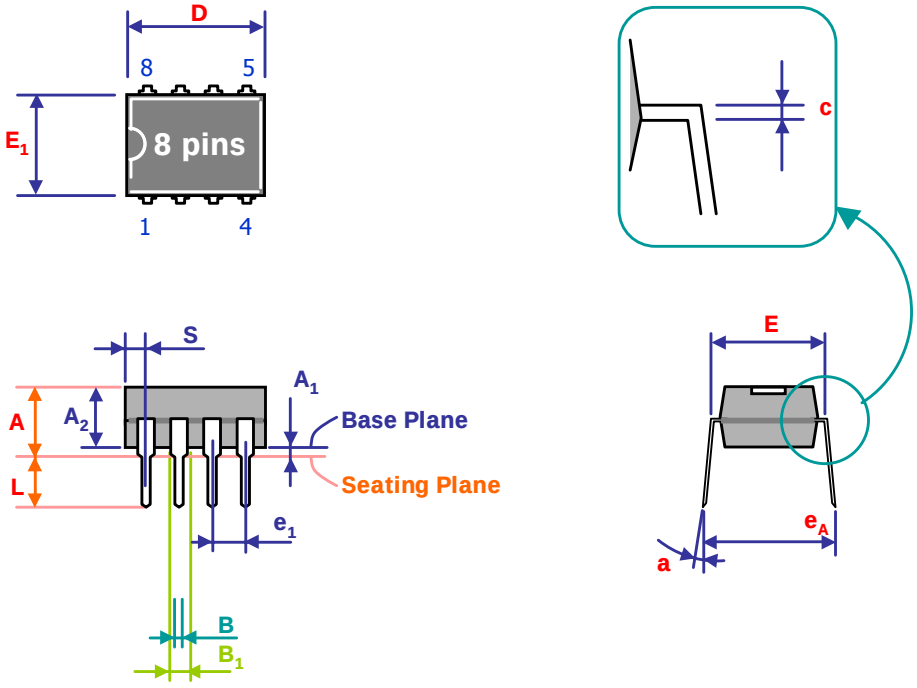


The Pin Configuration of the 8-pin SPDIP Package

Pin Descriptions

Symbol	Direction	Description	Pin Sharing
VDD	Input	Power	
VSS	Input	Ground	
RESETB / VPP / P1.2	Input/Output	◆ External Reset (Default) ◆ Bit Programmable	VPP (11.5V)
XTAL1 / P1.0	Input/Output	◆ Crystal Input/Output (Default) ◆ Bit programmable with Schmitt Trigger - Pull-up control	Crystal Input
XTAL2 / P1.1			Crystal Output
P0.0	Input/Output	◆ Bit Programmable with Schmitt Trigger - Pull-up control - Push-pull output (Default)	/INT0, PWM, TVO
P0.1	Input/Output		ADC0, /INT1, RXD
P0.2	Input/Output		ADC1, INT2, TXD

4. Physical Dimension



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	–	–	0.200	–	–	5.080
A_1	0.015	–	–	0.381	–	–
A_2	0.150	0.155	0.160	3.810	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B_1	0.045	0.055	0.065	1.143	1.397	1.651
c	0.008	0.010	0.012	0.203	0.254	0.356
D	0.445	0.455	0.475	11.303	11.557	12.065
E	0.290	0.300	0.310	7.366	7.62	7.874
E_1	0.249	0.250	0. 251	6.10	6.35	6.60
e_1	0.090	0.100	0.110	2.286	2.540	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0°	–	15°	0°	–	15°
e_A	0.330	0.350	0.370	8.382	8.89	9.398
S	–	–	0.090	–	–	2.286

Notes:

1. Dimension D Max. & S include mold flash or tie bar Burns.
2. Dimension E_1 dose not include interlead flash.
3. Dimension D & E_1 include mold mismatch and are determined at the mold parting line.
4. Dimension B_1 does not include dambar protrusion/intrusion.
5. General appearance spec. should be based on final visual inspection spec.

5. Marking Spec

CORERIVER

1. Purpose

To provide the information of the marking process

2. Scope

GC87C510A0-SP8IP (8 DIP)

3. Explanation

3.1 Marking Method : Laser

3.2 Character Type : Arial

3.3 Marking Size and Instruction

Marking Size		Marking Instruction	
①	1.0 mm	⑧	* Work Week 1) YY: Year (2007->07,2008->08…) 2) WW: Week (01,02,03,…,53)
Line Space	0.5 mm		

3.4 Marking Layout & Area

3.4.1 GC87C510A0-SP8IP

***NOTE : Center alignment

***NOTE : 1's of "GC-M11P" on the first row are numbers.

Reliability Report

GC87C510A0

V 1.0

June 2007

Contents

Confidential

1. Used Process Reliability

◆ Electrical Stress Test Results

Test Items	Conditions	# of Lot	S.S Per Lot	Total Units	#of Fail	Duration	Results
H.T.O.L (High Temperature Operating Life Test)	Ta=145℃, Dynamic V_{DD}=6V	3	77	231	0	1,008 Hrs	PASS
T.H.B (Temp. & Humidity With Bias)	Ta=85℃, R.H=85% Static, V_{CC}=5.5V (*)	3	38	114	0	1,008 Hrs	PASS

✓ Notes

a. No Failures counted for this qualification test.

b. "*": Starting reliability test after preconditioning test according to JEDEC-STD JESD22 A113 Level III.

◆ Environmental Stress Test Results

Test Items	Conditions	#of Lot	S.S Per Lot	Total Units	#of Fail	Duration	LTPD	Result
P.C.T (Pressure Cooker Test)	Ta=121℃,2ATM, R.H=100% (*)	3	32	96	0	200 Hrs	7%	PASS
T.C (Temperature Cycle)	Ta= -65℃/150℃ 15Min/15Min=1Cyc Air to Air (*)	3	77	231	0	1,000 Cycle	5%	PASS
H.T.S.T (High Temperature Storage Test)	Ta=150℃ Storage No Biased	3	22	66	0	1,008 Hrs	10%	PASS

✓ Notes

a. No Failures counted for this qualification test.

b. "*" Starting reliability test after preconditioning test according to JEDEC-STD JESD22A113 Level III.

2. Used Library Reliability

◆ Electrical Stress Test Results

Test Items	Conditions	# of Lot	S.S Per Lot	Total Units	#of Fail	Duration	LTPD	Results
H.T.O.L (High Temperature Operating Life Test)	Ta=145℃,Dynamic V_{DD}=6V	1	77	77	0	504Hrs	5%	PASS

✓ Notes

a. No Failures counted for this qualification test.

◆ Environmental Stress Test Results

Test Items	Conditions	#of Lot	S.S Per Lot	Total Units	#of Fail	Duration	LTPD	Result
T.H.S (temp&Humidity With No Bias)	Ta=85℃,R.H=85% Static(*)	1	38	38	0	504 Hrs	10%	PASS
P.C.T (Pressure Cooker Test)	Ta=121℃,2ATM, R.H=85%(*)	1	32	32	0	200 Hrs	7%	PASS
T.C (Temperature Cycle)	Ta= -65℃/150℃ 15Min/15Min=1 Cycle Air to Air(*)	1	77	77	0	1,000 Cyc	5%	PASS
H.T.S.T (High Temperature Storage Test)	Ta=150℃ Storage No Biased	1	22	22	0	504 Hrs	10%	PASS

✓ Notes

a. No Failures counted for this qualification test.

b. "*" Starting reliability test after preconditioning test according to JEDEC-STD JESD22A113 Level III.

◆ ESD Test Results

Model	Mode	S/S	Spec	Results
HBM	V_{DD},V_{SS},I/O	9	2000V	PASS
MM	V_{DD},V_{SS},I/O	9	200V	PASS
CDM	Socket Mode	3	800V	PASS

◆ Latch- Up Test Results

Mode		Voltage/Current	S/S(EA)	Result
Voltage (E-Mode)	+	10.0(V)	3	PASS
	-	-10.0(V)	3	PASS
Current (I-Mode)	+	250(mA)	3	PASS
	-	-250(mA)	3	PASS
V_{DD}-V_{SS} (Overvoltage)		10.0(V)	3	align

Electrical Stress Test Results

Test Items	Conditions	# of Lot	S.S Per Lot	Total Units	#of Fail	Duration	Results
H.T.O.L (High Temperature Operating Life Test)	Ta=145℃,Dynamic V_{DD}=6v	1	77	77	0	168 Hrs (*)	PASS

✓ Notes

a. No Failures counted for this qualification test.

b. "*" H.T.O.L for product reliability was tested only for 168 hours. It is because 1,008 hour H.T.O.L was tested for the used process reliability. Refer to the used process reliability for 1,008 hour H.T.O.L.

◆ Environmental Stress Test Results

Test Items	Conditions	#of Lot	S.S Per Lot	Total Units	#of Fail	Duration	LTPD	Result
T.H.S (Temp.&Humidity With No Bias)	Ta=85℃,R.H=85% Static(*)	1	38	38	0	504 Hrs	10%	PASS
P.C.T (Pressure Cooker Test)	Ta=121℃,2ATM, R.H=85%(*)	1	32	32	0	200 Hrs	7%	PASS
T.C (Temperature Cycle)	Ta= -65℃/150℃ 15Min/15Min=1Cyc Air to Air(*)	1	77	77	0	1,000 Cycle	5%	PASS
H.T.S.T (High Temperature Storage Test)	Ta=150℃ Storage No Biased	1	22	22	0	504 Hrs	10%	PASS

✓ Note

a. No Failures counted for this qualification test.

b. "*" Starting reliability test after preconditioning test according to JEDEC-STD JESD22A113 Level III.

c. This is the used library reliability information obtained from the GC87C520A0 samples. GC87C520A0 and GC87C510A0 are designed with the same library and fabricated by the same process.

◆ Estimation of Failure Rate from HTOL

✓ FIT CALCULATION

Temperature acceleration for semiconductor failure mechanism is usually described by the Arrhenius equation.

$$\mathbf{AF_T = exp\,[(Ea/k)*\,(1/T_1 - 1/T_2)] = 77.94}$$

Where :

AF_T = Temperature acceleration factor

exp = Exponential function of the natural logarithm

Ea = Activation energy in electron volts (Model acceleration factor : 0.7eV for Gate oxide defect)

k= Boltzmann's constant(8.617×10^{-5} electron volts/Kelvins(328K)

T1 = Temperature at normal use conditions(55℃) in Kelvins(328K)

T2 = Temperature at accelerated condition(125℃) in Kelvins(398K)

◆ Estimation of Failure Rate from HTOL (Cont'd)

✓ FIT CALCULATION (Cont'd)

The Failure rate is described by the following equation:

$$\lambda = [\chi^2(\alpha, d.f) * 10^9 / 2\,EDH]\ FITs = 907\ FITs$$

Where :

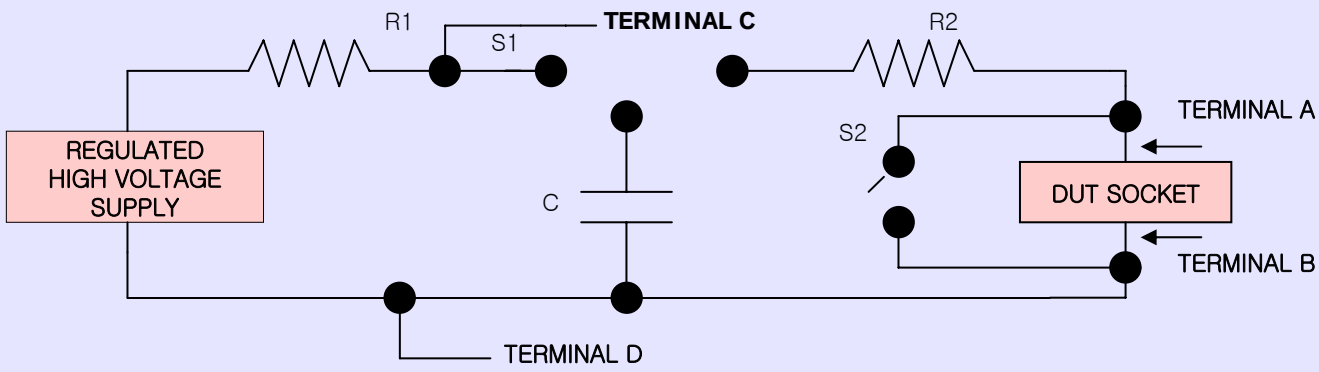
- λ = Failure rate in FITs
- χ^2 = Chi-square distribution value
- α = confidence level 60%(0.4)
- d.f = Degree of freedom = 2(n+1)
- n = Number of observed failure during test
- EDH = Equivalent Device Hour(AF* Sample size*Stress time t)

✓ MTTF CALCULATION

MTTF = 1/ λ = 126 Years

ESD Test Results

✓ TEST CIRCUIT



R1=10 OHM

C1=100 PF

C1=200PF

R2=1500 OHM (HUMAN BODY MODEL : JESD22-A114-B)

R2=ZERO OHM (MACHINE MODEL : JESD22-A115-A)

✓ FORCING METHOD OF ESD PULSE

- THREE POSITIVE AND THREE NEGATIVE PULSES ON EACH PIN

ESD Test Results (Cont'd)

✓ TEST RESULTS

METHOD	TARGET	RESULTS
HUMAN BODY (JEDEC STD)	>=2,000V	>=2,000V
MACHINE (JEDEC STD)	>=200V	>=200V

ESD Test Results (Cont'd)

✓ TEST RESULTS FOR HBM

METHOD	RESULTS	CLASSIFICATION
JESD22-A114-B	≥2,000V	CLASS 2

✓ TEST RESULTS FOR HM

METHOD	RESULTS	CLASSIFICATION
JESD22-A114-A	≥200V	CLASS B

✓ SUMMARY

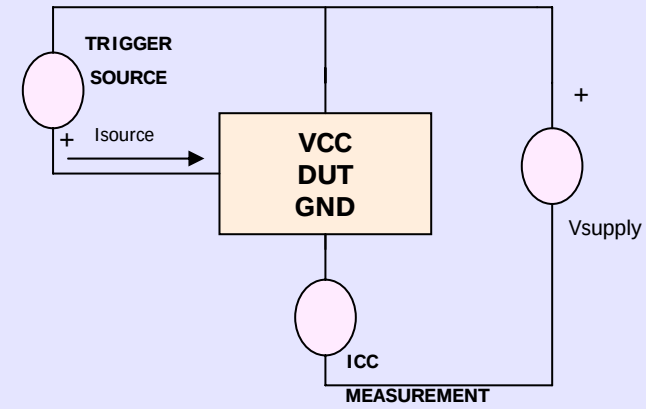
Model	Test Condition	Samples	No. of fail	Result
HBM	± 2,000V	9	0	Pass
MM	±200V	9	0	Pass
CDM (*)	800V, Socket Mode	3	0	Pass

✓ Notes

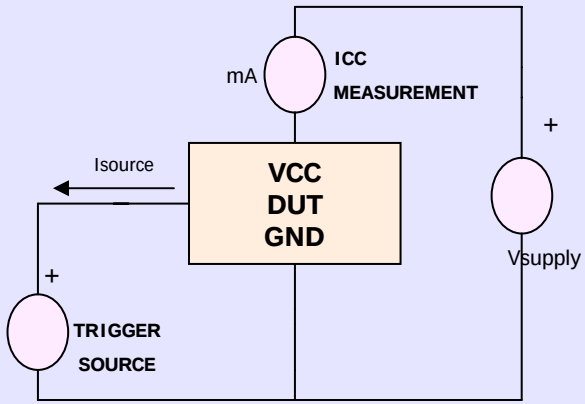
"*" The CDM information is obtained from used 87C520A0 samples. 87C520A0 samples and 87C510A0 samples are designed with the same library and fabricated by the same process. So 87C510A0 has same I/O characteristics with the 87C510A0.

Latch- Up Test Results

✓ TEST CIRCUIT : EIA JEDEC



POSITIVE INPUT/OUTPUT TRIGGER CURRENT



NEGATIVE INPUT/OUTPUT TRIGGER CURRENT

✓ TEST CONDITION

- PULSE WIDTH : 10ms
- CLAMP VOLTAGE : 7V

◆ Latch- Up Test Results

✓ TEST RESULTS

METHOD	TARGET	SAMPLE	No. of fail	RESULTS
POSITIVE	>=Inom*1.5	9	0	>250mA
NEGATIVE	<=Inom*1.5	9	0	>-250mA
VOLTAGE IMMUNITY	±5.4V (Max Vcc*1.5)			±10V

5. Appendix

- V1.0: Released in February, 2007.