a-Si TFT LCD Single Chip Driver 132RGBx162 Resolution and 262K color

Specification

Preliminary

Version: V2.00
Document No.: GC9102DS_V200.pdf

1. Introduction

The GC9102 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 132RGBx162dots, comprising a 396-channel source driver, a 162-channel gate driver, 48,114 bytes GRAM for graphic display data of 132RGBx162 dots, and power supply circuit.

The GC9102 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The GC9102 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9102 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9102 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

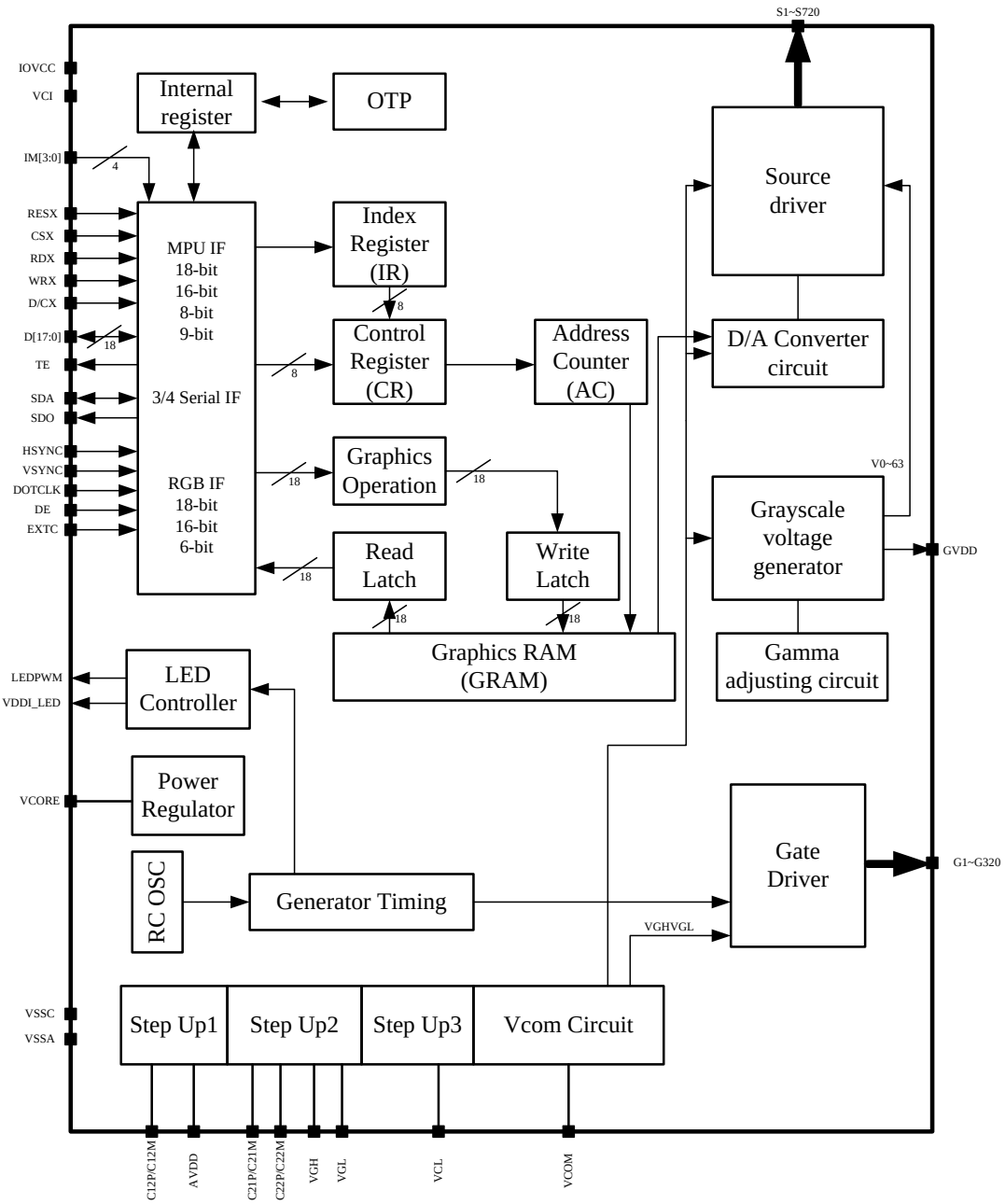
2. Features

- No need for external electronic component.
- Display resolution: [132xRGB](H) x 162(V)
- Output:
  - 396 source outputs
  - 162 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 48,114 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080/6800 series MCU
  - 3-line / 4-line serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VDD = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - AVDD - GND = 4.5V ~ 5.5V
    - VCL - GND = -1.5V ~ -3.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL ≦32V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (AVDD – 0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH - VCOML≦6.0V

- Operate temperature range: -40℃to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1. Block diagram



3.2. Pin Descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDD	i	Power	Power supply for analog, digital system and booster circuit
VDDI	I	Power	Low voltage power supply for interface logic circuits(1.65~3.3V)
DGND	I	Digital Ground	System ground level for logic blocks and I/O circuit
AGND	I	Analog Ground	System ground level for analog blocks and booster circuit.

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>P68</td><td>I</td><td>(VDDI/DGND)</td><td>8080/6800 MCU Interface mode selection.
P68=’1’: select 6800-MCU parallel interface
P68=’0’: select 8080-MCU parallel interface
If not used, please fix this pin at GND level.</td></tr>
<tr><td>IM2</td><td>I</td><td>(VDDI/DGND)</td><td>MCU Parallel interface bus and Serial interface select
- IM2=’1’;Parallel Interface
- IM2=’0’;Serial Interface</td></tr>
<tr><td>IM1,IM0</td><td>I</td><td>(VDDI/DGND)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>MCU 8-bit bus interface</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>1</td><td>MCU 16-bit bus interface</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>1</td><td>0</td><td>MCU 9-bit bus interface</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>1</td><td>1</td><td>MCU 18-bit bus interface</td><td>D[7:0]</td><td>D[17:0]</td></tr>
</table>
*:Fix this pin at VDDI or DGND.</td></tr>
<tr><td>SPIW4</td><td>I</td><td>(VDDI/DGND)</td><td>SPI interface selection pin
SPI4W=’0’: 3-wire SPI. (default)
SPI4W=’1’: 4-wire SPI.
This pin is internal pull low.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(VDDI/DGND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>EXTC</td><td>I</td><td>MCU
(VDDI/DGND)</td><td>Extended command set enable.
Low: extended command set is discarded.
High: extended command set is accepted.
Please connect EXTC to VDDI to read/write extended registers</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(VDDI/DGND)</td><td>Chip select input pin ("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only. *note1,2</td></tr>
</table>

<table>
<tr><td>D/CX
（SCL）</td><td>I</td><td>MCU
(VDDI/DGND)</td><td>This pin is used to select "Data or Command" in the parallel interface。
When DCX='1', data is selected. When DCX='0', command is selected.
This pin is used serial interface clock in 3-wire 9-bit/4-write 8-bit serial data interface.
If not used, this pin should be connected to VDDI or DGND.</td></tr>
<tr><td>RDX
(E)</td><td>I</td><td>MCU
(VDDI/DGND)</td><td>8080 system (RDX): Serves as a read signal and MCU read data at the rising edge.
6800 system (RDX): servers as a operation pin and MCU read/write data at the falling edge
Fix to VDDI level when not in use</td></tr>
<tr><td>WRX
(R/WX)
(D/CX)</td><td>I</td><td>MCU
(VDDI/DGND)</td><td>8080 system (WRX): Serves as a write signal and writes data at the rising edge.
6800 system (R/WX): Serves as read signal at high level and read signal at low level.
4-write 8-bit serial data interface: serves as D/CX(data/command selection).
Fix to VDDI level when not in use.</td></tr>
<tr><td>D[17:1]
D0/SDIO</td><td>I/O</td><td>MCU
(VDDI/DGND)</td><td>18-bit parallel bi-directional data bus for MCU system and D0 is also the serial input/output signal in SPI interface mode.
Fix to DGND level when not in use</td></tr>
<tr><td>GM[1:0]</td><td>I</td><td>(VDDI/DGND)</td><td>Panel Resolution selection pins
<table>
<tr><th>GM1</th><th>GM0</th><th>Resolution selection</th></tr>
<tr><td>0</td><td>0</td><td>132RGB x 162 (S1~S396 & G1~G162 output)</td></tr>
<tr><td>0</td><td>1</td><td>132RGB x 132 (S1~S396 & G1~G132 Output)</td></tr>
<tr><td>1</td><td>1</td><td>128RGB x 160 (S7~S390 & G2~G161 output)</td></tr>
<tr><td></td><td></td><td></td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td>MCU
(VDDI/DGND)</td><td>Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command.
When this pin is not activated, this pin is low. If not used, open this pin.</td></tr>
<tr><td>SRGB</td><td>I</td><td>(VDDI/DGND)</td><td>RGB Direction Select H/W Pin for Color Filter Setting.
<table>
<tr><th>SRGB</th><th>RGB Arrangement</th></tr>
<tr><td>0</td><td>S1, S2, S3 Filter Order = ’R’, ’G’, ’B’</td></tr>
<tr><td>1</td><td>S1, S2, S3 Filter Order = ‘B’, ‘G’, ‘R</td></tr>
</table></td></tr>
<tr><td>SMX</td><td>I</td><td>(VDDI/DGND)</td><td>Module Source Output Direction H/W Selection Pin.
<table>
<tr><th>SMX</th><th colspan="3">Scanning direction of source output</th></tr>
<tr><td></td><td>GM=’00’</td><td>GM=’01’</td><td>GM=’11’</td></tr>
<tr><td>0</td><td>S1 -> S396</td><td>S1 -> S396</td><td>S7 -> S390</td></tr>
<tr><td>1</td><td>S396 -> S1</td><td>S396 -> S1</td><td>S390 -> S7</td></tr>
</table></td></tr>
<tr><td>SMY</td><td>I</td><td>(VDDI/DGND)</td><td>Module Gate Output Direction H/W Selection Pin.
<table>
<tr><th>SMY</th><th colspan="3">Scanning direction of gate output</th></tr>
<tr><td></td><td>GM=’00’</td><td>GM=’01’</td><td>GM=’11’</td></tr>
<tr><td>0</td><td>G1 -> G162</td><td>G1 -> G132</td><td>G2 -> G161</td></tr>
<tr><td>1</td><td>G162 -> G1</td><td>G132 -> G1</td><td>G161 -> G2</td></tr>
</table></td></tr>
<tr><td>LCM</td><td>I</td><td>(VDDI/DGND)</td><td>Liquid Crystal (LC) Type Selection Pins.
<table>
<tr><th>LCM</th><th>Selection of LC Type</th></tr>
<tr><td>0</td><td>Normally White LC Type</td></tr>
<tr><td>1</td><td>Normally Black LC Type</td></tr>
</table></td></tr>
</table>

Note.

1. If CSX is connected to DGND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using

the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S396~S1	O	Source	Source output signals.. Leave the pin to open when not in use.
G162~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
AVDD	O	Power	Output voltage of 1st step up circuit (2*VDD).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
VGH	O	Power	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits.
VGL	O	Power	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits.
VCL	O	Power	Power supply for VCOML. VCL=0~-VDD
GVDD	O		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VCOM	O		Power supply pad for the TFT-display counter electrode. Charge recycling method is used with VDD and AGND voltage. Connect this pad to the TFT-display counter electrode.
VDDIO	O		VDDI voltage output level for monitoring
DGNDO	O		DGND voltage output level for monitoring

Test Pins			
Pin Name	I/O	Type	Descriptions
TEST2P TEST1P	I	Digital Ground	These test pins for driver vender test used Please connect these pins to DGND
TESTOP[8:1]	O	Open	These test pins for driver vender test used Please leave these pins open
DUMMYR	-	Open	These pins are dummy. During normal operation, leave these pads open.
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		396 pins (132*RGB)
2	TFT Gate Driver		162 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S396	V0~V63 grayscales
		G1~G162	VGH-VGL
		VCOM	VCOMH-VCOML :Amplitude = electronic volumes
5	Input Voltage	VDDI	1.65~3.30V
		VDD	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	4.5~5.5V
		VGH	10.0~20.0V
		VGL	-5.0~-15.0V
		VCL	-1.9~-3.0V
		VGH-VGL	Max. 32.0V
7	Internal Step-up Circuits	AVDD	VDD*2
		VGH	VDD*6
		VGL	VDD*-6
		VCL	VDD*-1

3.3. PAD coordinates

No.	Pad name	X	Y
1	Dummy	-4750.0	-231.0
2	VDDIO	-4700.0	-231.0
3	EXTC	-4650.0	-231.0
4	DGNDO	-4600.0	-231.0
5	IM<0>	-4550.0	-231.0
6	VDDIO	-4500.0	-231.0
7	IM<1>	-4450.0	-231.0
8	DGNDO	-4400.0	-231.0
9	P68	-4350.0	-231.0
10	VDDIO	-4300.0	-231.0
11	Dummy	-4250.0	-231.0
12	DGNDO	-4200.0	-231.0
13	Dummy	-4150.0	-231.0
14	VDDIO	-4100.0	-231.0
15	SRGB	-4050.0	-231.0
16	DGNDO	-4000.0	-231.0
17	SMX	-3950.0	-231.0
18	VDDIO	-3900.0	-231.0
19	SMY	-3850.0	-231.0
20	DGNDO	-3800.0	-231.0
21	Dummy	-3750.0	-231.0
22	VDDIO	-3700.0	-231.0
23	Dummy	-3650.0	-231.0
24	DGNDO	-3600.0	-231.0
25	Dummy	-3550.0	-231.0
26	VDDIO	-3500.0	-231.0
27	Dummy	-3450.0	-231.0
28	DGNDO	-3400.0	-231.0
29	Dummy	-3350.0	-231.0
30	VDDIO	-3300.0	-231.0
31	LCM	-3250.0	-231.0
32	DGNDO	-3200.0	-231.0
33	DUMMY	-3150.0	-231.0
34	VDDIO	-3100.0	-231.0
35	Dummy	-3050.0	-231.0
36	DGNDO	-3000.0	-231.0
37	GM<1>	-2950.0	-231.0
38	VDDIO	-2900.0	-231.0
39	GM<0>	-2850.0	-231.0
40	DGNDO	-2800.0	-231.0
41	Dummy	-2750.0	-231.0
42	DUMMY	-2700.0	-231.0
43	SPI4W	-2650.0	-231.0
44	VDDIO	-2600.0	-231.0
45	TESTOP[8]	-2550.0	-231.0
46	TESTOP[7]	-2500.0	-231.0
47	TESTOP[6]	-2450.0	-231.0
48	TESTOP[5]	-2400.0	-231.0
49	TESTOP[4]	-2350.0	-231.0
50	OSC	-2300.0	-231.0
51	VDD	-2250.0	-231.0
52	VDD	-2200.0	-231.0
53	VDD	-2150.0	-231.0
54	VDD	-2100.0	-231.0
55	VDD	-2050.0	-231.0
56	VDD	-2000.0	-231.0
57	AGND	-1950.0	-231.0
58	AGND	-1900.0	-231.0
59	AGND	-1850.0	-231.0
60	AGND	-1800.0	-231.0
61	AGND	-1750.0	-231.0
62	AGND	-1700.0	-231.0
63	RD	-1630.0	-231.0
64	DCX	-1570.0	-231.0
65	TESEL	-1510.0	-231.0
66	DGNDO	-1450.0	-231.0
67	D<17>	-1390.0	-231.0
68	D<16>	-1330.0	-231.0
69	D<15>	-1270.0	-231.0
70	D<14>	-1210.0	-231.0
71	D<13>	-1150.0	-231.0
72	D<12>	-1090.0	-231.0
73	D<11>	-1030.0	-231.0
74	D<10>	-970.0	-231.0
75	D<9>	-910.0	-231.0
76	D<8>	-850.0	-231.0
77	D<1>	-790.0	-231.0
78	D<3>	-730.0	-231.0
79	D<5>	-670.0	-231.0
80	D<7>	-610.0	-231.0
81	TE	-550.0	-231.0
82	RESX	-490.0	-231.0
83	CS	-430.0	-231.0
84	D<6>	-370.0	-231.0
85	D<4>	-310.0	-231.0
86	D<2>	-250.0	-231.0
87	IM<2>	-190.0	-231.0
88	D<0>	-130.0	-231.0
89	WR	-70.0	-231.0
90	Dummy	0.0	-231.0
91	Dummy	50.0	-231.0
92	Dummy	100.0	-231.0
93	Dummy	150.0	-231.0
94	TESTOP[3]	200.0	-231.0
95	TESTOP[2]	250.0	-231.0
96	TESTOP[1]	300.0	-231.0
97	DGND	350.0	-231.0
98	DGND	400.0	-231.0
99	DGND	450.0	-231.0
100	DGND	500.0	-231.0
51	VDD	-2250.0	-231.0
101	DGND	550.0	-231.0
102	DGND	600.0	-231.0
103	VDDI	650.0	-231.0
104	VDDI	700.0	-231.0
105	VDDI	750.0	-231.0
106	VDDI	800.0	-231.0
107	VDDI	850.0	-231.0
108	VDDI	900.0	-231.0
109	VPP	950.0	-231.0
110	VPP	1000.0	-231.0
111	VPP	1050.0	-231.0
112	GVDD	1100.0	-231.0
113	GVDD	1150.0	-231.0
114	GVDD	1200.0	-231.0
115	VCC	1250.0	-231.0
116	Dummy	1300.0	-231.0
117	Dummy	1350.0	-231.0
118	DUMMY	1400.0	-231.0
119	Dummy	1450.0	-231.0
120	AVDD	1500.0	-231.0
121	AVDD	1550.0	-231.0
122	AVDD	1600.0	-231.0
123	AVDD	1650.0	-231.0
124	AVDD	1700.0	-231.0
125	Dummy	1750.0	-231.0
126	Dummy	1800.0	-231.0
127	Dummy	1850.0	-231.0
128	Dummy	1900.0	-231.0
129	Dummy	1950.0	-231.0
130	Dummy	2000.0	-231.0
131	Dummy	2050.0	-231.0
132	Dummy	2100.0	-231.0
133	Dummy	2150.0	-231.0
134	Dummy	2200.0	-231.0
135	Dummy	2250.0	-231.0
136	Dummy	2300.0	-231.0
137	Dummy	2350.0	-231.0
138	Dummy	2400.0	-231.0
139	Dummy	2450.0	-231.0
140	Dummy	2500.0	-231.0
141	Dummy	2550.0	-231.0
142	Dummy	2600.0	-231.0
143	Dummy	2650.0	-231.0
144	Dummy	2700.0	-231.0
145	Dummy	2750.0	-231.0
146	AGND	2800.0	-231.0
147	AGND	2850.0	-231.0
148	AGND	2900.0	-231.0
149	VCL(AVCL)	2950.0	-231.0
150	VCL(AVCL)	3000.0	-231.0
151	VCL(AVCL)	3050.0	-231.0
152	Dummy	3100.0	-231.0
153	Dummy	3150.0	-231.0
154	Dummy	3200.0	-231.0
155	Dummy	3250.0	-231.0
156	Dummy	3300.0	-231.0
157	Dummy	3350.0	-231.0
158	Dummy	3400.0	-231.0
159	Dummy	3450.0	-231.0
160	Dummy	3500.0	-231.0
161	Dummy	3550.0	-231.0
162	Dummy	3600.0	-231.0
163	Dummy	3650.0	-231.0
164	Dummy	3700.0	-231.0
165	Dummy	3750.0	-231.0
166	Dummy	3800.0	-231.0
167	Dummy	3850.0	-231.0
168	Dummy	3900.0	-231.0
169	Dummy	3950.0	-231.0
170	VGL	4000.0	-231.0
171	VGL	4050.0	-231.0
172	VGL	4100.0	-231.0
173	VGH	4150.0	-231.0
174	VGH(DUMMY)	4200.0	-231.0
175	VGH(DUMMY)	4250.0	-231.0
176	VCOMH(DUMMY)	4300.0	-231.0
177	VCOMH(DUMMY)	4350.0	-231.0
178	VCOMH(DUMMY)	4400.0	-231.0
179	VCOML(VCL)	4450.0	-231.0
180	VCOML(VCL)	4500.0	-231.0
181	VCOMLVCL)	4550.0	-231.0
182	VCOM	4600.0	-231.0
183	VCOM	4650.0	-231.0
184	VCOM	4700.0	-231.0
185	Dummy	4750.0	-231.0
186	Dummy	4772.0	110.0
187	Dummy	4756.0	227.0
188	G<162>	4740.0	110.0
189	G<160>	4724.0	227.0
190	G<158>	4708.0	110.0
191	G<156>	4692.0	227.0
192	G<154>	4676.0	110.0
193	G<152>	4660.0	227.0
194	G<150>	4644.0	110.0
195	G<148>	4628.0	227.0
196	G<146>	4612.0	110.0
197	G<144>	4596.0	227.0
198	G<142>	4580.0	110.0
199	G<140>	4564.0	227.0
200	G<138>	4548.0	110.0

No.	Pad name	X	Y
201	G<136>	4532.0	227.0
202	G<134>	4516.0	110.0
203	G<132>	4500.0	227.0
204	G<130>	4484.0	110.0
205	G<128>	4468.0	227.0
206	G<126>	4452.0	110.0
207	G<124>	4436.0	227.0
208	G<122>	4420.0	110.0
209	G<120>	4404.0	227.0
210	G<118>	4388.0	110.0
211	G<116>	4372.0	227.0
212	G<114>	4356.0	110.0
213	G<112>	4340.0	227.0
214	G<110>	4324.0	110.0
215	G<108>	4308.0	227.0
216	G<106>	4292.0	110.0
217	G<104>	4276.0	227.0
218	G<102>	4260.0	110.0
219	G<100>	4244.0	227.0
220	G<98>	4228.0	110.0
221	G<96>	4212.0	227.0
222	G<94>	4196.0	110.0
223	G<92>	4180.0	227.0
224	G<90>	4164.0	110.0
225	G<88>	4148.0	227.0
226	G<86>	4132.0	110.0
227	G<84>	4116.0	227.0
228	G<82>	4100.0	110.0
229	G<80>	4084.0	227.0
230	G<78>	4068.0	110.0
231	G<76>	4052.0	227.0
232	G<74>	4036.0	110.0
233	G<72>	4020.0	227.0
234	G<70>	4004.0	110.0
235	G<68>	3988.0	227.0
236	G<66>	3972.0	110.0
237	G<64>	3956.0	227.0
238	G<62>	3940.0	110.0
239	G<60>	3924.0	227.0
240	G<58>	3908.0	110.0
241	G<56>	3892.0	227.0
242	G<54>	3876.0	110.0
243	G<52>	3860.0	227.0
244	G<50>	3844.0	110.0
245	G<48>	3828.0	227.0
246	G<46>	3812.0	110.0
247	G<44>	3796.0	227.0
248	G<42>	3780.0	110.0
249	G<40>	3764.0	227.0
250	G<38>	3748.0	110.0

No.	Pad	X	Y
251	G<36>	3732.0	227.0
252	G<34>	3716.0	110.0
253	G<32>	3700.0	227.0
254	G<30>	3684.0	110.0
255	G<28>	3668.0	227.0
256	G<26>	3652.0	110.0
257	G<24>	3636.0	227.0
258	G<22>	3620.0	110.0
259	G<20>	3604.0	227.0
260	G<18>	3588.0	110.0
261	G<16>	3572.0	227.0
262	G<14>	3556.0	110.0
263	G<12>	3540.0	227.0
264	G<10>	3524.0	110.0
265	G<8>	3508.0	227.0
266	G<6>	3492.0	110.0
267	G<4>	3476.0	227.0
268	G<2>	3460.0	110.0
269	Dummy	3444.0	227.0
270	Dummy	3428.0	110.0
271	Dummy	3412.0	227.0
272	Dummy	3396.0	110.0
273	S<396>	3380.0	227.0
274	S<395>	3364.0	110.0
275	S<394>	3348.0	227.0
276	S<393>	3332.0	110.0
277	S<392>	3316.0	227.0
278	S<391>	3300.0	110.0
279	S<390>	3284.0	227.0
280	S<389>	3268.0	110.0
281	S<388>	3252.0	227.0
282	S<387>	3236.0	110.0
283	S<386>	3220.0	227.0
284	S<385>	3204.0	110.0
285	S<384>	3188.0	227.0
286	S<383>	3172.0	110.0
287	S<382>	3156.0	227.0
288	S<381>	3140.0	110.0
289	S<380>	3124.0	227.0
290	S<379>	3108.0	110.0
291	S<378>	3092.0	227.0
292	S<377>	3076.0	110.0
293	S<376>	3060.0	227.0
294	S<375>	3044.0	110.0
295	S<374>	3028.0	227.0
296	S<373>	3012.0	110.0
297	S<372>	2996.0	227.0
298	S<371>	2980.0	110.0
299	S<370>	2964.0	227.0
300	S<369>	2948.0	110.0

No.	Pad name	X	Y
301	S<368>	2932.0	227.0
302	S<367>	2916.0	110.0
303	S<366>	2900.0	227.0
304	S<365>	2884.0	110.0
305	S<364>	2868.0	227.0
306	S<363>	2852.0	110.0
307	S<362>	2836.0	227.0
308	S<361>	2820.0	110.0
309	S<360>	2804.0	227.0
310	S<359>	2788.0	110.0
311	S<358>	2772.0	227.0
312	S<357>	2756.0	110.0
313	S<356>	2740.0	227.0
314	S<355>	2724.0	110.0
315	S<354>	2708.0	227.0
316	S<353>	2692.0	110.0
317	S<352>	2676.0	227.0
318	S<351>	2660.0	110.0
319	S<350>	2644.0	227.0
320	S<349>	2628.0	110.0
321	S<348>	2612.0	227.0
322	S<347>	2596.0	110.0
323	S<346>	2580.0	227.0
324	S<345>	2564.0	110.0
325	S<344>	2548.0	227.0
326	S<343>	2532.0	110.0
327	S<342>	2516.0	227.0
328	S<341>	2500.0	110.0
329	S<340>	2484.0	227.0
330	S<339>	2468.0	110.0
331	S<338>	2452.0	227.0
332	S<337>	2436.0	110.0
333	S<336>	2420.0	227.0
334	S<335>	2404.0	110.0
335	S<334>	2388.0	227.0
336	S<333>	2372.0	110.0
337	S<332>	2356.0	227.0
338	S<331>	2340.0	110.0
339	S<330>	2324.0	227.0
340	S<329>	2308.0	110.0
341	S<328>	2292.0	227.0
342	S<327>	2276.0	110.0
343	S<326>	2260.0	227.0
344	S<325>	2244.0	110.0
345	S<324>	2228.0	227.0
346	S<323>	2212.0	110.0
347	S<322>	2196.0	227.0
348	S<321>	2180.0	110.0
349	S<320>	2164.0	227.0
350	S<319>	2148.0	110.0

No.	Pad name	X	Y
351	S<318>	2132.0	227.0
352	S<317>	2116.0	110.0
353	S<316>	2100.0	227.0
354	S<315>	2084.0	110.0
355	S<314>	2068.0	227.0
356	S<313>	2052.0	110.0
357	S<312>	2036.0	227.0
358	S<311>	2020.0	110.0
359	S<310>	2004.0	227.0
360	S<309>	1988.0	110.0
361	S<308>	1972.0	227.0
362	S<307>	1956.0	110.0
363	S<306>	1940.0	227.0
364	S<305>	1924.0	110.0
365	S<304>	1908.0	227.0
366	S<303>	1892.0	110.0
367	S<302>	1876.0	227.0
368	S<301>	1860.0	110.0
369	S<300>	1844.0	227.0
370	S<299>	1828.0	110.0
371	S<298>	1812.0	227.0
372	S<297>	1796.0	110.0
373	S<296>	1780.0	227.0
374	S<295>	1764.0	110.0
375	S<294>	1748.0	227.0
376	S<293>	1732.0	110.0
377	S<292>	1716.0	227.0
378	S<291>	1700.0	110.0
379	S<290>	1684.0	227.0
380	S<289>	1668.0	110.0
381	S<288>	1652.0	227.0
382	S<287>	1636.0	110.0
383	S<286>	1620.0	227.0
384	S<285>	1604.0	110.0
385	S<284>	1588.0	227.0
386	S<283>	1572.0	110.0
387	S<282>	1556.0	227.0
388	S<281>	1540.0	110.0
389	S<280>	1524.0	227.0
390	S<279>	1508.0	110.0
391	S<278>	1492.0	227.0
392	S<277>	1476.0	110.0
393	S<276>	1460.0	227.0
394	S<275>	1444.0	110.0
395	S<274>	1428.0	227.0
396	S<273>	1412.0	110.0
397	S<272>	1396.0	227.0
398	S<271>	1380.0	110.0
399	S<270>	1364.0	227.0
400	S<269>	1348.0	110.0

No.	Pad name	X	Y
401	S<268>	1332.0	227.0
402	S<267>	1316.0	110.0
403	S<266>	1300.0	227.0
404	S<265>	1284.0	110.0
405	S<264>	1268.0	227.0
406	S<263>	1252.0	110.0
407	S<262>	1236.0	227.0
408	S<261>	1220.0	110.0
409	S<260>	1204.0	227.0
410	S<259>	1188.0	110.0
411	S<258>	1172.0	227.0
412	S<257>	1156.0	110.0
413	S<256>	1140.0	227.0
414	S<255>	1124.0	110.0
415	S<254>	1108.0	227.0
416	S<253>	1092.0	110.0
417	S<252>	1076.0	227.0
418	S<251>	1060.0	110.0
419	S<250>	1044.0	227.0
420	S<249>	1028.0	110.0
421	S<248>	1012.0	227.0
422	S<247>	996.0	110.0
423	S<246>	980.0	227.0
424	S<245>	964.0	110.0
425	S<244>	948.0	227.0
426	S<243>	932.0	110.0
427	S<242>	916.0	227.0
428	S<241>	900.0	110.0
429	S<240>	884.0	227.0
430	S<239>	868.0	110.0
431	S<238>	852.0	227.0
432	S<237>	836.0	110.0
433	S<236>	820.0	227.0
434	S<235>	804.0	110.0
435	S<234>	788.0	227.0
436	S<233>	772.0	110.0
437	S<232>	756.0	227.0
438	S<231>	740.0	110.0
439	S<230>	724.0	227.0
440	S<229>	708.0	110.0
441	S<228>	692.0	227.0
442	S<227>	676.0	110.0
443	S<226>	660.0	227.0
444	S<225>	644.0	110.0
445	S<224>	628.0	227.0
446	S<223>	612.0	110.0
447	S<222>	596.0	227.0
448	S<221>	580.0	110.0
449	S<220>	564.0	227.0
450	S<219>	548.0	110.0

No.	Pad	X	Y
451	S<218>	532.0	227.0
452	S<217>	516.0	110.0
453	S<216>	500.0	227.0
454	S<215>	484.0	110.0
455	S<214>	468.0	227.0
456	S<213>	452.0	110.0
457	S<212>	436.0	227.0
458	S<211>	420.0	110.0
459	S<210>	404.0	227.0
460	S<209>	388.0	110.0
461	S<208>	372.0	227.0
462	S<207>	356.0	110.0
463	S<206>	340.0	227.0
464	S<205>	324.0	110.0
465	S<204>	308.0	227.0
466	S<203>	292.0	110.0
467	S<202>	276.0	227.0
468	S<201>	260.0	110.0
469	S<200>	244.0	227.0
470	S<199>	228.0	110.0
471	S<198>	-228.0	110.0
472	S<197>	-244.0	227.0
473	S<196>	-260.0	110.0
474	S<195>	-276.0	227.0
475	S<194>	-292.0	110.0
476	S<193>	-308.0	227.0
477	S<192>	-324.0	110.0
478	S<191>	-340.0	227.0
479	S<190>	-356.0	110.0
480	S<189>	-372.0	227.0
481	S<188>	-388.0	110.0
482	S<187>	-404.0	227.0
483	S<186>	-420.0	110.0
484	S<185>	-436.0	227.0
485	S<184>	-452.0	110.0
486	S<183>	-468.0	227.0
487	S<182>	-484.0	110.0
488	S<181>	-500.0	227.0
489	S<180>	-516.0	110.0
490	S<179>	-532.0	227.0
491	S<178>	-548.0	110.0
492	S<177>	-564.0	227.0
493	S<176>	-580.0	110.0
494	S<175>	-596.0	227.0
495	S<174>	-612.0	110.0
496	S<173>	-628.0	227.0
497	S<172>	-644.0	110.0
498	S<171>	-660.0	227.0
499	S<170>	-676.0	110.0
500	S<169>	-692.0	227.0

No.	Pad name	X	Y
501	S<168>	-708.0	110.0
502	S<167>	-724.0	227.0
503	S<166>	-740.0	110.0
504	S<165>	-756.0	227.0
505	S<164>	-772.0	110.0
506	S<163>	-788.0	227.0
507	S<162>	-804.0	110.0
508	S<161>	-820.0	227.0
509	S<160>	-836.0	110.0
510	S<159>	-852.0	227.0
511	S<158>	-868.0	110.0
512	S<157>	-884.0	227.0
513	S<156>	-900.0	110.0
514	S<155>	-916.0	227.0
515	S<154>	-932.0	110.0
516	S<153>	-948.0	227.0
517	S<152>	-964.0	110.0
518	S<151>	-980.0	227.0
519	S<150>	-996.0	110.0
520	S<149>	-1012.0	227.0
521	S<148>	-1028.0	110.0
522	S<147>	-1044.0	227.0
523	S<146>	-1060.0	110.0
524	S<145>	-1076.0	227.0
525	S<144>	-1092.0	110.0
526	S<143>	-1108.0	227.0
527	S<142>	-1124.0	110.0
528	S<141>	-1140.0	227.0
529	S<140>	-1156.0	110.0
530	S<139>	-1172.0	227.0
531	S<138>	-1188.0	110.0
532	S<137>	-1204.0	227.0
533	S<136>	-1220.0	110.0
534	S<135>	-1236.0	227.0
535	S<134>	-1252.0	110.0
536	S<133>	-1268.0	227.0
537	S<132>	-1284.0	110.0
538	S<131>	-1300.0	227.0
539	S<130>	-1316.0	110.0
540	S<129>	-1332.0	227.0
541	S<128>	-1348.0	110.0
542	S<127>	-1364.0	227.0
543	S<126>	-1380.0	110.0
544	S<125>	-1396.0	227.0
545	S<124>	-1412.0	110.0
546	S<123>	-1428.0	227.0
547	S<122>	-1444.0	110.0
548	S<121>	-1460.0	227.0
549	S<120>	-1476.0	110.0
550	S<119>	-1492.0	227.0

No.	Pad name	X	Y
551	S<118>	-1508.0	110.0
552	S<117>	-1524.0	227.0
553	S<116>	-1540.0	110.0
554	S<115>	-1556.0	227.0
555	S<114>	-1572.0	110.0
556	S<113>	-1588.0	227.0
557	S<112>	-1604.0	110.0
558	S<111>	-1620.0	227.0
559	S<110>	-1636.0	110.0
560	S<109>	-1652.0	227.0
561	S<108>	-1668.0	110.0
562	S<107>	-1684.0	227.0
563	S<106>	-1700.0	110.0
564	S<105>	-1716.0	227.0
565	S<104>	-1732.0	110.0
566	S<103>	-1748.0	227.0
567	S<102>	-1764.0	110.0
568	S<101>	-1780.0	227.0
569	S<100>	-1796.0	110.0
570	S<99>	-1812.0	227.0
571	S<98>	-1828.0	110.0
572	S<97>	-1844.0	227.0
573	S<96>	-1860.0	110.0
574	S<95>	-1876.0	227.0
575	S<94>	-1892.0	110.0
576	S<93>	-1908.0	227.0
577	S<92>	-1924.0	110.0
578	S<91>	-1940.0	227.0
579	S<90>	-1956.0	110.0
580	S<89>	-1972.0	227.0
581	S<88>	-1988.0	110.0
582	S<87>	-2004.0	227.0
583	S<86>	-2020.0	110.0
584	S<85>	-2036.0	227.0
585	S<84>	-2052.0	110.0
586	S<83>	-2068.0	227.0
587	S<82>	-2084.0	110.0
588	S<81>	-2100.0	227.0
589	S<80>	-2116.0	110.0
590	S<79>	-2132.0	227.0
591	S<78>	-2148.0	110.0
592	S<77>	-2164.0	227.0
593	S<76>	-2180.0	110.0
594	S<75>	-2196.0	227.0
595	S<74>	-2212.0	110.0
596	S<73>	-2228.0	227.0
597	S<72>	-2244.0	110.0
598	S<71>	-2260.0	227.0
599	S<70>	-2276.0	110.0
600	S<69>	-2292.0	227.0

No.	Pad name	X	Y
601	S<68>	-2308.0	110.0
602	S<67>	-2324.0	227.0
603	S<66>	-2340.0	110.0
604	S<65>	-2356.0	227.0
605	S<64>	-2372.0	110.0
606	S<63>	-2388.0	227.0
607	S<62>	-2404.0	110.0
608	S<61>	-2420.0	227.0
609	S<60>	-2436.0	110.0
610	S<59>	-2452.0	227.0
611	S<58>	-2468.0	110.0
612	S<57>	-2484.0	227.0
613	S<56>	-2500.0	110.0
614	S<55>	-2516.0	227.0
615	S<54>	-2532.0	110.0
616	S<53>	-2548.0	227.0
617	S<52>	-2564.0	110.0
618	S<51>	-2580.0	227.0
619	S<50>	-2596.0	110.0
620	S<49>	-2612.0	227.0
621	S<48>	-2628.0	110.0
622	S<47>	-2644.0	227.0
623	S<46>	-2660.0	110.0
624	S<45>	-2676.0	227.0
625	S<44>	-2692.0	110.0
626	S<43>	-2708.0	227.0
627	S<42>	-2724.0	110.0
628	S<41>	-2740.0	227.0
629	S<40>	-2756.0	110.0
630	S<39>	-2772.0	227.0
631	S<38>	-2788.0	110.0
632	S<37>	-2804.0	227.0
633	S<36>	-2820.0	110.0
634	S<35>	-2836.0	227.0
635	S<34>	-2852.0	110.0
636	S<33>	-2868.0	227.0
637	S<32>	-2884.0	110.0
638	S<31>	-2900.0	227.0
639	S<30>	-2916.0	110.0
640	S<29>	-2932.0	227.0
641	S<28>	-2948.0	110.0
642	S<27>	-2964.0	227.0
643	S<26>	-2980.0	110.0
644	S<25>	-2996.0	227.0
645	S<24>	-3012.0	110.0
646	S<23>	-3028.0	227.0
647	S<22>	-3044.0	110.0
648	S<21>	-3060.0	227.0
649	S<20>	-3076.0	110.0
650	S<19>	-3092.0	227.0

No.	Pad	X	Y
651	S<18>	-3108.0	110.0
652	S<17>	-3124.0	227.0
653	S<16>	-3140.0	110.0
654	S<15>	-3156.0	227.0
655	S<14>	-3172.0	110.0
656	S<13>	-3188.0	227.0
657	S<12>	-3204.0	110.0
658	S<11>	-3220.0	227.0
659	S<10>	-3236.0	110.0
660	S<9>	-3252.0	227.0
661	S<8>	-3268.0	110.0
662	S<7>	-3284.0	227.0
663	S<6>	-3300.0	110.0
664	S<5>	-3316.0	227.0
665	S<4>	-3332.0	110.0
666	S<3>	-3348.0	227.0
667	S<2>	-3364.0	110.0
668	S<1>	-3380.0	227.0
669	Dummy	-3396.0	110.0
670	Dummy	-3412.0	227.0
671	Dummy	-3428.0	110.0
672	Dummy	-3444.0	227.0
673	G<1>	-3460.0	110.0
674	G<3>	-3476.0	227.0
675	G<5>	-3492.0	110.0
676	G<7>	-3508.0	227.0
677	G<9>	-3524.0	110.0
678	G<11>	-3540.0	227.0
679	G<13>	-3556.0	110.0
680	G<15>	-3572.0	227.0
681	G<17>	-3588.0	110.0
682	G<19>	-3604.0	227.0
683	G<21>	-3620.0	110.0
684	G<23>	-3636.0	227.0
685	G<25>	-3652.0	110.0
686	G<27>	-3668.0	227.0
687	G<29>	-3684.0	110.0
688	G<31>	-3700.0	227.0
689	G<33>	-3716.0	110.0
690	G<35>	-3732.0	227.0
691	G<37>	-3748.0	110.0
692	G<39>	-3764.0	227.0
693	G<41>	-3780.0	110.0
694	G<43>	-3796.0	227.0
695	G<45>	-3812.0	110.0
696	G<47>	-3828.0	227.0
697	G<49>	-3844.0	110.0
698	G<51>	-3860.0	227.0
699	G<53>	-3876.0	110.0
700	G<55>	-3892.0	227.0

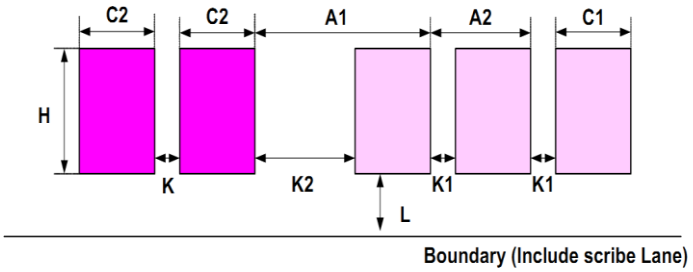
No.	Pad name	X	Y
701	G<57>	-3908.0	110.0
702	G<59>	-3924.0	227.0
703	G<61>	-3940.0	110.0
704	G<63>	-3956.0	227.0
705	G<65>	-3972.0	110.0
706	G<67>	-3988.0	227.0
707	G<69>	-4004.0	110.0
708	G<71>	-4020.0	227.0
709	G<73>	-4036.0	110.0
710	G<75>	-4052.0	227.0
711	G<77>	-4068.0	110.0
712	G<79>	-4084.0	227.0
713	G<81>	-4100.0	110.0
714	G<83>	-4116.0	227.0
715	G<85>	-4132.0	110.0
716	G<87>	-4148.0	227.0
717	G<89>	-4164.0	110.0
718	G<91>	-4180.0	227.0
719	G<93>	-4196.0	110.0
720	G<95>	-4212.0	227.0
721	G<97>	-4228.0	110.0
722	G<99>	-4244.0	227.0
723	G<101>	-4260.0	110.0
724	G<103>	-4276.0	227.0
725	G<105>	-4292.0	110.0
726	G<107>	-4308.0	227.0
727	G<109>	-4324.0	110.0
728	G<111>	-4340.0	227.0
729	G<113>	-4356.0	110.0
730	G<115>	-4372.0	227.0
731	G<117>	-4388.0	110.0
732	G<119>	-4404.0	227.0
733	G<121>	-4420.0	110.0
734	G<123>	-4436.0	227.0
735	G<125>	-4452.0	110.0
736	G<127>	-4468.0	227.0
737	G<129>	-4484.0	110.0
738	G<131>	-4500.0	227.0
739	G<133>	-4516.0	110.0
740	G<135>	-4532.0	227.0
741	G<137>	-4548.0	110.0
742	G<139>	-4564.0	227.0
743	G<141>	-4580.0	110.0
744	G<143>	-4596.0	227.0
745	G<145>	-4612.0	110.0
746	G<147>	-4628.0	227.0
747	G<149>	-4644.0	110.0
748	G<151>	-4660.0	227.0
749	G<153>	-4676.0	110.0
750	G<155>	-4692.0	227.0

No.	Pad name	X	Y
751	G<157>	-4708.0	110.0
752	G<159>	-4724.0	227.0
753	G<161>	-4740.0	110.0
754	Dummy	-4756.0	227.0
755	Dummy	-4772.0	110.0

Alignment mark	X	Y
Alignment_R	4841	-220
Alignment_L	-4841	-220

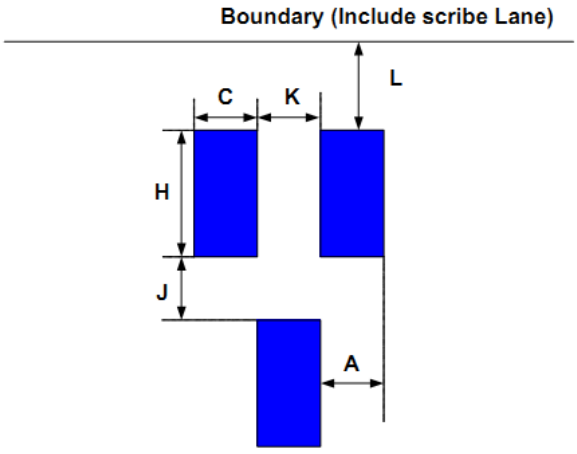
BUMP Size

Input Pad



Item	Symbol	Size
Bump Pitch 1	A1	72.5 um
Bump Pitch 2	A2	60 um
Bump Width 1	C1	38 um
Bump Width 2	C2	33 um
Bump Height	H	88 um
Bump Gap	K	17 um
Bump Gap1	K1	22 um
Bump Gap2	K2	34.5 um
Bump Area 1	C1 X H	3344 um2
Bump Area 2	C2 X H	2904 um2
Chip Boundary(Include Scribe Lane)	L	60 um

Output Pad



Item	Symbol	Size
Bump Pitch	A	16 um
Bump Width	C	16 um
Bump Height	H	98 um
Bump Gap1 (Vertical)	J	19 um
Bump Gap2 (Horizontal)	K	16 um
Bump Area	C x H	1568 um2
Chip Boundary (Include Scribe Lane)	L	59 um

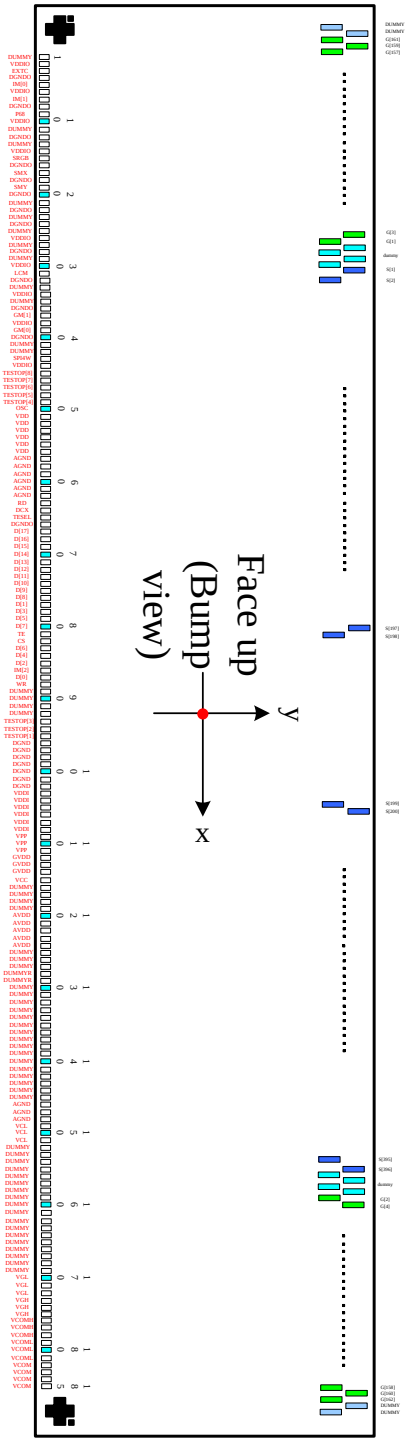
Chip Size: 10080um x 670um

Chip thickness: 280um(typ.)

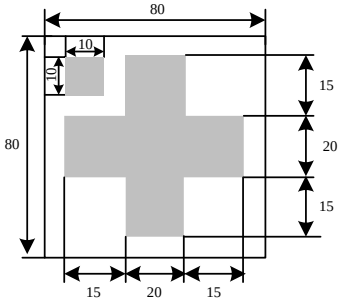
Pad Location: Pad Center.

Coordinate Origin: Chip center

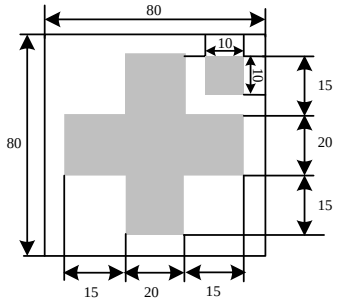
Au bump height: 12um(typ.)



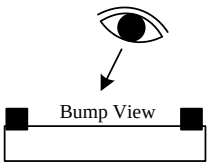
Alignment Marks



Alignment Mark:A1



Alignment Mark:A2



4. Interface setting

4.1. MCU interfaces

GC9102 provides the 8-/9-/16-/18-bit parallel system interface for 8080/6800 series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [2:0] and the bit formal per pixel color order is selected by IFPF [2:0] bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins P68, IM2, IM1 and IM0 as shown in the following table.

P68	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	1	0	0	8080 MCU 8-bit bus interface	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	1	0	1	8080 MCU 16-bit bus interface	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	1	1	0	8080 MCU 9-bit bus interface	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	1	1	1	8080 MCU 18-bit bus interface	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
-	0	-	-	serial interface	SCL,SDIO,CSX (D/CX)	
1	1	0	0	6800 MCU 8-bit bus interface	D[7:0]	D[7:0], WRX,RDX,CSX,D/CX
1	1	0	1	6800 MCU 16-bit bus interface	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
1	1	1	0	6800 MCU 9-bit bus interface	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
1	0	1	1	6800 MCU 18-bit bus interface	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
-	0	-	-	serial interface	SCL,SDIO,CSX (D/CX)	

4.1.2. 8080 Series Parallel Interface

GC9102 can be accessed via 8-/9-/16-/18-bit MCU 8080 series parallel interface. The chip select CSX (active low) is used to enable or disable GC9102 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D [17:0] is parallel data bus.

GC9102 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

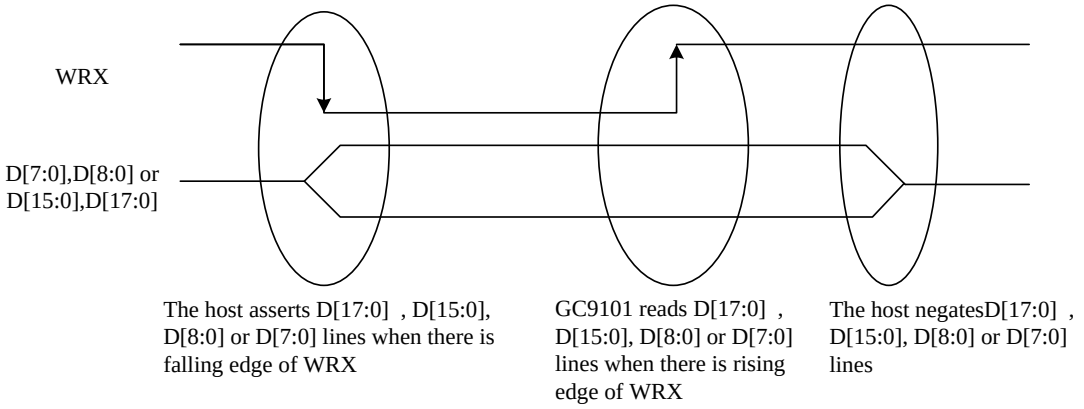
The 8080 series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080 Interface selection is done when P68 pin is low state (DGND level). Interface bus width can be selected by IM2, IM1, IM0.
The selection of 8080 series parallel interface is shown as the table in the following.

P68	IM2	IM1	IM0	MPU-interface	CSX	WRX	RDX	D/CX	Function
0	1	0	0	8-bit parallel	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	0	1	16-bit parallel	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	0	9-bit parallel	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	1	1	1	18-bit parallel	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

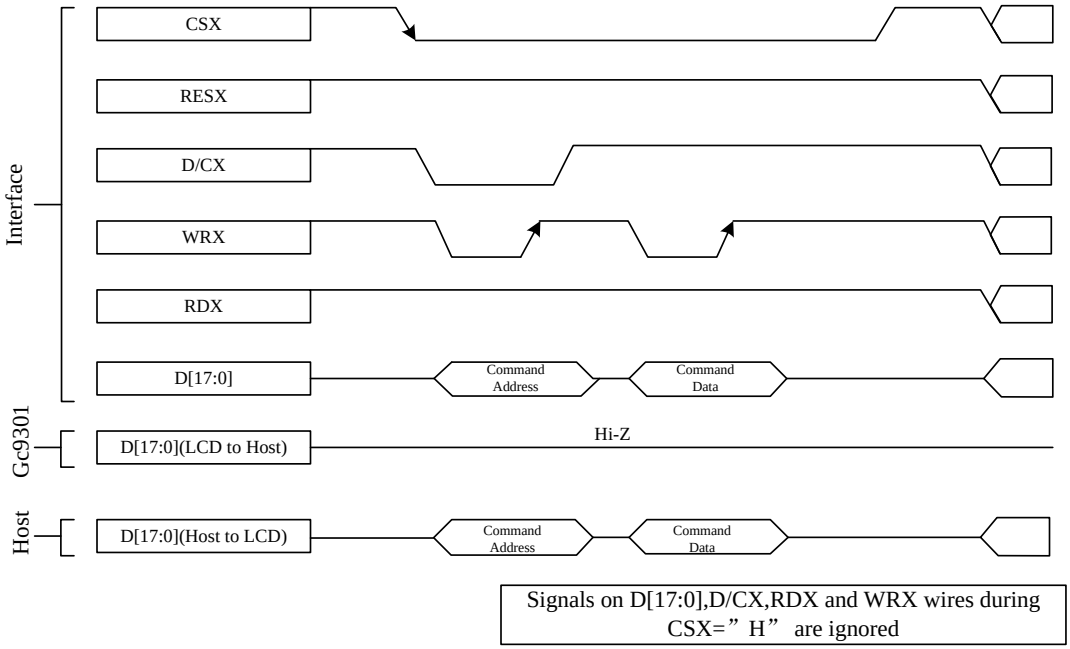
4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080 MCU interface.



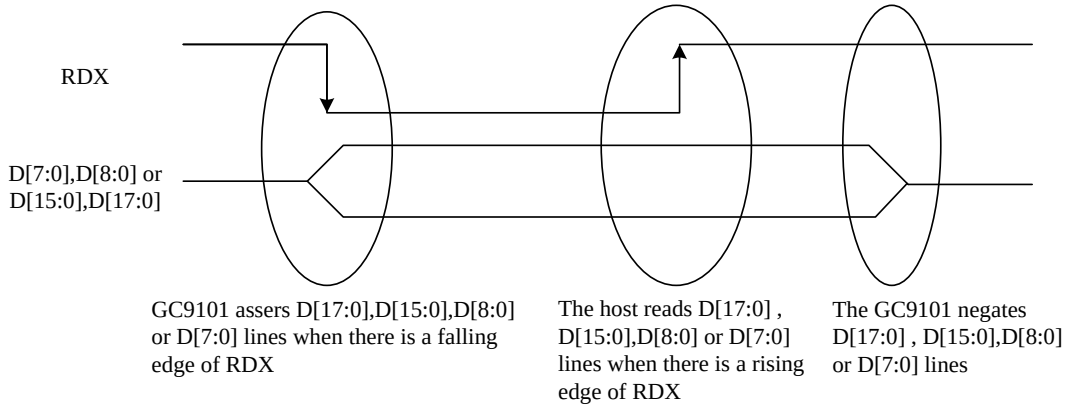
Note: WRX is an unsynchronized signal (It can be stopped)



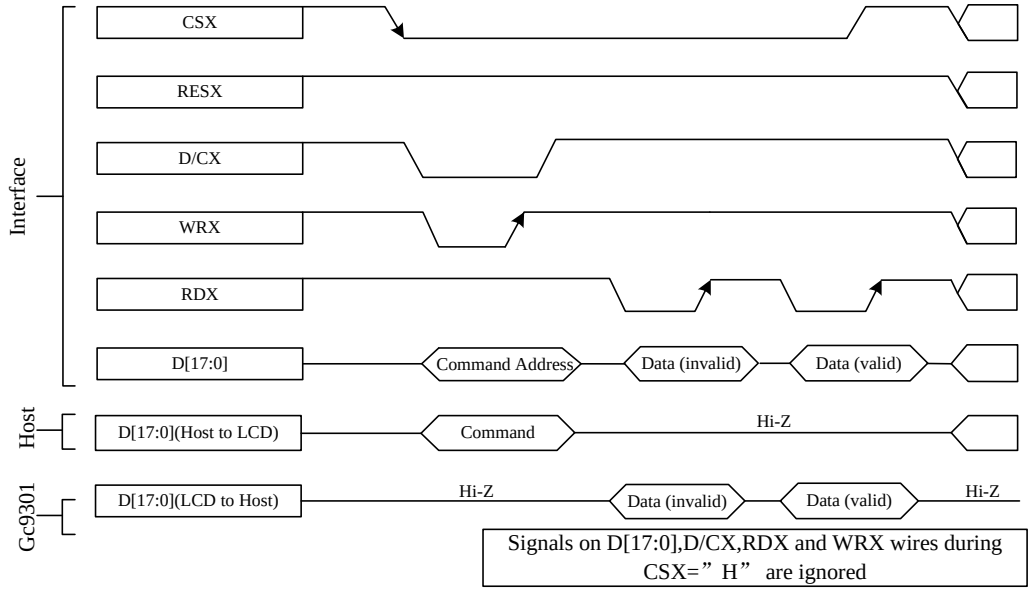
4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 6800 Series Parallel Interface

GC9102 can be accessed via 8-/9-/16-/18-bit MCU 6800 series parallel interface. The chip select CSX (active low) is used to enable or disable GC9102 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D [17:0] is parallel data bus.

GC9102 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

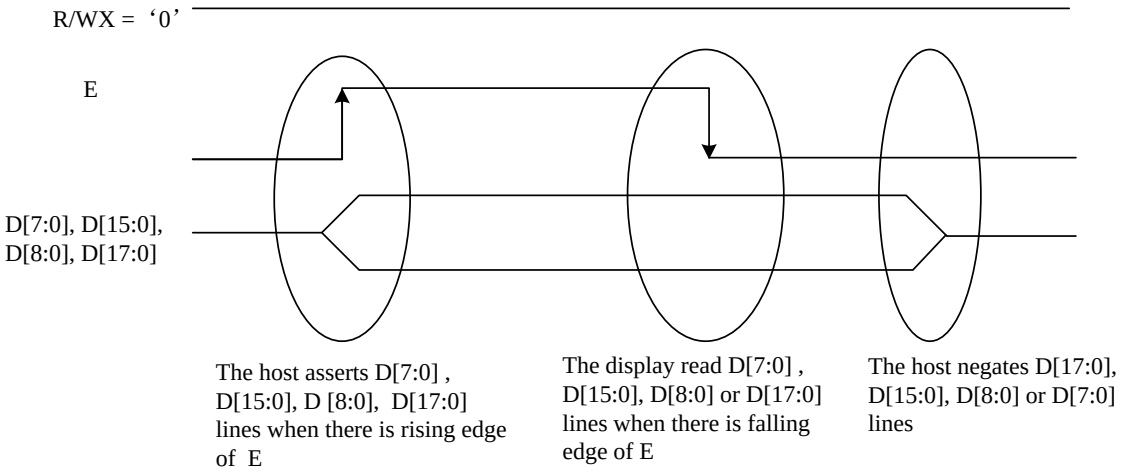
The 6800 series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 6800 Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.
The selection of 6800 series parallel interface is shown as the table in the following.

P68	IM2	IM1	IM0	MPU-interface	CSX	R/WX	E	D/CX	Function
1	1	0	0	8-bit parallel	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.
1	1	0	1	16-bit parallel	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.
1	1	1	0	9-bit parallel	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.
1	1	1	1	18-bit parallel	"L"	"L"	↓	"L"	Write command code.
					"L"	"H"	↓	"H"	Read internal status.
					"L"	"L"	↓	"H"	Write parameter or display data.
					"L"	"H"	↓	"H"	Reads parameter or display data.

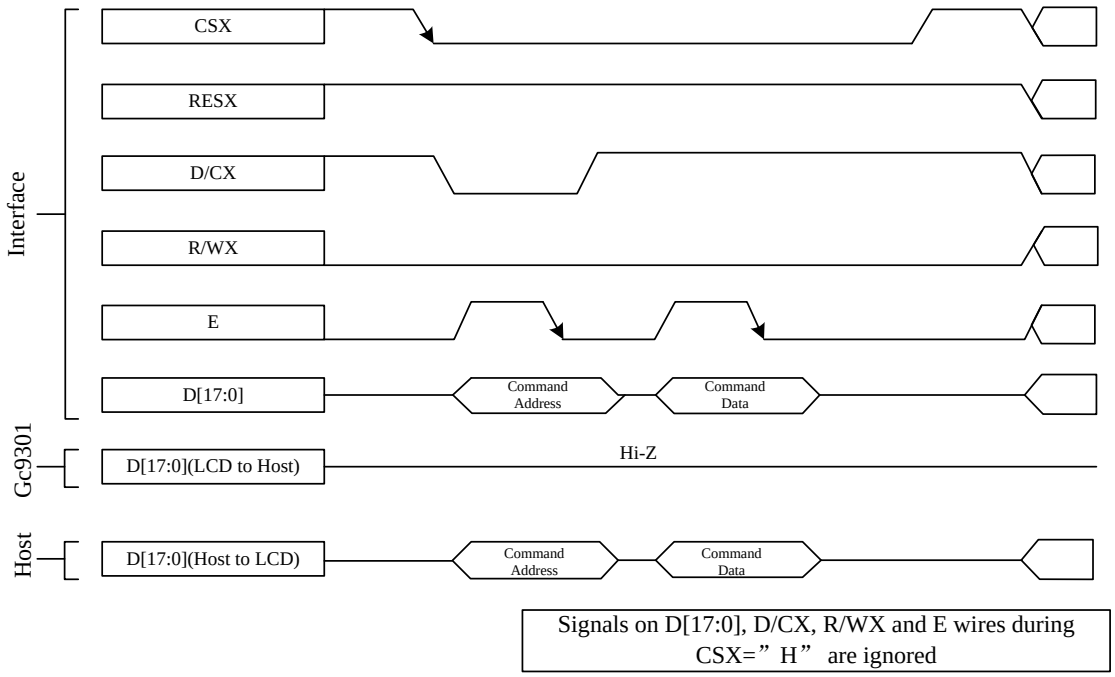
4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 6800 MCU interface.



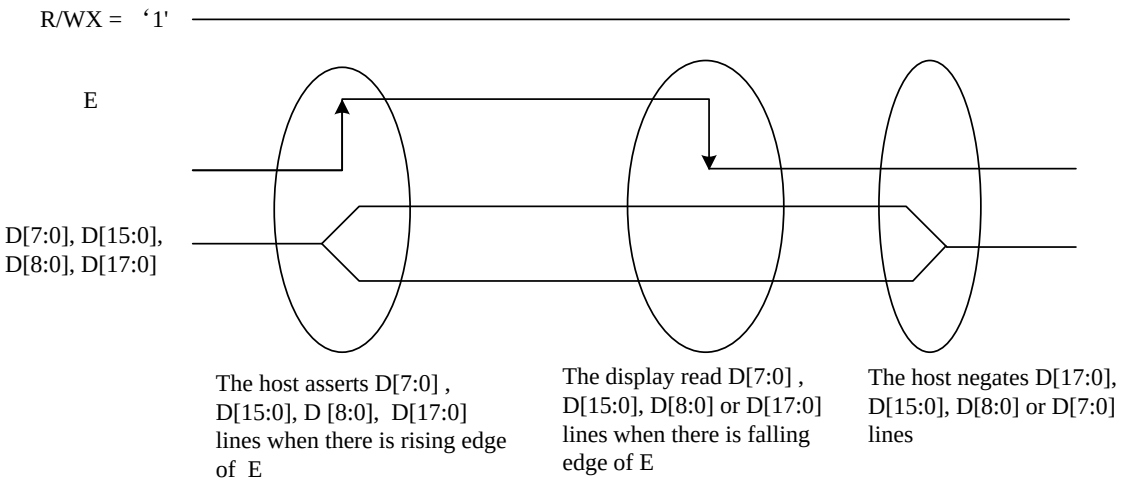
Note: E is an unsynchronized signal (It can be stopped)



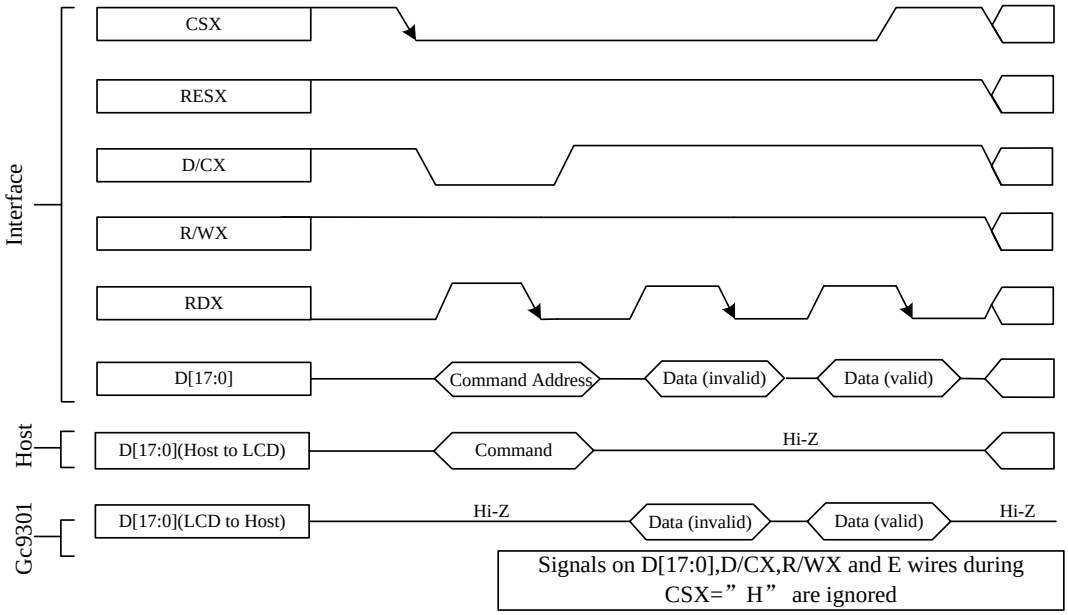
4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 6800 MCU interface.



Note: E is an unsynchronized signal (It can be stopped).



4.1.8. Serial Interface

The selection of interface is done by IM2 bit. Please refer to the Table in the following.

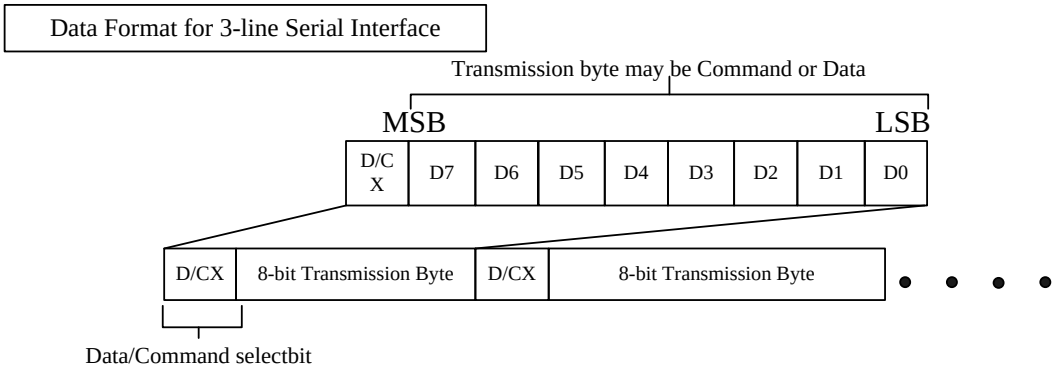
IM2	SPI4W	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	0	3-line serial interface	"L"	-		Read/Write command, parameter or display data.
0	1	4-line serial interface	"L"	"H/L"		Read/Write command, parameter or display data.

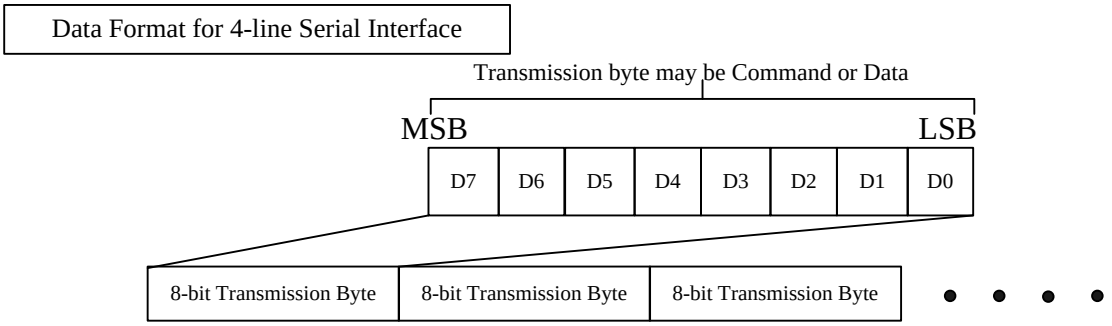
GC9102 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9102. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (D0/SDIO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (D0/SDIO) for data transmission. The data bus (D [17:1]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

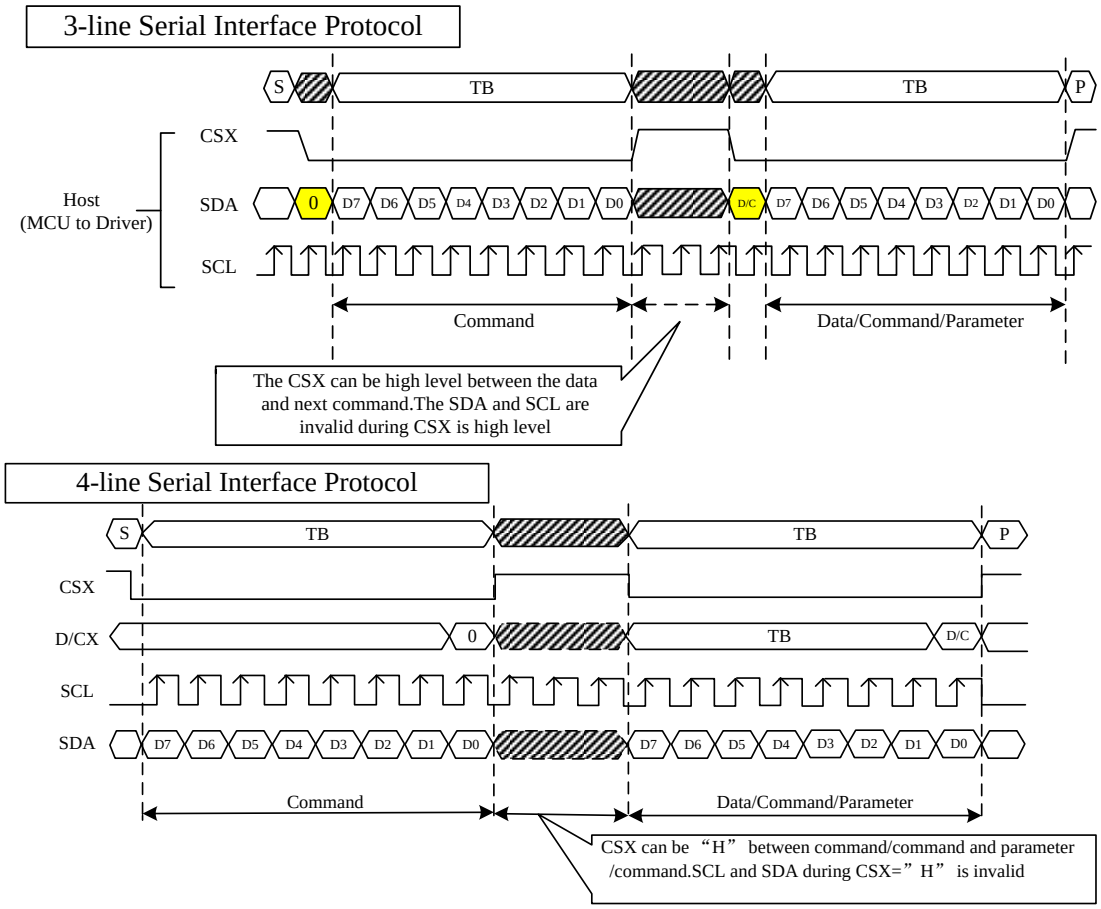
The write mode of the interface means that host writes commands or data to GC9102. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9102 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.





Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9102 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

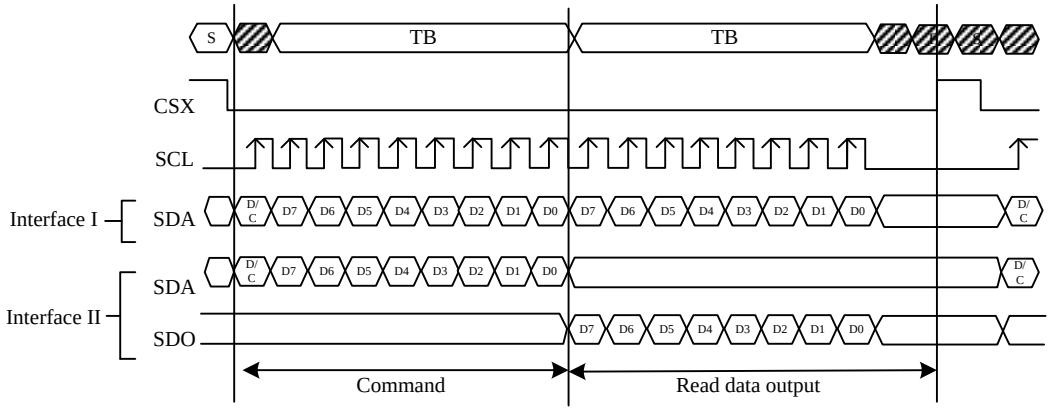


4.1.10. Read Cycle Sequence

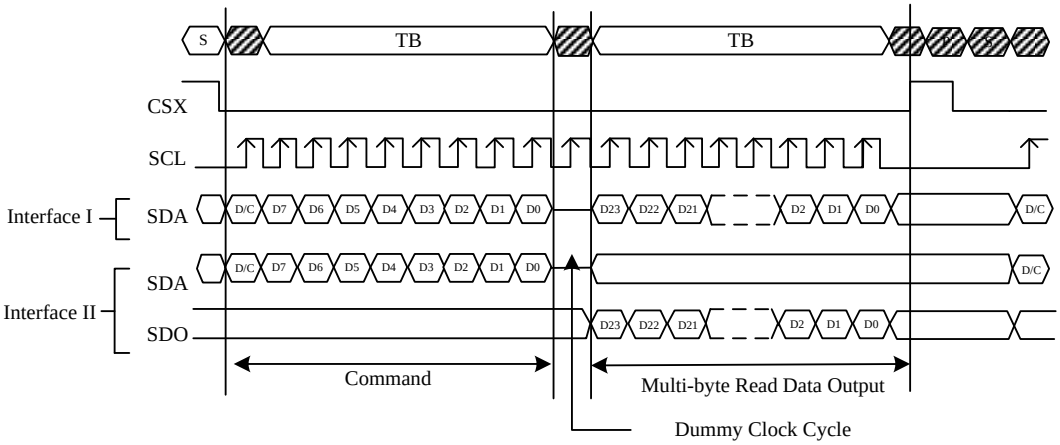
The read mode of interface means that the host reads register's parameter from GC9102. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9102 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol

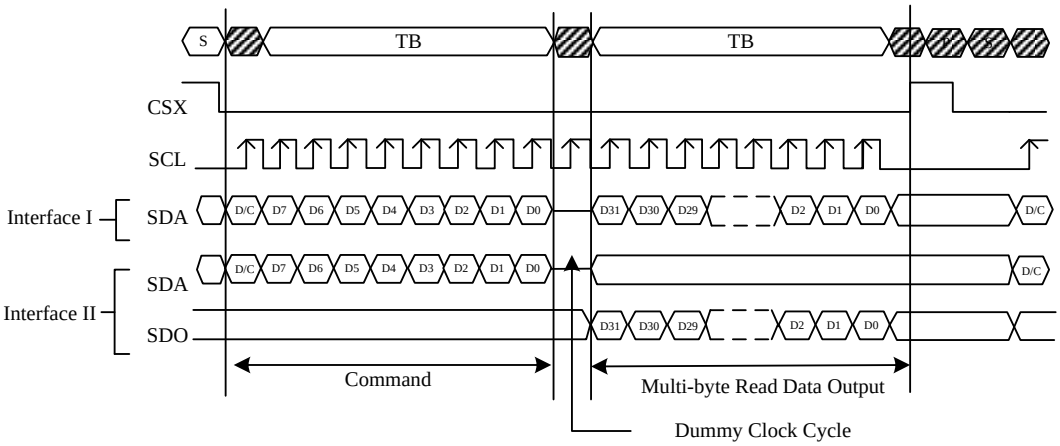
3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



3-wire Serial Protocol (for RDDID command:24-bit read)

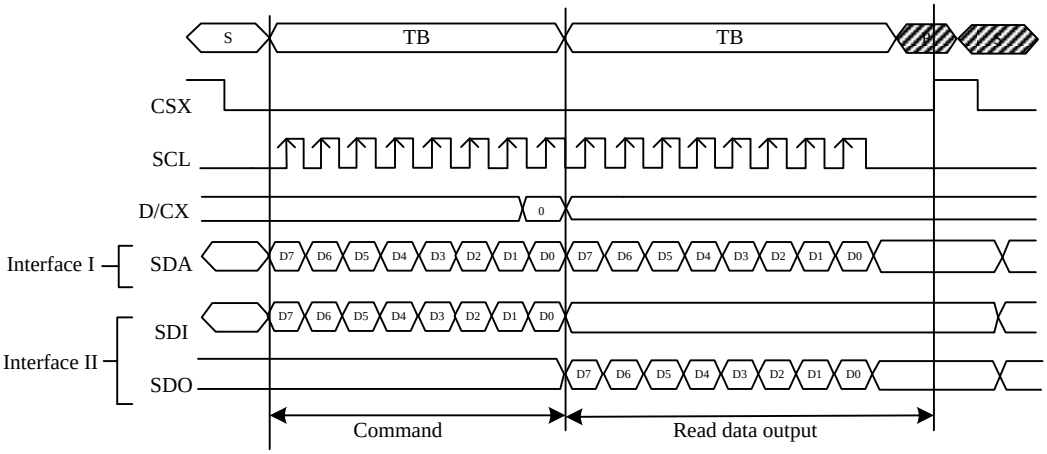


3-wire Serial Protocol (for RDDST command:32-bit read)

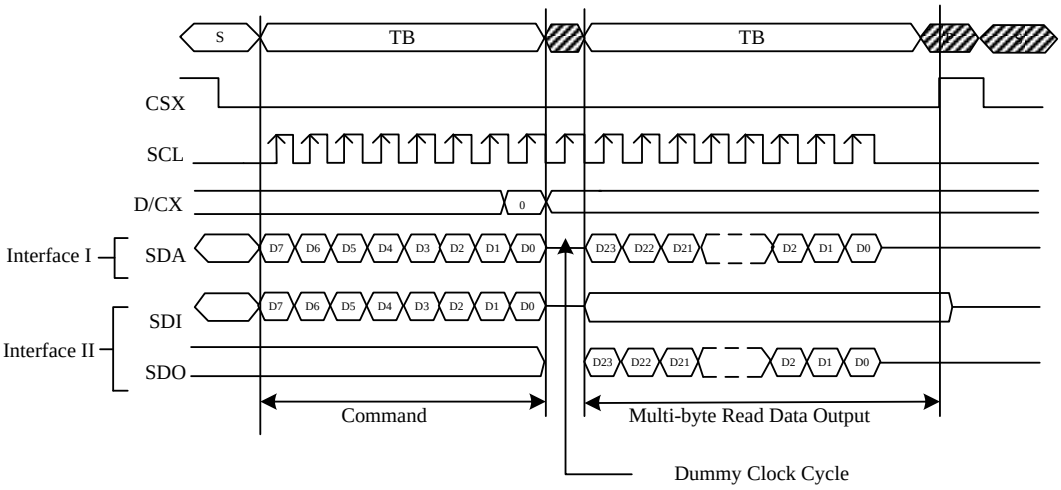


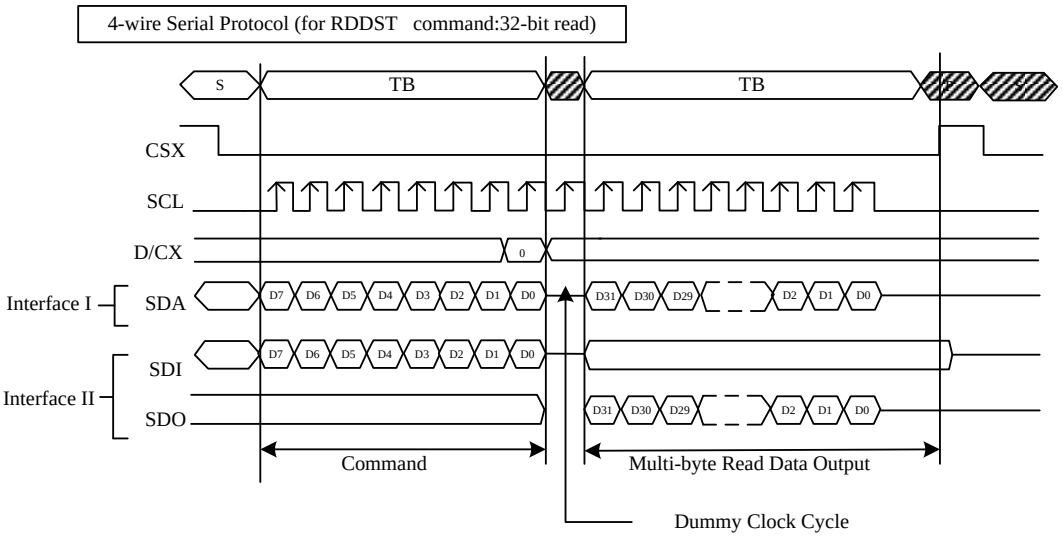
4-wire Serial Interface Protocol

4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



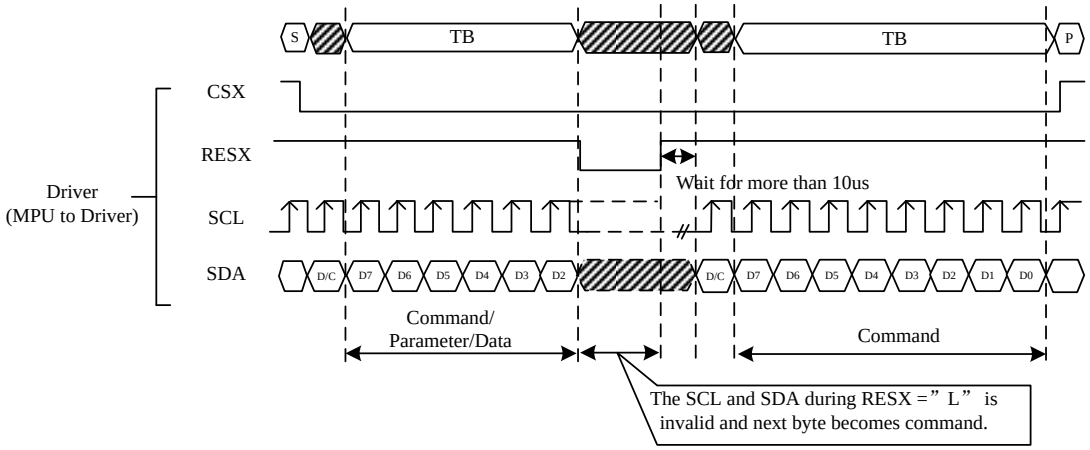
4-wire Serial Protocol (for RDDID command:24-bit read)



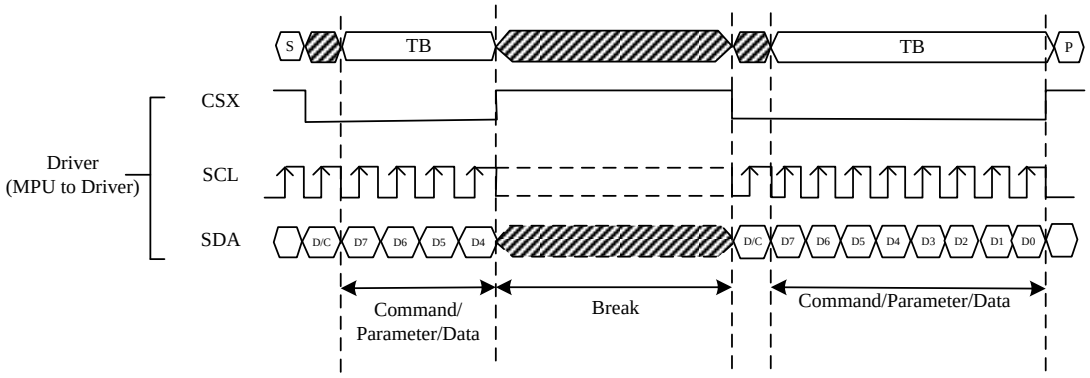

4-wire Serial Protocol (for RDDST command:32-bit read)
S
TB
TB
CSX
SCL
D/CX
0
Interface I
SDA
D7
D6
D5
D4
D3
D2
D1
D0
D31
D30
D29
D2
D1
D0
Interface II
SDI
SDO
Command
Multi-byte Read Data Output
Dummy Clock Cycle

4.1.11. Data Transfer Break and Recovery

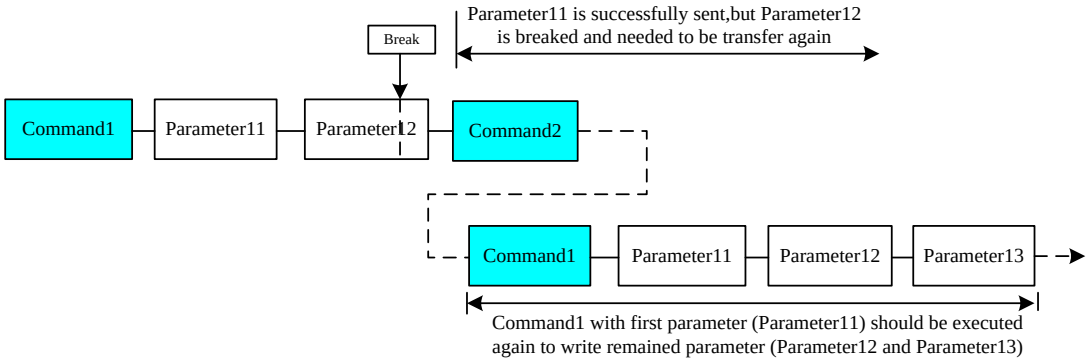
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



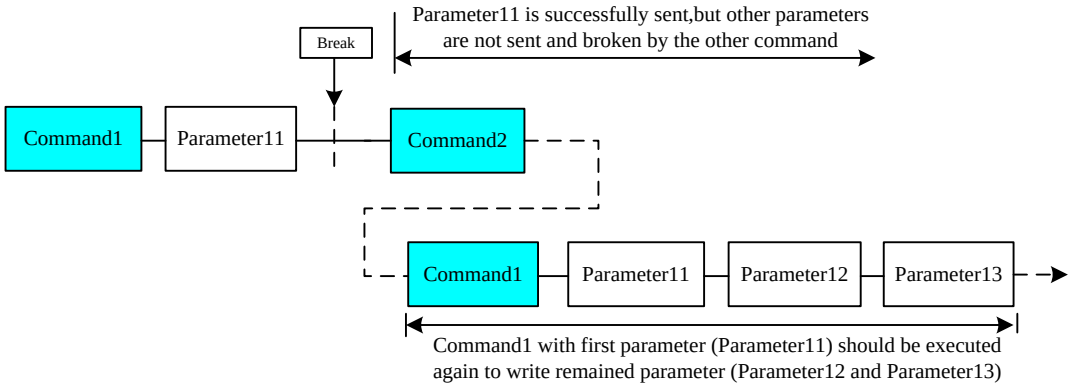
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



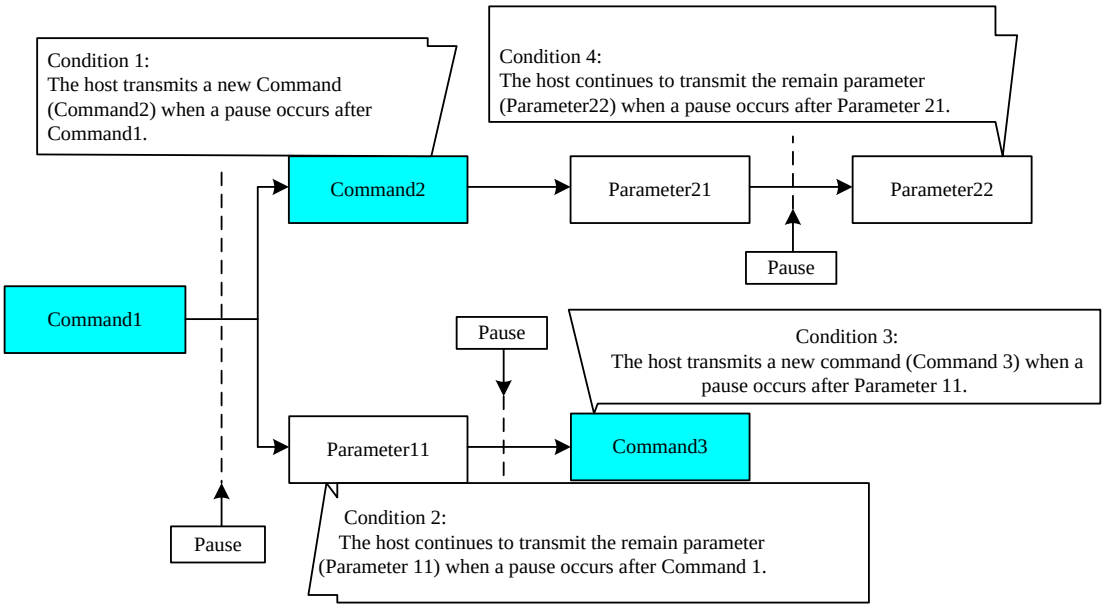
If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



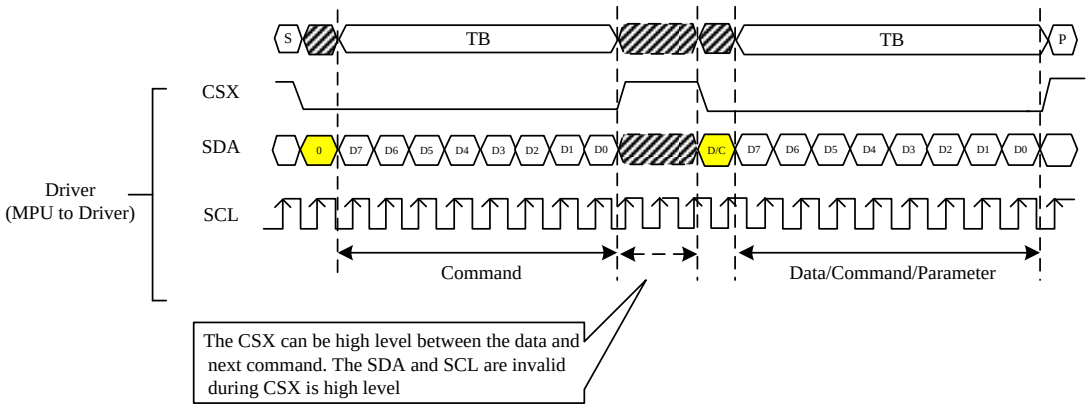
4.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9102 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

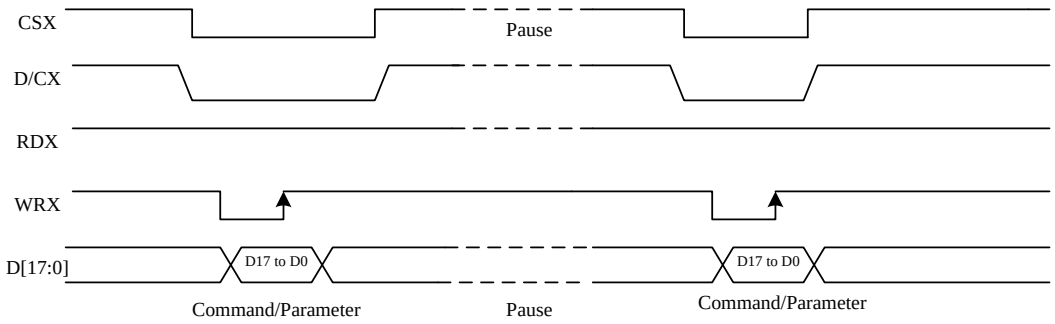
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter



4.1.13. Serial Interface Pause (3_wire)



4.1.14. Parallel Interface Pause

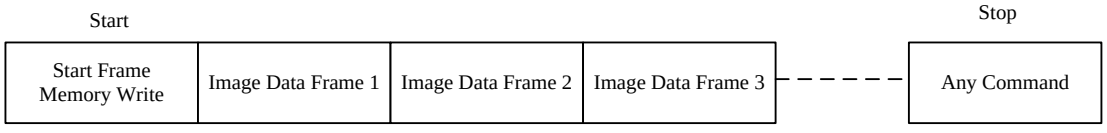


4.1.15. Data Transfer Mode

GC9102 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

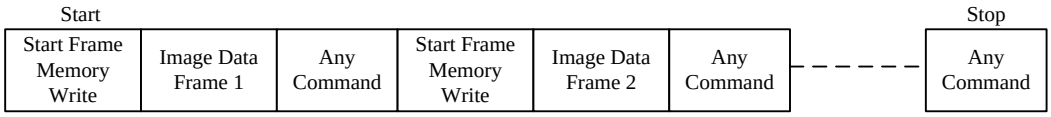
4.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



4.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



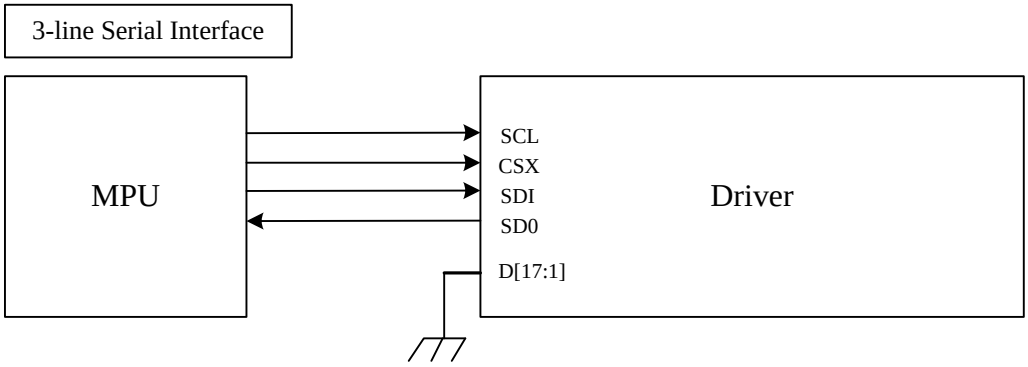
Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. Display Data Format

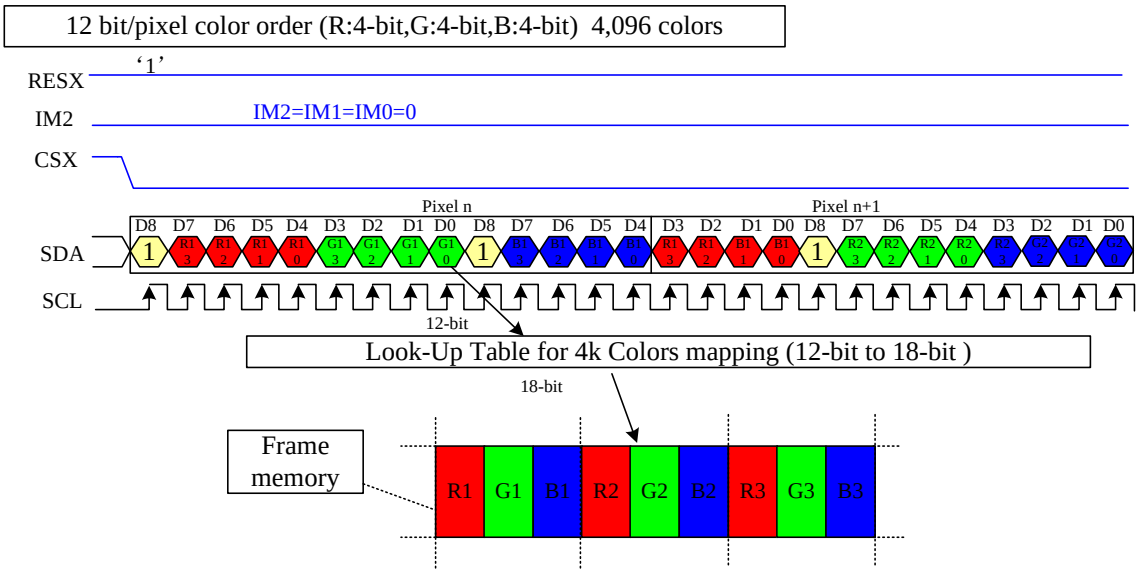
GC9102 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080 /6800 series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM2, IM1, IM0, P68 and SPI4W.

4.2.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9102 can be used by setting external pin as IM2 to “0” and SPI4W to “0” . The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.
-4k color, RGB 4, 4, 4, -bits input
-65k colors, RGB 5, 6, 5 -bits input
-262k colors, RGB 6, 6, 6 -bits input.

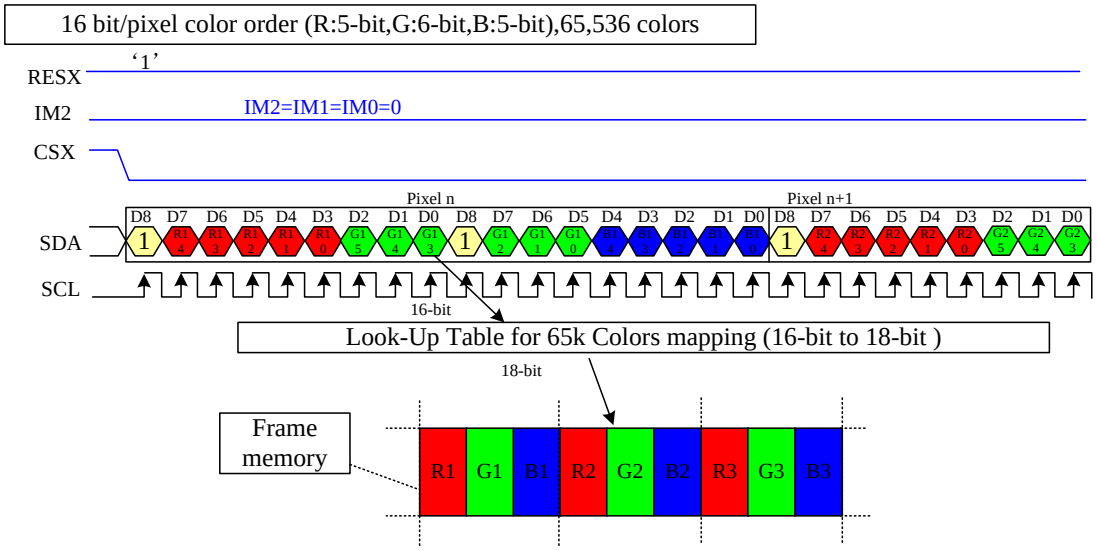


Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".

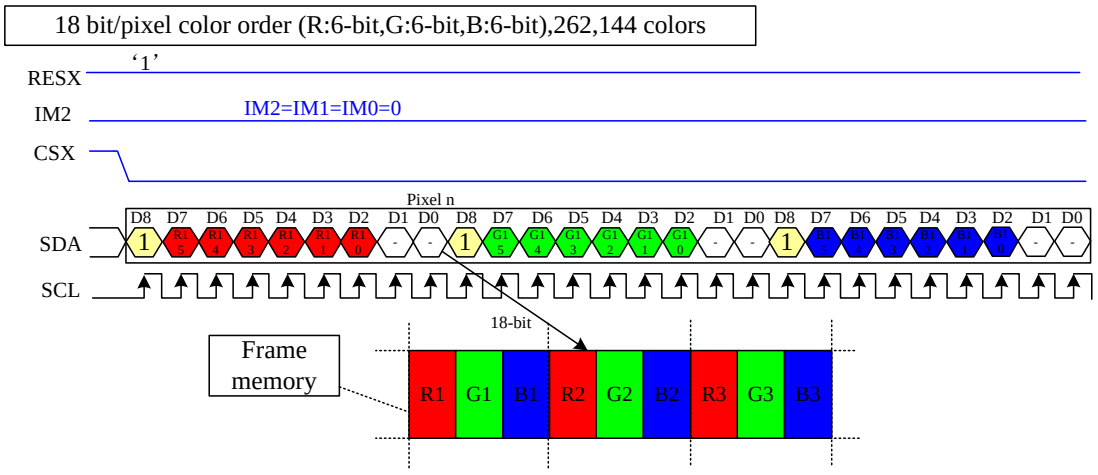


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.

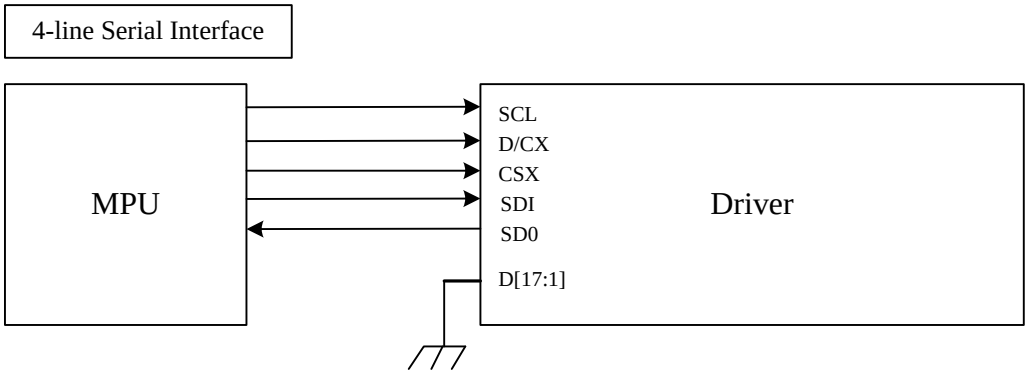
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

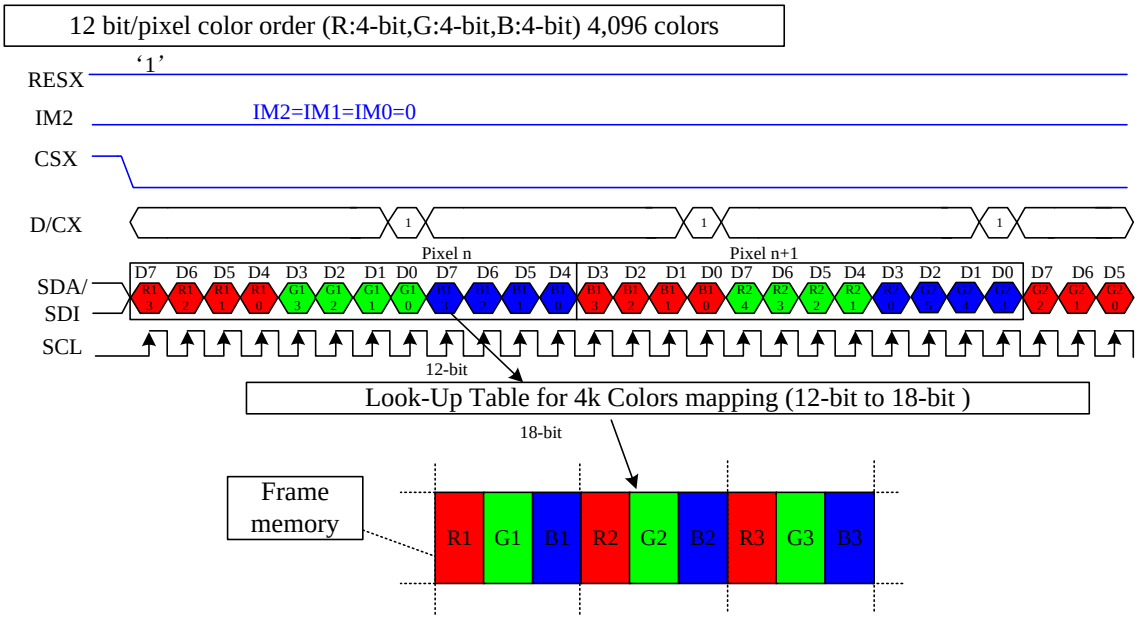
Note 4: '-'= don't care - Can be set "0" or "1".

4.2.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9102 can be used by setting external pin as IM2 to "0" and SPI4W to "1". The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.
-4Kk color, RGB 4, 4, 4 -bits input.
-65k colors, RGB 5, 6, 5 -bits input.
-262k colors, RGB 6, 6, 6 -bits input.

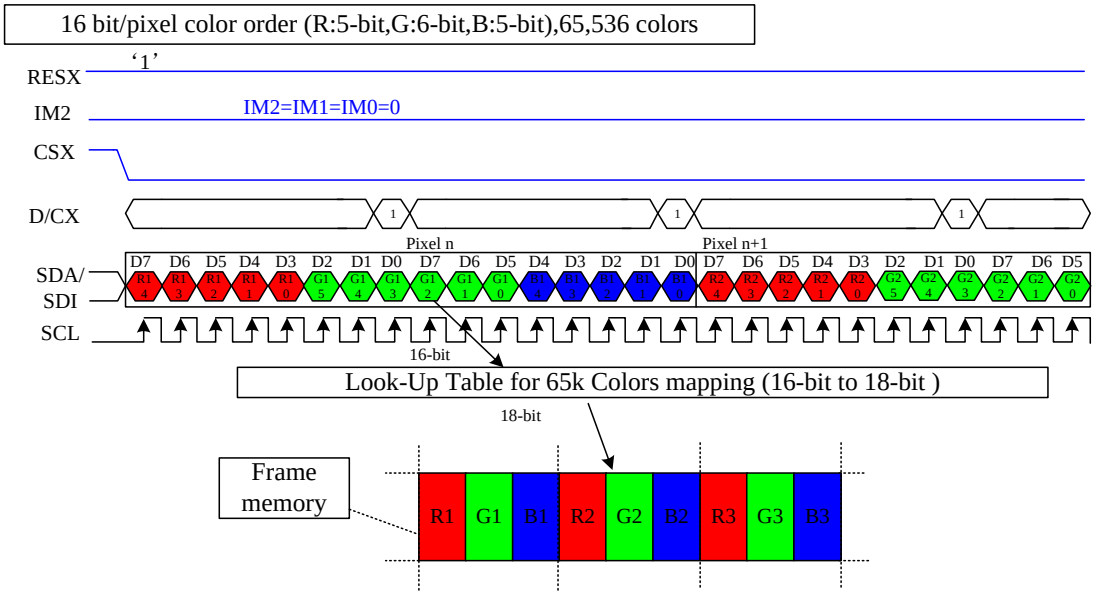


Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".

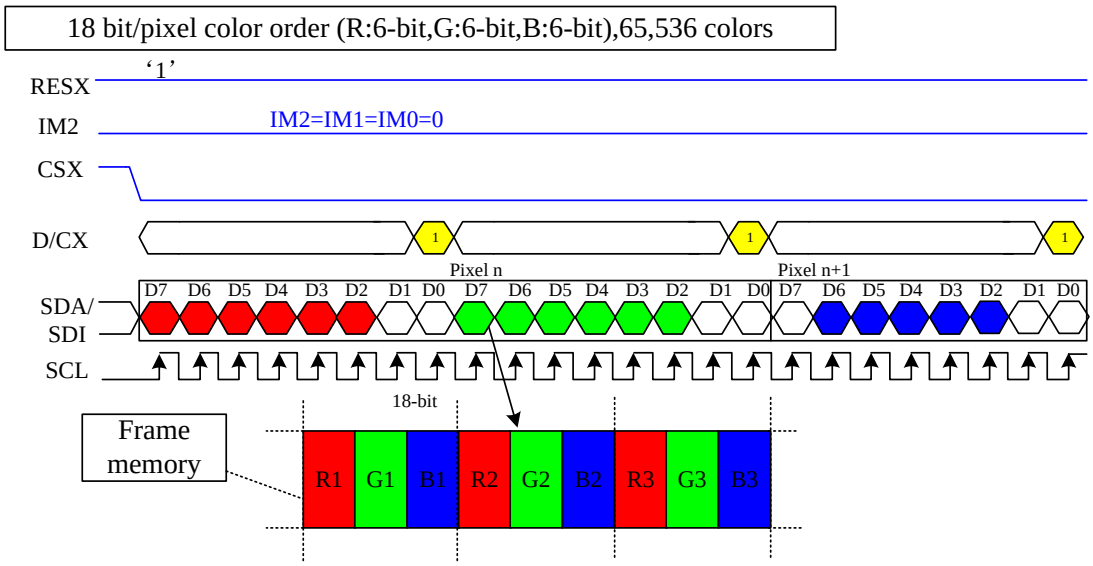


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.

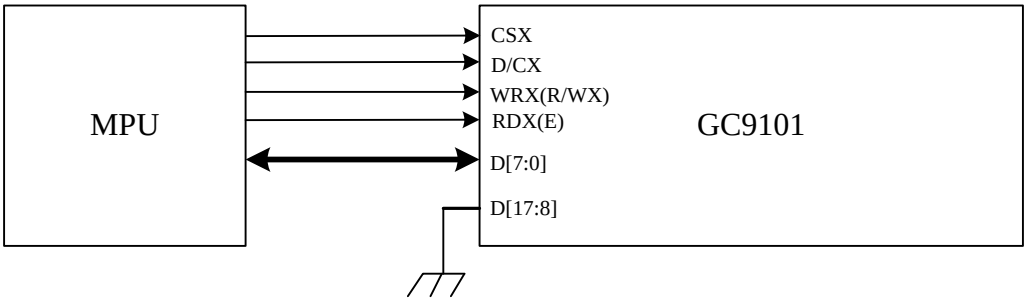
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".

4.2.3. 8-bit Parallel MCU Interface

The 8-bit parallel bus interface of GC9102 can be used by setting external pin as IM [2:0] to“000”.The following shown figure is the example of interface with 8-bits MCU system interface.



Different display data formats are available for three color depths supported by listed below.
- 4K-Color, RGB 4, 4, 4, -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

4K color: 12-bit/pixel (RGB 4-4-4 bits input)

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when IFPF [2:0] bits of 3Ah register are set to “011”.

Count	0	1	2	3	4	5	6	…
D/CX	0	1	1	1	1	1	1	…
D7	C7	0R3	0B3	1G3	2R4	2R3	3G3	…
D6	C6	0R2	0B2	1G2	2R3	2R2	3G2	…
D5	C5	0R1	0B1	1G1	2R2	2R1	3G1	…
D4	C4	0R0	0B0	1G0	2R1	2R0	3G0	…
D3	C3	0G3	1R3	1B3	2G3	3R3	3B3	…
D2	C2	0G2	1R2	1B2	2G2	3R2	3B2	…
D1	C1	0G1	1R1	1B1	2G1	3R1	3B1	…
D0	C0	0G0	1R0	1B0	2G0	3R0	3B0	…

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when IFPF [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…
D/CX	0	1	1	1	1	…
D7	C7	0R4	0G2	1R4	1G2	…
D6	C6	0R3	0G1	1R3	1G1	…
D5	C5	0R2	0G0	1R2	1G0	…
D4	C4	0R1	0B4	1R1	1B4	…
D3	C3	0R0	0B3	1R0	1B3	…
D2	C2	0G5	0B2	1G5	1B2	…
D1	C1	0G4	0B1	1G4	1B1	…
D0	C0	0G3	0B0	1G3	1B0	…

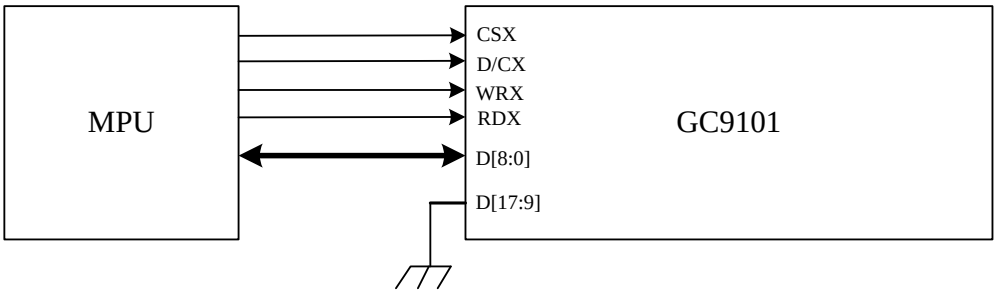
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when IFPF [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	4	5	6	…
D/CX	0	1	1	1	1	1	1	…
D7	C7	0R5	0G5	0B5	1R5	1G5	1B5	…
D6	C6	0R4	0G4	0B4	1R4	1G4	1B4	…
D5	C5	0R3	0G3	0B3	1R3	1G3	1B3	…
D4	C4	0R2	0G2	0B2	1R2	1G2	1B2	…
D3	C3	0R1	0G1	0B1	1R1	1G1	1B1	…
D2	C2	0R0	0G0	0B0	1R0	1G0	1B0	…
D1	C1							…
D0	C0							…

4.2.4. 9-bit Parallel MCU Interface

The 9-bit parallel bus interface of GC9102 can be selected by setting hardware pin IM [2:0] to "010". The following shown figure is the example of interface with MCU system interface.



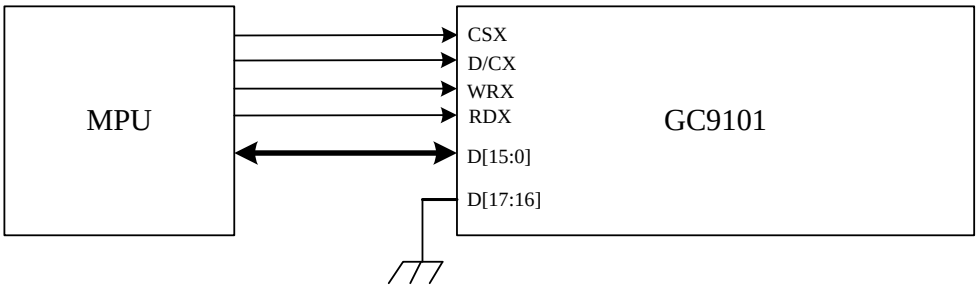
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There is 1 pixel (6 sub-pixels) display data is sent by two transfers, when IFPF [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	4	…
D/CX	0	1	1	1	1	…
D8		0R5	0G2	1R5	1G2	…
D7	C7	0R4	0G1	1R4	1G1	…
D6	C6	0R3	0G0	1R3	1G0	…
D5	C5	0R2	0B5	1R2	1B5	…
D4	C4	0R1	0B4	1R1	1B4	…
D3	C3	0R0	0B3	1R0	1B3	…
D2	C2	0G5	0B2	1G5	1B2	…
D1	C1	0G4	0B1	1G4	1B1	…
D0	C0	0G3	0B0	1G3	1B0	…

4.2.5. 16-bit Parallel MCU Interface

The system 16-bit parallel bus interface of GC9102 can be selected by setting hardware pin IM [2:0] to “001”.The following shown figure is the example of interface with MCU system interface.



Different display data format is available for two colors depth supported by listed below.
- 4K-Color, RGB 4, 4, 4 –bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

4K color: 12-bit/pixel (RGB 4-4-4 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when IFPF [2:0] bits of 3Ah register are set to “011”.

Count	0	1	2	3	…
D/CX	0	1	1	1	…
D15					
D14					
D13					
D12					
D11		0R3	1R3	2R3	…
D10		0R2	1R2	2R2	…
D9		0R1	1R1	2R1	…
D8		0R0	1R0	2R0	…
D7	C7	0G3	1G3	2G3	…
D6	C6	0G2	1G2	2G2	…
D3	C5	0G1	1G1	2G1	…
D4	C4	0G0	1G0	2G0	…
D3	C3	0B3	1B3	2B3	…
D2	C2	0B2	1B2	2B2	…
D1	C1	0B1	1B1	2B1	…
D0	C0	0B0	1B0	2B0	…

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when IFPF [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	…
D/CX	0	1	1	1	…
D15		0R4	1R4	2R4	…
D14		0R3	1R3	2R3	…
D13		0R2	1R2	2R2	…
D12		0R1	1R1	2R1	…
D11		0R0	1R0	2R0	…
D10		0G5	1G5	2G5	…
D9		0G4	1G4	2G4	…
D8		0G3	1G3	2G3	…
D7	C7	0G2	1G2	2G2	…
D6	C6	0G1	1G1	2G1	…
D5	C5	0G0	1G0	2G0	…
D4	C4	0B4	1B4	2B4	…
D3	C3	0B3	1B3	2B3	…
D2	C2	0B2	1B2	2B2	…
D1	C1	0B1	1B1	2B1	…
D0	C0	0B0	1B0	2B0	…

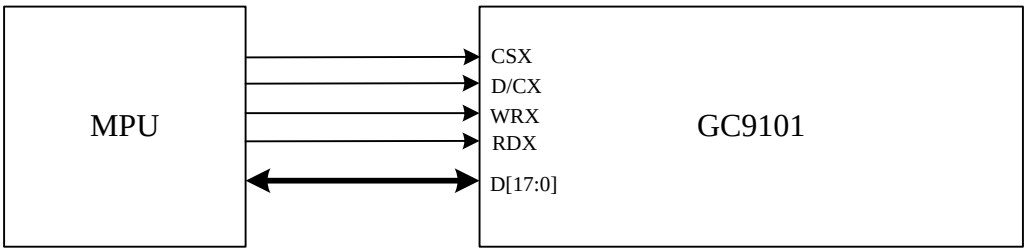
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

Two pixel (3 sub-pixels) display data is sent by 3 transfers when IFPF [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…
D/CX	0	1	1	1	…
D15		0R5	0B5	1G5	…
D14		0R4	0B4	1G4	…
D13		0R3	0B3	1G3	…
D12		0R2	0B2	1G2	…
D11		0R1	0B1	1G1	…
D10		0R0	0B0	1G0	…
D9					
D8					
D7	C7	0G5	1R5	1B5	…
D6	C6	0G4	1R4	1B4	…
D5	C5	0G3	1R3	1B3	…
D4	C4	0G2	1R2	1B2	…
D3	C3	0G1	1R1	1B1	…
D2	C2	0G0	1R0	1B0	…
D1	C1				
D0	C0				

4.2.6. 18-bit Parallel MCU Interface

The system 18-bit parallel bus interface of GC9102 can be selected by setting hardware pin IM [2:0] to “011”.The following shown figure is the example of interface with MCU system interface.



Different display data format is available for 3 colors depth supported by listed below.
- 4K-Color, RGB 4, 4, 4 –bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

4K color: 12-bit/pixel (RGB 4-4-4 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when IFPF [2:0] bits of 3Ah register are set to “011”.

Count	0	1	2	3	…
D/CX	0	1	1	1	…
D17					
D16					
D15					
D14					
D13					
D12					
D11		0R3	1R3	2R3	…
D10		0R2	1R2	2R2	…
D9		0R1	1R1	2R1	…
D8		0R0	1R0	2R0	…
D7	C7	0G3	1G3	2G3	…
D6	C6	0G2	1G2	2G2	…
D5	C5	0G1	1G1	2G1	…
D4	C4	0G0	1G0	2G0	…
D3	C3	0B3	1B3	2B3	…
D2	C2	0B2	1B2	2B2	…
D1	C1	0B1	1B1	2B1	…
D0	C0	0B0	1B0	2B0	…

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when IFPF [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	…
D/CX	0	1	1	1	…
D17					
D16					
D15		0R4	1R4	2R4	…
D14		0R3	1R3	2R3	…
D13		0R2	1R2	2R2	…
D12		0R1	1R1	2R1	…
D11		0R0	1R0	2R0	…
D10		0G5	1G5	2G5	…
D9		0G4	1G4	2G4	…
D8		0G3	1G3	2G3	…
D7	C7	0G2	1G2	2G2	…
D6	C6	0G1	1G1	2G1	…
D5	C5	0G0	1G0	2G0	…
D4	C4	0B4	1B4	2B4	…
D3	C3	0B3	1B3	2B3	…
D2	C2	0B2	1B2	2B2	…
D1	C1	0B1	1B1	2B1	…
D0	C0	0B0	1B0	2B0	…

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

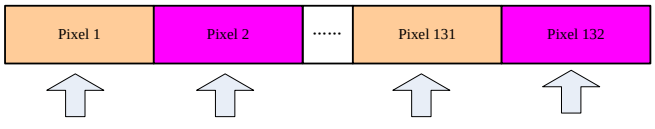
One pixel (3 sub-pixels) display data is sent by 1 transfer when IFPF [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…
D/CX	0	1	1	1	…
D17		0R5	1R5	2R5	…
D16		0R4	1R4	2R4	…
D15		0R3	1R3	2R3	…
D14		0R2	1R2	2R2	…
D13		0R1	1R1	2R1	…
D12		0R0	1R0	2R0	…
D11		0G5	1G5	2G5	…
D10		0G4	1G4	2G4	…
D9		0G3	1G3	2G3	…
D8		0G2	1G2	2G2	…
D7	C7	0G1	1G1	2G1	…
D6	C6	0G0	1G0	2G0	…
D5	C5	0B5	1B5	2B5	…
D4	C4	0B4	1B4	2B4	…
D3	C3	0B3	1B3	2B3	…
D2	C2	0B2	1B2	2B2	…
D1	C1	0B1	1B1	2B1	…
D0	C0	0B0	1B0	2B0	…

5. Function Description

5.1. Display data GRAM mapping

5.1.1. 132RGBx162 resolution (GM = “00”)



Gate Out	Source Out		S1	S2	S3	S4	S5	S6	……	S391	S392	S393	S394	S395	S396		
			RGB = 0		RGB = 1	RGB = 0		RGB = 1	……	RGB = 0		RGB = 1	RGB = 0		RGB = 1		
	RA								……							SA	
	MY= ‘0’	MY= ‘1’							……							ML= ‘0’	ML= ‘1’
1	0	161	R0	G0	B0	R1	G1	B1	……	R131	G131	B131	R132	G132	B132	0	161
2	1	160							……							1	160
3	2	159							……							2	159
4	3	158							……							3	158
5	4	157							……							4	157
6	5	156							……							5	156
7	6	155							……							6	155
8	7	154							……							7	154
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
155	154	7							……							154	7
156	155	6							……							155	6
157	156	5							……							156	5
158	157	4							……							157	4
159	158	3							……							158	3
160	159	2							……							159	2
161	160	1							……							160	1
162	161	0							……							161	0
	CA	MX= ‘0’	0			1			……	130			131				
		MX= ‘1’	131			130			……	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

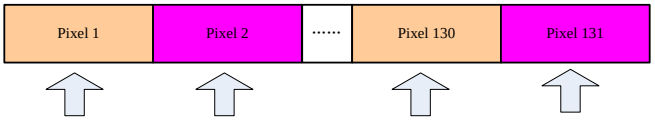
MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.1.2. 132RGBx132 resolution (GM = “01”)



Gate Out	Source Out		S1	S2	S3	S4	S5	S6	……	S391	S392	S393	S394	S395	S396		
			RGB = 0		RGB = 1	RGB = 0		RGB = 1	……	RGB = 0		RGB = 1	RGB = 0		RGB = 1		
	RA								……							SA	
	MY= ‘0’	MY= ‘1’							……							ML= ‘0’	ML= ‘1’
1	0	131	R0	G0	B0	R1	G1	B1	……	R130	G130	B130	R131	G131	B131	0	131
2	1	130							……							1	130
3	2	129							……							2	129
4	3	128							……							3	128
5	4	127							……							4	127
6	5	126							……							5	126
7	6	125							……							6	125
8	7	124							……							7	124
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
125	124	7							……							124	7
126	125	6							……							125	6
127	126	5							……							126	5
128	127	4							……							127	4
129	128	3							……							128	3
130	129	2							……							129	2
131	130	1							……							130	1
132	131	0							……							131	0
	CA	MX= ‘0’	0			1			……	130			131				
		MX= ‘1’	131			130			……	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.1.3. 128RGBx160 resolution (GM = “11”)

Gate Out	Source Out		S7	S8	S9	S10	S11	S12	……	S385	S386	S387	S388	S389	S390		
			RGB = 0		RGB = 1	RGB = 0		RGB = 1	……	RGB = 0		RGB = 1	RGB = 0		RGB = 1		
	RA								……							SA	
	MY= ‘0’	MY= ‘1’							……							ML= ‘0’	ML= ‘1’
2	0	159	R0	G0	B0	R1	G1	B1	……	R126	G126	B126	R127	G127	B127	0	159
3	1	158							……							1	158
4	2	157							……							2	157
5	3	156							……							3	156
6	4	155							……							4	155
7	5	154							……							5	154
8	6	153							……							6	153
9	7	152							……							7	152
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
154	152	7							……							152	7
155	153	6							……							153	6
156	154	5							……							154	5
157	155	4							……							155	4
158	156	3							……							156	3
159	157	2							……							157	2
160	158	1							……							158	1
161	159	0							……							159	0
	CA	MX= ‘0’	0			1			……	126			127				
		MX= ‘1’	127			126			……	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

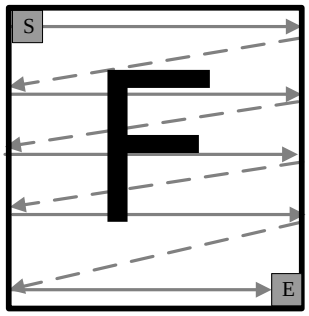
ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

5.2. Address Counter (AC) of GRAM

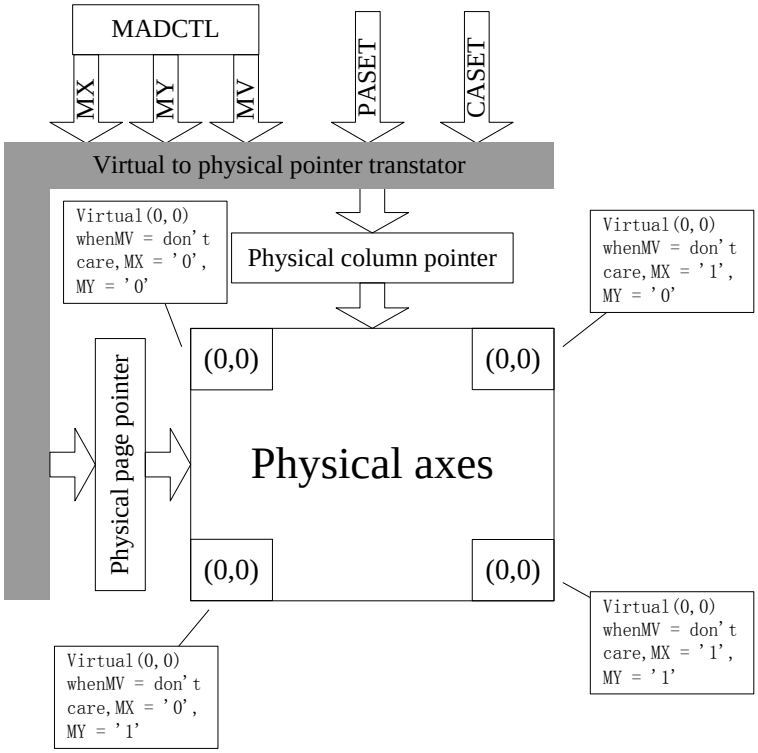
The GC9102 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.
Image data sending order from host and data stream update as shown in the following figure



The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

Image data writing control:



For each image orientation, the controls for the column and page counters apply as below:

condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start column"	Return to "Start Page"

5.2.1 132RGBx162 (GM == '00')

CASET and PASET control for physical column/page pointers:

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161 - Physical Page Pointer)
0	1	0	Direct to (131 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (131 - Physical Column Pointer)	Direct to (161 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (131 - Physical Column Pointer)
1	1	1	Direct to (161 - Physical Page Pointer)	Direct to (131 - Physical Column Pointer)

5.2.1. 132RGBx132 (GM == '01')

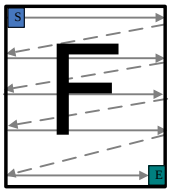
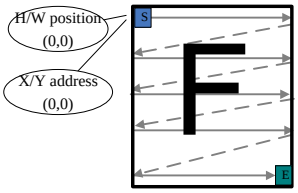
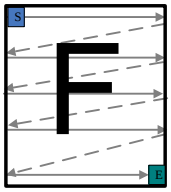
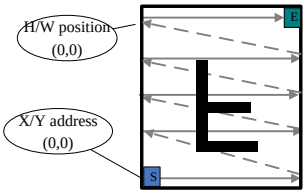
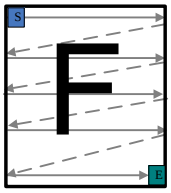
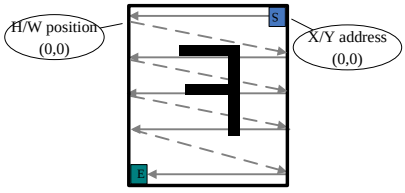
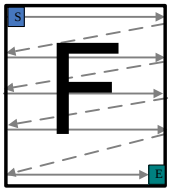
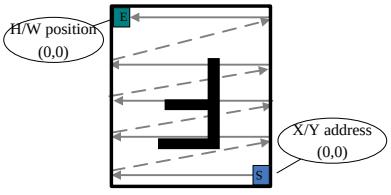
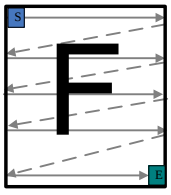
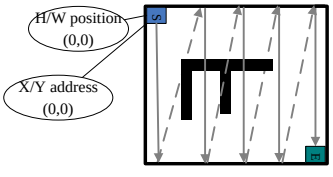
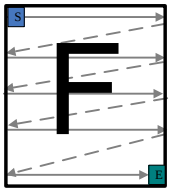
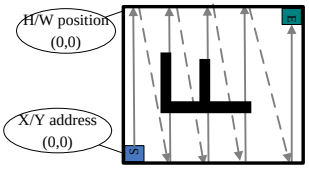
MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (131 - Physical Page Pointer)
0	1	0	Direct to (131 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (131 - Physical Column Pointer)	Direct to (131 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (131 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (131 - Physical Column Pointer)
1	1	1	Direct to (131 - Physical Page Pointer)	Direct to (131 - Physical Column Pointer)

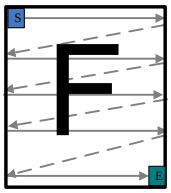
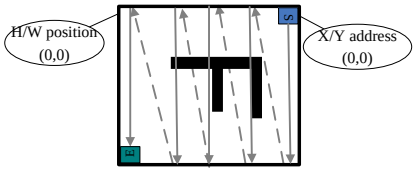
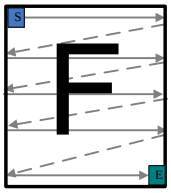
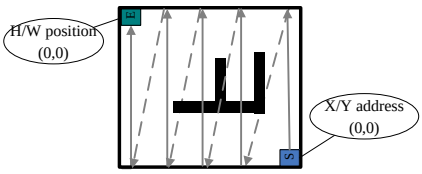
5.2.2. 128RGBx160 (GM == '11')

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159 - Physical Page Pointer)
0	1	0	Direct to (127 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (131 - Physical Column Pointer)	Direct to (159 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (127 - Physical Column Pointer)
1	1	1	Direct to (159 - Physical Page Pointer)	Direct to (127 - Physical Column Pointer)

5.2.3. Frame Data Write Direction According to the MADCTL Parameters (MV, MX and MY)

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Display data direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
normal	0	0	0		
Y-invert	0	0	1		
X-ivert	0	1	0		
Y-invert X-invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-invert	1	0	1		

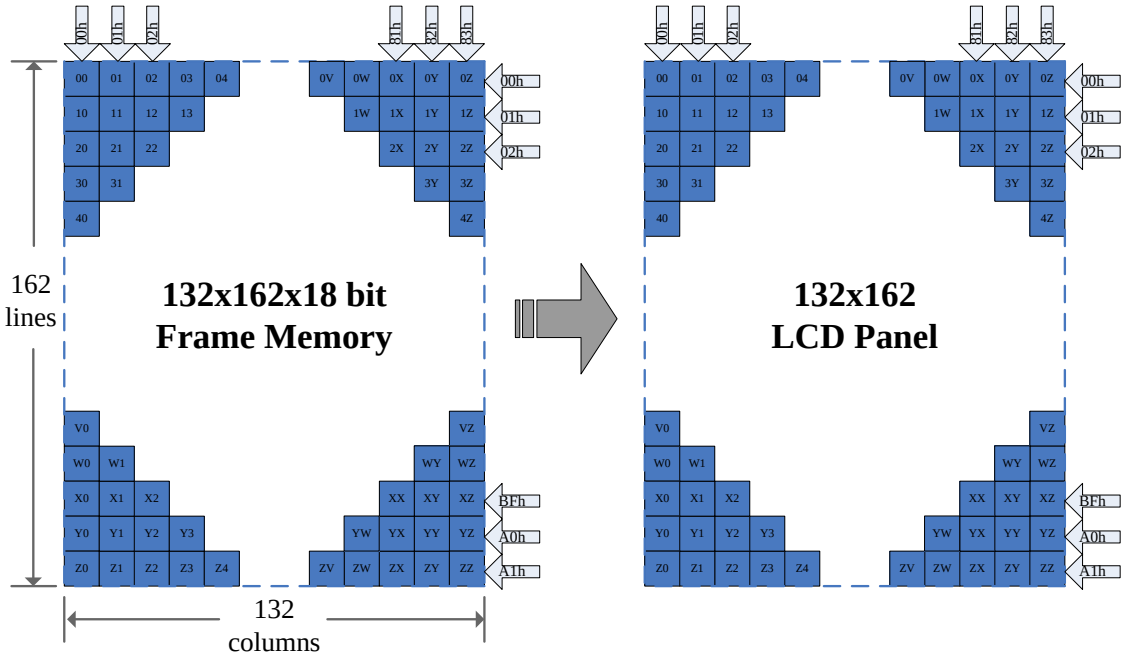
X-Y exchange X-invert	1	1	0		
X-Y exchange Y-invert X-invert	1	1	1		

5.3. GRAM to display address mapping

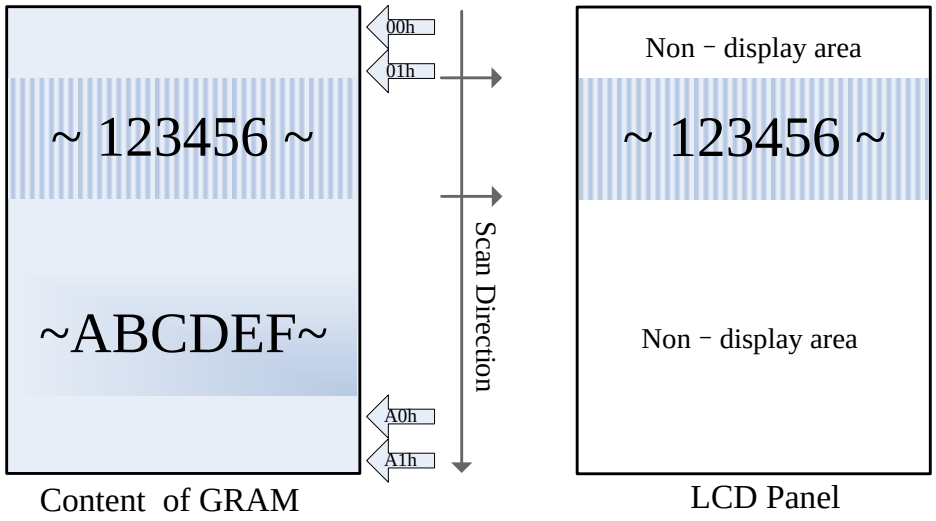
GC9102 supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

5.3.1. Normal display on or partial mode on, vertical scroll off

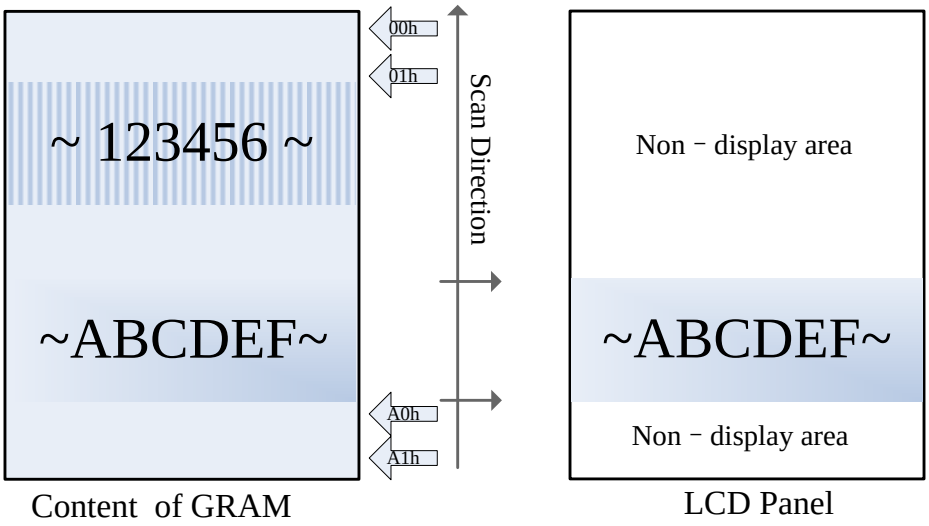
In this mode, content of the frame memory within an area where column pointer is 0000h to 0083h and page pointer is 0000h to 00A1h is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)



Example1:
(1) Partial mode on (setting 12h)
(2) SR [15:0] =’20d’, ER [15:0] =’50d’, MADCTL’s **B4(ML)= ‘0’**.

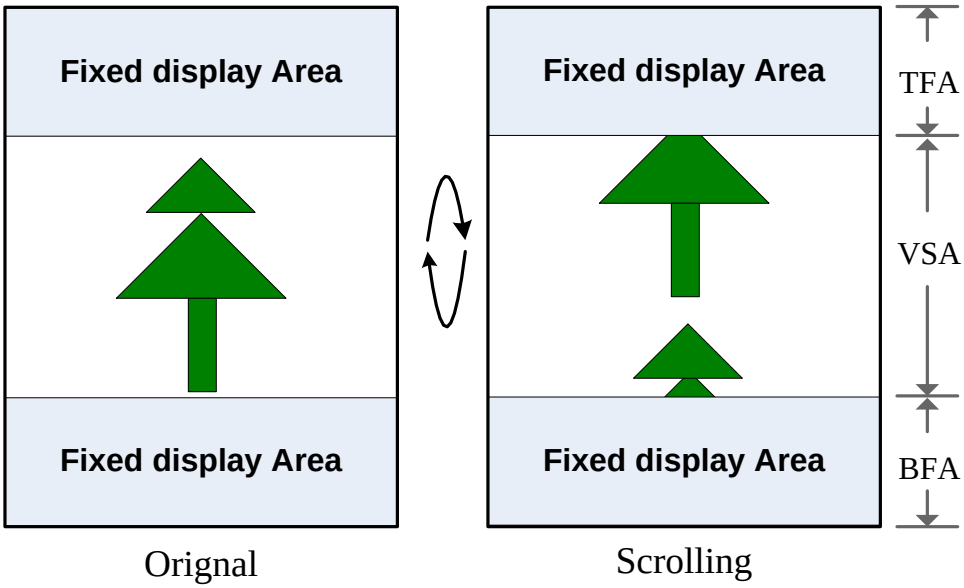


Example2:
(1) Partial mode on (setting 12h)
(2) SR [15:0] =’20d’, ER [15:0] =’50d’, MADCTL’s **B4(ML)= ‘1’**.



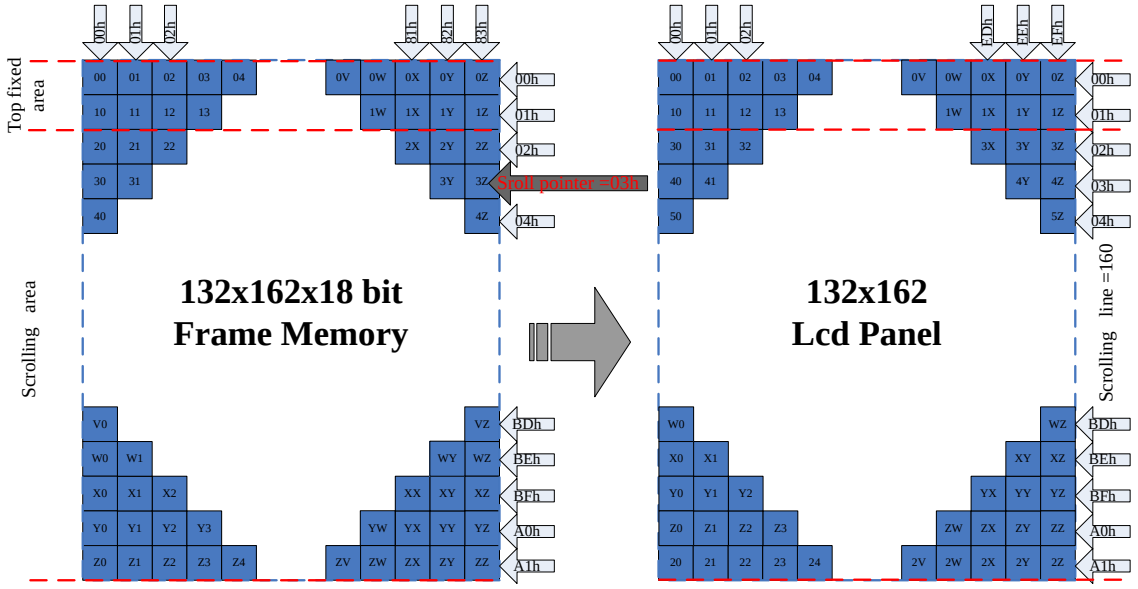
5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).

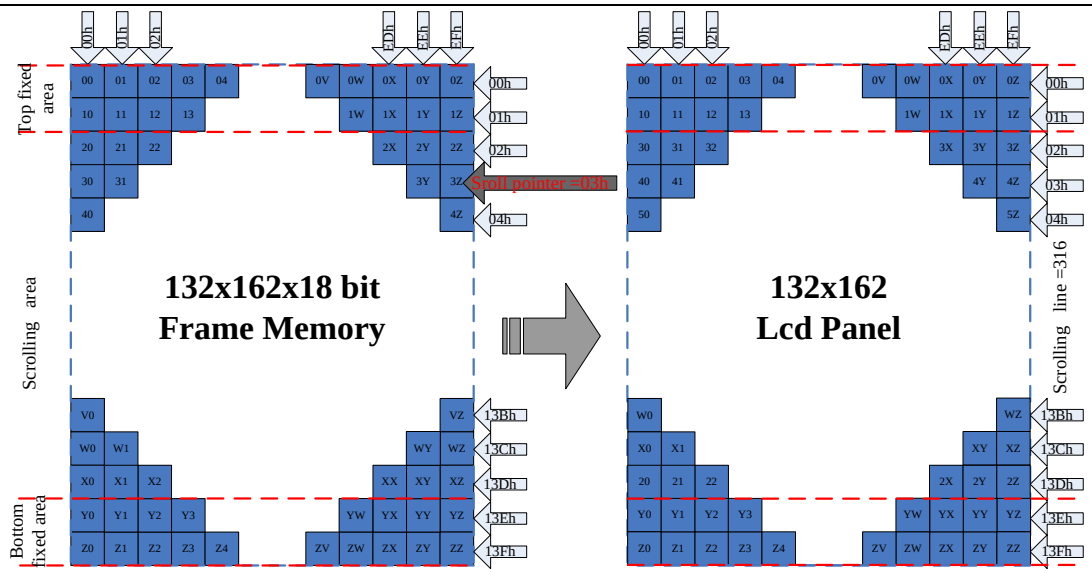


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =162. In this case, scrolling is applied as shown below.

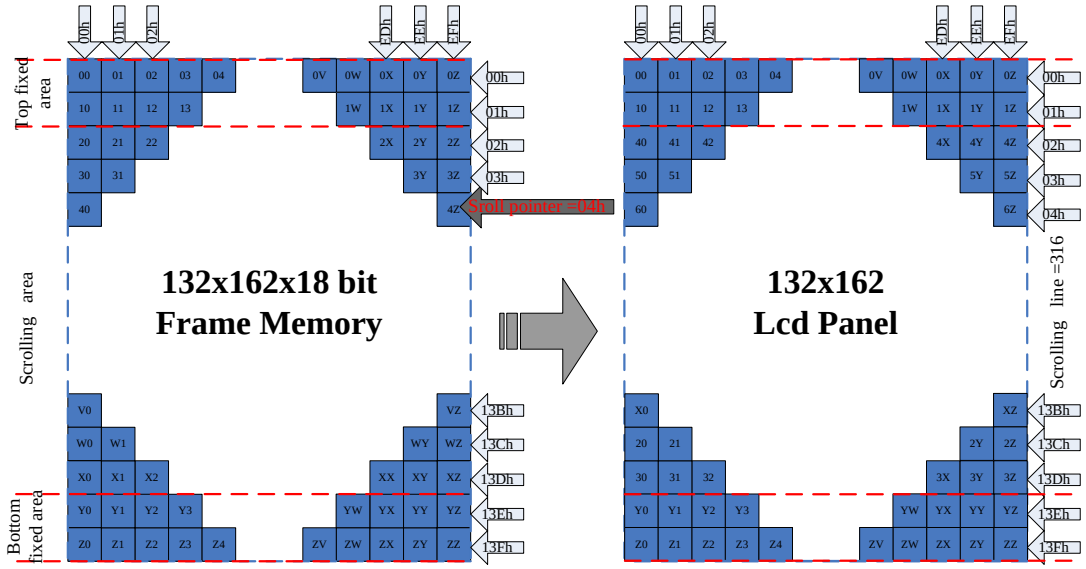
Example 1 .TFA=’2d’, VSA=’160d’, BFA=’0d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 1:



Example 2 .TFA=’2d’, VSA=’158d’, BFA=’2d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 2:



Example 3 .TFA=’2d’, VSA=’158d’, BFA=’2d’, VSP=’4d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 3:



Vertical scroll example

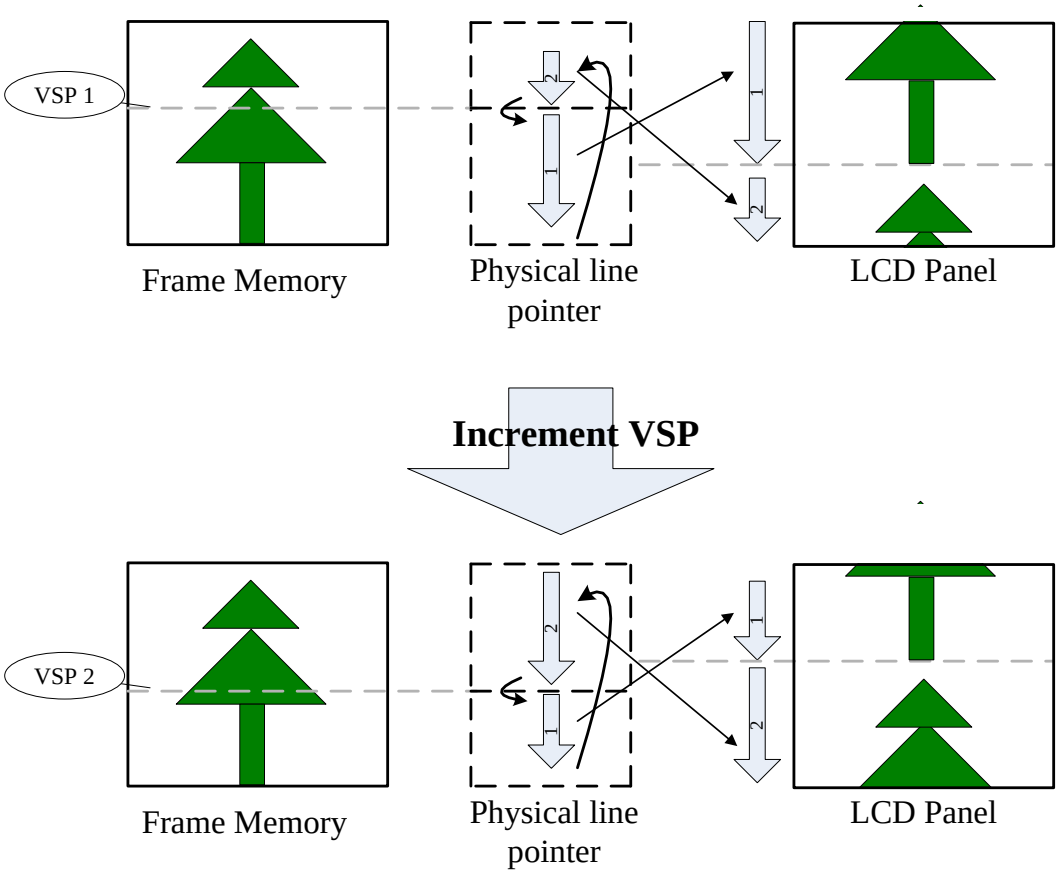
There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits and **VSP** bits

Case 1: TFA + VSA + BFA ≠ ‘162d’

N/A: Do not set TFA + VSA + BFA ≠ ‘162d’. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = ‘162d’ (Scrolling)

Example (1) When TFA=’0d’, VSA=’162d’, BFA=’0d’ and VSP1=’40d’ & VSP2=’100d’ (SS =’0’, GS=’0’)

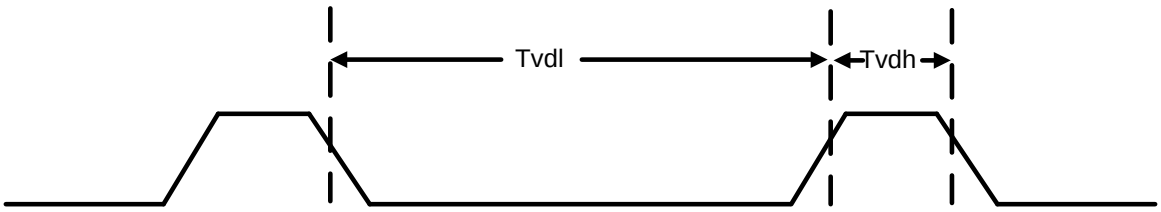


5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory writing when displaying video images.

5.4.1. Tearing effect line modes

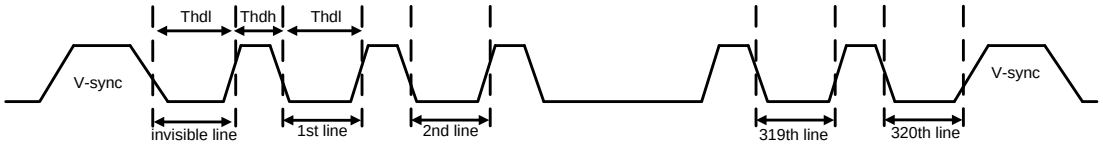
Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:



t_{vdh}= The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.

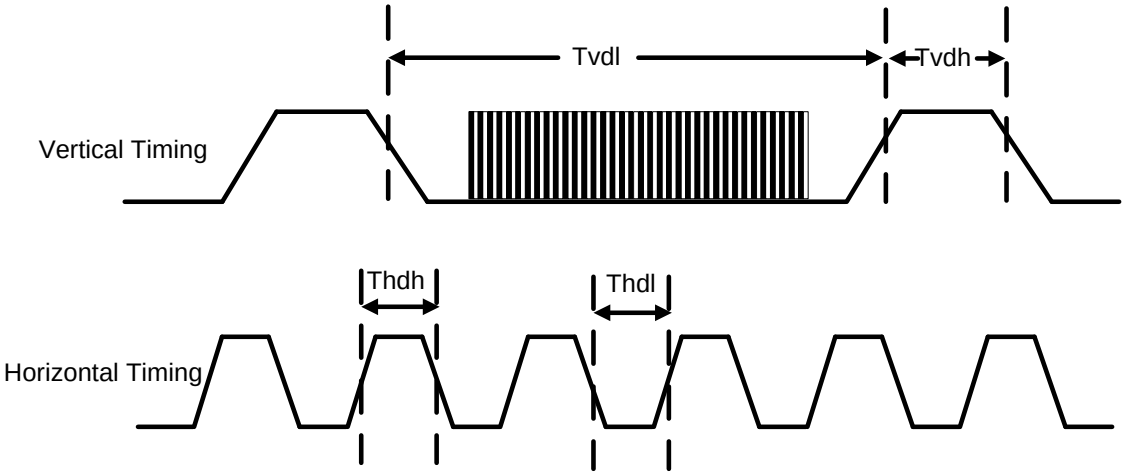


t_{hdh}= The LCD display is not updated from the Frame Memory

t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

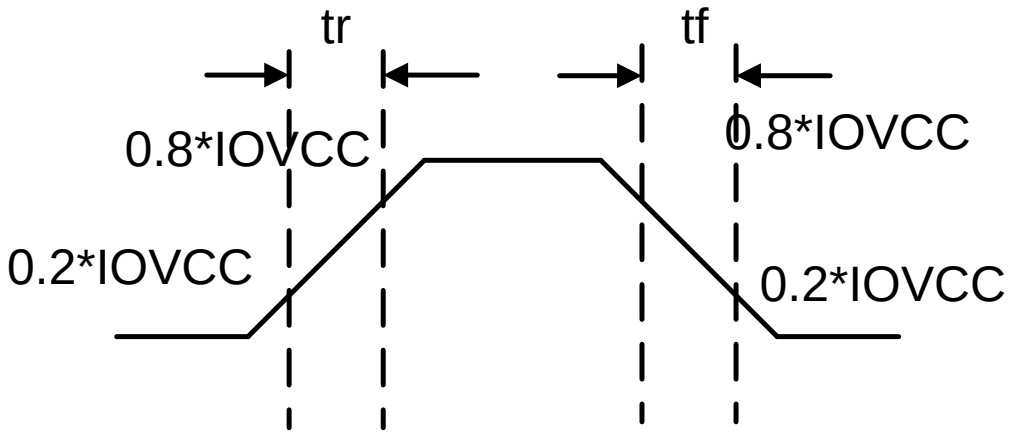
The Tearing Effect signal is described below.



Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) **,**The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9102 contains a 396 channels of source driver (S1~S396) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 396 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously.
Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

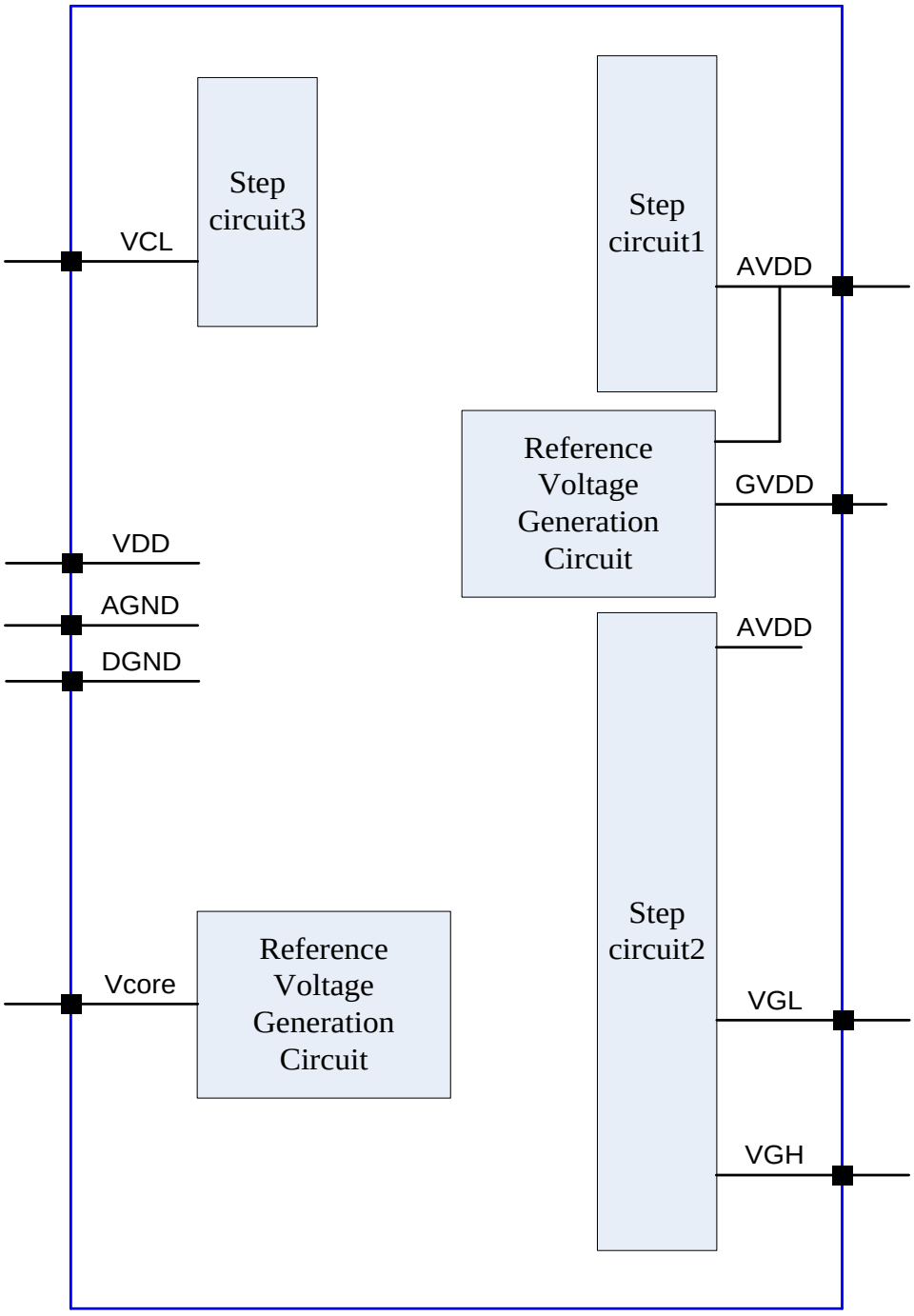
5.6. Gate driver

The GC9102 contains a 162 gate channels of gate driver (G1~G162) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7. LCD power generation circuit

5.7.1. Power supply circuit

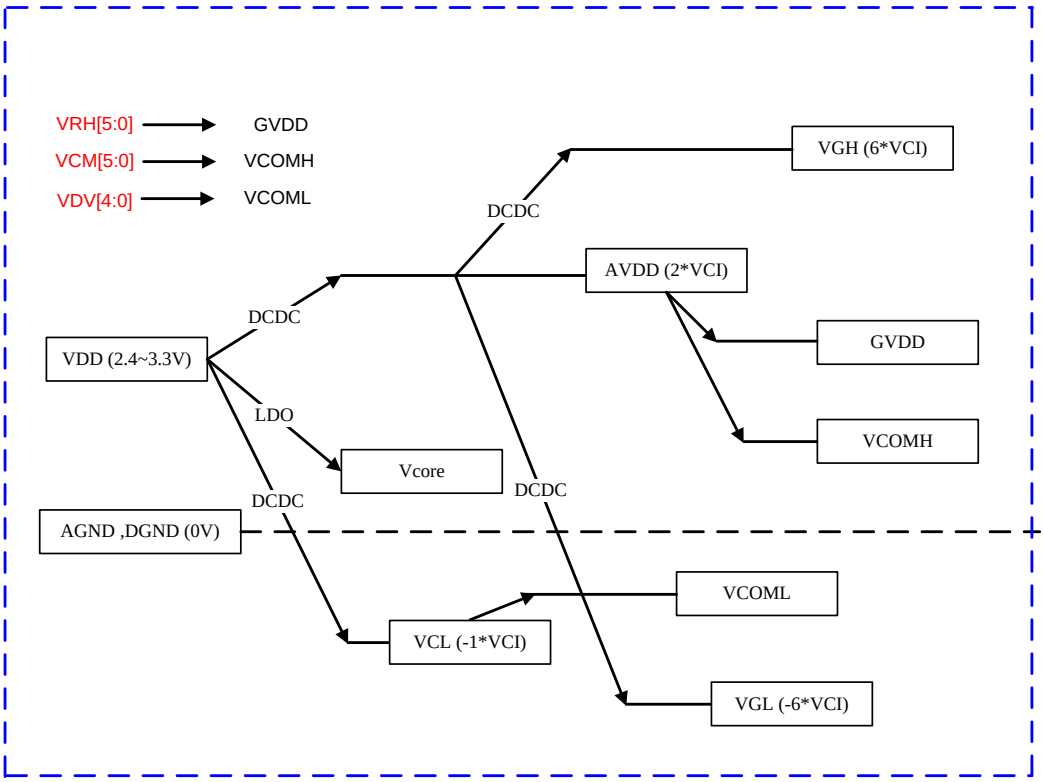
The power circuit of GC9102 is used to generate supply voltages for LCD panel driving.



Block diagram of GC9102 power circuit

5.7.2. LCD power generation scheme

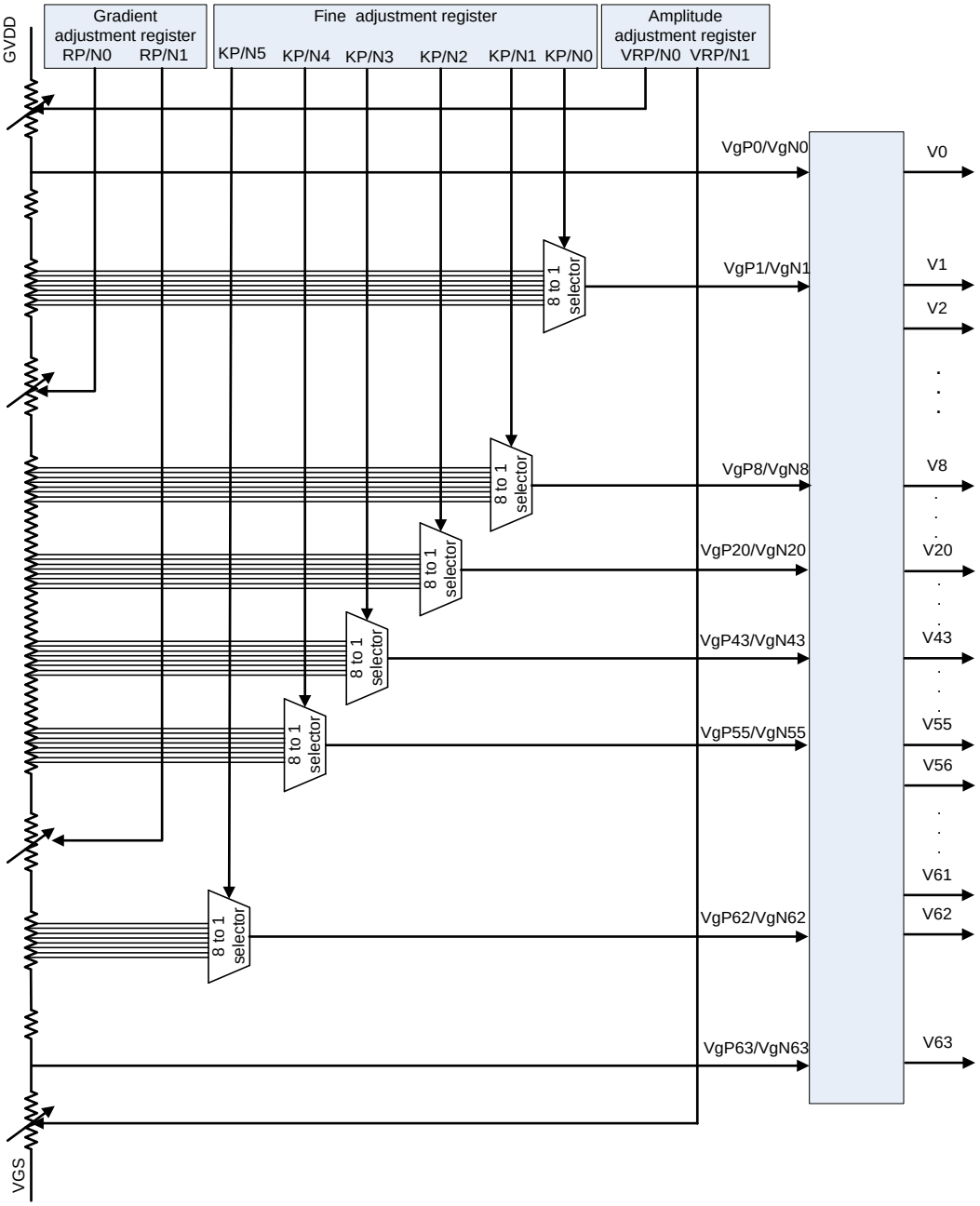
The boost voltage generated is shown as below.



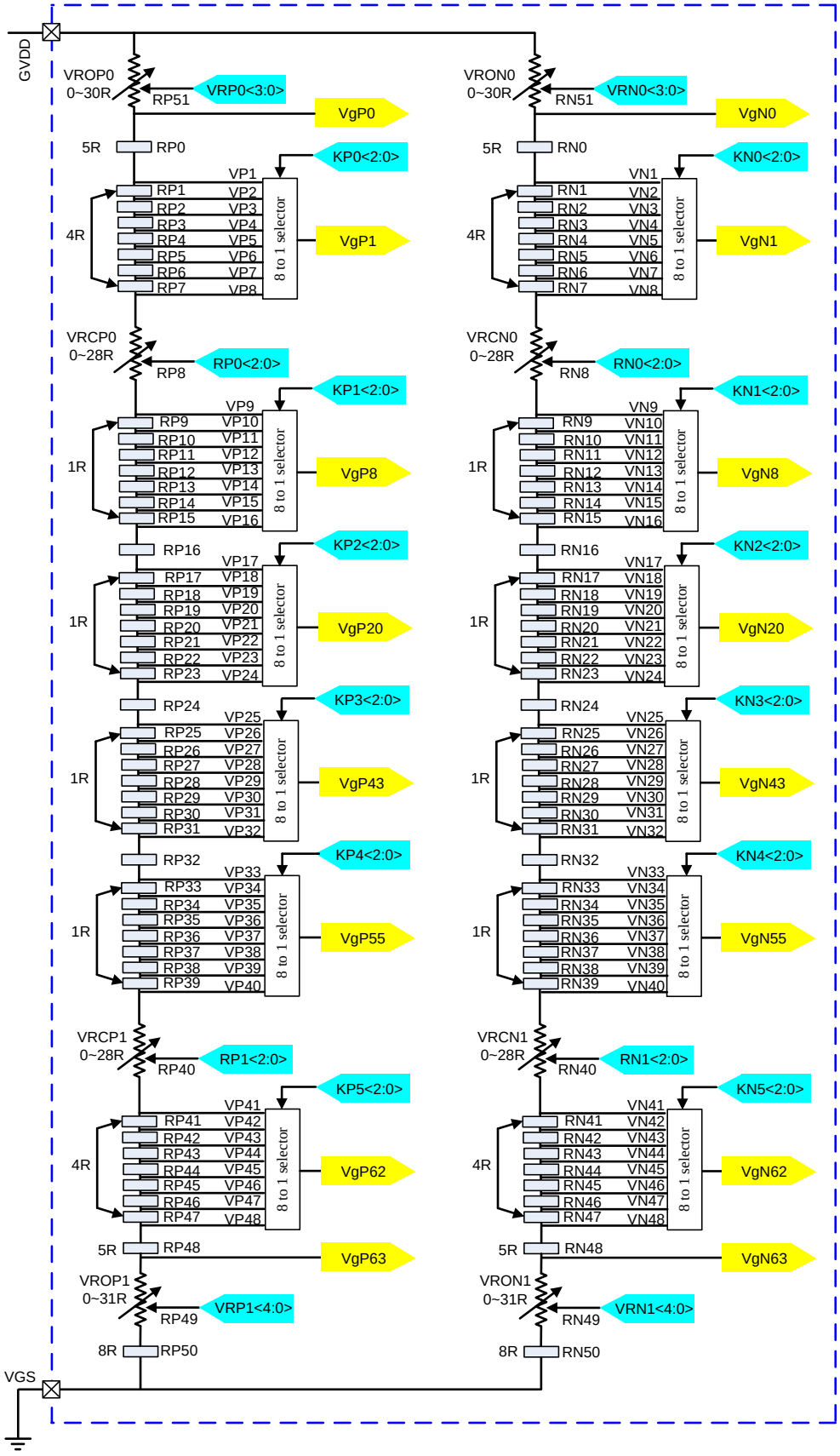
LCD power generation scheme

5.8. Gamma Correction

GC9102 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9102 available with liquid crystal panels of various characteristics.



Grayscale Voltage Generation



Grayscale Voltage Adjustment

1. Gradient adjustment registers

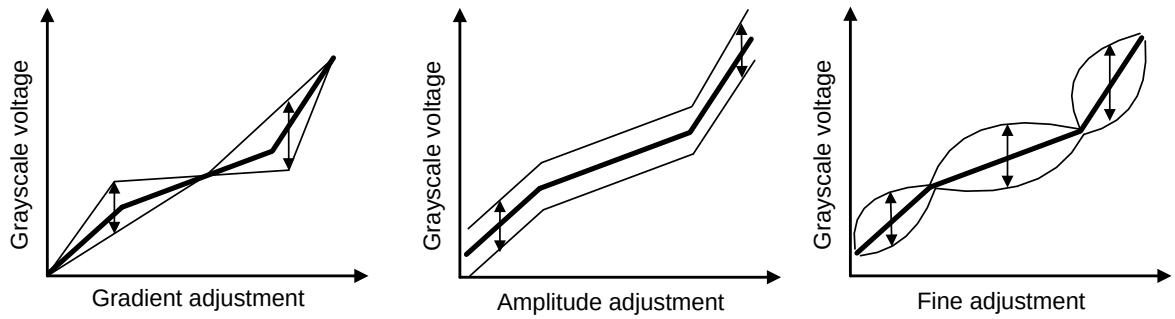
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers RP0[2:0]/RN0[2:0], RP1[2:0]/RN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.



Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	RP0[2:0]	RN0[2:0]	Variable resistor VRCP0, VRCN0
	RP1[2:0]	RN1[2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VROP0, VRON0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0[2:0]	KN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1[2:0]	KN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2[2:0]	KN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3[2:0]	KN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4[2:0]	KN4[2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5[2:0]	KN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

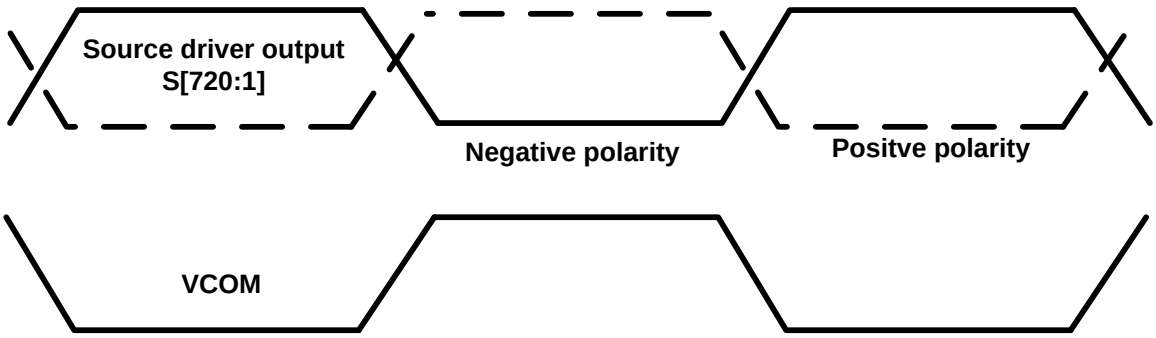
GC9102 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment		**Amplitude adjustment (1)**		**Amplitude adjustment (2)**	
RP(N)0/1[2:0]	**VRCP(N)0 Resistance**	**VRP(N)0[3:0] Register**	**VROP(N)0 Resistance**	**VRP(N)1[4:0] Register**	**VROP(N)1 Resistance**
000	0R	0000	0R	00000	0R
001	4R	0001	2R	00001	1R
010	8R	0010	4R	00010	2R
011	12R				
100	16R	••••	••••	••••	••••
101	20R	1101	26R	11101	29R
110	24R	1110	28R	11110	30R
111	28R	1111	30R	11111	31R

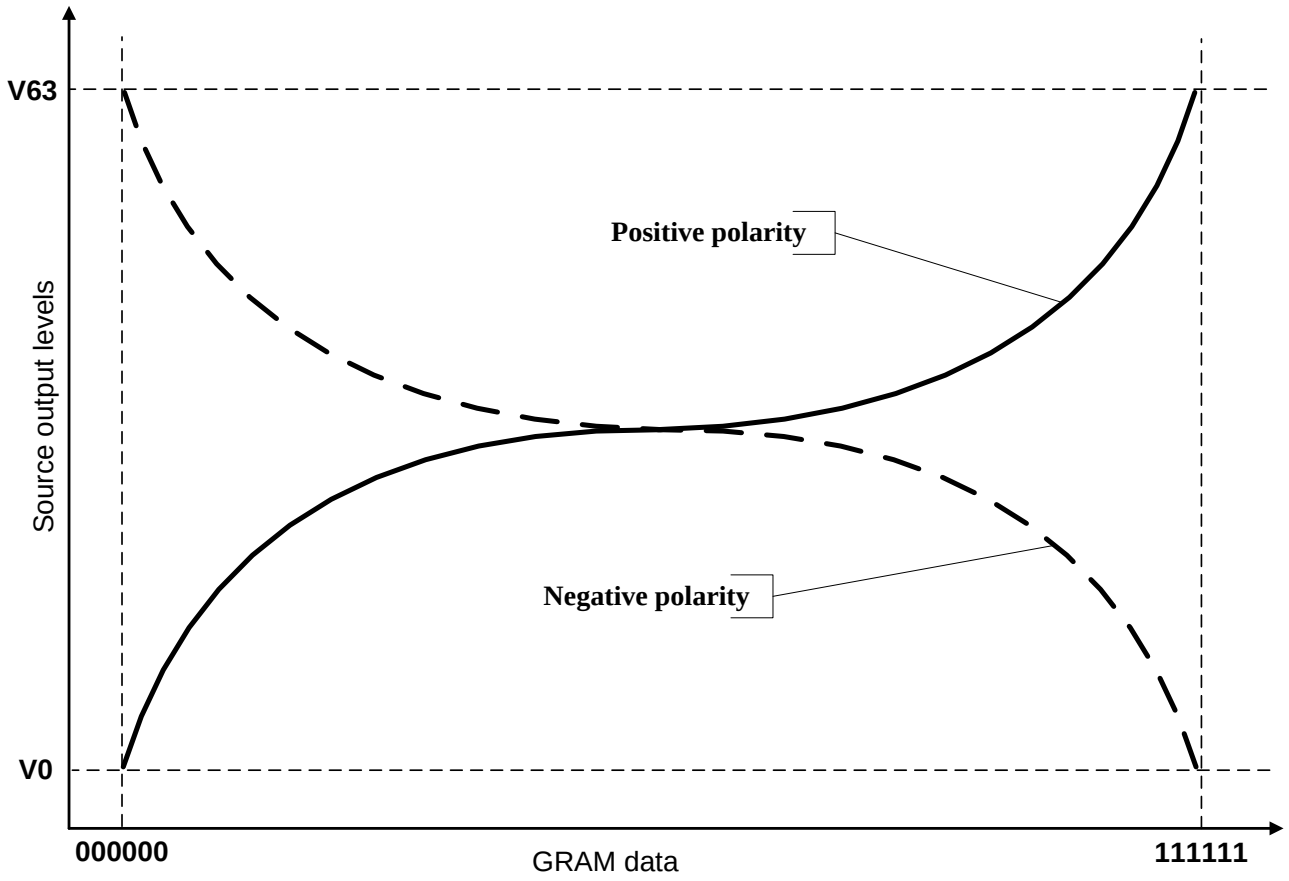
8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	**Selected Voltage**					
KP/N[2:0]	**VgP/N1**	**VgP/N8**	**VgP/N20**	**VgP/N43**	**VgP/N55**	**VgP/N62**
000	VP/N1	VP/N9	VP/N17	VP/N25	VP/N33	VP/N41
001	VP/N2	VP/N10	VP/N18	VP/N26	VP/N34	VP/N42
010	VP/N3	VP/N11	VP/N19	VP/N27	VP/N35	VP/N43
011	VP/N4	VP/N12	VP/N20	VP/N28	VP/N36	VP/N44
100	VP/N5	VP/N13	VP/N21	VP/N29	VP/N37	VP/N45
101	VP/N6	VP/N14	VP/N22	VP/N30	VP/N38	VP/N46
110	VP/N7	VP/N15	VP/N23	VP/N31	VP/N39	VP/N47
111	VP/N8	VP/N16	VP/N24	VP/N32	VP/N40	VP/N48



Relationship between Source Output and VCOM


V63
V0
Source output levels
Positive polarity
Negative polarity
000000
GRAM data
111111

5.9. Power Level Definition

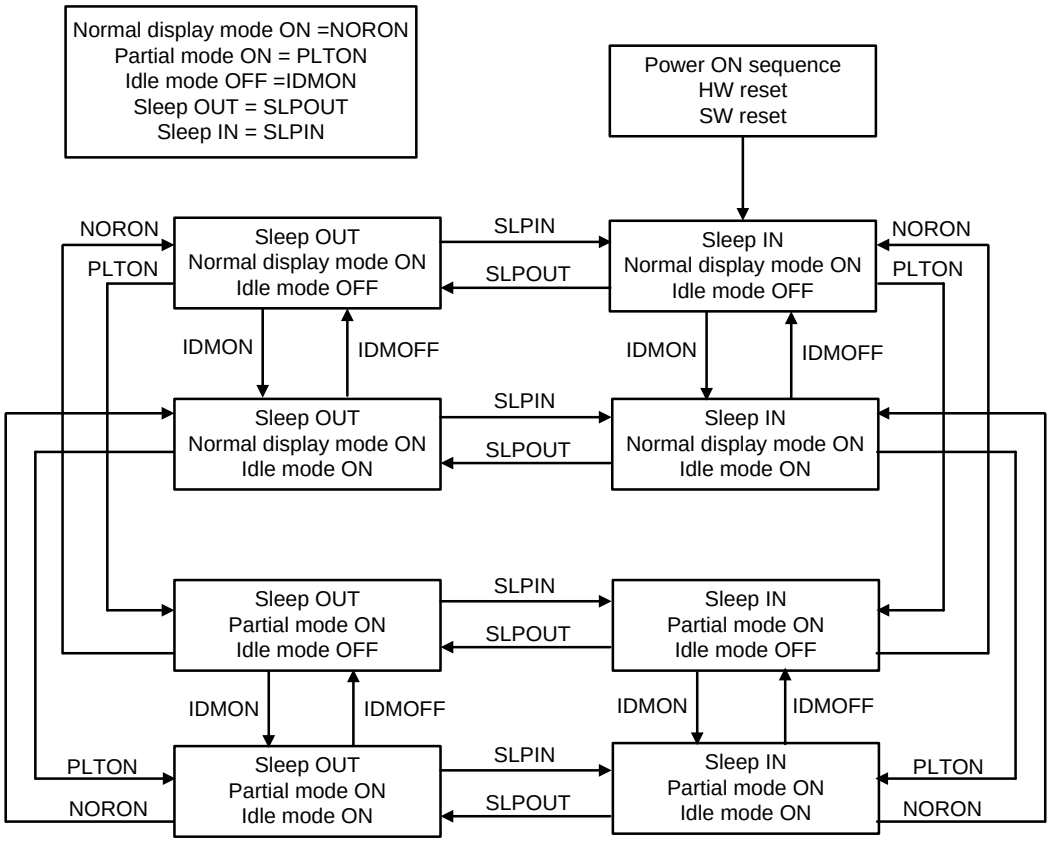
5.9.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDD and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.9.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.
Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

6. Command

6.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 1	0	1	↑	XX	0	0	0	0	0	1	0	0	00h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1_1[7:0]								00
	1	↑	1	XX	ID1_2[7:0]								91
	1	↑	1	XX	ID1_3[7:0]								01
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1[7:0]								7C
	1	↑	1	XX	ID2[7:0]								89
	1	↑	1	XX	ID3[7:0]								F0
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:2]						0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:2]						0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	IFPF [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	X	D5	X	X	D [2:0]			00

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00
Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:4]				X	X	X	X	00
Sleep In	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Gamma Set	0	1	↑	XX	0	0	1	0	0	1	1	0	26h
	1	↑	1	XX	0	0	0	0	GC [3:0]				01
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								-
	1	1	↑	XX	SC[7:0]								-
	1	1	↑	XX	EC[15:8]								-
	1	1	↑	XX	EC[7:0]								-
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								-
	1	1	↑	XX	SP[7:0]								-
	1	1	↑	XX	EP[15:8]								-
	1	1	↑	XX	EP[7:0]								-
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									-
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									-

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								00
	1	1	↑	XX	ER[7:0]								A1
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								00
	1	1	↑	XX	VSA[7:0]								A2
	1	1	↑	XX	BFA[15:8]								00
	1	1	↑	XX	BFA[7:0]								00
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	X	X	X	X	IFPF[2:0]			66
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2_1								7C
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver Version [7:0]								89
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								F0

Extc Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Display Inversion Control	0	1	↑	XX	1	0	1	0	0	0	1	1	E1h
	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	07

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Frame Rate	0	1	↑	XX	1	0	1	0	0	0	1	1	A3h
	1	1	↑	XX		RTN1[5:0]							16
	1	1	↑	XX	RTN_SEL	RTN2[5:0]							16
	1	1	↑	XX		RTN3[5:0]							16
Display Inversion Control	0	1	↑	XX	1	0	1	0	0	0	1	1	E1h
	1	1	↑	XX	0	0	0	0	1	INV_CTL		0	08
Power control 1	0	1	↑	XX	1	0	1	0	0	1	0	0	A4h
	1	1	↑	XX	VCIRE	X	VRH[5:0]						16
Power control 2	0	1	↑	XX	1	1	1	0	1	1	0	1	EDh
	1	1	↑	XX	DC1 [3:0]				DC0 [3:0]				11
	1	1	↑	XX	0	0	0	0	DC2 [3:0]				06
Power control 3	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh
	1	1	↑	XX	X	X	VCM[5:0]						1C
Power control 4	0	1	↑	XX	1	1	1	1	1	1	1	1	FFh
	1	1	↑	XX	X	X	X	VDV[4:0]					16

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
.SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	X	KP1[2:0]			X	KP0[2:0]			00
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	X	KP3[2:0]			X	KP2[2:0]			55
SET_GAMMA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	X	KP5[2:0]			X	KP4[2:0]			07
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
	1	1	↑	XX	X	RP1[2:0]			X	RP0[2:0]			52
SET_GAMMA5	0	1	↑	XX	1	1	1	1	0	1	0	0	F4h
	1	1	↑	XX	X	X	X	X	VRP0[3:0]				00
SET_GAMMA6	0	1	↑	XX	1	1	1	1	0	1	0	1	F5h
	1	1	↑	XX	X	X	X	VRP1[4:0]					00
SET_GAMMA7	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h
	1	1	↑	XX	X	KN1[2:0]			X	KN0[2:0]			07
SET_GAMMA8	0	1	↑	XX	1	1	1	1	1	0	0	0	F8h
	1	1	↑	XX	X	KN3[2:0]			X	KN2[2:0]			22
SET_GAMMA9	0	1	↑	XX	1	1	1	1	1	0	0	1	F9h
	1	1	↑	XX	X	KN5[2:0]			X	KN4[2:0]			77
SET_GAMMA10	0	1	↑	XX	1	1	1	1	1	0	1	0	FAh
	1	1	↑	XX	X	RN1[2:0]			X	RN0[2:0]			25
SET_GAMMA11	0	1	↑	XX	1	1	1	1	1	0	1	1	FBh
	1	1	↑	XX	X	X	X	X	VRN0[3:0]				00
SET_GAMMA12	0	1	↑	XX	1	1	1	1	1	1	0	0	FCh
	1	1	↑	XX	X	X	X	VRN1[4:0]					00

6.2. Description of Level 1 Command

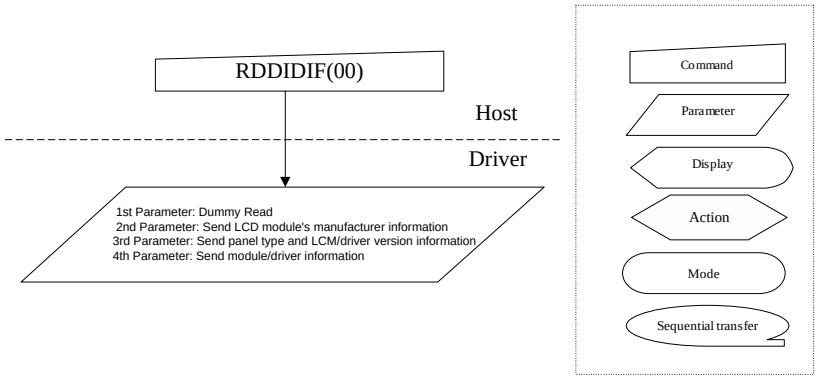
6.2.1. Read display identification information 1 (00h)

00h	Read display identification information 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1_1[7:0]								00
3rd Parameter	1	↑	1	XX	ID1_2[7:0]								91
4th Parameter	1	↑	1	XX	ID1_3[7:0]								02
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID1_2 [7:0]): LCD module/driver version ID. The 4th parameter (ID1_3 [7:0]): LCD module/driver ID.												
Restriction													
Register Availability													

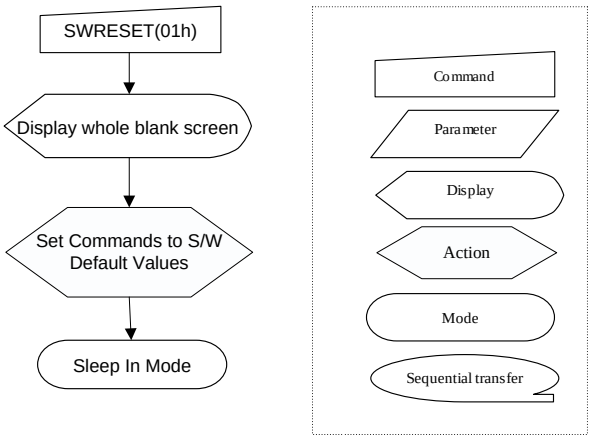
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009101h
SW Reset	24'h009101h
HW Reset	24'h009101h

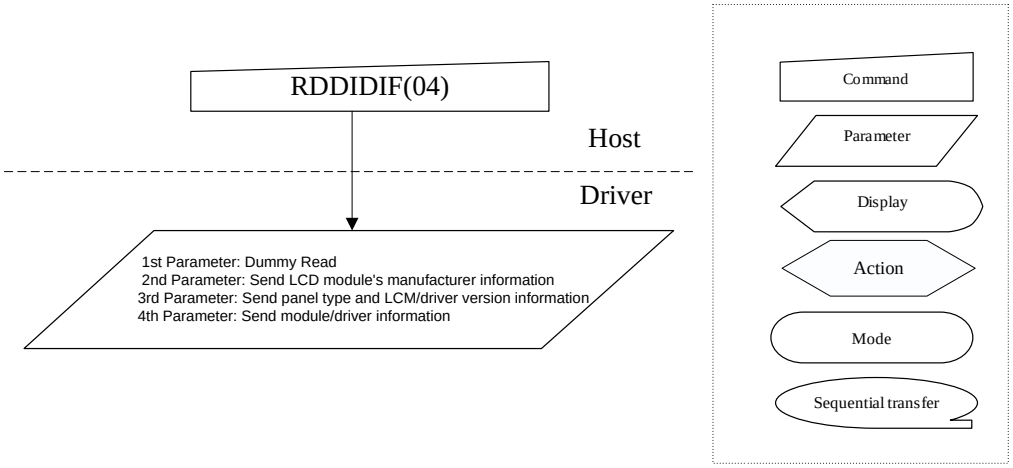
Flow Chart	 RDDIDIF(00) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send LCD module's manufacturer information 3rd Parameter: Send panel type and LCM/driver version information 4th Parameter: Send module/driver information Command Parameter Display Action Mode Sequential transfer

6.2.2. Software Reset (01h)

<table>
<tr><td>01h</td><td colspan="13">Software Reset</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are unaffected by this command</td></tr>
<tr><td>Restriction</td><td colspan="13">It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.3. Read display identification information 2 (04h)

<table>
<tr><td>04h</td><td colspan="13">Read display identification information 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1[7:0]</td><td>7C</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID2 [7:0]</td><td>89</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3[7:0]</td><td>F0</td></tr>
<tr><td>Description</td><td colspan="13">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (ID1 [7:0]): LCD module’s manufacturer ID.
The 3rd parameter (ID2 [7:0]): LCD module/driver version ID.
The 4th parameter (ID3 [7:0]): LCD module/driver ID.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h7C89F0</td></tr><tr><td>SW Reset</td><td>24’h7C89F0</td></tr><tr><td>HW Reset</td><td>24’h7C89F0</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.4. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	BSTON	MY	MX	MV	ML	RGB	MH	D24	00h
3rd Parameter	1	↑	1	XX	D23	IFPF[2:0]			IDMON	PTLON	SLPOUT	NORON	61h
4th Parameter	1	↑	1	XX	D15	D14	INVON	D12	D11	DISON	TEON	GCS2	00h
5th Parameter	1	↑	1	XX	GCS1	GCS0	TEM	D4	D3	D2	D1	D0	00h

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
BSTON	Booster voltage status	0	Booster OFF
		1	Booster ON
MY	Row address order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
MX	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
MV	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
ML	Vertical refresh	0	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
RGB	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
MH	Horizontal refresh order	0	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	0	-
D23	Not used	0	-
IFPF	Interface color pixel format definition	011	12-bit/pixel
		101	16-bit/pixel
		110	18-bit/pixel
IDMON	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON
PTLON	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON
SLPOUT	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode
NORON	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.

D15	Not used	0	-
D14	Not used	0	-
INVON	Inversion status	0	Inversion off
		1	Inversion on
D12	Not used	0	-
D11	Not used	0	-
DISON	Display ON/OFF	0	Display is OFF
		1	Display is ON
TEON	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
GCS [2:0]	Gamma Curve Selection	000	GC0
		001	GC1
		010	GC2
		011	GC3
TEM	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking
D4	Not used	0	-
D3	Not used	0	-
D2	Not used	0	-
D1	Not used	0	-
D0	Not used	0	-

- = Don’t care.

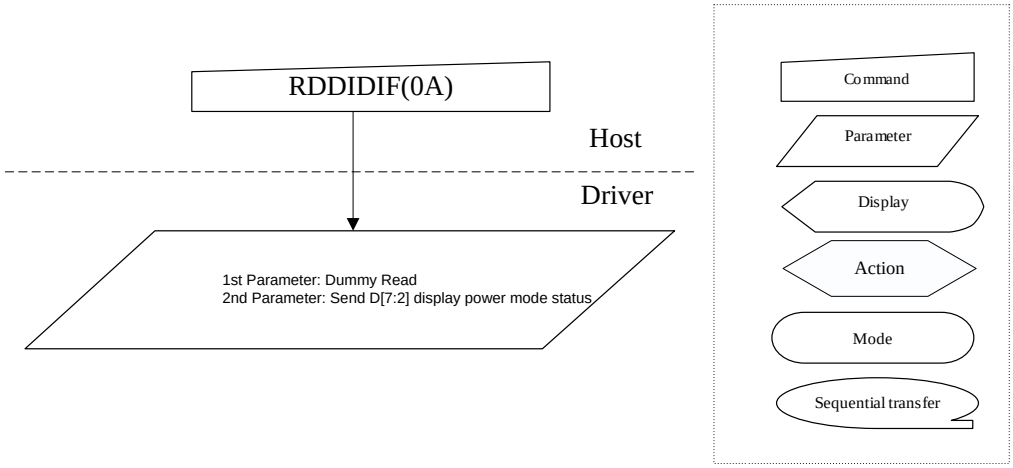
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.5. Read Display Power Mode (0Ah)

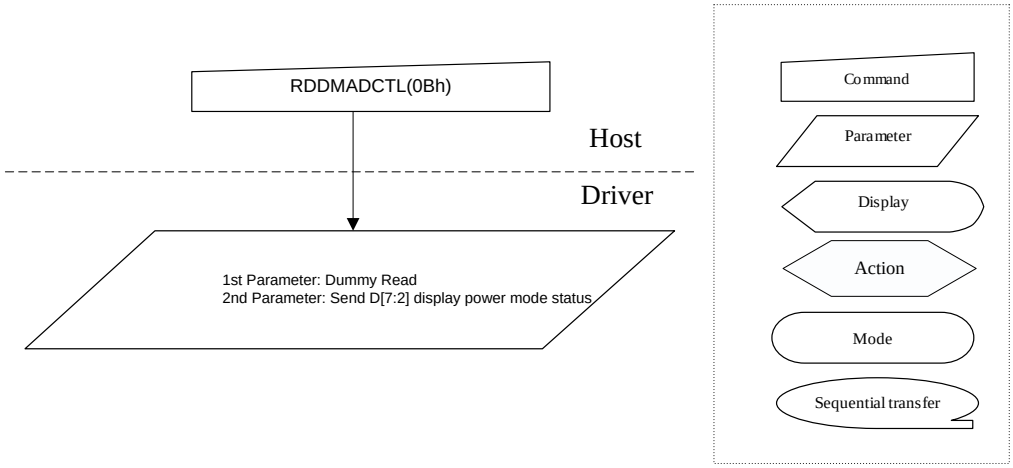
<table>
<tr><td>0Ah</td><td colspan="13">Read Display Power Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>BSTON</td><td>IDMON</td><td>PTLON</td><td>SLPON</td><td>NORON</td><td>DISON</td><td>D1</td><td>D0</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">BSTON</td><td>Booster Off or has a fault.</td><td>0</td></tr>
<tr><td>Booster On and working OK.</td><td>1</td></tr>
<tr><td rowspan="2">IDMON</td><td>Idle Mode Off.</td><td>0</td></tr>
<tr><td>Idle Mode On.</td><td>1</td></tr>
<tr><td rowspan="2">PTLON</td><td>Partial Mode Off.</td><td>0</td></tr>
<tr><td>Partial Mode On.</td><td>1</td></tr>
<tr><td rowspan="2">SLPON</td><td>Sleep In Mode</td><td>0</td></tr>
<tr><td>Sleep Out Mode</td><td>1</td></tr>
<tr><td rowspan="2">NORON</td><td>Display Normal Mode Off.</td><td>0</td></tr>
<tr><td>Display Normal Mode On</td><td>1</td></tr>
<tr><td rowspan="2">DISON</td><td>Display is Off.</td><td>0</td></tr>
<tr><td>Display is On</td><td>1</td></tr>
<tr><td>D1</td><td>Not Defined</td><td>0</td></tr>
<tr><td>D0</td><td>Not Defined</td><td>0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h08</td></tr>
<tr><td>SW Reset</td><td>8’h08</td></tr>
<tr><td>HW Reset</td><td>8’h08</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDIDIF(0A)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.6. Read Display MADCTL (0Bh)

<table>
<tr><td>0Bh</td><td colspan="13">Read Display MADCTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>RGB</td><td>MH</td><td>D1</td><td>D0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">MY</td><td>Top to Bottom (When MADCTL B7=’0’).</td><td>0</td></tr>
<tr><td>Bottom to Top(When MADCTL B7=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">MX</td><td>Left to Right (When MADCTL B6=’0’)</td><td>0</td></tr>
<tr><td>Right to Left (When MADCTL B6=’1’)</td><td>1</td></tr>
<tr><td rowspan="2">MV</td><td>Normal Mode (When MADCTL B5=’0’)</td><td>0</td></tr>
<tr><td>Reverse Mode (When MADCTL B5=’1’)</td><td>1</td></tr>
<tr><td rowspan="2">ML</td><td>LCD Refresh Top to Bottom (When MADCTL B4=’0’)</td><td>0</td></tr>
<tr><td>LCD Refresh Bottom to Top (When MADCTL B4=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">RGB</td><td>RGB (When MADCTL B3=’0’)</td><td>0</td></tr>
<tr><td>BGR (When MADCTL B3=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">MH</td><td>LCD Refresh Left to Right (When MADCTL B2=’0’)</td><td>0</td></tr>
<tr><td>LCD Refresh Right to Left (When MADCTL B2=’1’)</td><td>1</td></tr>
<tr><td>D1</td><td>Not used</td><td>0</td></tr>
<tr><td>D0</td><td>Not used</td><td>0</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDMADCTL(0Bh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.7. Read Display Pixel Format (0Ch)

0Ch	Read Display Pixel Format												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	IFPF[2:0]			06

Description

This command indicates the current status of the display as described in the table below:

IFPF [2:0]	MCU Interface Format
010	12 bits / pixle
101	16 bits / pixel
110	18 bits / pixel
others	Not used

Restriction

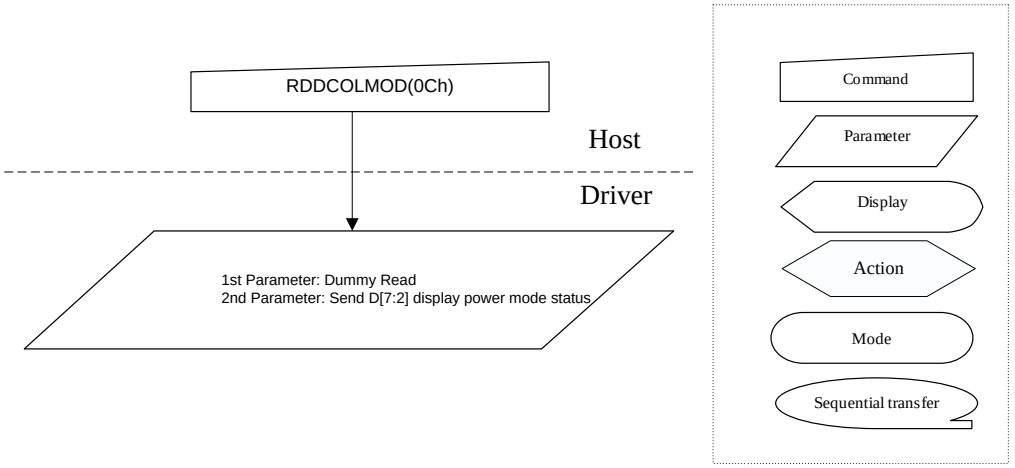
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

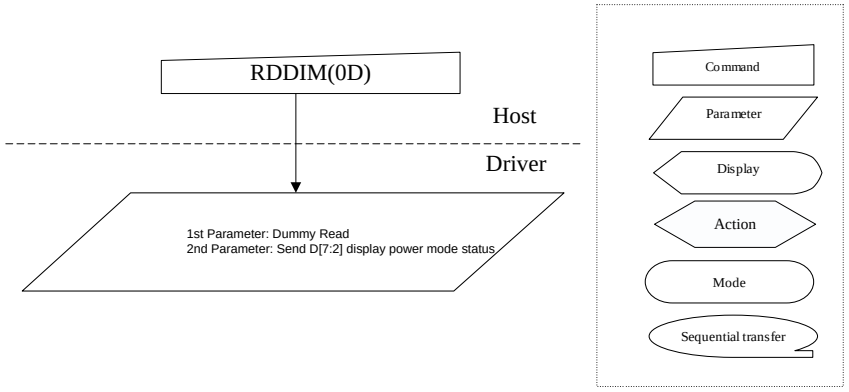
Status	Default Value
	IFPF [2:0]
Power On Sequence	3'b110
SW Reset	No Chang
HW Reset	3'b110

Flow Chart



6.2.8. Read Display Image Format (0Dh)

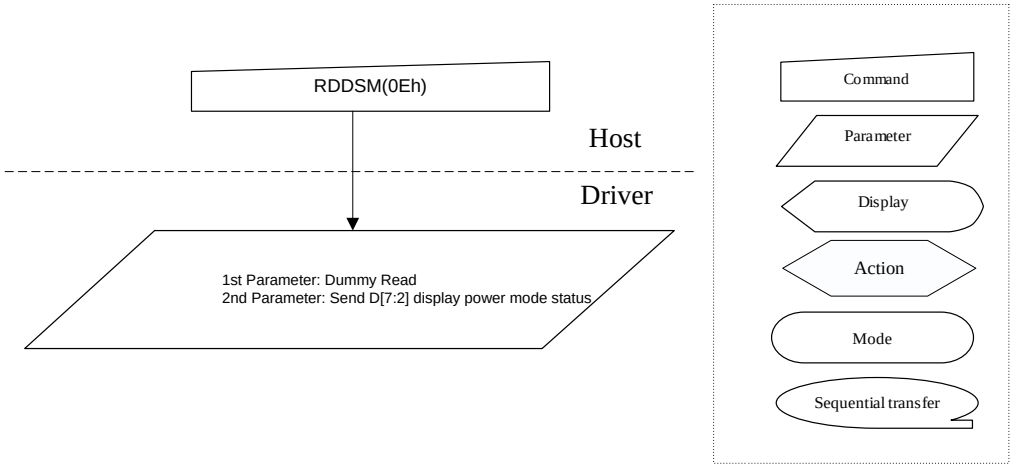
<table>
<tr><td>0Dh</td><td colspan="13">Read Display Image Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>VSSON</td><td>0</td><td>INVON</td><td>0</td><td>0</td><td colspan="3">GCS [2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">VSSON</td><td>Vertical mode off</td><td>0</td></tr>
<tr><td>Vertical mode on</td><td>1</td></tr>
<tr><td rowspan="2">INVON</td><td>Inversion off</td><td>0</td></tr>
<tr><td>Inversion on</td><td>1</td></tr>
<tr><td rowspan="5">GCS [2:0]</td><td>GC0</td><td>000</td></tr>
<tr><td>GC1</td><td>001</td></tr>
<tr><td>GC2</td><td>010</td></tr>
<tr><td>GC3</td><td>011</td></tr>
<tr><td>other</td><td>Not define</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’b00000000</td></tr>
<tr><td>SW Reset</td><td>8’b00000000</td></tr>
<tr><td>HW Reset</td><td>8’b00000000</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDIM(0D)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.9. Read Display Signal Mode (0Eh)

<table>
<tr><td>0Eh</td><td colspan="13">Read Display Signal Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>TEON</td><td>TEM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">TEON</td><td>0</td><td>Tearing effect line OFF</td></tr>
<tr><td>1</td><td>Tearing effect line ON</td></tr>
<tr><td rowspan="2">TEM</td><td>0</td><td>Tearing effect line mode 1</td></tr>
<tr><td>1</td><td>Tearing effect line mode 2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDSM(0Eh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	Read Display Self-Diagnostic Result												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	F	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	RELD	FUND	ATTD	BRD	0	0	0	0	F0

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	value
RELD	Register Loading Detection	1
FUND	Functionality Detection	1
ATTD	Chip Attachment Detection	1
BRD	Display Glass Break Detection	1

Restriction

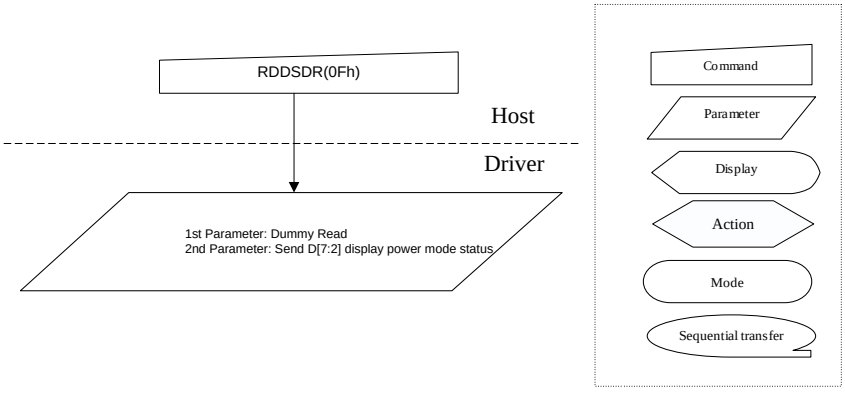
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

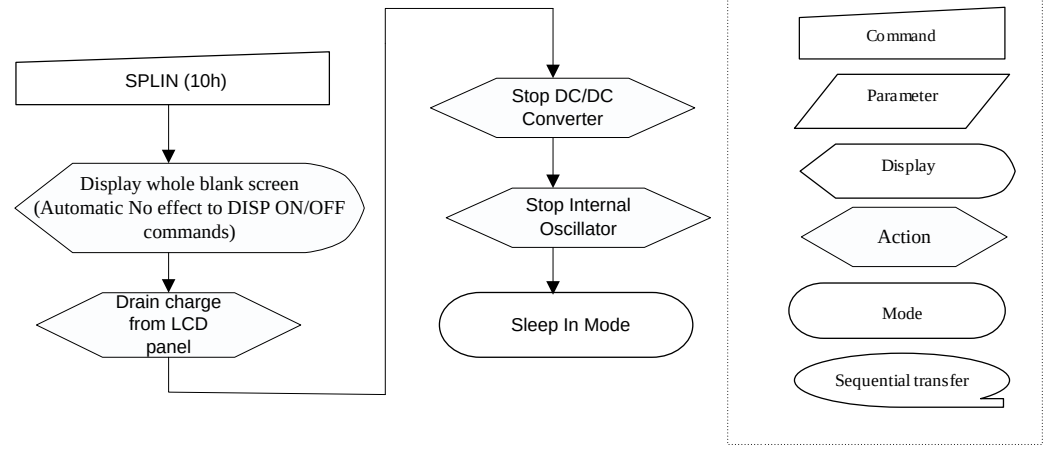
Status	Default Value
Power On Sequence	8'hF0
SW Reset	8'hF0
HW Reset	8'hF0

Flow Chart



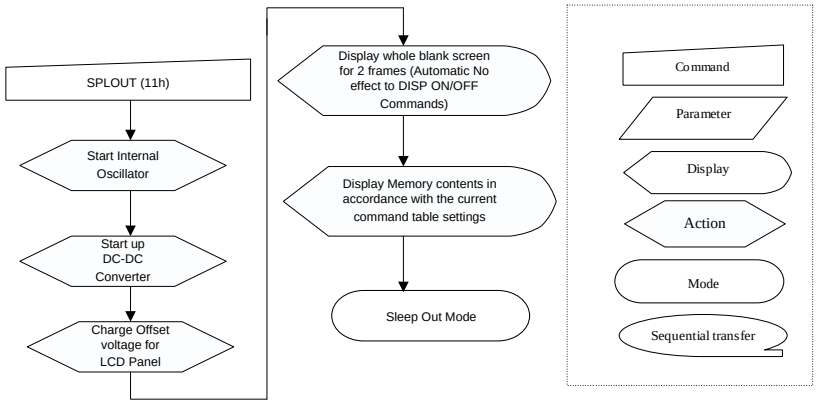
6.2.11. Sleep In (10h)

<table>
<tr><td>10h</td><td colspan="13">Enter Sleep Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode.
In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped
MCU interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued. 

6.2.12. Sleep Out (11h)

<table>
<tr><td>11h</td><td colspan="13">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize.
The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.
The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

SPLOUT (11h)
Start Internal Oscillator
Start up DC-DC Converter
Charge Offset voltage for LCD Panel
Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)
Display Memory contents in accordance with the current command table settings
Sleep Out Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

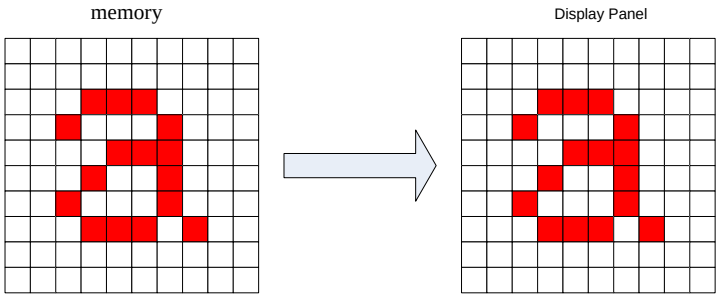
6.2.13. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="12">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

6.2.14. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="12">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

6.2.15. Display Inversion OFF (20h)

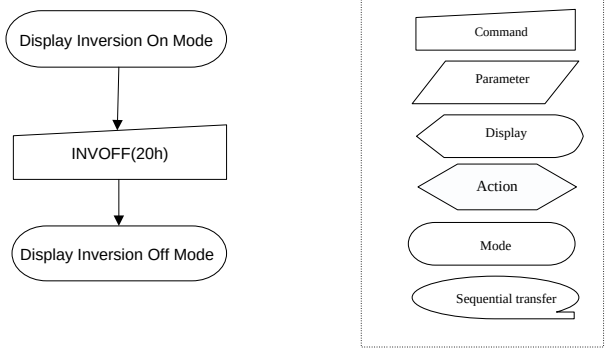
20h	Display Inversion OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status. 												
Restriction	This command has no effect when module already is inversion OFF mode.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

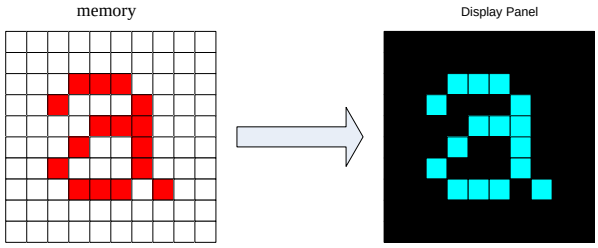
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart	

Display Inversion On Mode
INVOFF(20h)
Display Inversion Off Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.16. Display Inversion ON (21h)

21h	Display Inversion ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written.. 												
Restriction	This command has no effect when module already is inversion ON mode.												

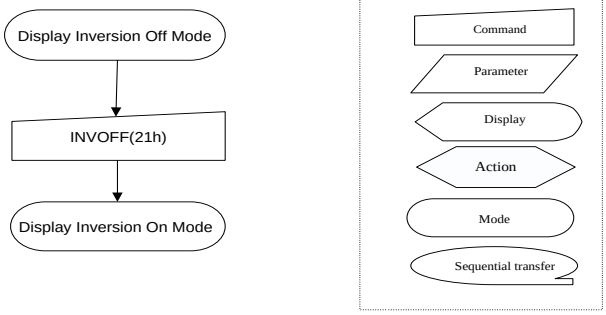
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

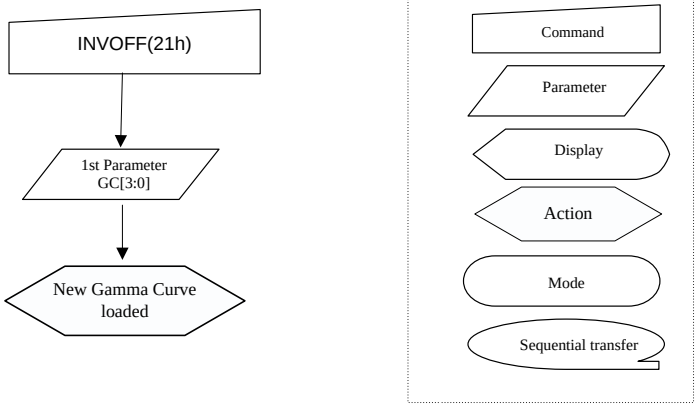
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

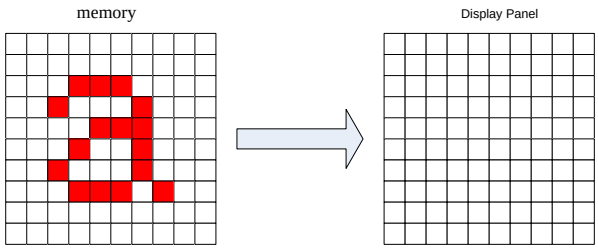
Flow Chart



6.2.17. Gamma Set (26h)

<table>
<tr><td>26h</td><td colspan="13">Display Inversion ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>26h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>GC3</td><td>GC2</td><td>GC1</td><td>GC0</td><td>01h</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.
<table>
<tr><th>GC [3:0]</th><th>Parameter</th><th>Curve Selection</th></tr>
<tr><td>01h</td><td>GC0</td><td>Gamma Curve 1</td></tr>
<tr><td>02h</td><td>GC1</td><td>Gamma Curve 2</td></tr>
<tr><td>04h</td><td>GC2</td><td>Gamma Curve 3</td></tr>
<tr><td>08h</td><td>GC3</td><td>Gamma Curve 4</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>01h</td></tr>
<tr><td>SW Reset</td><td>01h</td></tr>
<tr><td>HW Reset</td><td>01h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.18. Display OFF (28h)

28h	Display OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. 												
Restriction	This command has no effect when module is already in display off mode.												

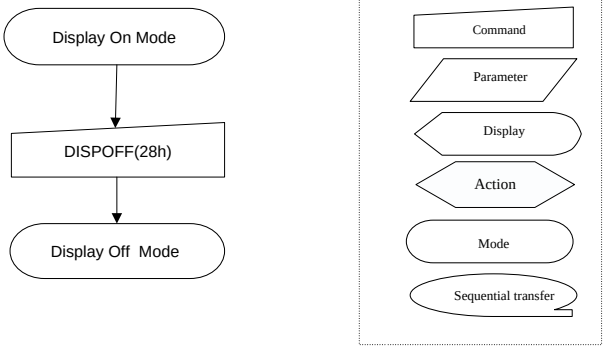
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

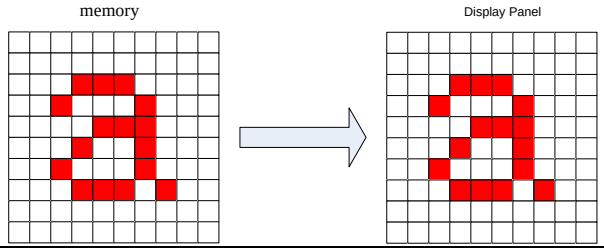
Default

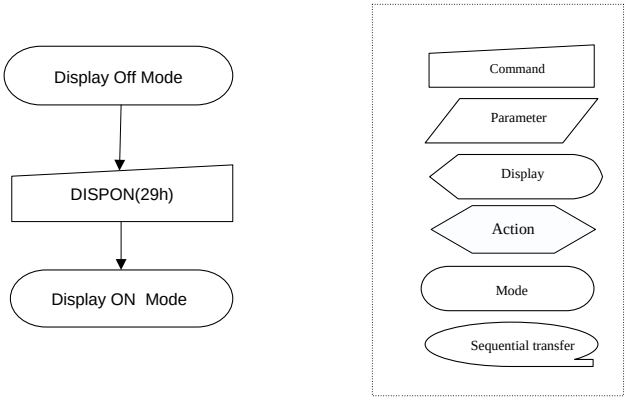
Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart



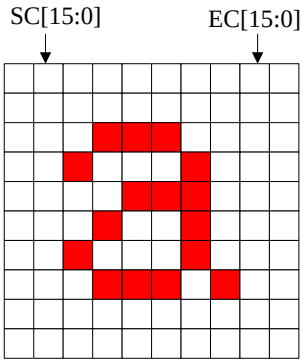
6.2.19. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="12">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display OFF</td></tr>
<tr><td>SW Reset</td><td>Display OFF</td></tr>
<tr><td>HW Reset</td><td>Display OFF</td></tr>
</table></td></tr>
</table>

Flow Chart	

Display Off Mode
DISPON(29h)
Display ON Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

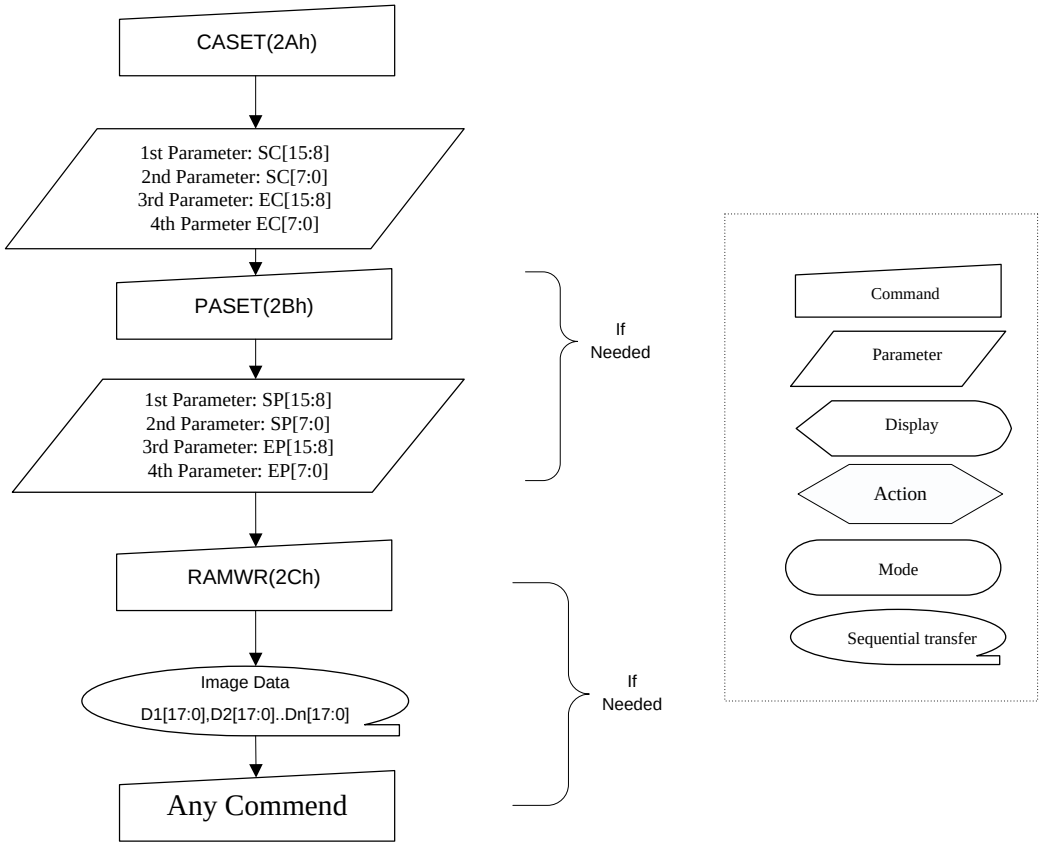
6.2.20. Column Address Set (2Ah)

<table>
<tr><td>2Ah</td><td colspan="13">Column Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC15</td><td>SC14</td><td>SC13</td><td>SC12</td><td>SC11</td><td>SC10</td><td>SC9</td><td>SC8</td><td></td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC7</td><td>SC6</td><td>SC5</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>SC0</td><td></td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC15</td><td>EC14</td><td>EC13</td><td>EC12</td><td>EC11</td><td>EC10</td><td>EC9</td><td>EC8</td><td></td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC7</td><td>EC6</td><td>EC5</td><td>EC4</td><td>EC3</td><td>EC2</td><td>EC1</td><td>EC0</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13">SC [15:0] always must be equal to or less than EC [15:0].
When SC [15:0] or EC [15:0] is greater than maximum address like below, data of out of range will be ignored
1. 132X162 memory base (GM = ‘00’)
(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 131 (0083h)): MV=”0”)
(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 161 (00A1h)): MV=”1”)
2. 132X132 memory base (GM = ‘01’)
(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 131 (0083h)): MV=”0”)
(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 131 (0083h)): MV=”1”)
3. 128X160 memory base (GM = ‘11’)
(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 127 (007Fh)): MV=”0”)
(Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 159 (009Fh)): MV=”1”)</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

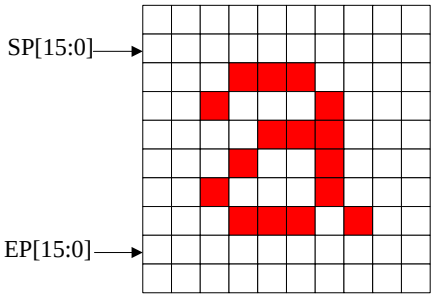
Default

GM	Status	Default Value		
		SC	EC (MV=0)	EC (MV=1)
GM= '00' (132x162 memory base)	Power On Sequence	0000h	0083h (131)	
	SW Reset	0000h	0083h (131)	00A1h (161)
	HW Reset	0000h	0083h (131)	
GM= '01' (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
	SW Reset	0000h	0083h (131)	0083h (131)
	HW Reset	0000h	0083h (131)	
GM= '11' (128x160 memory base)	Power On Sequence	0000h	007Fh (127)	
	SW Reset	0000h	007Fh (127)	009Fh (159)
	HW Reset	0000h	007Fh (127)	

Flow Chart



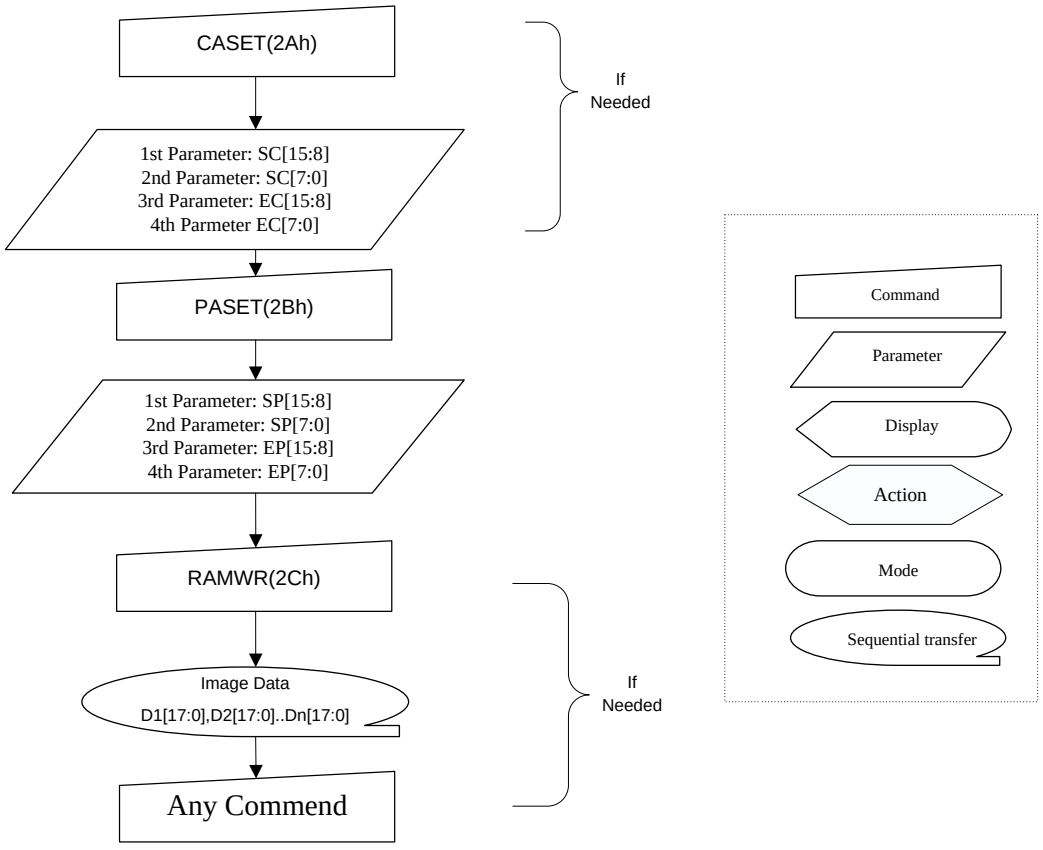
6.2.21. Row Address Set (2Bh)

2Bh	Row Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	
2nd Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.  												
Restriction	SP [15:0] always must be equal to or less than EP [15:0]. When SP [15:0] or EP [15:0] is greater than maximum address like below, data of out of range will be ignored. 3. 132X162 memory base (GM = ’00’) (Parameter range: 0 < SP [15:0] < EP [15:0] < 161 (00A1h)): MV=”0” (Parameter range: 0 < SP [15:0] < EP [15:0] < 131 (0083h)): MV=”1” 2. 132X132 memory base (GM = ’00’) (Parameter range: 0 < SP [15:0] < EP [15:0] < 131 (00A1h)): MV=”0” (Parameter range: 0 < SP [15:0] < EP [15:0] < 131 (0083h)): MV=”1” 1. 128X160 memory base (GM = ’11’) (Parameter range: 0 < SP [15:0] < EP [15:0] < 159 (009Fh)): MV=”0” (Parameter range: 0 < SP [15:0] < EP [15:0] < 127 (007Fh)): MV=”1”												
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												

Default

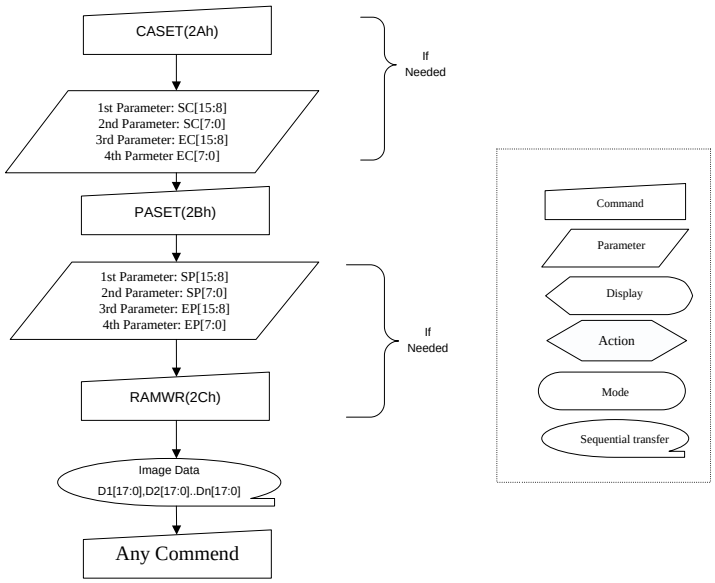
GM	Status	Default Value		
		SC	EC (MV=0)	EC (MV=1)
GM= ‘00’ (132x162 memory base)	Power On Sequence	0000h	00A1h (161)	
	SW Reset	0000h	00A1h (161)	0083h (131)
	HW Reset	0000h	00A1h (161)	
GM= ‘01’ (132x132 Memory Base)	Power On Sequence	0000h	0083h (131)	
	SW Reset	0000h	0083h (131)	0083h (131)
	HW Reset	0000h	0083h (131)	
GM= ‘11’ (128x160 memory base)	Power On Sequence	0000h	009Fh (159)	
	SW Reset	0000h	009Fh (159)	007Fh (127)
	HW Reset	0000h	009Fh (159)	

Flow Chart



6.2.22. Memory Write (2Ch)

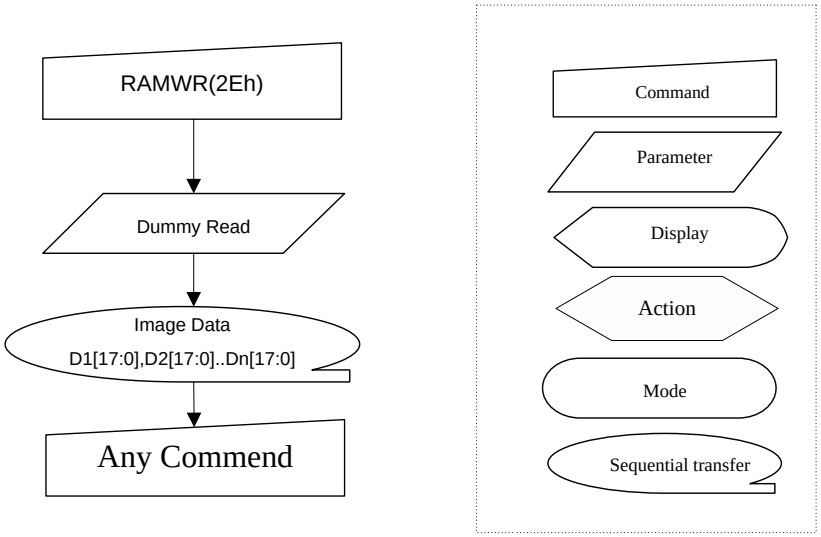
<table>
<tr><td>2Ch</td><td colspan="13">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2Ch</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">D1 [17:0]</td><td rowspan="2"></td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dx [17:0]</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="9">Dn [17:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is not cleared</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Flow Chart	

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
If Needed
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
If Needed
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
Command
Parameter
Display
Action
Mode
Sequential transfer

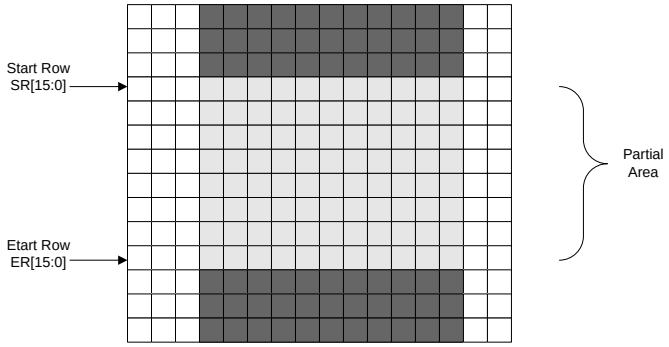
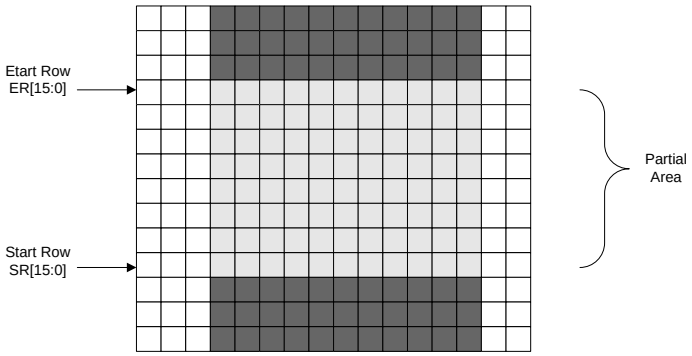
6.2.23. Memory Read (2Eh)

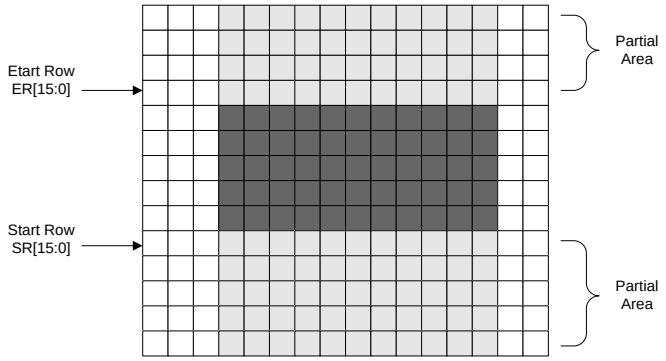
<table>
<tr><td>2Eh</td><td colspan="13">Memory Read</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2Eh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="9">D1 [17:0]</td><td rowspan="2"></td></tr>
<tr><td>:</td><td>1</td><td>↑</td><td>1</td><td colspan="9">Dx [17:0]</td></tr>
<tr><td>(N+1)th Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="9">Dn [17:0]</td><td></td></tr>
<tr><td>Description</td><td colspan="13">This command transfers image data from GC9102’s frame memory to the host processor starting at the pixel location specified by preceding Column_Address_Set and Row_Address_Set commands.
If Memory Access control B5 = 0:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.
If Memory Access Control B5 = 1:
The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>SW Reset</td><td rowspan="2">Contents of memory is set randomly
Contents of memory is set randomly</td></tr><tr><td>HW Reset</td></tr></table></td></tr>
</table>

Flow Chart	

RAMWR(2Eh)
Dummy Read
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.24. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when ML=0:  If End Row>Start Row when ML=1:  If End Row<Start Row when ML =0:													



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction

Register Availability

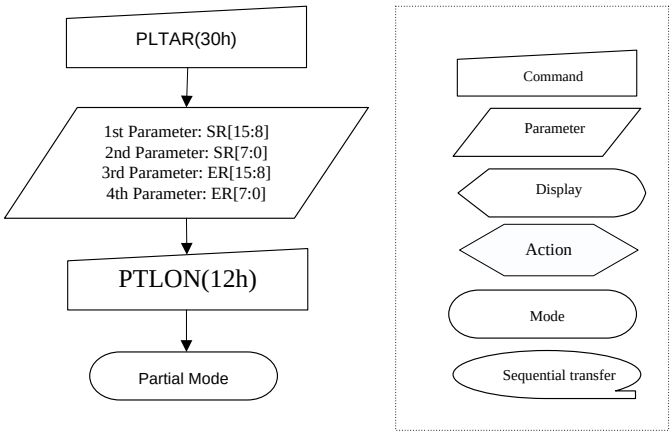
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

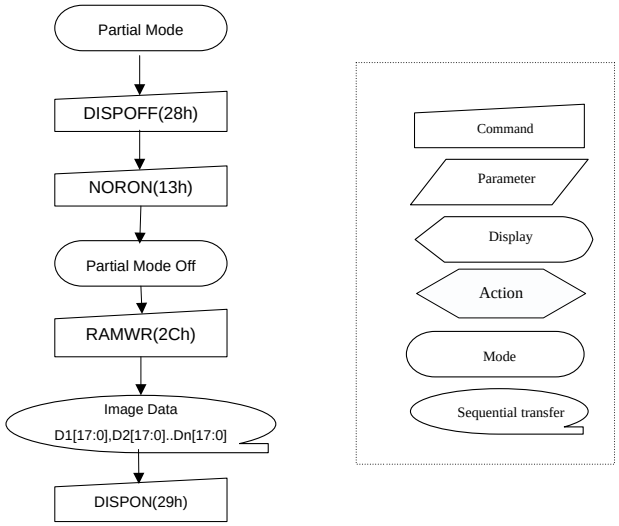
Status	Default Value			
	SR [15:0]	ER [15:0]		
GM[1:0]	xx	GM = '00'	GM = '01'	GM = '11'
Power On Sequence	16'h0000	16'h00A1	16'h0083	16'h009F
SW Reset	16'h0000	16'h00A1	16'h0083	16'h009F
HW Reset	16'h0000	16'h00A1	16'h0083	16'h009F

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



6.2.25. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								00
4th Parameter	1	1	↑	XX	VSA [7:0]								A2
5th Parameter	1	1	↑	XX	BFA [15:8]								00
6th Parameter	1	1	↑	XX	BFA [7:0]								00

Description

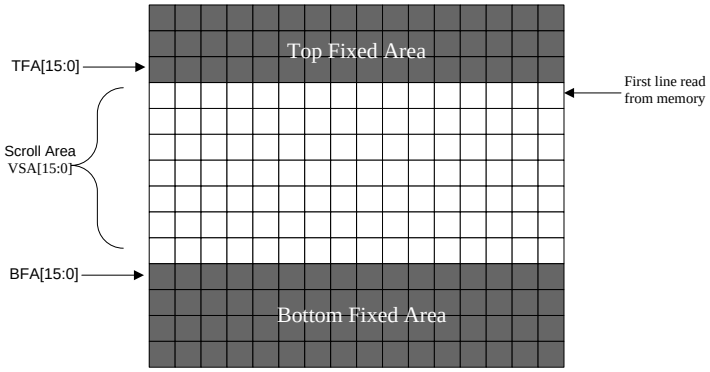
This command defines the Vertical Scrolling Area of the display.

When MADCTL B4=0

The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.

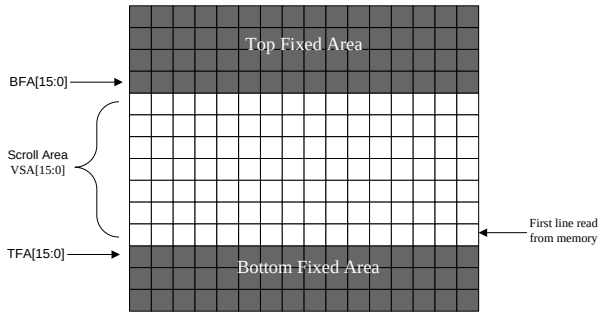


When MADCTL B4=1

The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.

The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).



X = Don't care.

Restriction

The condition is (TFA+VSA+BFA)=132 in 132RGBx132 (GM="01")
The condition is (TFA+VSA+BFA)=160 in 128RGBx160 (GM="11")
The condition is (TFA+VSA+BFA)=162 in 132RGBx162 (GM="00")
Otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTR parameter MV should be set to '0', this only affects the Frame Memory Write.

Register Availability

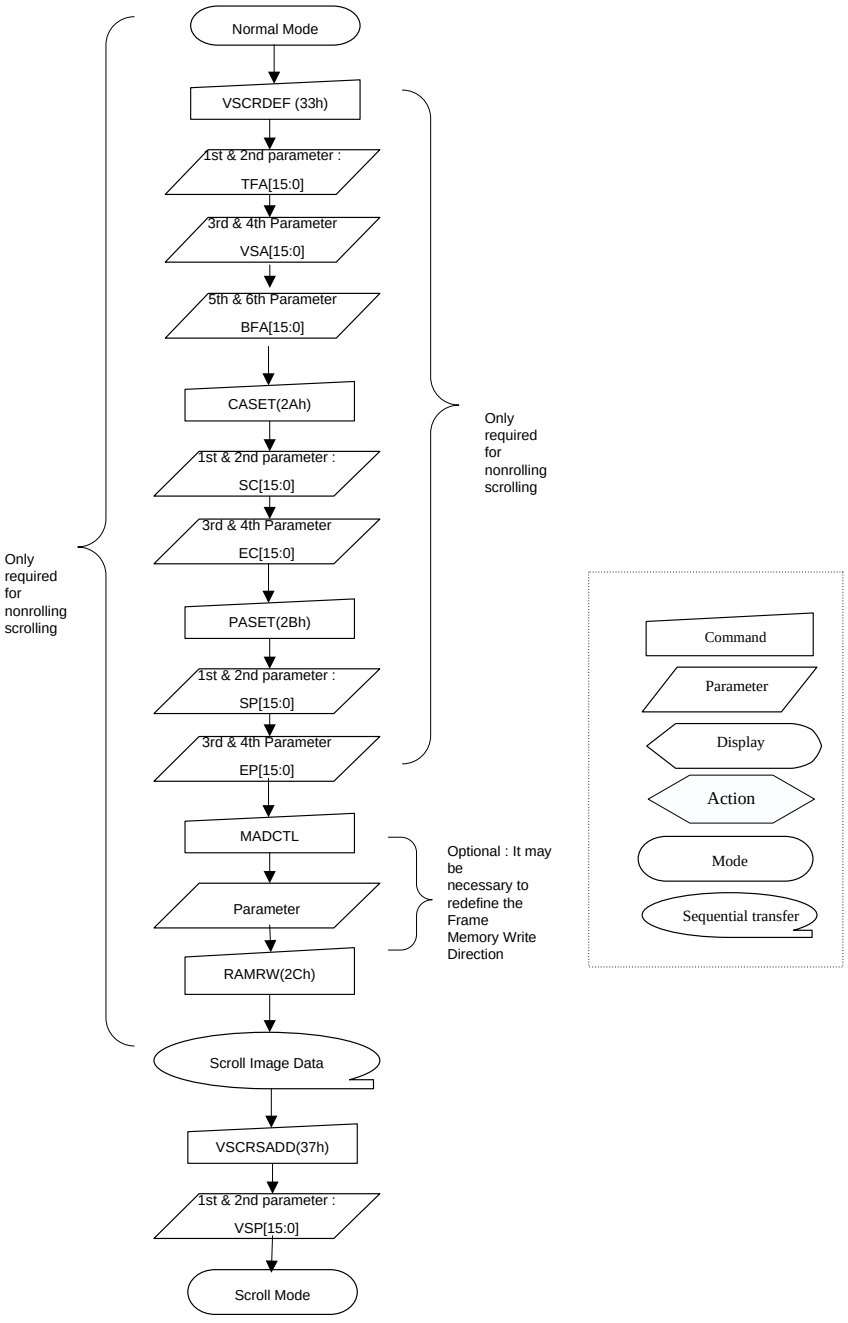
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	48'h0000_0000_0000	48'h0000_00A2_0000
SW Reset	48'h0000_0000_0000	48'h0000_00A2_0000
HW Reset	48'h0000_0000_0000	48'h0000_00A2_0000

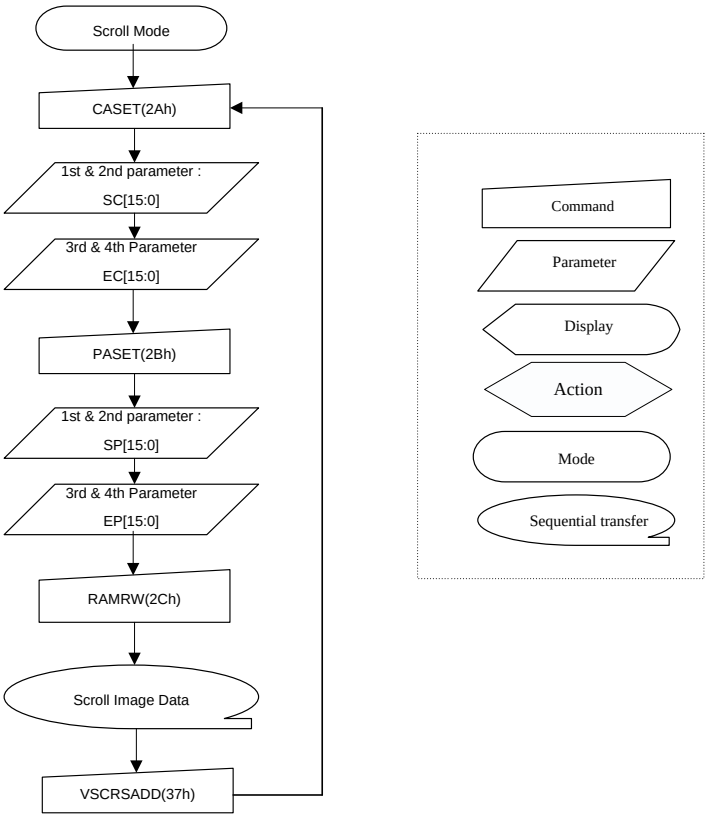
Flow Chart

1. To enter Vertical Scroll Mode :

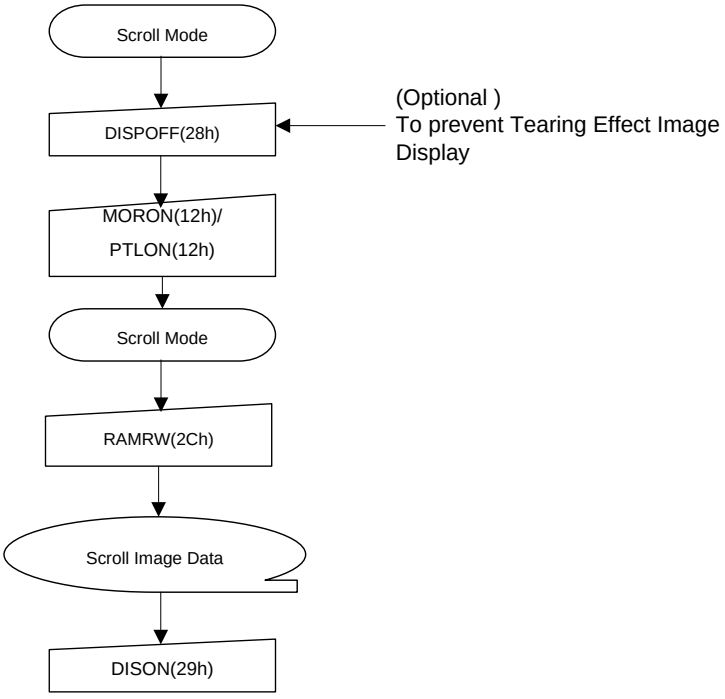


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :

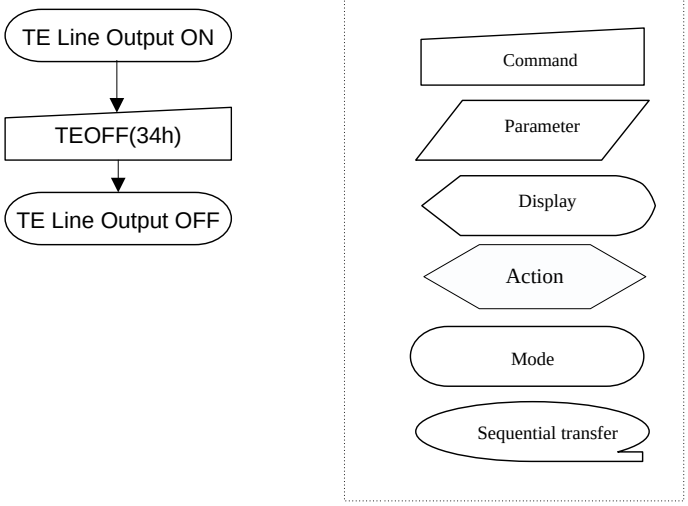


3.To Leave Vertical Scroll Mode:



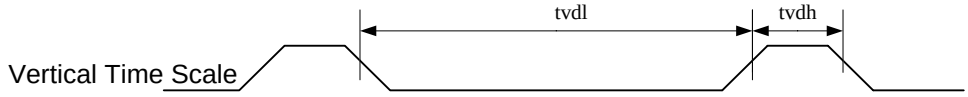
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

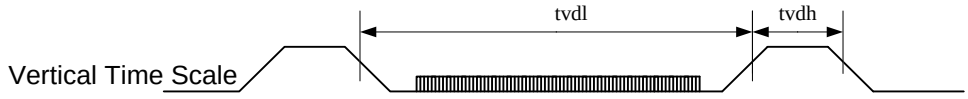
6.2.26. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

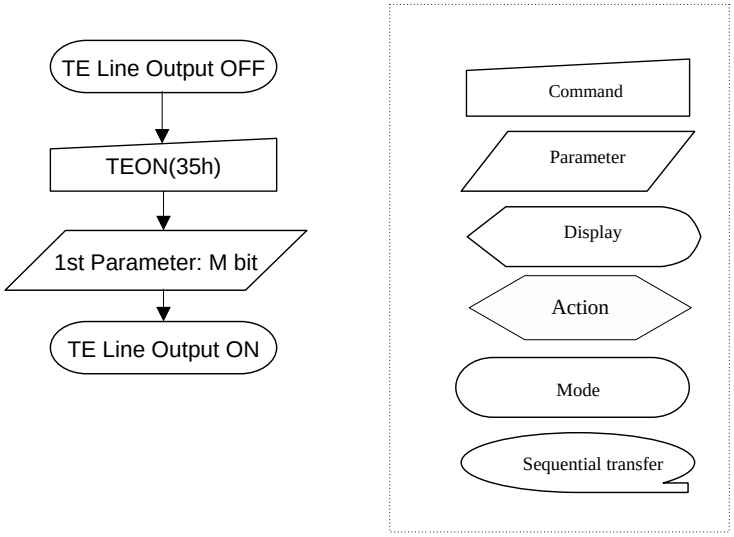
6.2.27. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

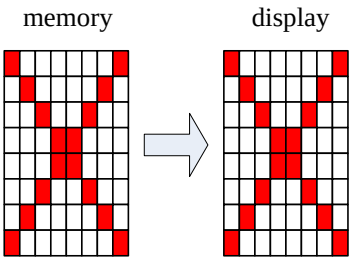
When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

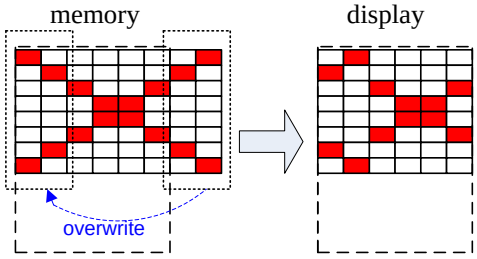
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

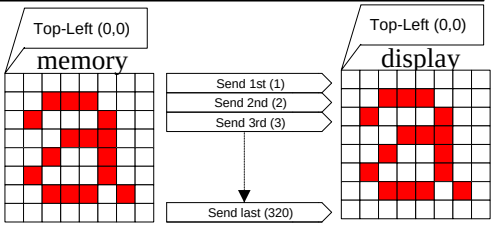
Flow Chart	

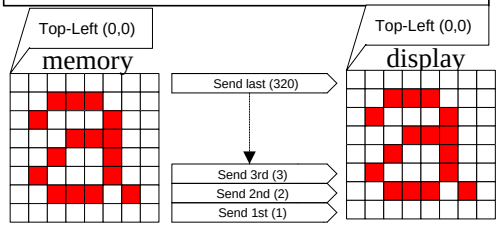
TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.28. Memory Access Ctrl (36h)

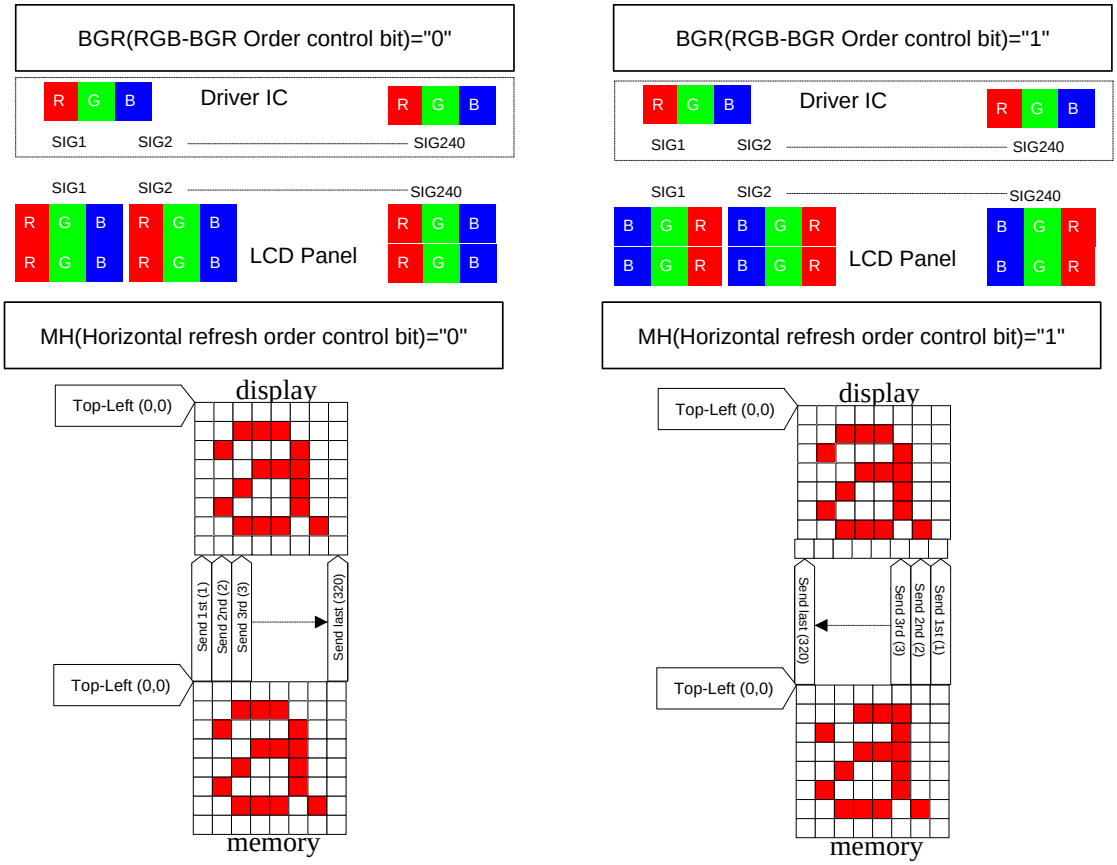
<table>
<tr><td>36h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>BGR</td><td>MH</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits control MCU to memory write/read direction.</td></tr>
<tr><td>MX</td><td>Column Address Order</td></tr>
<tr><td>MV</td><td>Row / Column Exchange</td></tr>
<tr><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr>
<tr><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr>
<tr><td>MH</td><td>Horizontal Refresh ORDER</td><td>LCD horizontal refreshing direction control.</td></tr>
</table>
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.
X = Don’t care.
MV(Row / Column Exchange bit)="0"


MV(Row / Column Exchange bit)="1"


MV(Vertical refresh order bit)="0"


MV(Vertical refresh order bit)="1"


</td></tr>
</table>



Note: Top-Left (0,0) means a physical memory location.

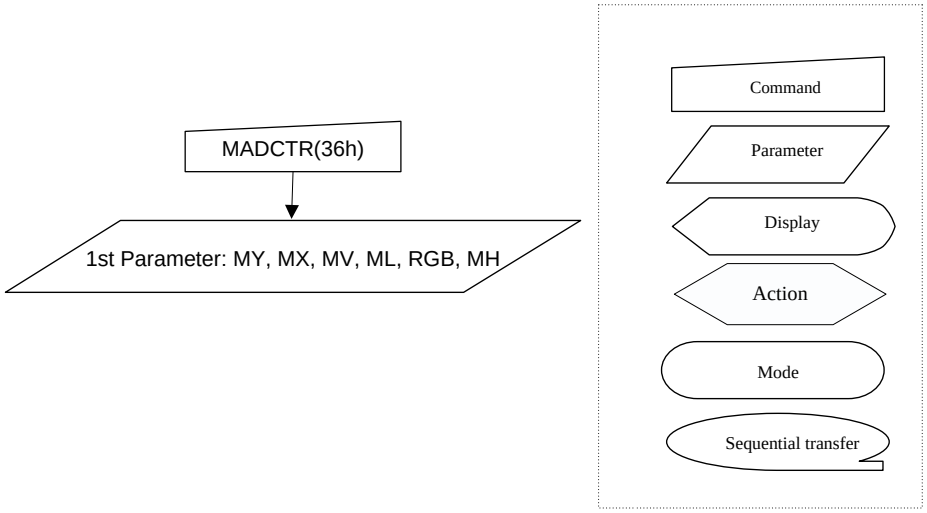
Restriction	This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

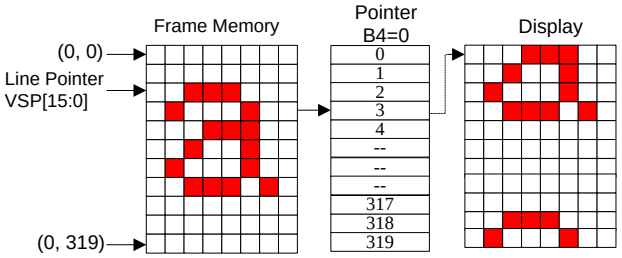
Default

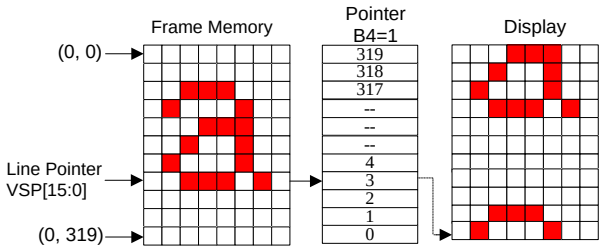
Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart	

MADCTR(36h)
1st Parameter: MY, MX, MV, ML, RGB, MH
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.29. Vertical Scrolling Start Address (37h)

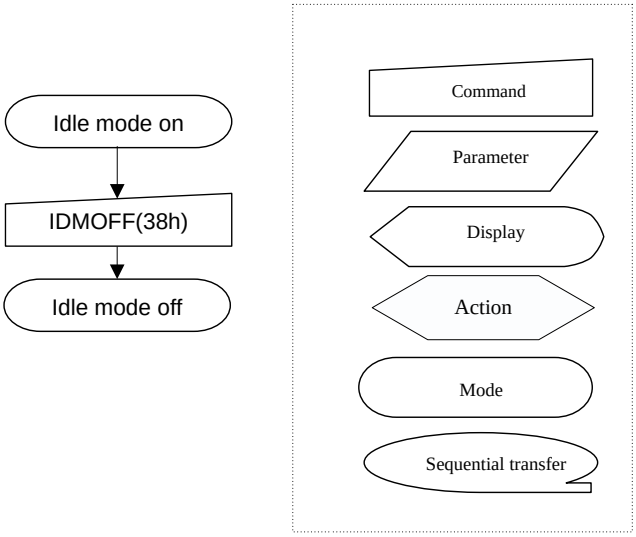
<table>
<tr><td>37h</td><td colspan="13">VSCRSADD (Vertical Scrolling Start Address)</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>37h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">00</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">SSA [7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area
and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:
When MADCTL B4=0
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP='3'.
 

When MADCTL B4=1
Example:
When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 162 and VSP='3'.
 

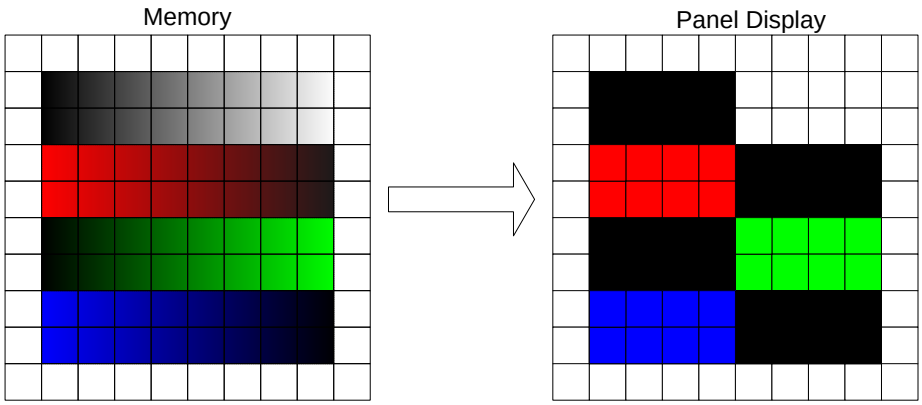
Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.
(2) This command is ignored when the GC9102 enters Partial mode.
X = Don't care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
</table>

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [7:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>SW Reset</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.30. Idle Mode OFF (38h)

<table>
<tr><td>38h</td><td colspan="13">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

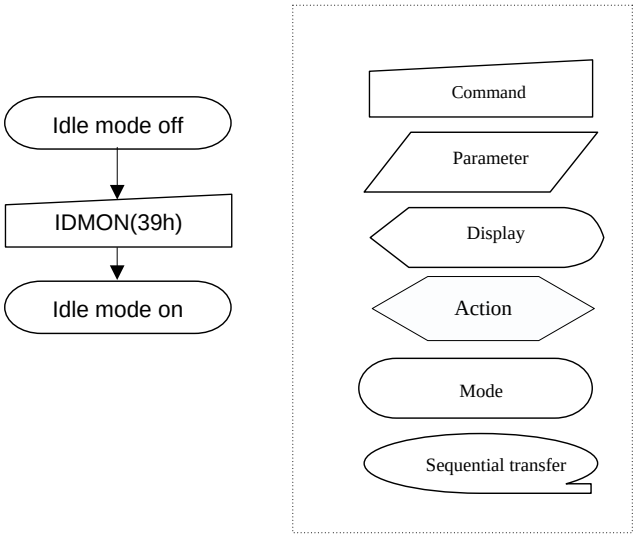
6.2.31. Idle Mode ON (39h)

<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
 
<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

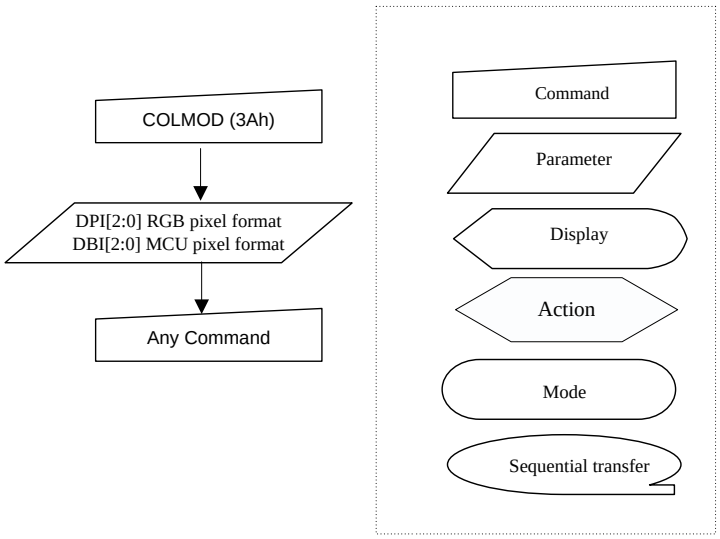
Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



6.2.32. COLMOD: Pixel Format Set (3Ah)

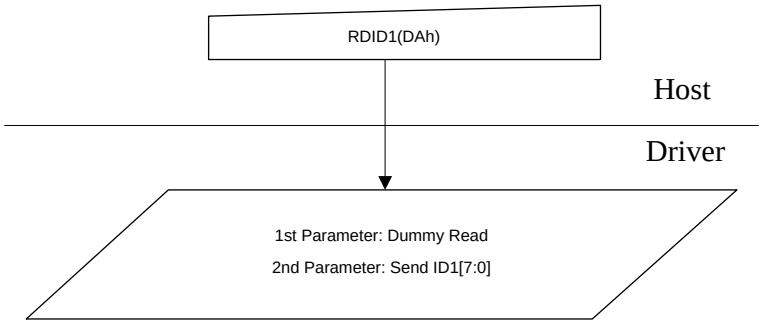
<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">IFPF [2:0]</td><td>06H</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. IFPF [2:0] is the pixel format of MCU interface. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">IFPF [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>12 bits / pixel</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td colspan="3">others</td><td>Reserved</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>IFPF [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

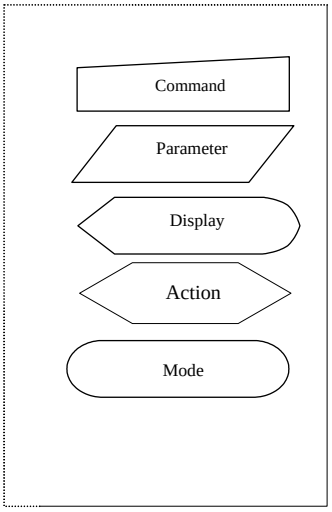
Flow Chart	

COLMOD (3Ah)
DPI[2:0] RGB pixel format
DBI[2:0] MCU pixel format
Any Command
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.33. Read ID1 (DAh)

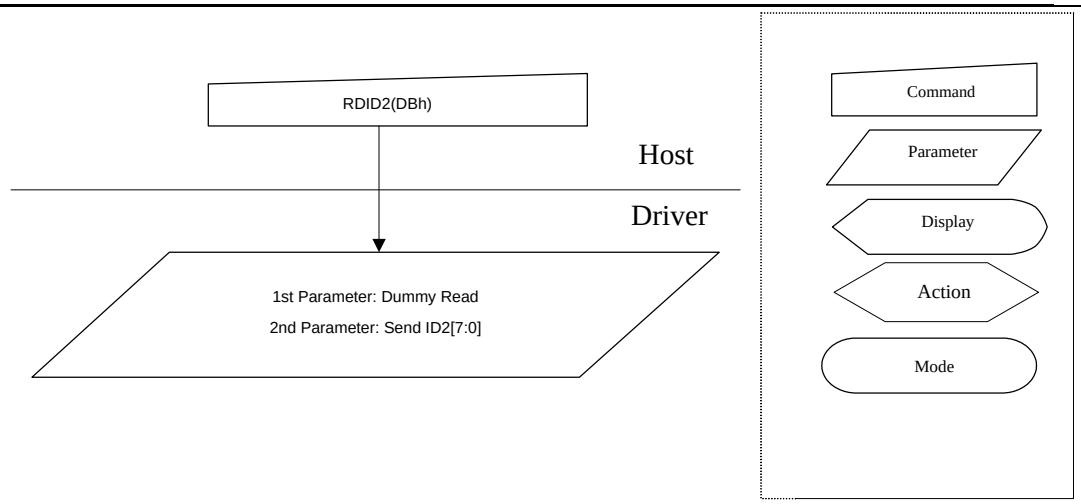
<table>
<tr><td>DAh</td><td colspan="13">Read ID1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DAh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID1 [7:0]</td><td>7C</td></tr>
<tr><td>Description</td><td colspan="13">This read byte identifies the LCD module’s manufacturer ID and it is specified by User
The 1st parameter is dummy data.
The 2nd parameter is LCD module’s manufacturer ID.
The ID2 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value (Before MTP program)</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h7Ch</td><td>MTP value</td></tr><tr><td>SW Reset</td><td rowspan="2">8’h7Ch</td><td>MTP value</td></tr><tr><td>HW Reset</td><td>MTP value</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDID1(DAh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID1[7:0]


Command
Parameter
Display
Action
Mode

6.2.34. Read ID2 (DBh)

<table>
<tr><td>DBh</td><td colspan="13">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DBh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID2 [7:0]</td><td>89</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.
The ID2 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value
(Before MTP program)</th><th>Default Value
(After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h89</td><td>MTP value</td></tr><tr><td>SW Reset</td><td>8’h89</td><td>MTP value</td></tr><tr><td>HW Reset</td><td>8’h89</td><td>MTP value</td></tr></table></td></tr>
</table>

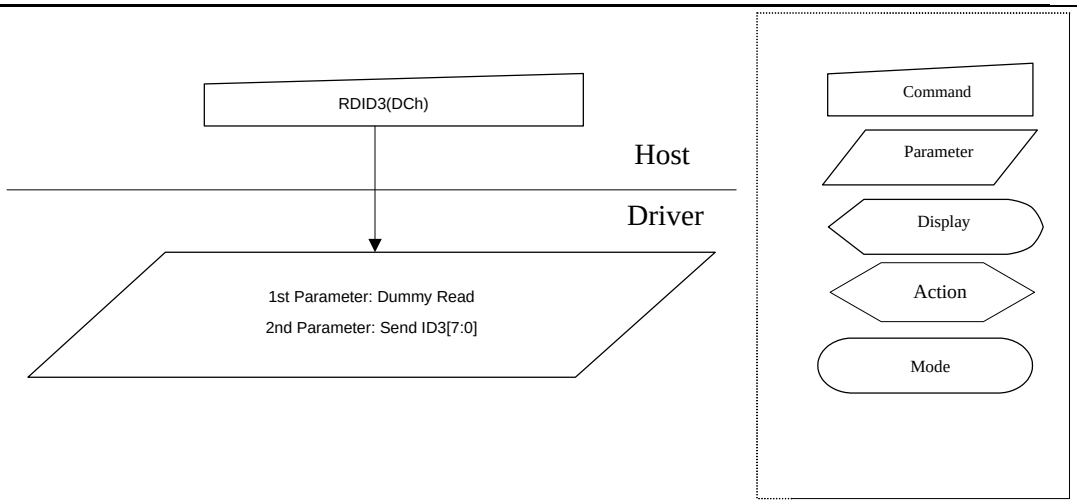
Flow Chart	

RDID2(DBh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID2[7:0]
Command
Parameter
Display
Action
Mode

6.2.35. Read ID3 (DCh)

<table>
<tr><td>DCh</td><td colspan="13">Read ID3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>DCh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">ID3 [7:0]</td><td>F0</td></tr>
<tr><td>Description</td><td colspan="13">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.
The ID3 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value
(Before MTP program)</th><th>Default Value
(After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’hF0</td><td>MTP value</td></tr><tr><td>SW Reset</td><td>8’hF0</td><td>MTP value</td></tr><tr><td>HW Reset</td><td>8’hF0</td><td>MTP value</td></tr></table></td></tr>
</table>

Flow Chart


RDID3(DCh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send ID3[7:0]
Command
Parameter
Display
Action
Mode

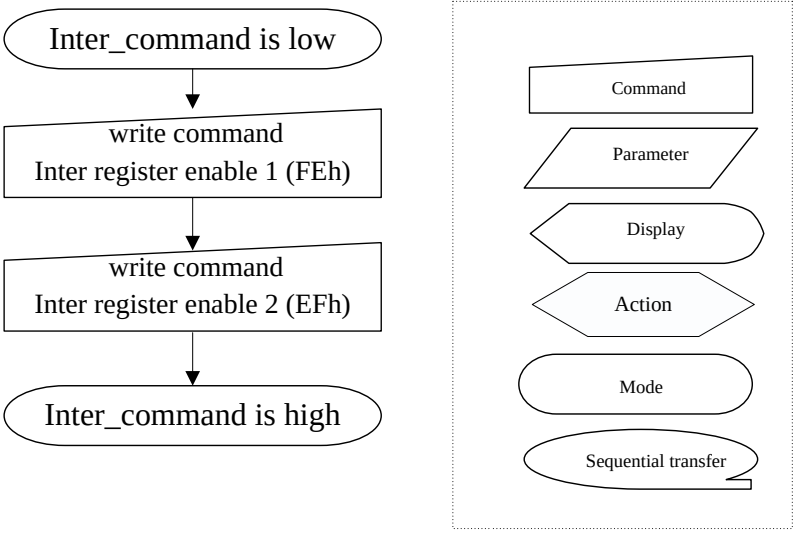
6.3. Description of Level 2 Command

6.3.1. Display Inversion Control (B4h)

<table>
<tr><td>E1h</td><td colspan="13">Frame Rate and Display Inversion Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>E1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>NLA</td><td>NLB</td><td>NLC</td><td>07</td></tr>
<tr><td>Description</td><td colspan="13">Display inversion mode set
NLA: Inversion setting in full colors normal mode(Normal mode on)
<table>
<tr><td>NLA</td><td>Inversion</td></tr>
<tr><td>0</td><td>Line inversion</td></tr>
<tr><td>1</td><td>Frame inversion</td></tr>
</table>
NLB: Inversion setting in Idle mode (Idle mode on)
<table>
<tr><td>NLB</td><td>Inversion</td></tr>
<tr><td>0</td><td>Line inversion</td></tr>
<tr><td>1</td><td>Frame inversion</td></tr>
</table>
NLC: inversion setting in partial mode (partial mode on / Idle mode off)
<table>
<tr><td>NLC</td><td>Inversion</td></tr>
<tr><td>0</td><td>Line inversion</td></tr>
<tr><td>1</td><td>Frame inversion</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><td>Status</td><td>Availability</td></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><td rowspan="2">Status</td><td>Default Value</td></tr>
<tr><td>INV_CTL</td></tr>
<tr><td>Power On Sequence</td><td>3’h7</td></tr>
<tr><td>SW Reset</td><td>3’h7</td></tr>
<tr><td>HW Reset</td><td>3’h7</td></tr>
</table></td></tr>
</table>

6.4. Description of Level 3 Command

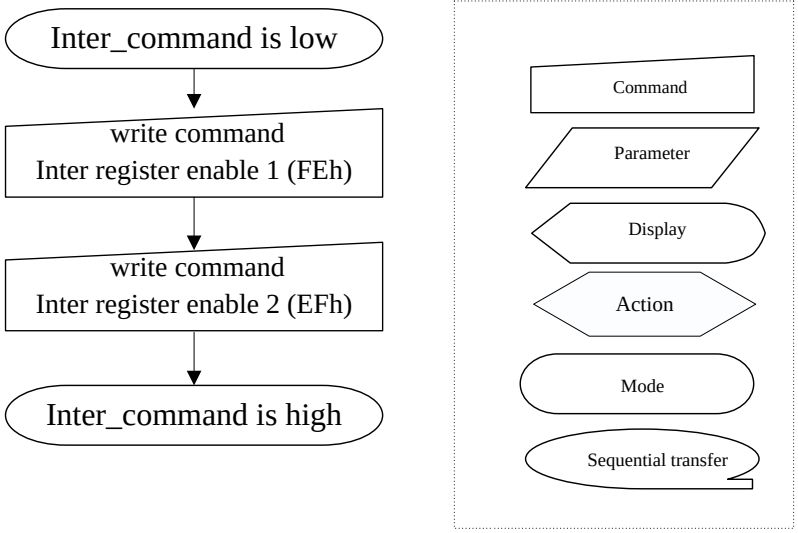
6.4.1. Inter register enable 1 (FEh)

FEh	Inter register enable 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high, you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.2. Inter register enable 2 (EFh)

<table>
<tr><td>EFh</td><td colspan="13">Inter register enable 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>EFh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high, you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.3. Frame Rate (A3h)

<table>
<tr><td>A3h</td><td colspan="13">Frame Rate and Display Inversion Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>A3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="7">RTN1 [6:0]</td><td>16h</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>RTN_SEL</td><td colspan="7">RTN2 [6:0]</td><td>16h</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="7">RTN3 [6:0]</td><td>16h</td></tr>
<tr><td>Description</td><td colspan="13">RTN_SEL: select RTN
<table><tr><th>RTN_SEL</th><th>RTN</th></tr><tr><td>1</td><td>rtn1, rtn2 , rtn3 all effect</td></tr><tr><td>0</td><td>Only rtn1 effect</td></tr></table>
RTN1/RTN2/RTN3 [6:0] Set the frame rate when the internal resistor is used for oscillator circuit.

If rtn_sel = 0 ,only RTN1 effect
Frame rate = (64+3 * RTN1)/(131*64)

If rtn_sel = 1, RTN1,RTN2,RTN3 all effect
Frame Rate = (64+ RTN1+RTN2+RTN3)/(131*64)</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr><tr><th>RTN_SEL</th><th>RTN1[6:0]</th><th>RTN2[6:0]</th><th>RTN3[6:0]</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>6’h16</td><td>6’h16</td><td>6’h16</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>6’h16</td><td>6’h16</td><td>6’h16</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>6’h16</td><td>6’h16</td><td>6’h16</td></tr></table></td></tr>
</table>

6.4.4. Power Control 1 (A4h)

A4h	Power control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	0	0	1	0	0	A4h
1st Parameter	1	1	1	XX	VCIRE	X	VRH[5:0]						16

Description

VRH [5:0] Set the voltage level value to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VCIRE: Select the external reference voltage VDD or internal reference voltage V22.

VCIRE=0	Internal reference voltage 2.2V (default)
VCIRE =1	External reference voltage VDD

When Vcire =0

VRH[5:0]	VREG1OUT	VRH[5:0]	VREG1OUT
6'h00	3.406	6'h16	4.507
6'h01	3.456	6'h17	4.557
6'h02	3.506	6'h18	4.607
6'h03	3.556	6'h19	4.658
6'h04	3.606	6'h1a	4.708
6'h05	3.656	6'h1b	4.758
6'h06	3.706	6'h1c	4.808
6'h07	3.756	6'h1d	4.858
6'h08	3.806	6'h1e	4.908
6'h09	3.856	6'h1f	4.958
6'h0a	3.906	6'h20	5.008
6'h0b	3.956	6'h21	5.058
6'h0c	4.007	6'h22	5.108
6'h0d	4.057	6'h23	5.158
6'h0e	4.107	6'h24	5.208
6'h0f	4.157	6'h25	5.259
6'h10	4.207	6'h26	5.309
6'h11	4.257	6'h27	5.359
6'h12	4.307	6'h28	5.409
6'h13	4.357	6'h29	5.459
6'h14	4.407	6'h2a~6'h3f	N/A
6'h15	4.457		

When Vcire=1

VRH[5:0]	VREG1OUT	VRH[5:0]	VREG1OUT
6'h00	3.256	6'h16	4.357
6'h01	3.306	6'h17	4.407
6'h02	3.356	6'h18	4.457
6'h03	3.406	6'h19	4.507
6'h04	3.456	6'h1a	4.557
6'h05	3.506	6'h1b	4.607
6'h06	3.556	6'h1c	4.658
6'h07	3.606	6'h1d	4.708
6'h08	3.656	6'h1e	4.758
6'h09	3.706	6'h1f	4.808
6'h0a	3.756	6'h20	4.858
6'h0b	3.806	6'h21	4.908
6'h0c	3.856	6'h22	4.958
6'h0d	3.906	6'h23	5.008
6'h0e	3.956	6'h24	5.058
6'h0f	4.007	6'h25	5.108
6'h10	4.057	6'h26	5.158
6'h11	4.107	6'h27	5.208
6'h12	4.157	6'h28	5.259
6'h13	4.207	6'h29	5.309
6'h14	4.257	6'h2a~6'h3f	N/A
6'h15	4.307		

Restriction: Inter_command should be set high to enable this command

Default

Status	Default Value	
	VCIRE	VRH[3:0]
Power On Sequence	1’b0	6’h16
SW Reset	1’b0	6’h16
HW Reset	1’b0	6’h16

6.4.5. Power Control 2 (EDh)

EDh	Power control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	0	1	EDh
1st Parameter	1	1	↑	XX	DC1[3:0]				DC0[3:0]				11
2nd Parameter	1	1	↑	XX	0	0	0	0	DC2[3:0]				06

Description

DC0 [2:0]: Selects the operating frequency of the ddvdh_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC1 [2:0]: Selects the operating frequency of the vcl_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC2 [2:0]: Selects the operating frequency of the vgh_vgl_clk. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC0 [3:0]	ddvdh_clk frequency	DC1 [3:0]	vcl_clk frequency	DC2 [3:0]	vgh_vgl_clk frequency
16'h0	Fosc/2	16'h0	Fosc/2	16'h0	Fosc/2
16'h1	Fosc/3	16'h1	Fosc/3	16'h1	Fosc/3
16'h2	Fosc/4	16'h2	Fosc/4	16'h2	Fosc/4
16'h3	Fosc/5	16'h3	Fosc/5	16'h3	Fosc/5
16'h4	Fosc/6	16'h4	Fosc/6	16'h4	Fosc/6
16'h5	Fosc/7	16'h5	Fosc/7	16'h5	Fosc/7
16'h6	Fosc/8	16'h6	Fosc/8	16'h6	Fosc/8
16'h7	Fosc/9	16'h7	Fosc/9	16'h7	Fosc/9
16'h8	Fosc/10	16'h8	Fosc/10	16'h8	Fosc/10
16'h9	Fosc/12	16'h9	Fosc/12	16'h9	Fosc/12
16'hA	Fosc/16	16'hA	Fosc/16	16'hA	Fosc/16
16'hB	Fosc/20	16'hB	Fosc/20	16'hB	Fosc/20
16'hC	Fosc/30	16'hC	Fosc/30	16'hC	Fosc/30
16'hD	Fosc/60	16'hD	Fosc/60	16'hD	Fosc/60
Other	Fosc/3	Other	Fosc/3	Other	Fosc/3

<table>
<tr><td>Restriction</td><td>Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>DC0 [3:0]</th><th>DC1[3:0]</th><th>DC2 [3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’h1</td><td>4’h1</td><td>4’h6</td></tr>
<tr><td>SW Reset</td><td>4’h1</td><td>4’h1</td><td>4’h6</td></tr>
<tr><td>HW Reset</td><td>4’h1</td><td>4’h1</td><td>4’h6</td></tr>
</table>
</td></tr>
</table>

6.4.6. Power Control 3 (FDh)

FDh	Power control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh
1st Parameter	1	1	↑	XX	X	X	VCM[5:0]						1C

Description

VCM[5:0] Set the internal VcomH voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH (*VREG1OUT)	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH (*VREG1OUT)
0	0	0	0	0	0	0.685	1	0	0	0	0	0	0.845
0	0	0	0	0	1	0.690	1	0	0	0	0	1	0.850
0	0	0	0	1	0	0.695	1	0	0	0	1	0	0.855
0	0	0	0	1	1	0.700	1	0	0	0	1	1	0.860
0	0	0	1	0	0	0.705	1	0	0	1	0	0	0.865
0	0	0	1	0	1	0.710	1	0	0	1	0	1	0.870
0	0	0	1	1	0	0.715	1	0	0	1	1	0	0.875
0	0	0	1	1	1	0.720	1	0	0	1	1	1	0.880
0	0	1	0	0	0	0.725	1	0	1	0	0	0	0.885
0	0	1	0	0	1	0.730	1	0	1	0	0	1	0.890
0	0	1	0	1	0	0.735	1	0	1	0	1	0	0.895
0	0	1	0	1	1	0.740	1	0	1	0	1	1	0.900
0	0	1	1	0	0	0.745	1	0	1	1	0	0	0.905
0	0	1	1	0	1	0.750	1	0	1	1	0	1	0.910
0	0	1	1	1	0	0.755	1	0	1	1	1	0	0.915
0	0	1	1	1	1	0.760	1	0	1	1	1	1	0.920
0	1	0	0	0	0	0.765	1	1	0	0	0	0	0.925
0	1	0	0	0	1	0.770	1	1	0	0	0	1	0.930
0	1	0	0	1	0	0.775	1	1	0	0	1	0	0.935
0	1	0	0	1	1	0.780	1	1	0	0	1	1	0.940
0	1	0	1	0	0	0.785	1	1	0	1	0	0	0.945
0	1	0	1	0	1	0.790	1	1	0	1	0	1	0.950
0	1	0	1	1	0	0.795	1	1	0	1	1	0	0.955
0	1	0	1	1	1	0.800	1	1	0	1	1	1	0.960
0	1	1	0	0	0	0.805	1	1	1	0	0	0	0.965
0	1	1	0	0	1	0.810	1	1	1	0	0	1	0.970
0	1	1	0	1	0	0.815	1	1	1	0	1	0	0.975
0	1	1	0	1	1	0.820	1	1	1	0	1	1	0.980
0	1	1	1	0	0	0.825	1	1	1	1	0	0	0.985
0	1	1	1	0	1	0.830	1	1	1	1	0	1	0.990
0	1	1	1	1	0	0.835	1	1	1	1	1	0	0.995
0	1	1	1	1	1	0.840	1	1	1	1	1	1	1.000

Restriction	Inter_command should be set high to enable this command

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VCM[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>5’h1c</td></tr>
<tr><td>SW Reset</td><td>5’h1c</td></tr>
<tr><td>HW Reset</td><td>5’h1c</td></tr>
</table>
</td></tr>
</table>

6.4.7. Power Control 4 (FFh)

<table>
<tr><td>FFh</td><td colspan="13">Power control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>FFh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td colspan="5">VDV[4:0]</td><td>16</td></tr>
<tr><td>Description</td><td colspan="13">VDV[4:0] Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 xVREG1OUT .
<table>
<tr><th>VDV4</th><th>VDV3</th><th>VDV2</th><th>VDV1</th><th>VDV0</th><th>VCOM Amplitude (*VREG1OUT)</th><th>VDV4</th><th>VDV3</th><th>VDV2</th><th>VDV1</th><th>VDV0</th><th>VCOM Amplitude (*VREG1OUT)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0.70</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0.94</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0.72</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0.96</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0.74</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0.98</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0.76</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1.00</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0.78</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1.02</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0.80</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1.04</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0.82</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1.06</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0.84</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1.08</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0.86</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1.10</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0.88</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1.12</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0.90</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1.14</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0.92</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1.16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0.94</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1.18</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0.96</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1.20</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0.98</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1.22</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1.00</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1.24</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

<table>
<tr>
<td>Default</td>
<td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VDV[4:0]</th></tr>
<tr><td>Power On Sequence</td><td>5’h16</td></tr>
<tr><td>SW Reset</td><td>5’h16</td></tr>
<tr><td>HW Reset</td><td>5’h16</td></tr>
</table>
</td>
</tr>
</table>

6.4.8. SET_GAMMA1 (F0h)

<table>
<tr><td>F0h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KP1[2:0]</td><td>X</td><td colspan="3">KP0[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">KP1-0[2:0] : γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KP1[2:0]</th><th>KP0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h0</td><td>3’h0</td></tr><tr><td>SW Reset</td><td>3’h0</td><td>3’h0</td></tr><tr><td>HW Reset</td><td>3’h0</td><td>3’h0</td></tr></table></td></tr>
</table>

6.4.9. SET_GAMMA2 (F1h)

<table>
<tr><td>F1h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>F1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KP3[2:0]</td><td>X</td><td colspan="3">KP2[2:0]</td><td>55</td></tr>
<tr><td>Description</td><td colspan="13">KP3-2[2:0] : γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KP3[2:0]</th><th>KP2[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h5</td><td>3’h5</td></tr><tr><td>SW Reset</td><td>3’h5</td><td>3’h5</td></tr><tr><td>HW Reset</td><td>3’h5</td><td>3’h5</td></tr></table></td></tr>
</table>

6.4.10. SET_GAMMA3 (F2h)

<table>
<tr><td>F2h</td><td colspan="13">SET_GAMMA3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>F2h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KP5[2:0]</td><td>X</td><td colspan="3">KP4[2:0]</td><td>07</td></tr>
<tr><td>Description</td><td colspan="13">KP5-4[2:0] : γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KP5[2:0]</th><th>KP4[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h0</td><td>3’h7</td></tr><tr><td>SW Reset</td><td>3’h0</td><td>3’h7</td></tr><tr><td>HW Reset</td><td>3’h0</td><td>3’h7</td></tr></table></td></tr>
</table>

6.4.11. SET_GAMMA4 (F3h)

<table>
<tr><td>F3h</td><td colspan="13">SET_GAMMA4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">RP1[2:0]</td><td>X</td><td colspan="3">RP0[2:0]</td><td>52</td></tr>
<tr><td>Description</td><td colspan="13">RP1-0[2:0] : γ gradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>RP1[2:0]</th><th>RP0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h5</td><td>3’h2</td></tr><tr><td>SW Reset</td><td>3’h5</td><td>3’h2</td></tr><tr><td>HW Reset</td><td>3’h5</td><td>3’h2</td></tr></table></td></tr>
</table>

6.4.12. SET_GAMMA5 (F4h)

<table>
<tr><td>F4h</td><td colspan="13">SET_GAMMA5</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>F4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="4">VRP0[3:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VRP0[4:0] : γ amplitude adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VRP0[3:0]</th></tr><tr><td>Power On Sequence</td><td>4’h00</td></tr><tr><td>SW Reset</td><td>4’h00</td></tr><tr><td>HW Reset</td><td>4’h00</td></tr></table></td></tr>
</table>

6.4.13. SET_GAMMA6 (F5h)

<table>
<tr><td>F5h</td><td colspan="13">SET_GAMMA6</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>F5h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">VRP1[3:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VRP1[4:0] : γ amplitude adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VRP1[3:0]</th></tr><tr><td>Power On Sequence</td><td>4’h00</td></tr><tr><td>SW Reset</td><td>4’h00</td></tr><tr><td>HW Reset</td><td>4’h00</td></tr></table></td></tr>
</table>

6.4.14. SET_GAMMA7(F7h)

<table>
<tr><td>F7h</td><td colspan="13">SET_GAMMA7</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>F7h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KN1[2:0]</td><td>X</td><td colspan="3">KN0[2:0]</td><td>07</td></tr>
<tr><td>Description</td><td colspan="13">KN1-0[2:0] : γfine adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KN1[2:0]</th><th>KN0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’b0</td><td>3’h7</td></tr><tr><td>SW Reset</td><td>3’b0</td><td>3’h7</td></tr><tr><td>HW Reset</td><td>3’b0</td><td>3’h7</td></tr></table></td></tr>
</table>

6.4.15. SET_GAMMA8(F8h)

<table>
<tr><td>F8h</td><td colspan="13">SET_GAMMA8</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>F8h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KN3[2:0]</td><td>X</td><td colspan="3">KN2[2:0]</td><td>22</td></tr>
<tr><td>Description</td><td colspan="13">KN3-2[2:0] : γ fine adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KN3[2:0]</th><th>KN2[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h2</td><td>3’h2</td></tr><tr><td>SW Reset</td><td>3’h2</td><td>3’h2</td></tr><tr><td>HW Reset</td><td>3’h2</td><td>3’h2</td></tr></table></td></tr>
</table>

6.4.16. SET_GAMMA9(F9h)

<table>
<tr><td>F9h</td><td colspan="13">SET_GAMMA9</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>F9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KN5[2:0]</td><td>X</td><td colspan="3">KN4[2:0]</td><td>77</td></tr>
<tr><td>Description</td><td colspan="13">KN5-4[2:0] : γ fine adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KN5[2:0]</th><th>KN4[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h7</td><td>3’h7</td></tr><tr><td>SW Reset</td><td>3’h7</td><td>3’h7</td></tr><tr><td>HW Reset</td><td>3’h7</td><td>3’h7</td></tr></table></td></tr>
</table>

6.4.17. SET_GAMMA10(FAh)

<table>
<tr><td>FAh</td><td colspan="13">SET_GAMMA10</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>FAh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">RN1[2:0]</td><td>X</td><td colspan="3">RN0[2:0]</td><td>25</td></tr>
<tr><td>Description</td><td colspan="13">RN1-0[2:0] : γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>RN1[2:0]</th><th>RN0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h2</td><td>3’h5</td></tr><tr><td>SW Reset</td><td>3’h2</td><td>3’h5</td></tr><tr><td>HW Reset</td><td>3’h2</td><td>3’h5</td></tr></table></td></tr>
</table>

6.4.18. SET_GAMMA11(FBh)

<table>
<tr><td>FBh</td><td colspan="13">SET_GAMMA11</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>FBh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="4">VRN0[3:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VRN0[3:0] : γ amplitude adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VRN0[3:0]</th></tr><tr><td>Power On Sequence</td><td>4’h0</td></tr><tr><td>SW Reset</td><td>4’h0</td></tr><tr><td>HW Reset</td><td>4’h0</td></tr></table></td></tr>
</table>

6.4.19. SET_GAMMA12 (FCh)

FCh	SET_GAMMA12												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	0	FCh
1st Parameter	1	1	↑	XX	X	X	X	VRN1[4:0]					00
Description	VRN1[4:0] : γ amplitude adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VRN1[4:0]
Power On Sequence	4'h00
SW Reset	4'h00
HW Reset	4'h00

7. Electrical Characteristics

7.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9102 is used out of the absolute maximum ratings, GC9102 may be permanently damaged. To use GC9102 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9102 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VDD	V	-0.3~+4.6
Supply voltage(Logic)	VDDI	V	-0.3~+4.6
Supply voltage(Digital)	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+85
Storage temperature	Tstg	℃	-55~+110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

7.2. DC Characteristics

General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VDD	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	DGND	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or DGND	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	|VCOMH-VCOML|	4.0	-	5.5	Note3
Source Driver							

Source Output Range	Vsout	V	-	0.1	-	AVDD -0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage(Source Output channel)	Vdev	mV	Sout>=4.2V Sout<=0.8V	-	-	20	Note4
			4.2V>Sout>0.8V	-	-	15	-
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation							
1st Boost（VDD*2) Voltage	AVDD	V	-	4.95 (Note5)	-	5.5 (Note6)	Note3
1st Booster（VDD*2) Drop Voltage	VDD*2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	AVDD -0.2	

Note 1: VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, AGND=DGND=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDD voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

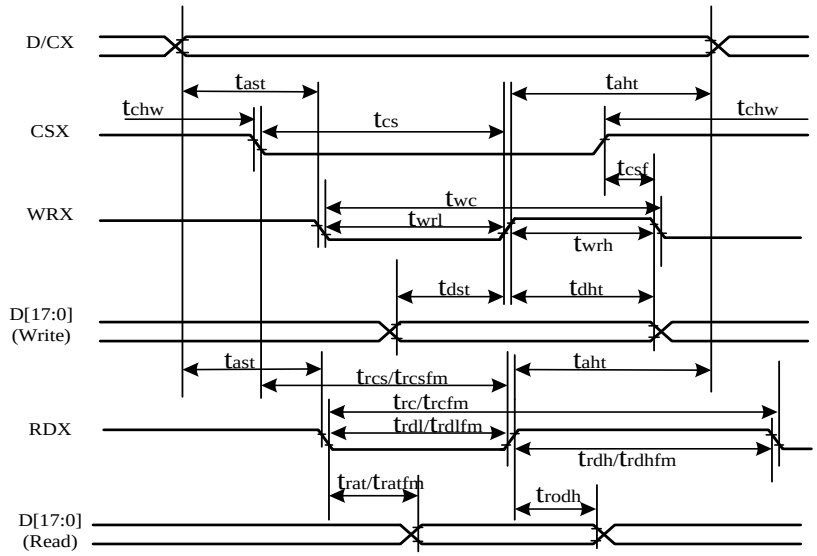
Note5: VDD=2.6V

Note6: VDD=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

7.3. AC Characteristics

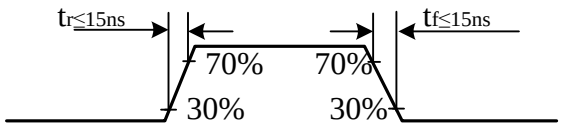
7.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080)



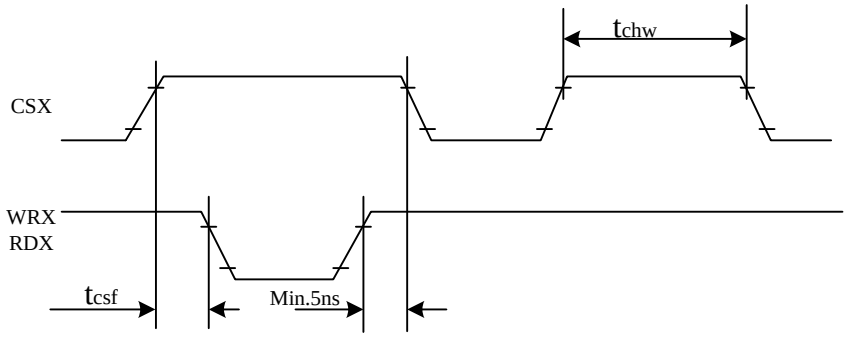
Signal	Symbol	Parameter	max	min	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	45	-	ns	
D[17:0],D[15:0],D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	

	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, DGND=0V

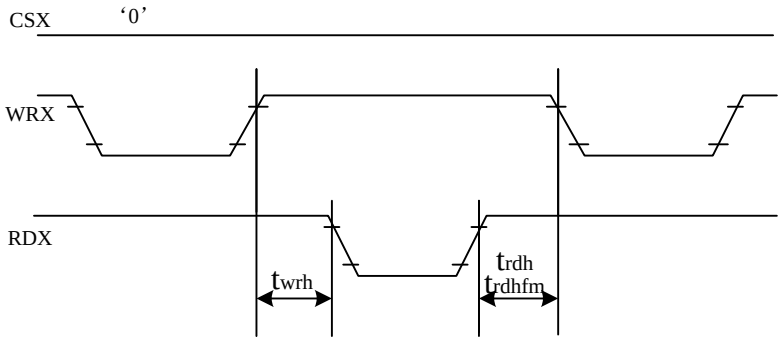


CSX timings :



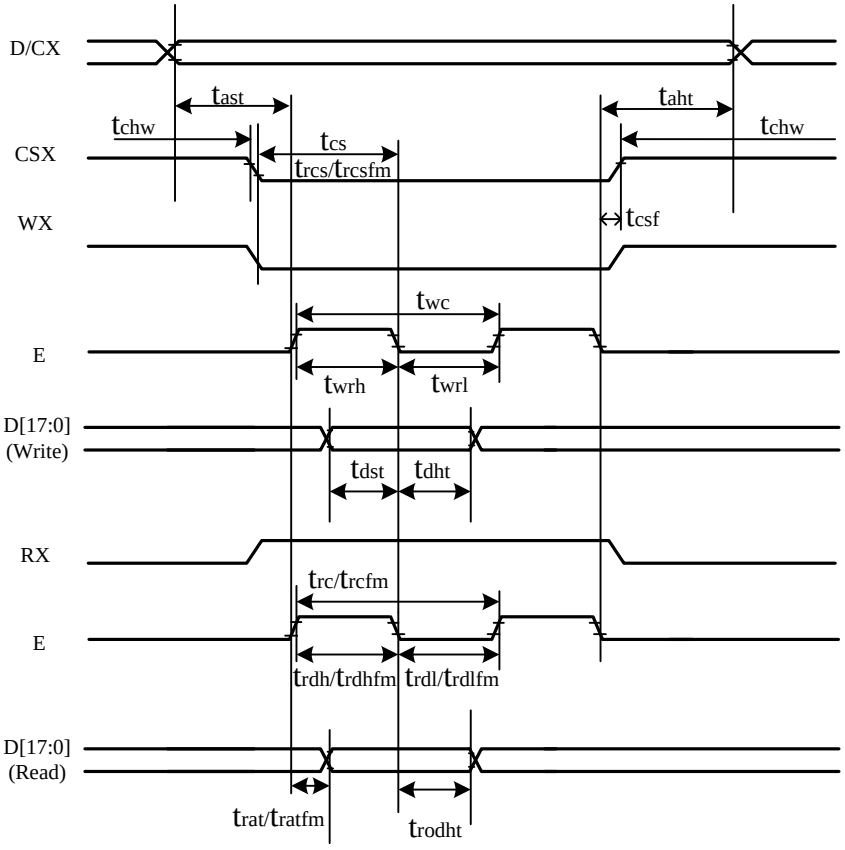
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

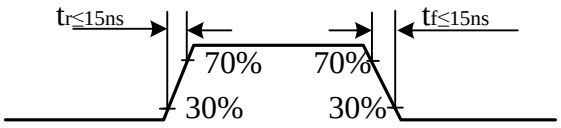
7.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (6800)



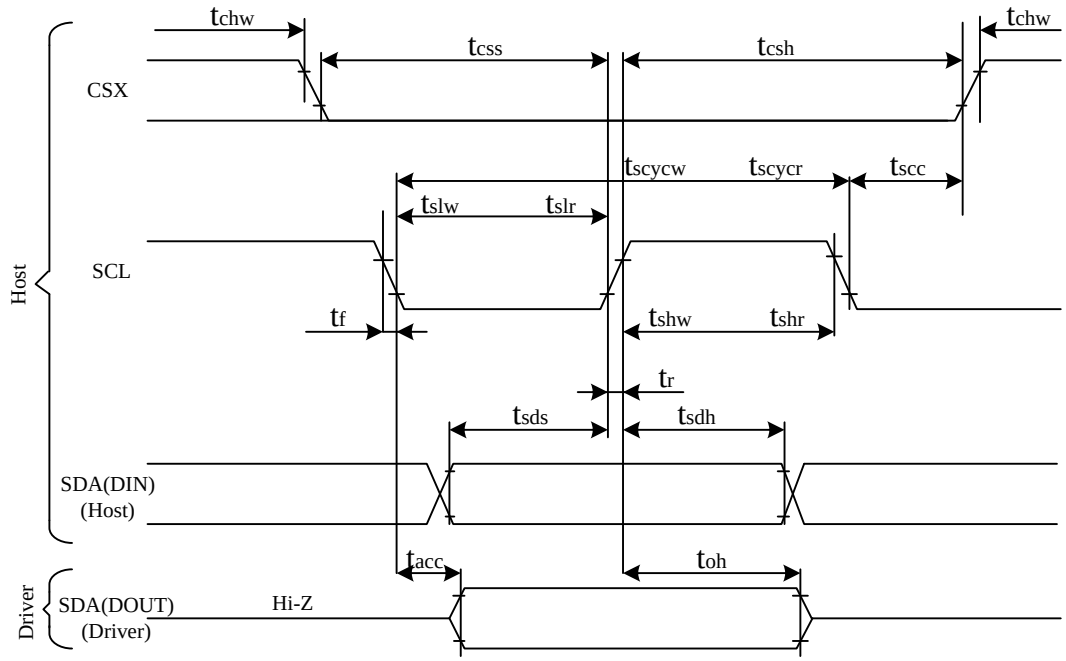
Signal	Symbol	Parameter	max	min	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0],D[17:10]& D[8:1],D[17:10],D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, DGND=0V.

Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

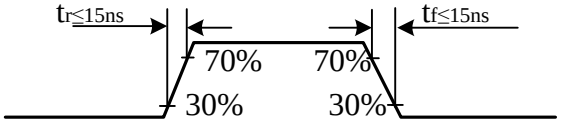


7.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

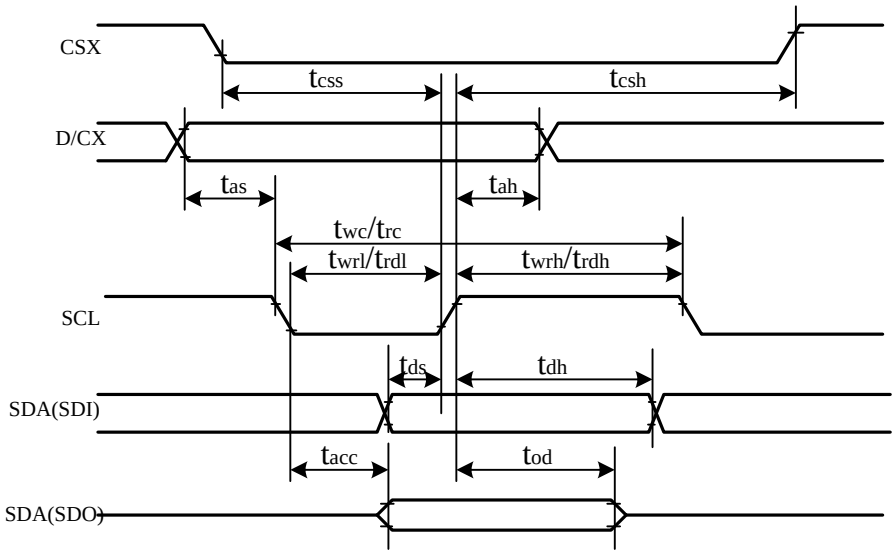


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V

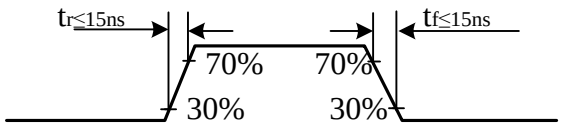


7.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	100	-	ns	
	twrh	SCL "H" Pulse Width (Write)	40	-	ns	
	twrl	SCL "L" Pulse Width (Write)	40	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	toh	Output disable time (Read)	10	50	ns	For minmum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, AGND=DGND=0V



8. Revision History

Version No.	Date	Page	Description
V1.00	2012-6-25	All	New Created
V2.00	2013-04-10	All	IC version to upgrade