a-Si TFT LCD Single Chip Driver 176RGBx220 Resolution and 262K color

Specification

Preliminary

Version: V1.00
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1. Introduction

The GC9201 is a 262,144-color single-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87,120 bytes GRAM for graphic data of 176RGBx220 dots, and power supply circuit.

The GC9201 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

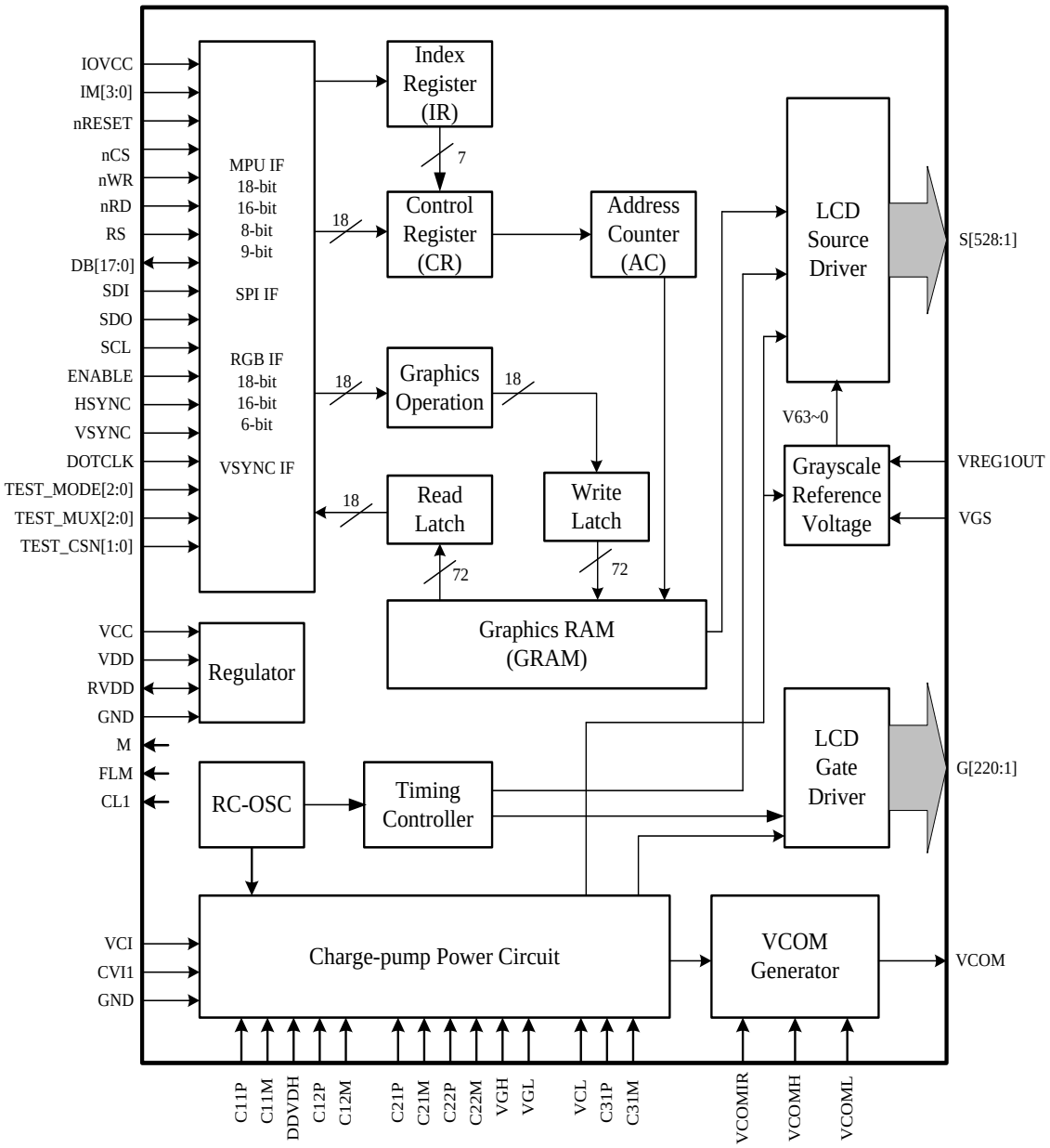
The GC9201 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9201 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9201 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [176xRGB](H) x 220(V)
- Output:
  - 528 source outputs
  - 220 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 87,120 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits bus width with i80 system interface
  - 8-bits, 9-bits, 16-bits, 18-bits bus width with m68 system interface
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - Serial Peripheral Interface (SPI)
- n-line liquid crystal AC drive: invert polarity at an interval of arbitrarily n lines (n: 1 ~ 64)
- Internal oscillator and hardware reset
- Reversible source/gate driver shift direction
- Window address function to specify a rectangular area for internal GRAM access
- Abundant functions for color display control
  - γ -correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- Power saving function:
  - 8-color mode
  - Standby mode
- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVcc(VDD3) = 1.65V ~ 3.3V (interface I/O)
    - Vci = 2.5V ~ 3.3V
  - Low voltage drive: DDVDH (DDVDH) = 4.5 ~ 5.5 V
- Operate temperature range: -40℃to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1. Block diagram



3.2. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td colspan="4">Input Interface</td></tr>
<tr><td>IM3,
IM2,
IM1,
IM0/ID</td><td>I</td><td>IOVcc</td><td>Select the MCU system interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface Mode</th><th>DB Pins in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>M68-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>M68-system 8-bit interface</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>I80-system 16-bit interface</td><td>D[17:10] D[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>I80-system 8-bit interface</td><td>D[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit 3 wires Serial Peripheral Interface</td><td>SDI,SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8-bit 4 wires Serial Peripheral Interface</td><td>SDI,SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Setting Invalid</td><td></td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>M68-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>M68-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>M68-system 9-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>M68-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting Invalid</td><td></td></tr>
</table>
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting</td></tr>
<tr><td>nCS</td><td>I</td><td>MCU
IOVcc</td><td>A chip select signal.
Low: the GC9201 is selected and accessible
High: the GC9201 is not selected and not accessible
Fix to IOVCC level when not in use.</td></tr>
<tr><td>RS</td><td>I</td><td>MCU
IOVcc</td><td>A register select signal.
Low: select an index or status register
High: select a control register
Fix to GND level when not in use.</td></tr>
<tr><td>RW_nWR
/SCL</td><td>I</td><td>MCU
IOVcc</td><td>In 68-system mode, this is used to select operation, read or write. (RW)
In 80-system mode, this serves as a write strobe signal (nWR).
In SPI mode, it serves as a synchronous clock (SCL).</td></tr>
<tr><td>E_nRD</td><td>I</td><td>MCU
IOVcc</td><td>In 68-system mode, this serves as write/read enable strobe (E).
In 80-system mode, this serves as a read strobe signal. (nRD).
Must be fixed to GND level when SPI mode.</td></tr>
<tr><td>nRESET</td><td>I</td><td>MCU
IOVcc</td><td>A reset pin.
Initializes the GC9201 with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MCU
IOVcc</td><td>18-bit parallel bi-directional data bus for MPU system interface mode
Serves as an input data bus for MPU I/F.
8-bit I/F: DB[17:10] is used.</td></tr>
</table>

Pin Name	I/O	Type	Descriptions
			9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. Serves as an input data bus for RGB I/F. 6-bit interface: DB[17:12] 16-bit interface: {DB[17:13], DB[11:1]} 18-bit interface: DB[17:0] Unused pins must be fixed GND level.
SDI/SDA	I/O	MCU IOVcc	Serial data input (SDI) pin in serial interface operation. The data is latched on the rising edge of the SCL signal. **Fix to GND level when not in use.**
SDO	O	MCU IOVcc	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. **When the SPI interface is not used, please let SDO as floating.**
DOTCLK	O	MCU IOVcc	A dot clock signal. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK **Fix to GND level when not in use**
VSYNC	I	MCU IOVcc	A frame synchronizing signal. VSPL = "0": Active low. VSPL = "1": Active high. **Fix to GND level when not in use.**
HSYNC	I	MCU IOVcc	A line synchronizing signal. HSPL = "0": Active low. HSPL = "1": Active high. **Fix to GND level when not in use.**
ENABLE	I	MCU IOVcc	A data ENEABLE signal in RGB interface mode. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. **Fix to GND level when not in use.**
LCD Driving signals			
S528~S1	O	LCD	Source output voltage signals applied to liquid crystal. To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "00000h" is output from S1 SS = "1", the data in the RAM address "00000h" is output from S528. S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G220~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines

Pin Name	I/O	Type	Descriptions
			VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
Charge-pump and Regulator Circuit			
VCOMH	O	Stabilizing capacitor	The high level of VCOM AC voltage. Connect to a stabilizing capacitor.
VCOML	O	Stabilizing capacitor	The low level of VCOM AC voltage. Connect to a stabilizing capacitor. Adjust the VCOML level with the VDV bits. When the VCOMG is set as "0", the VCOML level will be fixed to GND., and in this condition, the stabilizing capacitor is not necessary.
VCOM		open	This is a floating pad.
C11P, C11M C12P, C12M		Step-up capacitor	Connect the charge-pumping capacitor to generate DDVDH level.
C21P, C21M C22P, C22M		Step-up capacitor	Connect the charge-pumping capacitor to generate VGH, VGL level.
C31P,C31M		Step-up capacitor	Connect the charge-pumping capacitor to generate VCL level.
DDVDH	O	Stabilizing capacitor, DDVDH	An output voltage from the step-up circuit 1, twice the Vci1 level. Place a stabilizing capacitor between DDVDH and GND. DDVDH = 4.5 ~ 5.5V
VGH	O	Stabilizing capacitor, VGH	An output voltage from the step-up circuit 2, 4 ~ 6 times the Vci1 level. The step-up rate is set with the BT bits. Place a stabilizing capacitor between VGH and GND. VGH = max 16.5V
VGL	O	Stabilizing capacitor, VGL	An output voltage from the step-up circuit 2, -3 ~ -5 times the Vci1 level. The step-up rate is set with the BT bits. Place a stabilizing capacitor between VGL and GND. Place a shottkey diode between Vci. See "Configurations of Power supply circuit". VGL = min –16.5V
VCL	O	Stabilizing capacitor, VCL	An output voltage from the step-up circuit 2, –1 times the Vci1 level. Connect to a stabilizing capacitor between VCL and GND. VCL = 0 ~ –3.3V
VREG1OUT (GVDD)	O	Stabilizing capacitor or power supply	A reference voltage level. The voltage level of VREG1OUT can be adjusted by the VRH[3:0] bits. VREG1OUT is (1) a source driver grayscale reference voltage VDH, (2) a VCOMH level reference voltage, and (3) a VCOM amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V
VGS	I	GND or external resistor	A reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
VREF			Floating pin. This pin is a floating pin.

Pin Name	I/O	Type	Descriptions
DDVDH	P	Stabilizing capacitor	Generated power output pin for source driver block. Output voltage of 1st booster circuit (=2 x VCI1) This pin needs to connect a capacitor for storage function.
Power Pads			
Vci	I	Power supply	A supply voltage to the analog circuit and charge-pump. Connect this pin to an external power supply of 2.5 ~ 3.3V.
Vci1	O	Stabilizing capacitor	The amplitude between Vci and GND is determined by the VC[2:0] bits. Vci1 must be set so that the output voltages DDVDH, VGH, VGL are generated within the respective setting ranges.
IOVCC (VDD3)	I	Power supply	A supply voltage to the interface pins (IOVcc = 1.65 ~ 3.3V).
AVSS (GND)	P		GND for analog circuits
VSSC (GND)	P		GND for booster circuits.
VSS(GND)	P		GND for logic circuits.
RVDD	P	VDD	Voltage regulator output for VDD. Connect to VDD pad for supplying power. Connect a capacitor for stabilization
VDD	P	Stabilizing Capacitor	Power supply for memory and internal logic circuit. Connect this pin to regulated voltage output RVDD
Test pads			
CL1	O		Output pins used only for test purpose at vendor-side. In normal operation, leave this pin open.
FLM	O		Tearing effect output pin to synchronize MCU to frame writing, actived by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
M	O		Output pins used only for test purpose at vendor-side. In normal operation, leave this pin open.
TEST_MODE[2:0]	I		Input pins used only for test purpose In normal operation, connect this pin to GND or IOVCC.
TEXT_MUX[1:0]	I		Input pins used only for test purpose In normal operation, connect this pin to GND or IOVCC.
TEST_DA	I		Input pins used only for test purpose In normal operation, connect this pin to GND or IOVCC.
Contact	-		Contact resistance measurement pin.
EXCLK	I		Test pin In normal operation, connect this pin to GND or IOVCC.
EN_EXCLK	I		Test pin In normal operation, connect this pin to GND or IOVCC

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT data lines		528 pins (176*RGB)
2	TFT gate lines		220 pins
3	TFT Display's Capacitor Structure		Cst structure only (Common VCOM)
4	Liquid Crystal Drive Output	S1~S528	V0~V63 grayscales
		G1~G220	VGH-VGL
		VCOM	VCOMH-VCOML :Amplitude = electronic volumes
5	Input Voltage	IOVcc	1.65~3.30V
		Vci	2.50~3.30V
6	Liquid Crystal Drive Voltages	DDVDH	Vci1 x 2
		VGH	Vci1 x 4 , x 5, x 6
		VGL	Vci1 x -3, x -4, x -5
		VCL	Vci1 x -1

3.3. PAD coordinates

	Pad name	X	Y
1	DUMMY1	-6695	-253
2	DUMMY2	-6635	-253
3	VCOM	-6575	-253
4	VCOM	-6515	-253
5	VCOM	-6455	-253
6	VCOM	-6395	-253
7	DUMMY3	-6335	-253
8	VGH	-6275	-253
9	VGH	-6215	-253
10	VGH	-6155	-253
11	VGH	-6095	-253
12	VGH	-6035	-253
13	DUMMY4	-5975	-253
14	VGL	-5915	-253
15	VGL	-5855	-253
16	VGL	-5795	-253
17	VGL	-5735	-253
18	VGL	-5675	-253
19	DUMMY5	-5615	-253
20	C22P	-5555	-253
21	C22P	-5495	-253
22	C22P	-5435	-253
23	C22M	-5375	-253
24	C22M	-5315	-253
25	C22M	-5255	-253
26	C21P	-5195	-253
27	C21P	-5135	-253
28	C21P	-5075	-253
29	C21M	-5015	-253
30	C21M	-4955	-253
31	C21M	-4895	-253
32	DUMMY6	-4835	-253
33	DUMMY7	-4775	-253
34	GND	-4715	-253
35	GND	-4655	-253
36	GND	-4595	-253
37	GND	-4535	-253
38	GND	-4475	-253
39	GND	-4415	-253
40	GND	-4355	-253
41	GND	-4295	-253
42	GND	-4235	-253
43	GND	-4175	-253
44	VCI1	-4115	-253
45	VCI1	-4055	-253
46	VCI1	-3995	-253
47	VCI1	-3935	-253
48	VCI1	-3875	-253
49	VCI1	-3815	-253
50	C11P	-3755	-253

No.	Pad name	X	Y
51	C11P	-3695	-253
52	C11P	-3635	-253
53	C11P	-3575	-253
54	C11P	-3515	-253
55	C11P	-3455	-253
56	C11P	-3395	-253
57	C11P	-3335	-253
58	C11M	-3275	-253
59	C11M	-3215	-253
60	C11M	-3155	-253
61	C11M	-3095	-253
62	C11M	-3035	-253
63	C11M	-2975	-253
64	C11M	-2915	-253
65	C11M	-2855	-253
66	C12P	-2795	-253
67	C12P	-2735	-253
68	C12P	-2535	-253
69	C12P	-2615	-253
70	C12P	-2555	-253
71	C12P	-2495	-253
72	C12M	-2435	-253
73	C12M	-2375	-253
74	C12M	-2315	-253
75	C12M	-2255	-253
76	C12M	-2195	-253
77	C12M	-2135	-253
78	C31P	-2075	-253
79	C31P	-2015	-253
80	C31P	-1955	-253
81	C31P	-1895	-253
82	C31P	-1835	-253
83	C31M	-1775	-253
84	C31M	-1715	-253
85	C31M	-1655	-253
86	C31M	-1595	-253
87	VPP	-1535	-253
88	DDVDH	-1475	-253
89	DDVDH	-1415	-253
90	DDVDH	-1355	-253
91	DDVDH	-1295	-253
92	DDVDH	-1235	-253
93	DDVDH	-1175	-253
94	DDVDH	-1115	-253
95	DDVDH	-1055	-253
96	VCI	-995	-253
97	VCI	-935	-253
98	VCI	-875	-253
99	VCI	-815	-253
100	VCI	-755	-253

No.	Pad name	X	Y
101	VCI	-695	-253
102	VCI	-635	-253
103	VCI	-575	-253
104	VCI	-515	-253
105	VCI	-455	-253
106	VCL	-395	-253
107	VCL	-335	-253
108	VCL	-275	-253
109	VCL	-215	-253
110	VCL	-155	-253
111	DUMMY8	-95	-253
112	RS	-35	-253
113	CSB	25	-253
114	VSYNC	85	-253
115	HSYNC	145	-253
116	DOTCLK	205	-253
117	ENABLE	265	-253
118	RESETB	325	-253
119	SDI	385	-253
120	E_RDB	445	-253
121	RW_WRB	505	-253
122	DB<17>	565	-253
123	DB<16>	650	-253
124	DB<15>	735	-253
125	DB<14>	820	-253
126	DB<13>	905	-253
127	DB<12>	990	-253
128	DB<11>	1075	-253
129	DB<10>	1160	-253
130	DB<9>	1245	-253
131	DB<8>	1330	-253
132	DB<7>	1415	-253
133	DB<6>	1500	-253
134	DB<5>	1585	-253
135	DB<4>	1670	-253
136	DB<3>	1755	-253
137	DB<2>	1840	-253
138	DB<1>	1925	-253
139	DB<0>	2010	-253
140	IM<3>	2095	-253
141	IM<2>	2155	-253
142	IM<1>	2215	-253
143	IM<0>	2275	-253
144	SDO	2335	-253
145	M	2420	-253
146	FLM	2505	-253
147	CL1	2590	-253
148	TEST_MODE<2>	2675	-253
149	BIST_EN	2735	-253
150	TEST_MODE<0>	2795	-253

No.	Pad name	X	Y
151	TEST_MUX<2>	2855	-253
152	TEST_MUX<1>	2915	-253
153	TEST_MUX<0>	2975	-253
154	BGR_TEST	3035	-253
155	EN_EXCLK	3095	-253
156	EX_CLK	3155	-253
157	AVSS	3215	-253
158	AVSS	3275	-253
159	AVSS	3335	-253
160	AVSS	3395	-253
161	AVSS	3455	-253
162	AVSS	3515	-253
163	AVSS	3575	-253
164	AVSS	3635	-253
165	AVSS	3695	-253
166	VSS	3755	-253
167	VSS	3815	-253
168	VSS	3875	-253
169	VSS	3935	-253
170	VSS	3995	-253
171	VSS	4055	-253
172	VSS	4115	-253
173	VSS	4175	-253
174	VSS	4235	-253
175	VSS	4295	-253
176	VGS	4355	-253
177	VGS	4415	-253
178	RVDD	4475	-253
179	RVDD	4535	-253
180	RVDD	4595	-253
181	RVDD	4655	-253
182	RVDD	4715	-253
183	RVDD	4775	-253
184	VDD	4835	-253
185	VDD	4895	-253
186	VDD	4955	-253
187	VDD	5015	-253
188	VDD	5075	-253
189	VDD	5135	-253
190	IOVCC	5195	-253
191	IOVCC	5255	-253
192	IOVCC	5315	-253
193	IOVCC	5375	-253
194	IOVCC	5435	-253
195	IOVCC	5495	-253
196	DUMMY9	5555	-253
197	VREF	5615	-253
198	GVDDO	5675	-253
199	GVDDO	5735	-253
200	GVDDO	5795	-253

No.	Pad name	X	Y
201	GVDDO	5855	-253
202	VCOMH	5915	-253
203	VCOMH	5975	-253
204	VCOML	6035	-253
205	VCOML	6095	-253
206	VCOMR	6155	-253
207	CONTACT	6215	-253
208	CONTACT	6275	-253
209	DUMMY10	6335	-253
210	VCOM	6395	-253
211	VCOM	6455	-253
212	VCOM	6515	-253
213	VCOM	6575	-253
214	DUMMY11	6635	-253
215	DUMMY12	6695	-253
216	DUMMY13	6772	232
217	DUMMY14	6756	107
218	DUMMY15	6740	232
219	DUMMY16	6724	107
220	G2	6708	232
221	G4	6692	107
222	G6	6676	232
223	G8	6660	107
224	G10	6644	232
225	G12	6628	107
226	G14	6612	232
227	G16	6596	107
228	G18	6580	232
229	G20	6564	107
230	G22	6548	232
231	G24	6532	107
232	G26	6516	232
233	G28	6500	107
234	G30	6484	232
235	G32	6468	107
232	G34	6452	232
237	G36	6436	107
238	G38	6420	232
239	G40	6404	107
240	G42	6388	232
241	G44	6372	107
242	G46	6356	232
243	G48	6340	107
244	G50	6324	232
245	G52	6308	107
246	G54	6292	232
247	G56	6276	107
248	G58	6260	232
249	G60	6244	107
250	G62	6228	232

No.	Pad	X	Y
251	G64	6212	107
252	G66	6196	232
253	G68	6180	107
254	G70	6164	232
255	G72	6148	107
256	G74	6132	232
257	G76	6116	107
258	G78	6100	232
259	G80	6084	107
260	G82	6068	232
261	G84	6052	107
262	G86	6036	232
263	G88	6020	107
264	G90	6004	232
265	G92	5988	107
266	G94	5972	232
267	G96	5956	107
268	G98	5940	232
269	G100	5924	107
270	G102	5908	232
271	G104	5892	107
272	G106	5876	232
273	G108	5860	107
274	G110	5844	232
275	G112	5828	107
276	G114	5812	232
277	G116	5796	107
278	G118	5780	232
279	G120	5764	107
280	G122	5748	232
281	G124	5732	107
282	G126	5716	232
283	G128	5700	107
284	G130	5684	232
285	G132	5668	107
286	G134	5652	232
287	G136	5636	107
288	G138	5620	232
289	G140	5604	107
290	G142	5588	232
291	G144	5572	107
292	G146	5556	232
293	G148	5540	107
294	G150	5524	232
295	G152	5508	107
296	G154	5492	232
297	G156	5476	107
298	G158	5460	232
299	G160	5444	107
300	G162	5428	232

No.	Pad name	X	Y
301	G164	5412	107
302	G166	5396	232
303	G168	5380	107
304	G170	5364	232
305	G172	5348	107
306	G174	5332	232
307	G176	5316	107
308	G178	5300	232
309	G180	5284	107
310	G182	5268	232
311	G184	5252	107
312	G186	5232	232
313	G188	5220	107
314	G190	5204	232
315	G192	5188	107
316	G194	5172	232
317	G196	5156	107
318	G198	5140	232
319	G200	5124	107
320	G202	5108	232
321	G204	5092	107
322	G206	5076	232
323	G208	5060	107
324	G210	5044	232
325	G212	5028	107
326	G214	5012	232
327	G216	4996	107
328	G218	4980	232
329	G220	4964	107
330	DUMMY17	4948	232
331	DUMMY18	4932	107
332	DUMMY19	4916	232
333	DUMMY20	4900	107
334	DUMMY21	4884	232
335	DUMMY22	4868	107
336	DUMMY23	4852	232
337	DUMMY24	4836	107
338	DUMMY25	4820	232
339	S528	4804	107
340	S527	4788	232
341	S526	4772	107
342	S525	4756	232
343	S524	4740	107
344	S523	4724	232
345	S522	4708	107
346	S521	4692	232
347	S520	4676	107
348	S519	4660	232
349	S518	4644	107
350	S517	4628	232

No.	Pad name	X	Y
351	S516	4612	107
352	S515	4596	232
353	S514	4580	107
354	S513	4564	232
355	S512	4548	107
356	S511	4532	232
357	S510	4516	107
358	S509	4500	232
359	S508	4484	107
360	S507	4468	232
361	S506	4452	107
362	S505	4436	232
363	S504	4420	107
364	S503	4404	232
365	S502	4388	107
366	S501	4372	232
367	S500	4356	107
368	S499	4340	232
369	S498	4324	107
370	S497	4308	232
371	S496	4292	107
372	S495	4276	232
373	S494	4260	107
374	S493	4244	232
375	S492	4228	107
376	S491	4212	232
377	S490	4196	107
378	S489	4180	232
379	S488	4164	107
380	S487	4148	232
381	S486	4132	107
382	S485	4116	232
383	S484	4100	107
384	S483	4084	232
385	S482	4068	107
386	S481	4052	232
387	S480	4036	107
388	S479	4020	232
389	S478	4004	107
390	S477	3988	232
391	S476	3972	107
392	S475	3956	232
393	S474	3940	107
394	S473	3924	232
395	S472	3908	107
396	S471	3892	232
397	S470	3876	107
398	S469	3860	232
399	S468	3844	107
400	S467	3828	232

No.	Pad name	X	Y
401	S466	3812	107
402	S465	3796	232
403	S464	3780	107
404	S463	3764	232
405	S462	3748	107
406	S461	3732	232
407	S460	3716	107
408	S459	3700	232
409	S458	3684	107
410	S457	3668	232
411	S456	3652	107
412	S455	3636	232
413	S454	3620	107
414	S453	3604	232
415	S452	3588	107
416	S451	3572	232
417	S450	3556	107
418	S449	3540	232
419	S448	3524	107
420	S447	3508	232
421	S446	3492	107
422	S445	3476	232
423	S444	3460	107
424	S443	3444	232
425	S442	3428	107
426	S441	3412	232
427	S440	3396	107
428	S439	3380	232
429	S438	3364	107
430	S437	3348	232
431	S436	3332	107
432	S435	3316	232
433	S434	3300	107
434	S433	3284	232
435	S432	3268	107
436	S431	3252	232
437	S430	3232	107
438	S429	3220	232
439	S428	3204	107
440	S427	3188	232
441	S426	3172	107
442	S425	3156	232
443	S424	3140	107
444	S423	3124	232
445	S422	3108	107
446	S421	3092	232
447	S420	3076	107
448	S419	3060	232
449	S418	3044	107
450	S417	3028	232

No.	Pad	X	Y
451	S416	3012	107
452	S415	2996	232
453	S414	2980	107
454	S413	2964	232
455	S412	2948	107
456	S411	2932	232
457	S410	2916	107
458	S409	2900	232
459	S408	2884	107
460	S407	2868	232
461	S406	2852	107
462	S405	2836	232
463	S404	2820	107
464	S403	2804	232
465	S402	2788	107
466	S401	2772	232
467	S400	2756	107
468	S399	2740	232
469	S398	2724	107
470	S397	2708	232
471	S396	2642	107
472	S395	2626	232
473	S394	2610	107
474	S393	2594	232
475	S392	2578	107
476	S391	2562	232
477	S390	2546	107
478	S389	2530	232
479	S388	2514	107
480	S387	2498	232
481	S386	2482	107
482	S385	2466	232
483	S384	2450	107
484	S383	2434	232
485	S382	2418	107
486	S381	2402	232
487	S380	2386	107
488	S379	2370	232
489	S378	2354	107
490	S377	2338	232
491	S376	2322	107
492	S375	2306	232
493	S374	2290	107
494	S373	2274	232
495	S372	2258	107
496	S371	2242	232
497	S370	2226	107
498	S369	2210	232
499	S368	2194	107
500	S367	2178	232

No.	Pad name	X	Y
501	S366	2162	107
502	S365	2146	232
503	S364	2130	107
504	S363	2114	232
505	S362	2098	107
506	S361	2082	232
507	S360	2066	107
508	S359	2050	232
509	S358	2034	107
510	S357	2018	232
511	S356	2002	107
512	S355	1986	232
513	S354	1970	107
514	S353	1954	232
515	S352	1938	107
516	S351	1922	232
517	S350	1906	107
518	S349	1890	232
519	S348	1874	107
520	S347	1858	232
521	S346	1842	107
522	S345	1826	232
523	S344	1810	107
524	S343	1794	232
525	S342	1778	107
526	S341	1762	232
527	S340	1746	107
528	S339	1730	232
529	S338	1714	107
530	S337	1698	232
531	S336	1682	107
532	S335	1666	232
533	S334	1650	107
534	S333	1634	232
535	S332	1618	107
536	S331	1602	232
537	S330	1586	107
538	S329	1570	232
539	S328	1554	107
540	S327	1538	232
541	S326	1522	107
542	S325	1506	232
543	S324	1490	107
544	S323	1474	232
545	S322	1458	107
546	S321	1442	232
547	S320	1426	107
548	S319	1410	232
549	S318	1394	107
550	S317	1378	232

No.	Pad name	X	Y
551	S316	1362	107
552	S315	1346	232
553	S314	1330	107
554	S313	1314	232
555	S312	1298	107
556	S311	1282	232
557	S310	1266	107
558	S309	1250	232
559	S308	1234	107
560	S307	1218	232
561	S306	1202	107
562	S305	1186	232
563	S304	1170	107
564	S303	1154	232
565	S302	1138	107
566	S301	1122	232
567	S300	1106	107
568	S299	1090	232
569	S298	1074	107
570	S297	1058	232
571	S296	1042	107
572	S295	1026	232
573	S294	1010	107
574	S293	994	232
575	S292	978	107
576	S291	962	232
577	S290	946	107
578	S289	930	232
579	S288	914	107
580	S287	898	232
581	S286	882	107
582	S285	866	232
583	S284	850	107
584	S283	834	232
585	S282	818	107
586	S281	802	232
587	S280	786	107
588	S279	770	232
589	S278	754	107
590	S277	738	232
591	S276	722	107
592	S275	706	232
593	S274	690	107
594	S273	674	232
595	S272	658	107
596	S271	642	232
597	S270	626	107
598	S269	610	232
599	S268	594	107
600	S267	578	232

No.	Pad name	X	Y
601	S266	562	107
602	S265	546	232
603	S264	-554	107
604	S263	-570	232
605	S262	-586	107
606	S261	-602	232
607	S260	-618	107
608	S259	-634	232
609	S258	-650	107
610	S257	-666	232
611	S256	-682	107
612	S255	-698	232
613	S254	-714	107
614	S253	-730	232
615	S252	-746	107
616	S251	-762	232
617	S250	-778	107
618	S249	-794	232
619	S248	-810	107
620	S247	-826	232
621	S246	-842	107
622	S245	-858	232
623	S244	-874	107
624	S243	-890	232
625	S242	-906	107
626	S241	-922	232
627	S240	-938	107
628	S239	-954	232
629	S238	-970	107
630	S237	-986	232
631	S232	-1002	107
632	S235	-1018	232
633	S234	-1034	107
634	S233	-1050	232
635	S232	-1066	107
636	S231	-1082	232
637	S230	-1098	107
638	S229	-1114	232
639	S228	-1130	107
640	S227	-1146	232
641	S226	-1162	107
642	S225	-1178	232
643	S224	-1194	107
644	S223	-1210	232
645	S222	-1226	107
646	S221	-1242	232
647	S220	-1258	107
648	S219	-1274	232
649	S218	-1290	107
650	S217	-1306	232

No.	Pad	X	Y
651	S216	-1322	107
652	S215	-1338	232
653	S214	-1354	107
654	S213	-1370	232
655	S212	-1386	107
656	S211	-1402	232
657	S210	-1418	107
658	S209	-1434	232
659	S208	-1450	107
660	S207	-1466	232
661	S206	-1482	107
662	S205	-1498	232
663	S204	-1514	107
664	S203	-1530	232
665	S202	-1546	107
666	S201	-1562	232
667	S200	-1578	107
668	S199	-1594	232
669	S198	-1610	107
670	S197	-1626	232
671	S196	-1642	107
672	S195	-1658	232
673	S194	-1674	107
674	S193	-1690	232
675	S192	-1706	107
676	S191	-1722	232
677	S190	-1738	107
678	S189	-1754	232
679	S188	-1770	107
680	S187	-1786	232
681	S186	-1802	107
682	S185	-1818	232
683	S184	-1834	107
684	S183	-1850	232
685	S182	-1866	107
686	S181	-1882	232
687	S180	-1898	107
688	S179	-1914	232
689	S178	-1930	107
690	S177	-1946	232
691	S176	-1962	107
692	S175	-1978	232
693	S174	-1994	107
694	S173	-2010	232
695	S172	-2026	107
696	S171	-2042	232
697	S170	-2058	107
698	S169	-2074	232
699	S168	-2090	107
700	S167	-2106	232

No.	Pad name	X	Y
701	S166	-2122	107
702	S165	-2138	232
703	S164	-2154	107
704	S163	-2170	232
705	S162	-2186	107
706	S161	-2202	232
707	S160	-2218	107
708	S159	-2234	232
709	S158	-2250	107
710	S157	-2266	232
711	S156	-2282	107
712	S155	-2298	232
713	S154	-2314	107
714	S153	-2330	232
715	S152	-2346	107
716	S151	-2322	232
717	S150	-2378	107
718	S149	-2394	232
719	S148	-2410	107
720	S147	-2426	232
721	S146	-2442	107
722	S145	-2458	232
723	S144	-2474	107
724	S143	-2490	232
725	S142	-2506	107
726	S141	-2522	232
727	S140	-2538	107
728	S139	-2554	232
729	S138	-2570	107
730	S137	-2586	232
731	S136	-2602	107
732	S135	-2618	232
733	S134	-2634	107
734	S133	-2650	232
735	S132	-2716	107
736	S131	-2732	232
737	S130	-2748	107
738	S129	-2764	232
739	S128	-2780	107
740	S127	-2796	232
741	S126	-2812	107
742	S125	-2828	232
743	S124	-2844	107
744	S123	-2860	232
745	S122	-2876	107
746	S121	-2892	232
747	S120	-2908	107
748	S119	-2924	232
749	S118	-2940	107
750	S117	-2956	232

No.	Pad name	X	Y
751	S116	-2972	107
752	S115	-2988	232
753	S114	-3004	107
754	S113	-3020	232
755	S112	-3036	107
756	S111	-3052	232
757	S110	-3068	107
758	S109	-3084	232
759	S108	-3100	107
760	S107	-3116	232
761	S106	-3132	107
762	S105	-3148	232
763	S104	-3164	107
764	S103	-3180	232
765	S102	-3196	107
766	S101	-3212	232
767	S100	-3228	107
768	S99	-3244	232
769	S98	-3260	107
770	S97	-3276	232
771	S96	-3292	107
772	S95	-3308	232
773	S94	-3324	107
774	S93	-3340	232
775	S92	-3356	107
776	S91	-3372	232
777	S90	-3388	107
778	S89	-3404	232
779	S88	-3420	107
780	S87	-3436	232
781	S86	-3452	107
782	S85	-3468	232
783	S84	-3484	107
784	S83	-3500	232
785	S82	-3516	107
786	S81	-3532	232
787	S80	-3548	107
788	S79	-3564	232
789	S78	-3580	107
790	S77	-3596	232
791	S76	-3612	107
792	S75	-3628	232
793	S74	-3644	107
794	S73	-3660	232
795	S72	-3676	107
796	S71	-3692	232
797	S70	-3708	107
798	S69	-3724	232
799	S68	-3740	107
800	S67	-3756	232

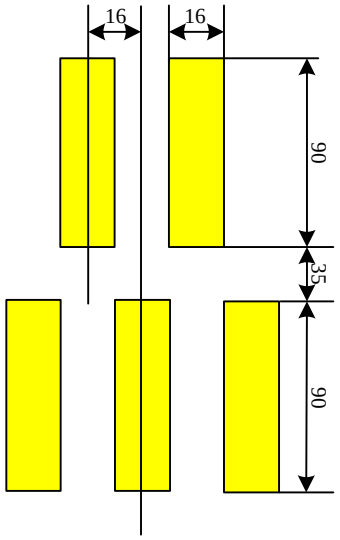
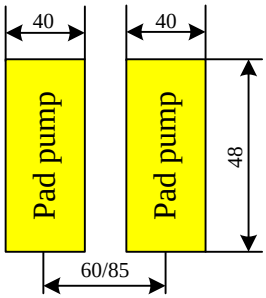
No.	Pad name	X	Y
801	S66	-3772	107
802	S65	-3788	232
803	S64	-3804	107
804	S63	-3820	232
805	S62	-3836	107
806	S61	-3852	232
807	S60	-3868	107
808	S59	-3884	232
809	S58	-3900	107
810	S57	-3916	232
811	S56	-3932	107
812	S55	-3948	232
813	S54	-3964	107
814	S53	-3980	232
815	S52	-3996	107
816	S51	-4012	232
817	S50	-4028	107
818	S49	-4044	232
819	S48	-4060	107
820	S47	-4076	232
821	S46	-4092	107
822	S45	-4108	232
823	S44	-4124	107
824	S43	-4140	232
825	S42	-4156	107
826	S41	-4172	232
827	S40	-4188	107
828	S39	-4204	232
829	S38	-4220	107
830	S37	-4232	232
831	S36	-4252	107
832	S35	-4268	232
833	S34	-4284	107
834	S33	-4300	232
835	S32	-4316	107
836	S31	-4332	232
837	S30	-4348	107
838	S29	-4364	232
839	S28	-4380	107
840	S27	-4396	232
841	S26	-4412	107
842	S25	-4428	232
843	S24	-4444	107
844	S23	-4460	232
845	S22	-4476	107
846	S21	-4492	232
847	S20	-4508	107
848	S19	-4524	232
849	S18	-4540	107
850	S17	-4556	232

No.	Pad name	X	Y
851	S16	-4572	107
852	S15	-4588	232
853	S14	-4604	107
854	S13	-4620	232
855	S12	-4636	107
856	S11	-4652	232
857	S10	-4668	107
858	S9	-4684	232
859	S8	-4700	107
860	S7	-4716	232
861	S6	-4732	107
862	S5	-4748	232
863	S4	-4764	107
864	S3	-4780	232
865	S2	-4796	107
866	S1	-4812	232
867	DUMMY	-4828	107
868	DUMMY	-4844	232
869	DUMMY	-4860	107
870	DUMMY	-4876	232
871	DUMMY	-4892	107
872	DUMMY	-4908	232
873	DUMMY	-4924	107
874	DUMMY	-4940	232
875	G219	-4956	107
876	G217	-4972	232
877	G215	-4988	107
878	G213	-5004	232
879	G211	-5020	107
880	G209	-5036	232
881	G207	-5052	107
882	G205	-5068	232
883	G203	-5084	107
884	G201	-5100	232
885	G199	-5116	107
886	G197	-5132	232
887	G195	-5148	107
888	G193	-5164	232
889	G191	-5180	107
890	G189	-5196	232
891	G187	-5212	107
892	G185	-5228	232
893	G183	-5244	107
894	G181	-5260	232
895	G179	-5276	107
896	G177	-5292	232
897	G175	-5308	107
898	G173	-5324	232
899	G171	-5340	107
900	G169	-5356	232

No.	Pad name	X	Y
901	G167	-5372	107
902	G165	-5388	232
903	G163	-5404	107
904	G161	-5420	232
905	G159	-5436	107
906	G157	-5452	232
907	G155	-5468	107
908	G153	-5484	232
909	G151	-5500	107
910	G149	-5516	232
911	G147	-5532	107
912	G145	-5548	232
913	G143	-5564	107
914	G141	-5580	232
915	G139	-5596	107
916	G137	-5612	232
917	G135	-5628	107
918	G133	-5644	232
919	G131	-5660	107
920	G129	-5676	232
921	G127	-5692	107
922	G125	-5708	232
923	G123	-5724	107
924	G121	-5740	232
925	G119	-5756	107
926	G117	-5772	232
927	G115	-5788	107
928	G113	-5804	232
929	G111	-5820	107
930	G109	-5836	232
931	G107	-5852	107
932	G105	-5868	232
933	G103	-5884	107
934	G101	-5900	232
935	G99	-5916	107
936	G97	-5932	232
937	G95	-5948	107
938	G93	-5964	232
939	G91	-5980	107
940	G89	-5996	232
941	G87	-6012	107
942	G85	-6028	232
943	G83	-6044	107
944	G81	-6060	232
945	G79	-6076	107
946	G77	-6092	232
947	G75	-6108	107
948	G73	-6124	232
949	G71	-6140	107
950	G69	-6156	232

No.	Pad name	X	Y
951	G67	-6172	107
952	G65	-6188	232
953	G63	-6204	107
954	G61	-6220	232
955	G59	-6232	107
956	G57	-6252	232
957	G55	-6268	107
958	G53	-6284	232
959	G51	-6300	107
960	G49	-6316	232
961	G47	-6332	107
962	G45	-6348	232
963	G43	-6364	107
964	G41	-6380	232
965	G39	-6396	107
966	G37	-6412	232
967	G35	-6428	107
968	G33	-6444	232
969	G31	-6460	107
970	G29	-6476	232
971	G27	-6492	107
972	G25	-6508	232
973	G23	-6524	107
974	G21	-6540	232
975	G19	-6556	107
976	G17	-6572	232
977	G15	-6588	107
978	G13	-6604	232
979	G11	-6620	107
980	G9	-6636	232
981	G7	-6652	107
982	G5	-6668	232
983	G3	-6684	107
984	G1	-6700	232
985	DUMMY34	-6716	107
986	DUMMY35	-6732	232
987	DUMMY36	-6748	107
988	DUMMY37	-6764	232
Alignment Mark Left		-6839	225
Alignment Mark Right		6806	-261

BUMP Size

S1 ~ S528 G1 ~ G220 (pin 216 ~ 988)	 Unit:um
I/O Pads (pin 1~215)	

Chip Size: 13980um x 670um

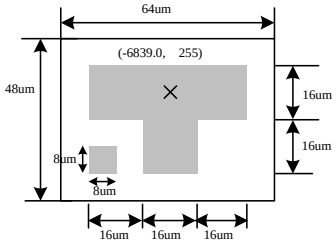
Chip thickness: 280 um / 400 um

Pad Location: Pad Center.

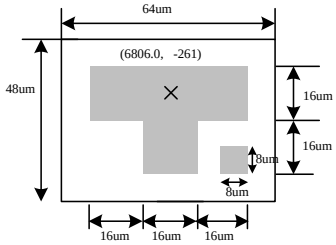
Coordinate Origin: Chip center

Au bump height: 12um

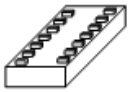
Alignment Marks-Left

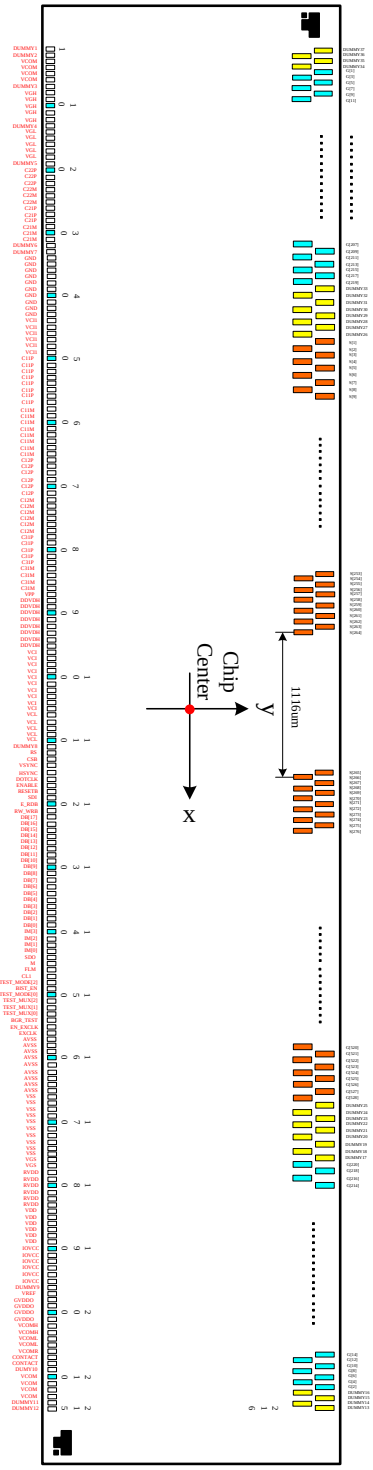


Alignment Mark-Right



Face Up
(Bimp View)





4. Block Decription

MPU System Interface

GC9201 supports three system high-speed interfaces: i80/M68-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM [3:0] pins.

GC9201 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the GC9201 read the first data from the internal GRAM. Valid data are read out after the GC9201 performs the second read operation.
Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

Registers selection by system interface (8-/9-/16-/18-bit bus width)	I80			M68	
function	RS	nWR	nRD	E	RW
Write an index to IR register	0	0	1	1	0
Read an internal status	0	1	0	1	1
Write to control registers or the internal GRAM by WDR register.	1	0	1	1	0
Read from the internal GRAM by RDR register.	1	1	0	1	1

Registers selection by the SPI system interface		
function	R/W	RS
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

GC9201 supports the RGB interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode,

data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data. In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the "External Display Interface" section. The GC9201 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data into the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 87,120 (176 x 220x 18/8) bytes, using 18 bits for each pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC.)

The GC9201 can provide R-C oscillation without external resistor. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be

obtained by adjusting the register setting value [R0Fh]. Since R-C oscillation stops during the standby mode, current consumption can be reduced.

LCD Driver Circuit

The LCD driver circuit of GC9201 consists of a 528-output source driver (S1 ~ S528) and a 220-output gate driver (G1~G220). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

5. System Interface

5.1. Interfaces Specifications

GC9201 has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

GC9201 also has the RGB interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB [17:0].

GC9201 operates in one of the following 4 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM =0)
RGB interface (1) (Displaying moving pictures)	System interface (RM = 1)	Internal operating clock (DM =1)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	Internal operating clock (DM =1)

Note 1) Registers are set only via the system interface.
Note 2) The RGB-I/F is not available simultaneously

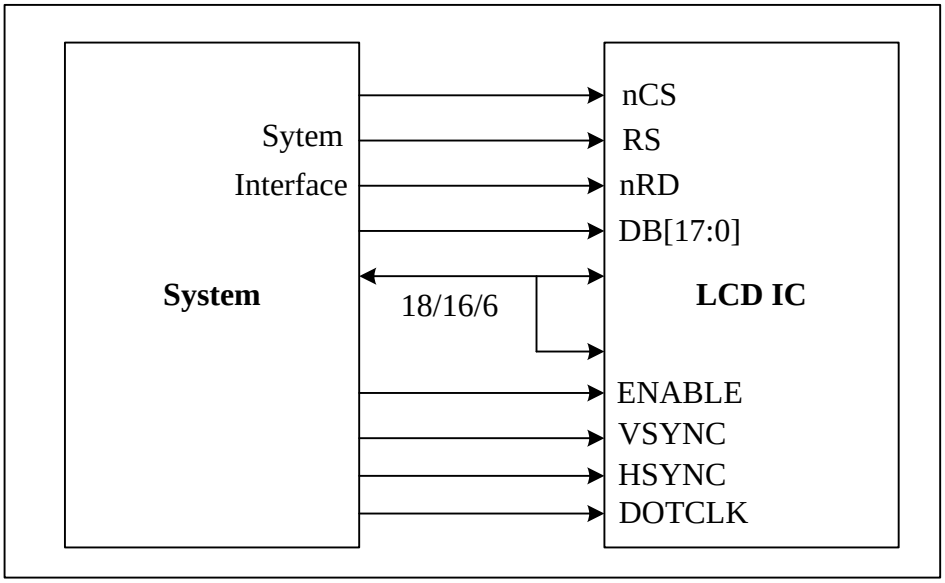


Figure1 System Interface and RGB Interface connection

5.2. Input Interface

The following are the system interfaces available with the GC9201. The interface is selected by setting the IM [3:0] pins. The system interface is used for setting instructions and RAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	M68-system 16-bit interface	DB[17:10], DB[8:1]
0	0	0	1	M68-system 8-bit interface	DB[17:10]
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDI, SDO(DB[1:0])
0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDI, SDO(DB[1:0])
0	1	1	*	Setting invalid	
1	0	0	0	M68-system18-bit interface	DB[17:0]
1	0	0	1	M68-system 9-bit interface	DB[17:9]
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

5.2.1. 18-bit System Interface

The data format for 18-bit data bus is as following,

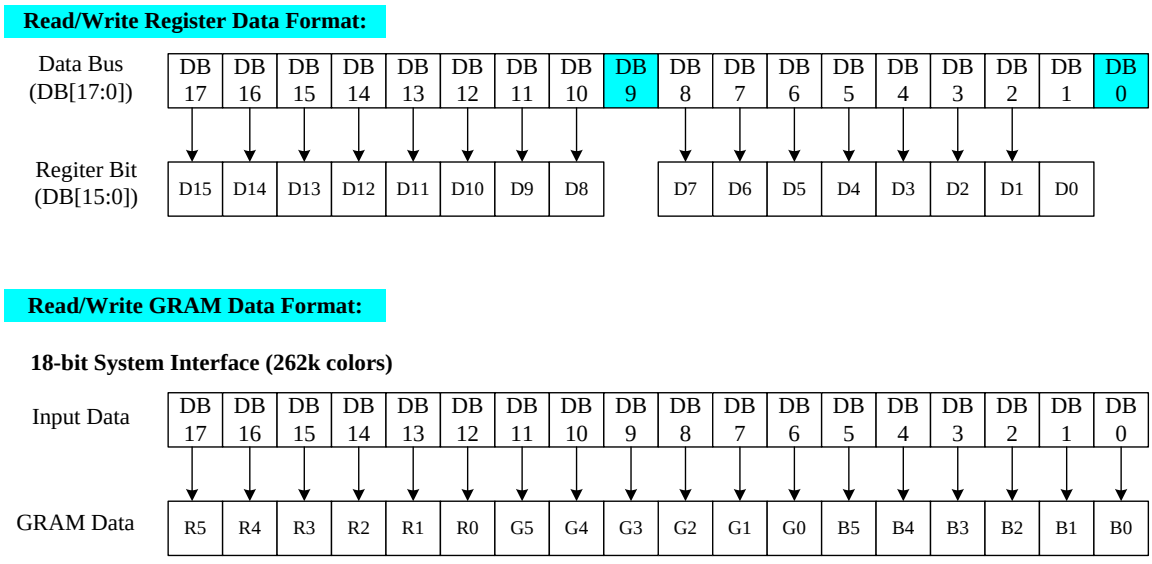


Figure2 18-bit System Interface Data Format

5.2.2. 16-bit System Interface

The data format for 16-bit data bus is as following,

Read/Write Register Data Format:

Data Bus (DB[17:0]), (DB[8:1])	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1
Regiter Bit (DB[15:0])	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Read/Write GRAM Data Format:

16-bit System Interface (262k colors) MDT[1:0]= "00"

Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1
GRAM Data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

16-bit System Interface MSB Mode(262k colors,2 Transfer/pixel) MDT[1:0]= "01"

Input Data	1st tranfer												2nd Transfer					
	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10
GRAM Data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	S(3n+1)						S(3n+2)						S(3n+3)					

Input Data	2nd Transfer						3rd tranfer											
	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2
GRAM Data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	S(3n+4)						S(3n+5)						S(3n+6)					

16-bit System Interface MSB Mode(262k colors,2 Transfer/pixel) MDT[1:0]= "10"

Input Data	1st tranfer																2nd Transfer	
	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 17	DB 16
GRAM Data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

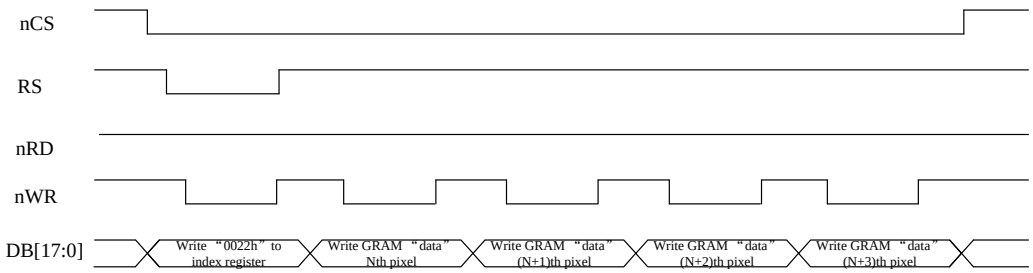
16-bit System Interface LSB Mode(262k colors,2 Transfer/pixel) MDT[1:0]= "11"

Input Data	1st Transfer		2nd tranfer															
	DB 2	DB 1	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1
GRAM Data	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Figure3 16-bit System Interface Data Format

I80 Read/Write Timing:

(a) Write to GRAM



(b) Read from GRAM

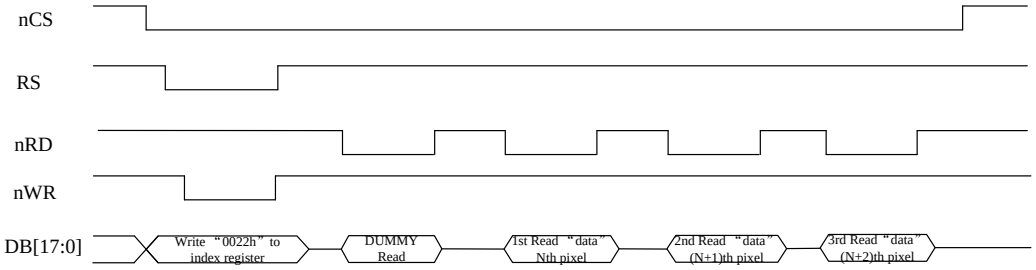
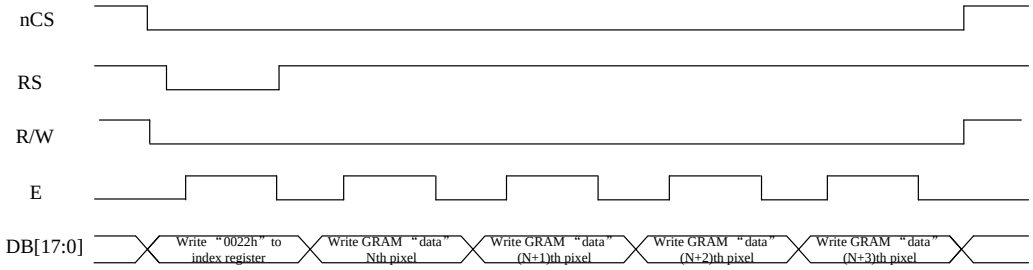


Figure4 i80 16/18-bit System Interface Timing

m68 Read/Write Timing:

(a) Write to GRAM



(b) Read from GRAM

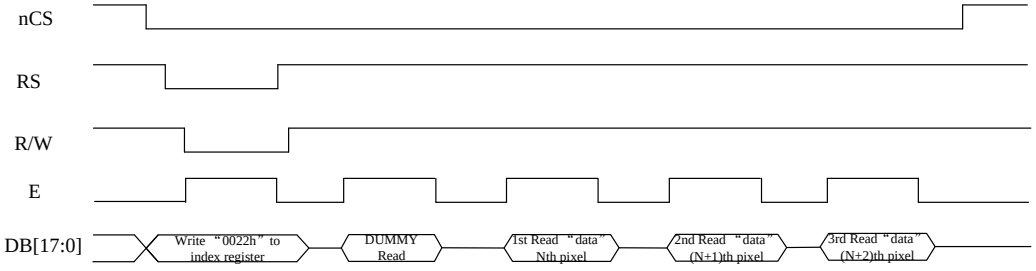
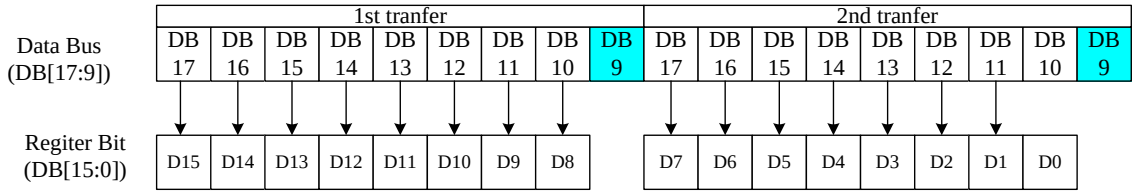


Figure5 M68 16/18-bit System Interface Timing

5.2.3. 9-bit System Interface

The DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to ground.

Read/Write Register Data Format:



Read/Write GRAM Data Format:

9-bit System Interface (262k colors)

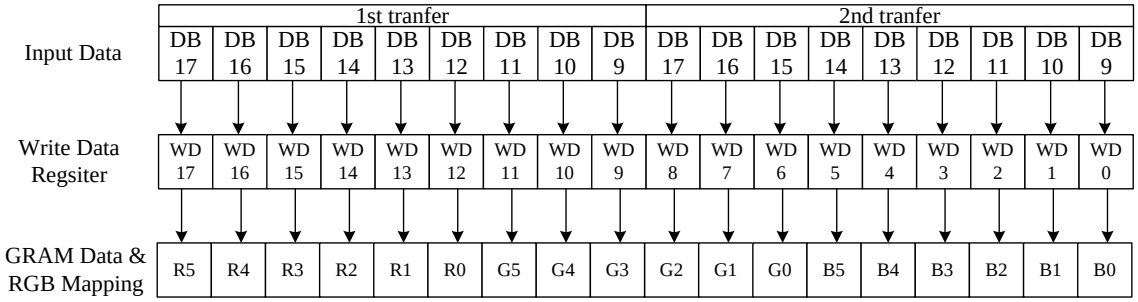


Figure6 9-bit System Interface Data Format

5.2.4. 8-bit System Interface

The DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to ground.

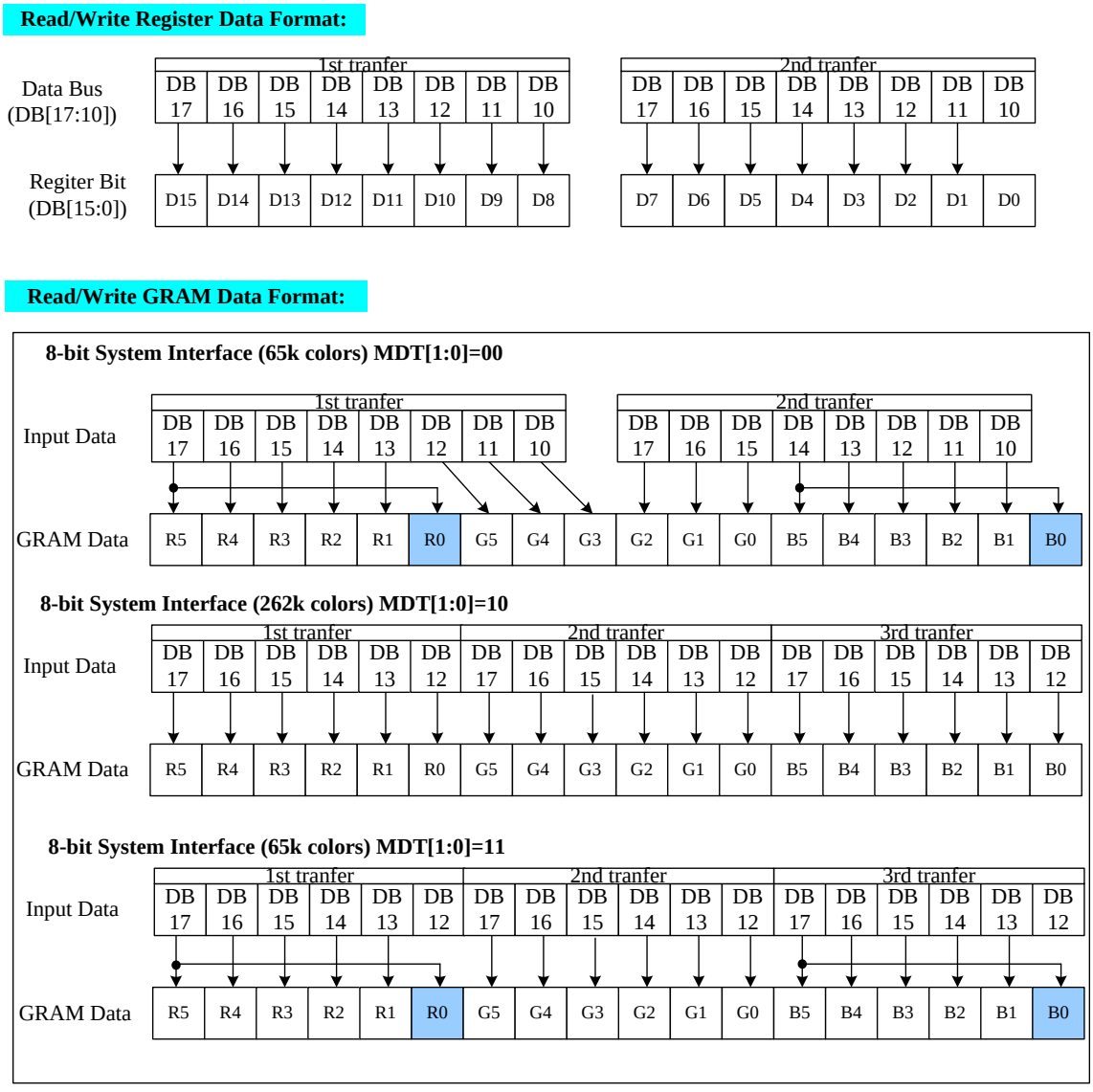


Figure7 8-bit System Interface Data Format

Data transfer synchronization in 8/9-bit bus interface mode

GC9201 supports a data transfer synchronization function to reset upper and lower counters which count the transfers number of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in then numbers of transfers between the upper and lower byte counters due to noise and so on, the “00”h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

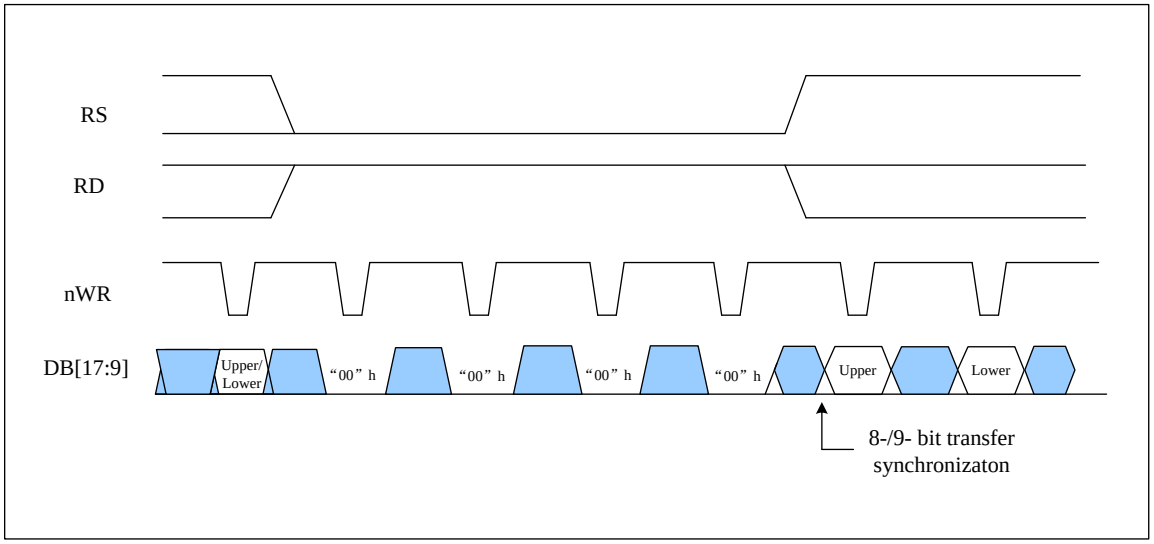


Figure8 Data Transfer Synchronization in 8/9-bit System Interface

5.3. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM [3:0] pins as "010x" level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[17:0] pins, which are not used, must be tied to ground.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by GC9201.

The seventh bit of start byte is RS bit. When RS = "0", either index write operation or status read operation is executed. When RS = "1", either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is "0" and read back when the R/W bit is "1".

After receiving the start byte, GC9201 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the GC9201 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 2 bytes dummy read is necessary and the valid data starts from 3rd byte of read back data.

Start Byte Format

Transfer bits	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin..

RS and R/W Bit Function

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

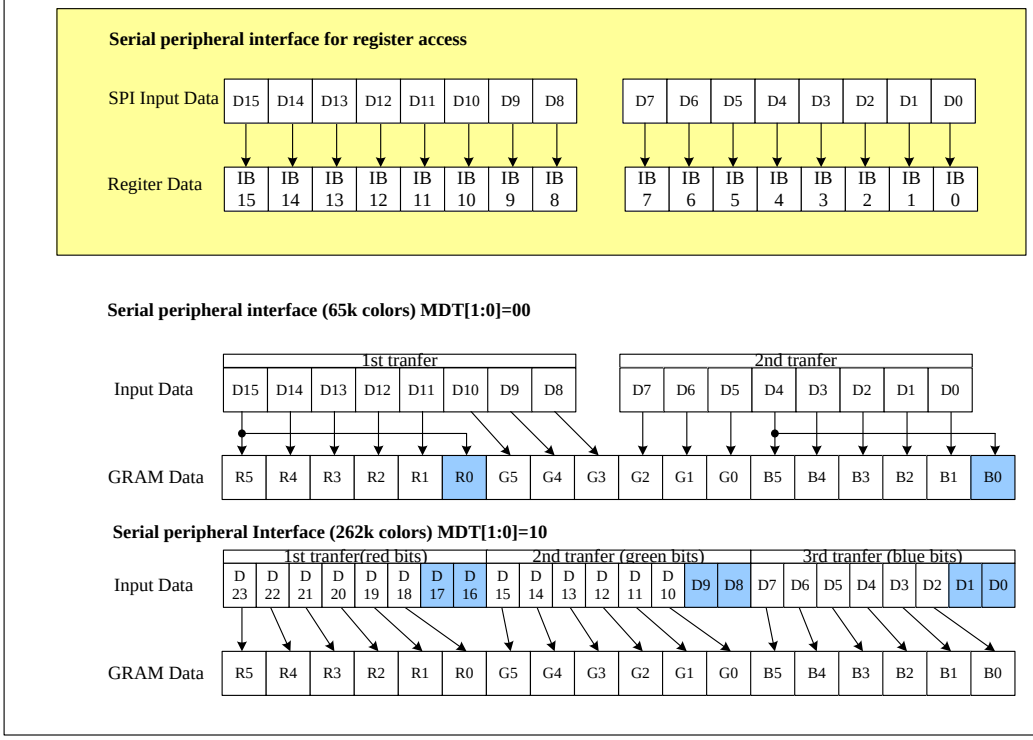


Figure9 Data Format of SPI Interface

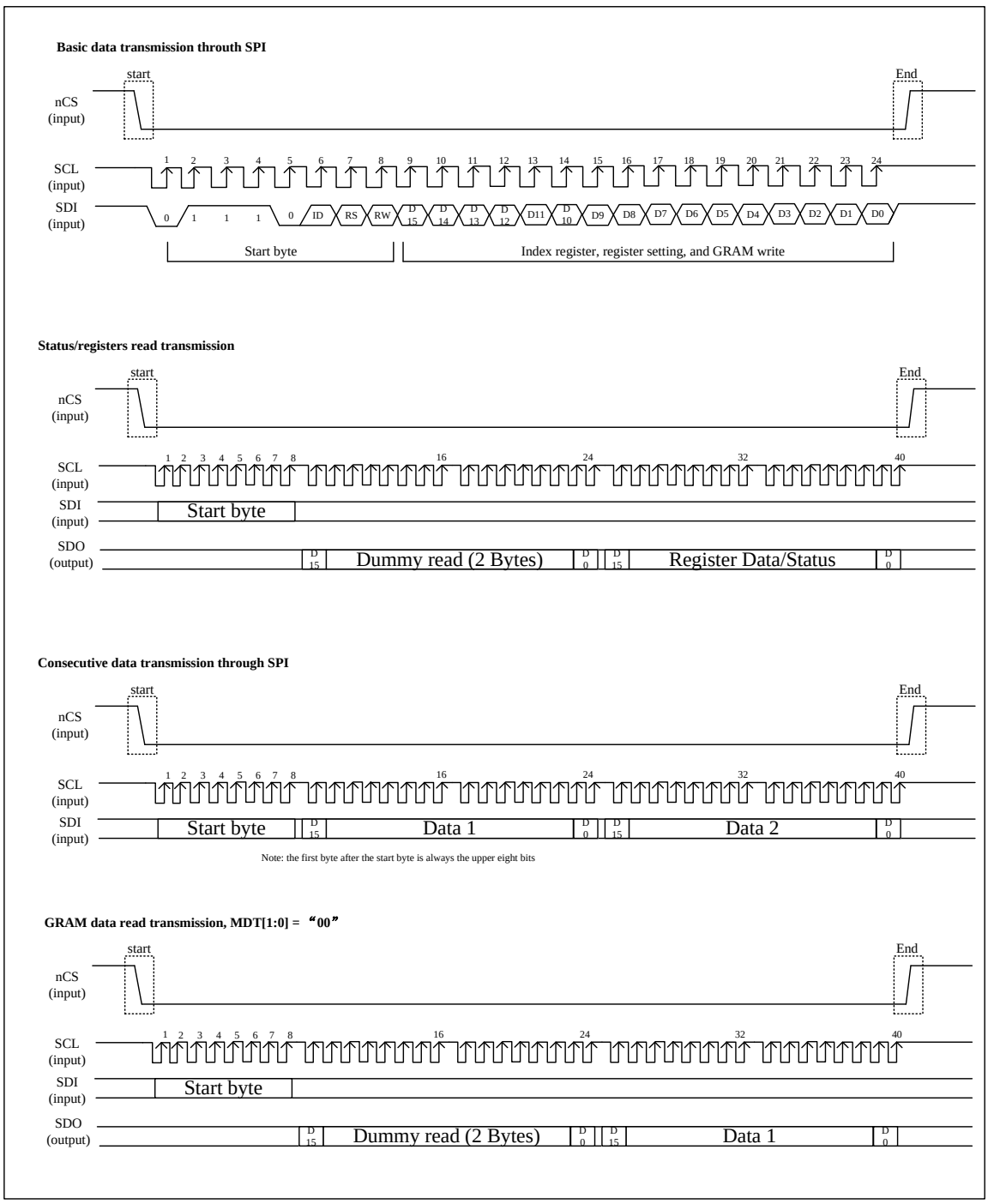


Figure10 Data transmission through SPI, 65 Color

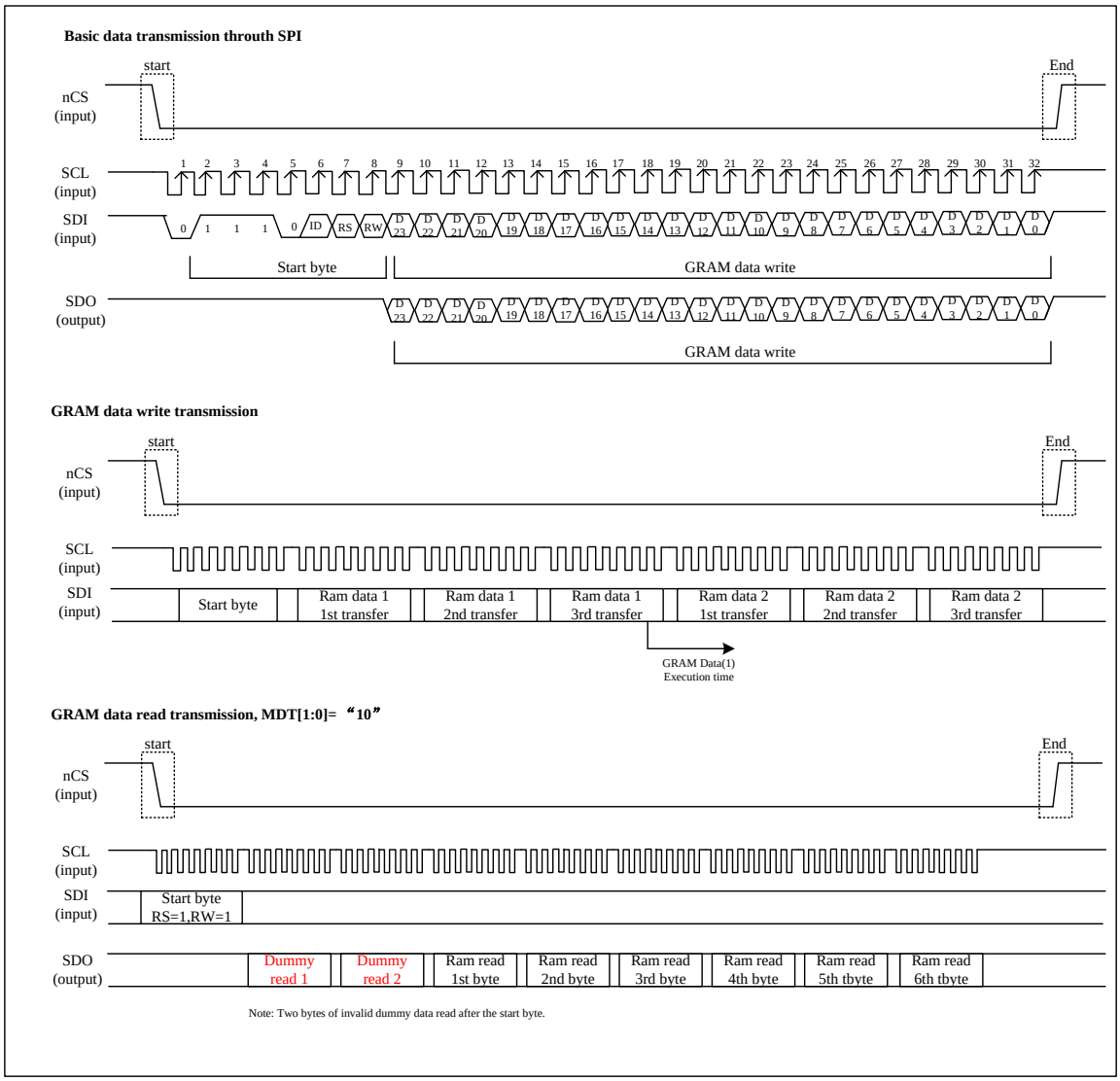
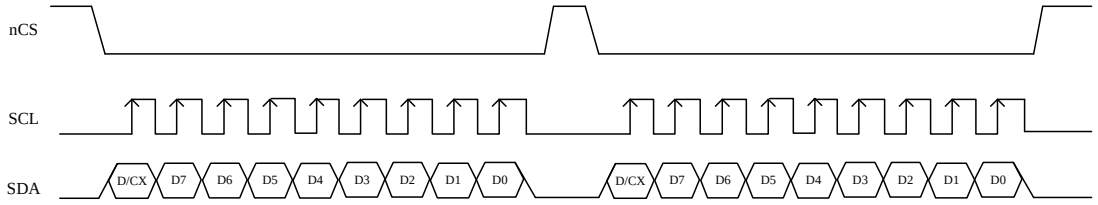


Figure11 Data transmission through SPI, 262K Color

5.3.1. 3-wire 9-bit Serial Interface

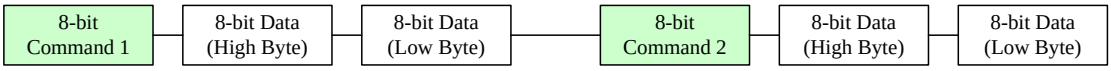
This SPI mode uses a 3-wire 9-bit serial interface. The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock and SDA is serial data.
Serial data must be input to SDA in the sequence D/CX, D7 to D0. The GC9201 reads the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode :



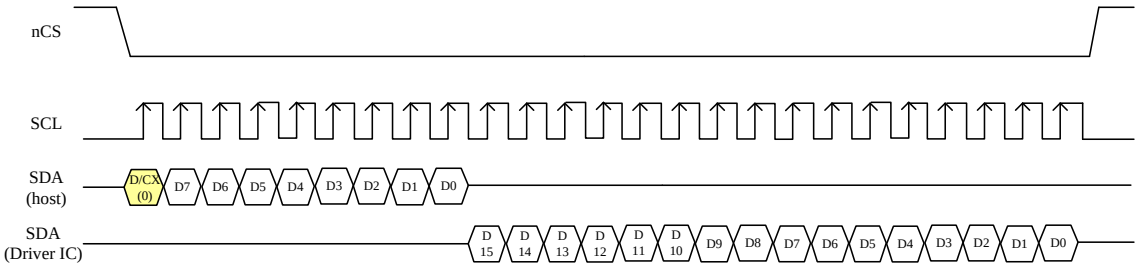
D/CX =0: register index (command)

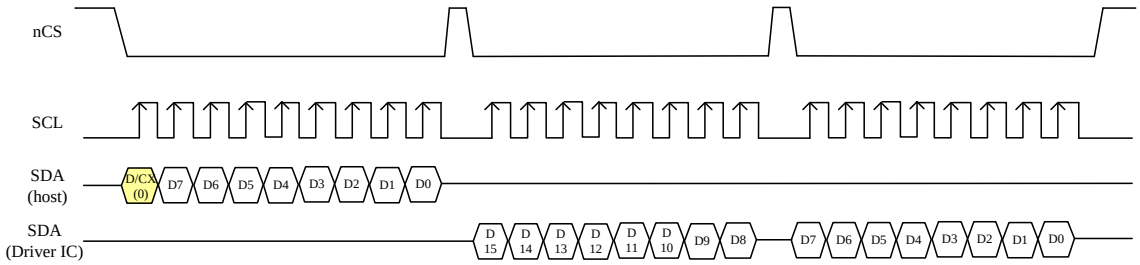
D/CX: register data or GRAMdata



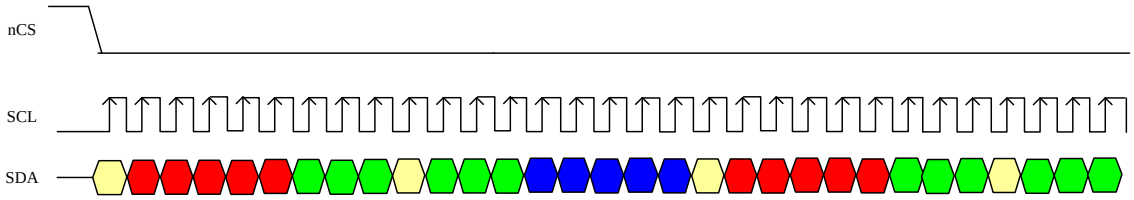
Register read Mode :

When users need to read back the register or GRAM data, the register R66h must be set as “1” first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

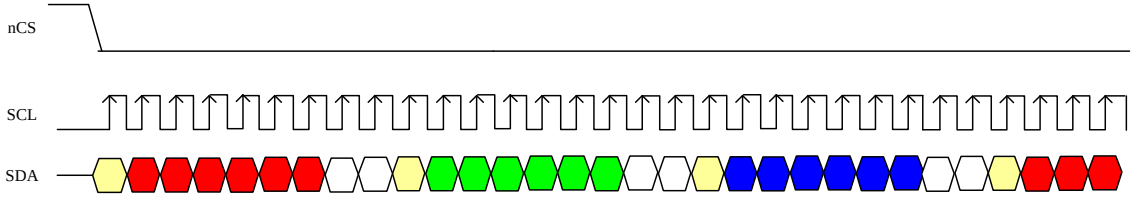




Serial Data transfer interface(65K color, MDT[1:0]=“00”)



Serial Data transfer interface(262K color, MDT[1:0]=“10”)

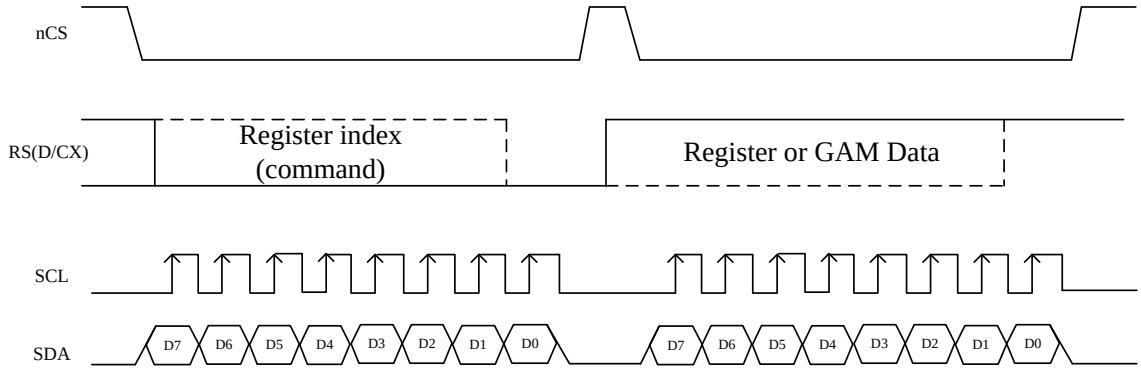


5.3.2. 4-wire 8-bit Serial Interface

This SPI mode uses a 4-wire 9-bit serial interface. The chip-select nCS (active low) enables and disables the serial interface. D/CX is the command or data select signal, SCL is the serial data clock and SDA is serial data.

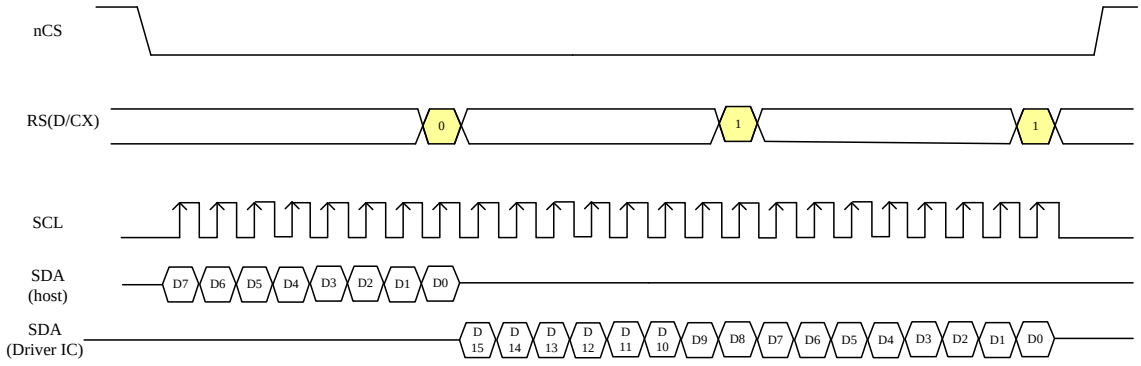
Serial data must be input to SDA in the sequence D7 to D0. The GC9201 reads the data at the rising edge of SCL signal. The D/CX signal indicates data/command. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

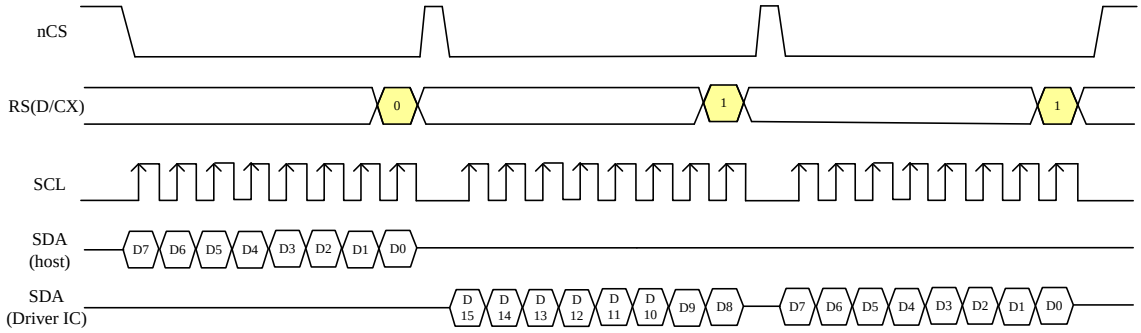
Register Write Mode :



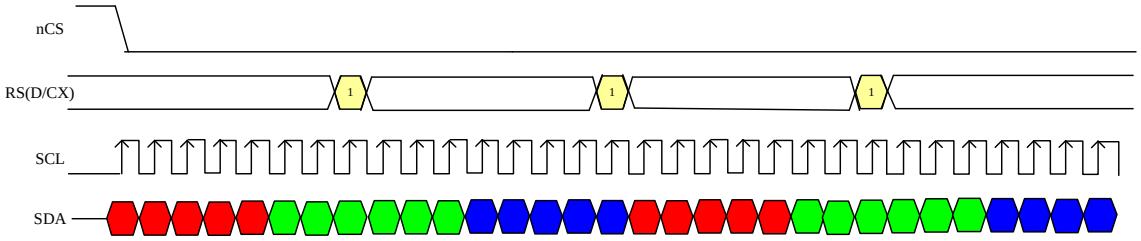
Register read Mode :

When users need to read back the register or GRAM data, the register R66h must be set as “1” first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

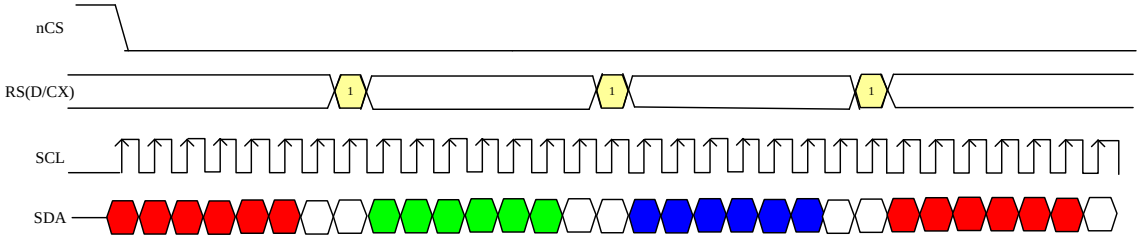




Serial Data transfer interface(65K color, MDT[1:0]=“00”)

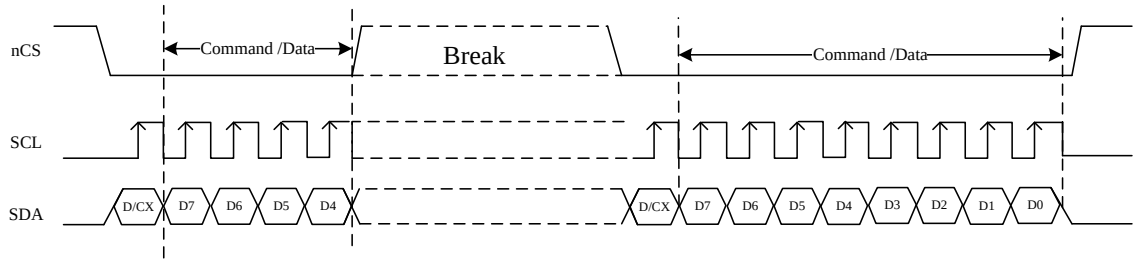


Serial Data transfer interface(262K color, MDT[1:0]=“10”)



5.3.3. Data Transfer Recovery

If there is a break in data transmission while transferring a command or GRAM data or multiple register data, before Bit D0 of the byte has been completed, then the GC9201 will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (nCS) is next activated. See the following example:



If the 2 parameter of command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as show below.
Note: Break can be e.g. another command or noise pulse.

5.4. RGB Input Interface

The RGB Interface mode is available for GC9201 and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB Pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

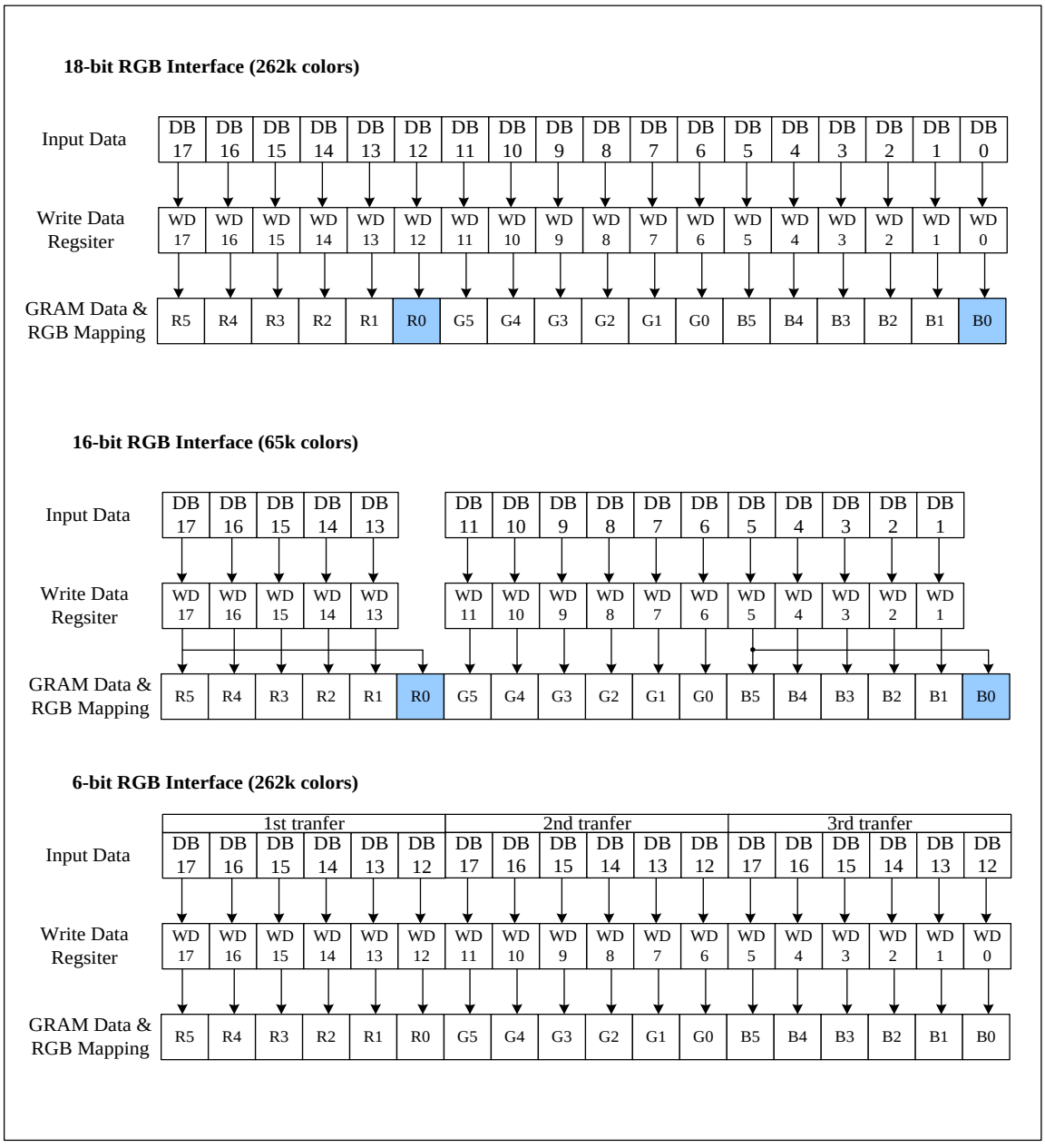


Figure12 RGB Interface Data Format

5.4.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

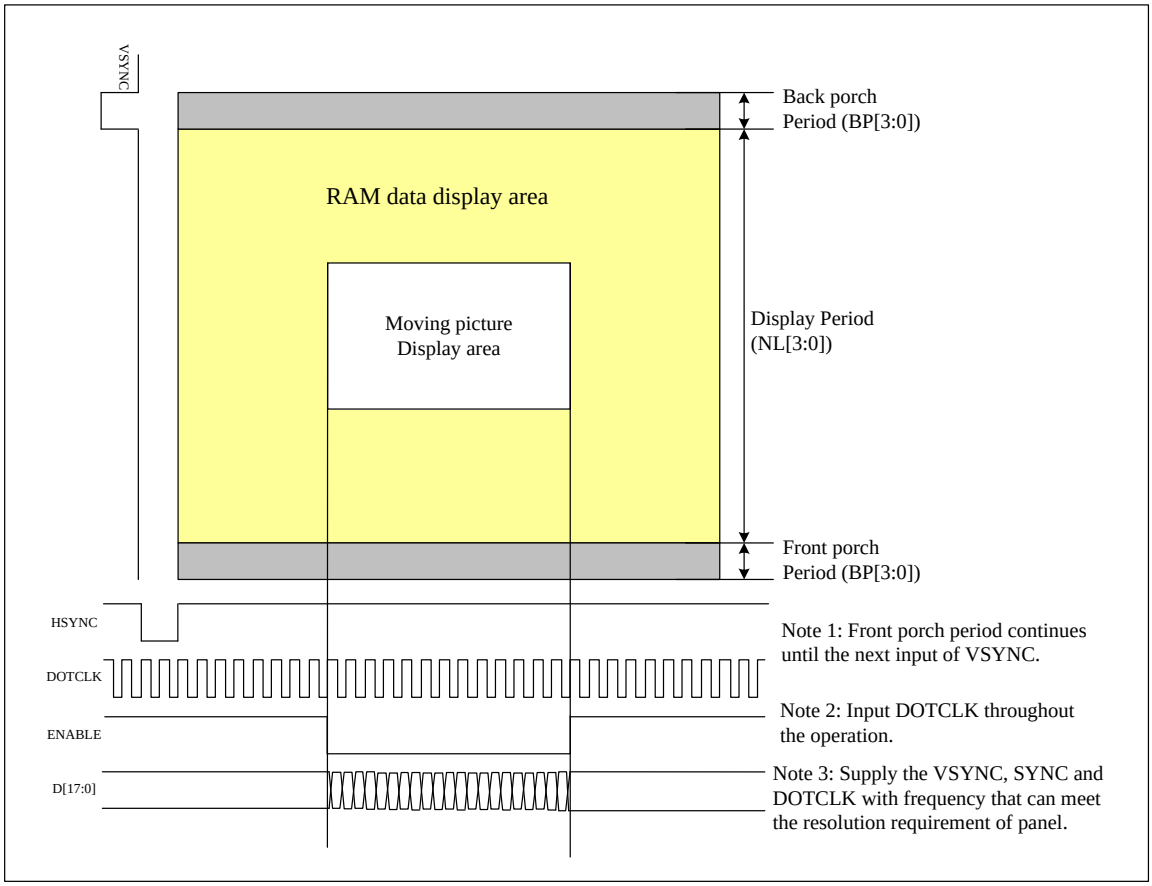


Figure13 GRAM Access Area by RGB Interface

5.4.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.

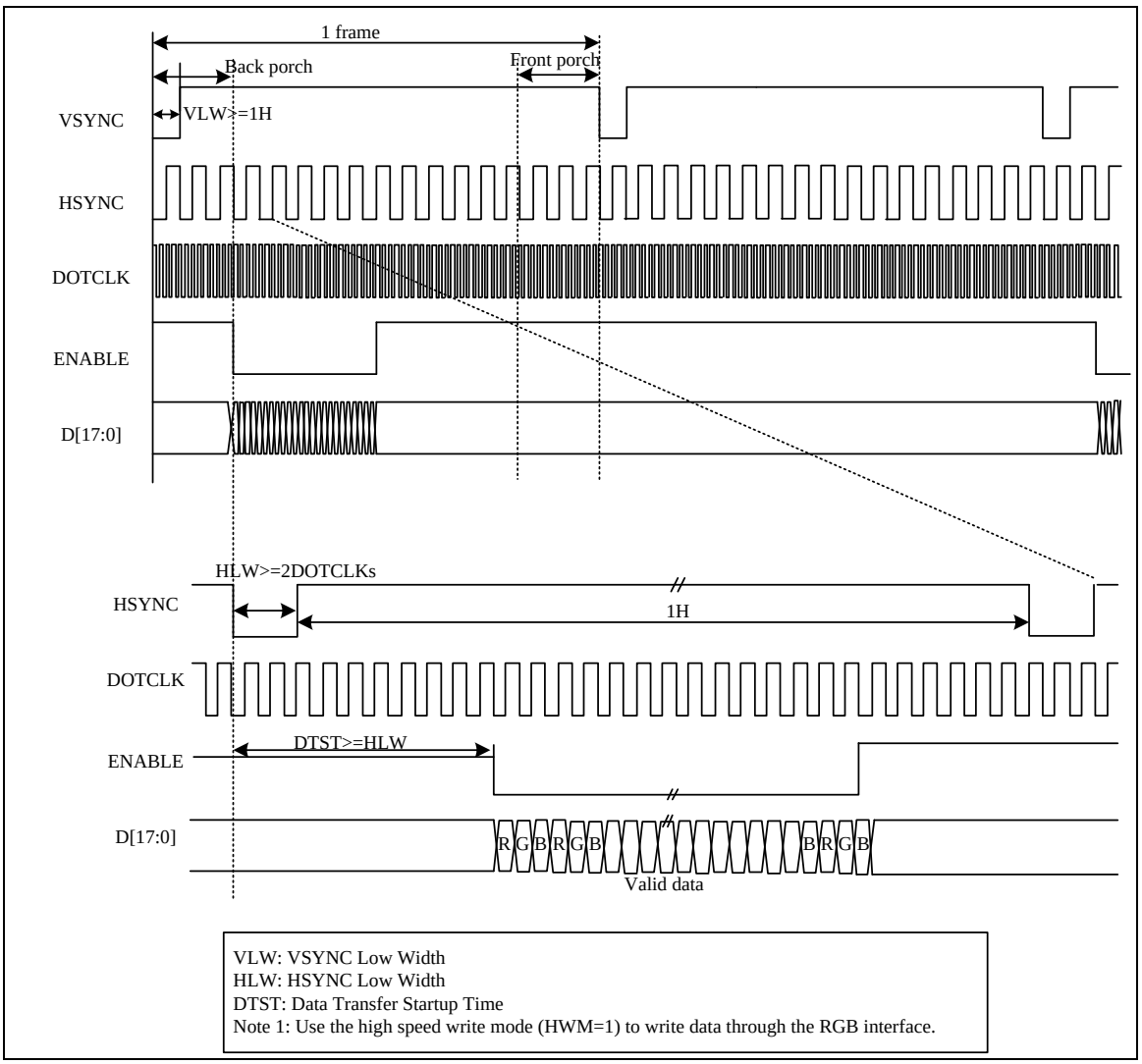
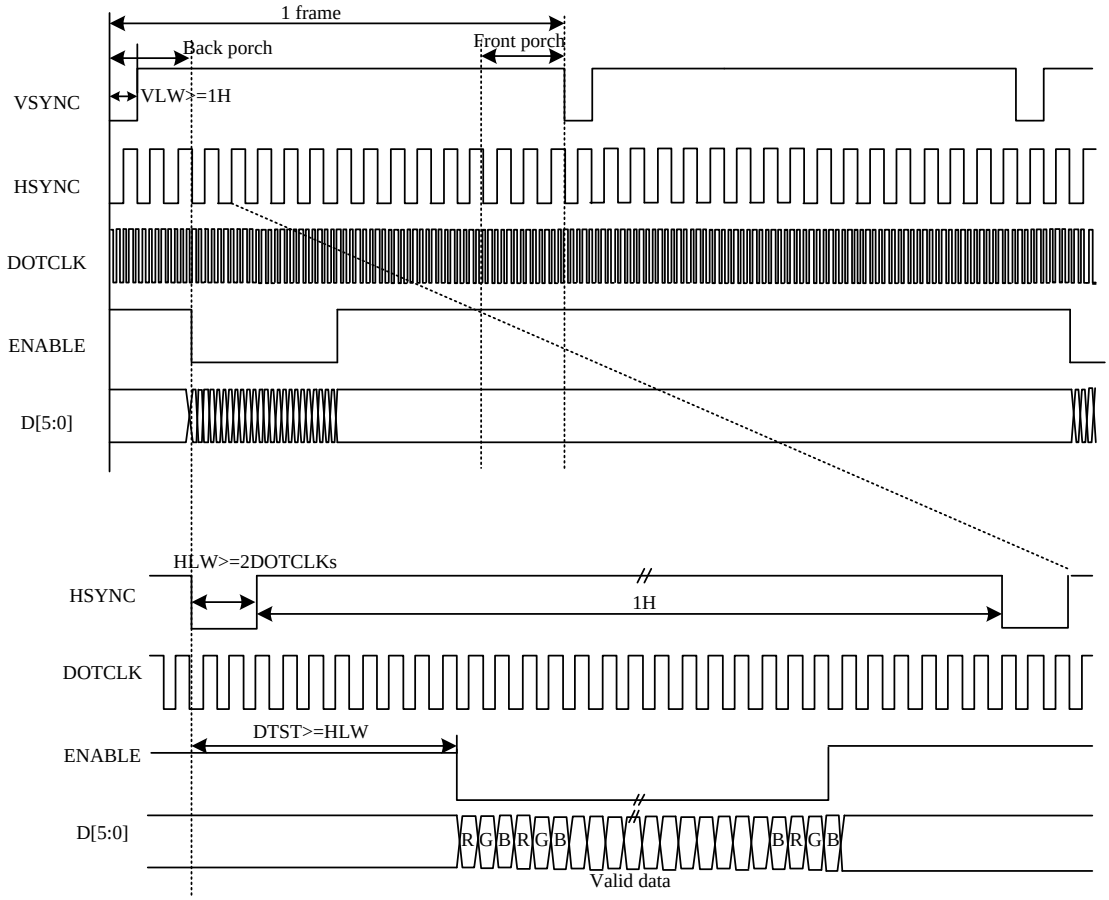


Figure14 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as below:



VLW: VSYNC Low Width
HLW: HSYNC Low Width
DTST: Data Transfer Startup Time

Note 1. In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLKs.

Note 2. In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLKs.

5.4.3. Moving Picture Mode

GC9201 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

GC9201 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the GC9201 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

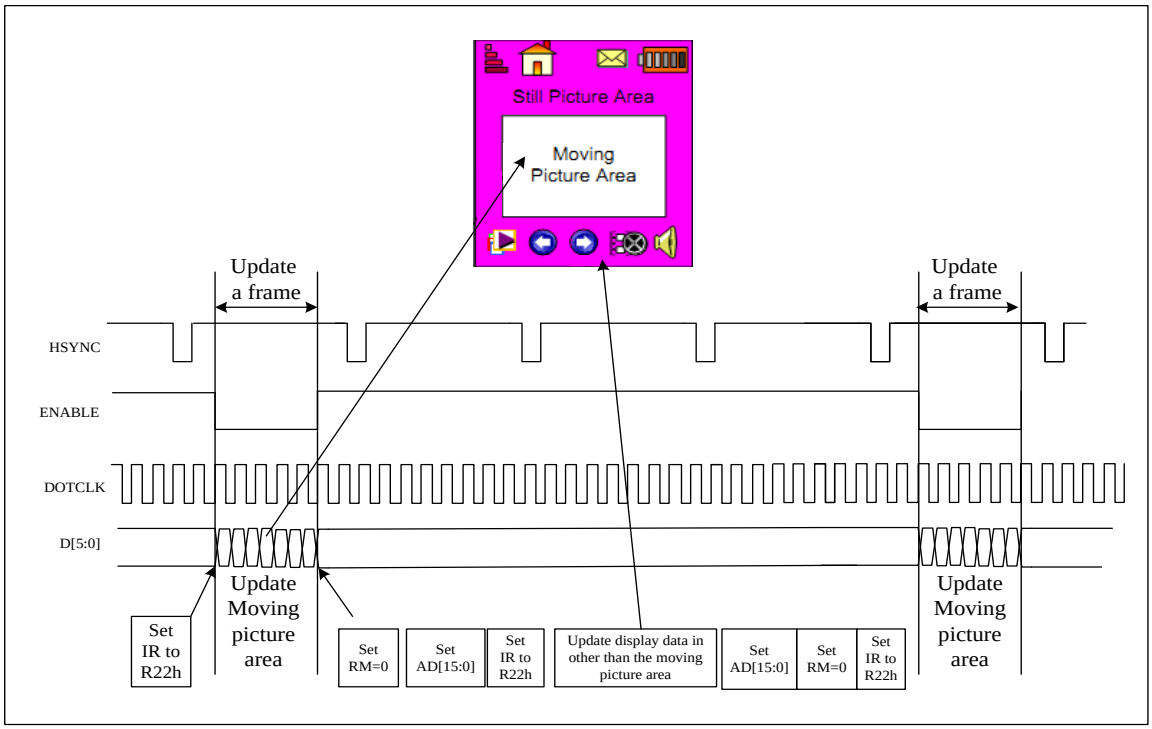


Figure14 Example of update the still and moving picture

5.4.4. 6-bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to "10". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at ground. Registers can be set by the system interface (i80/M68/SPI).

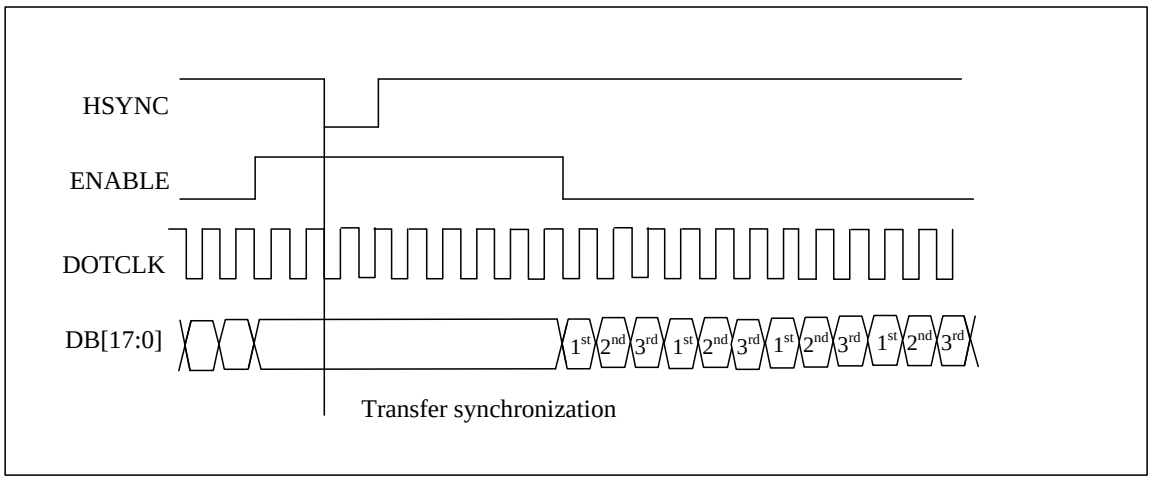
RGB Interface 6-bit data bus

	1st tranfer						2nd tranfer						3rd tranfer					
Input Data	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12	DB 17	DB 16	DB 15	DB 14	DB 13	DB 12
GRAM Data & RGB Mapping	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

Data transfer synchronization in 6-bit RGB interface mode

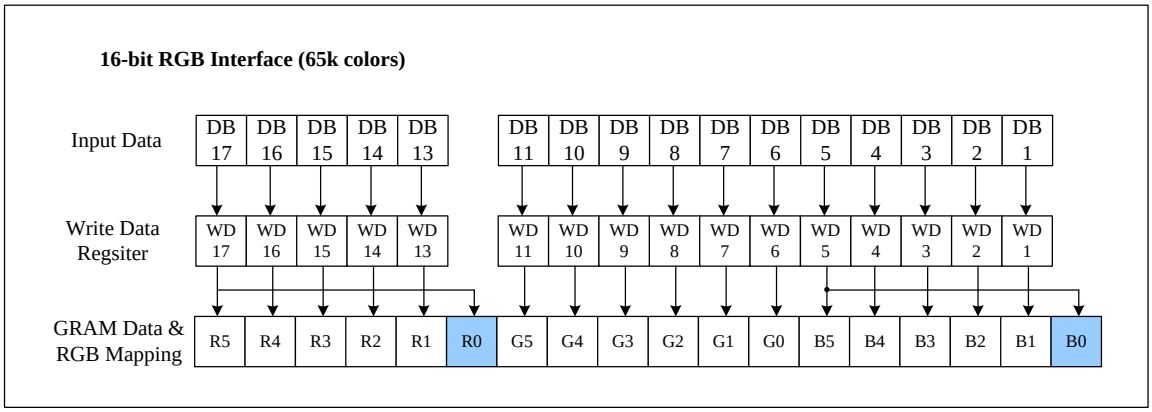
GC9201 has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



5.4.5. 16-bit RGB Interface

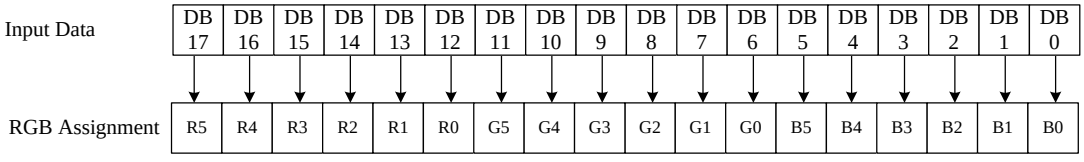
The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



5.4.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to "00". The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.

18-bit RGB Interface with 18-bit bus



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

function	RGB interface	I80/M68 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, and ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

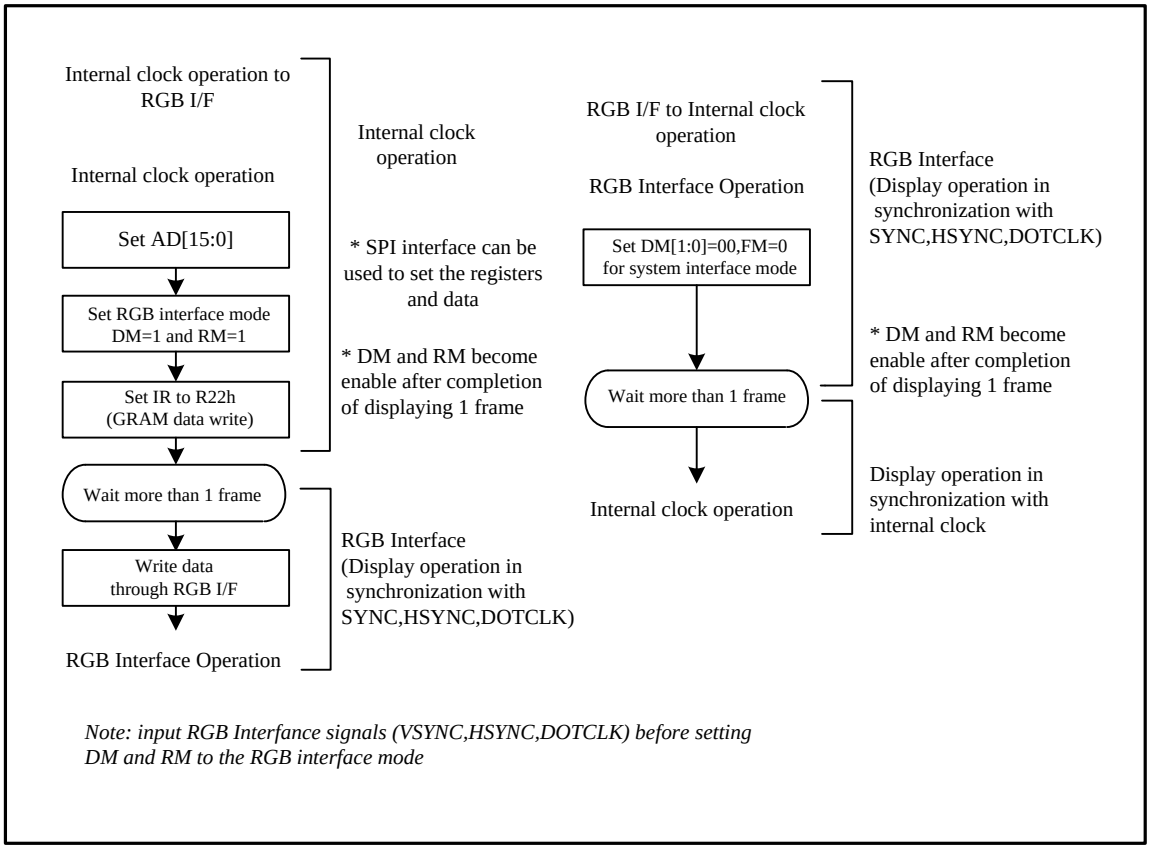


Figure15 Internal clock operation/RGB interface mode switching

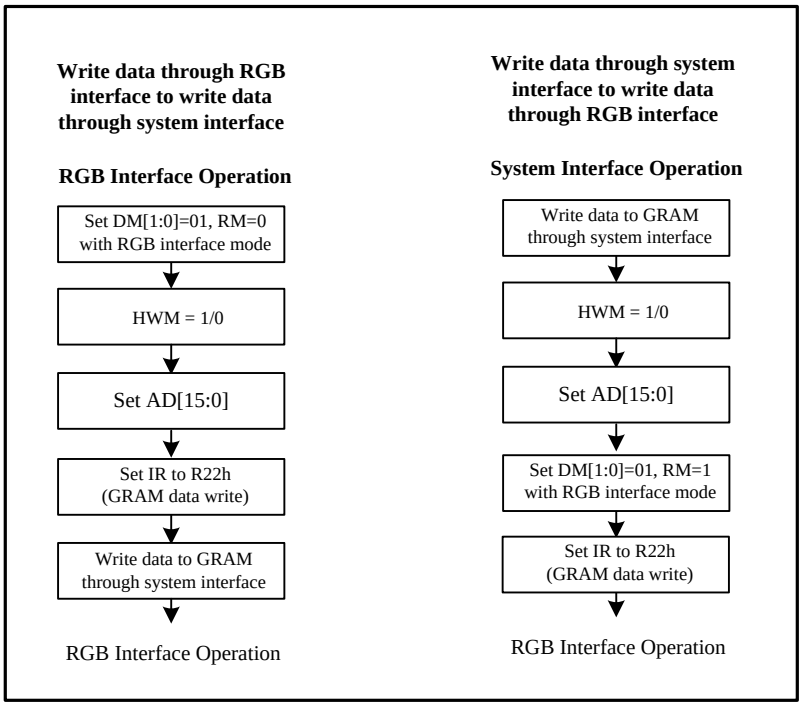


Figure16 GRAM access between system interface and RGB interface

5.5. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

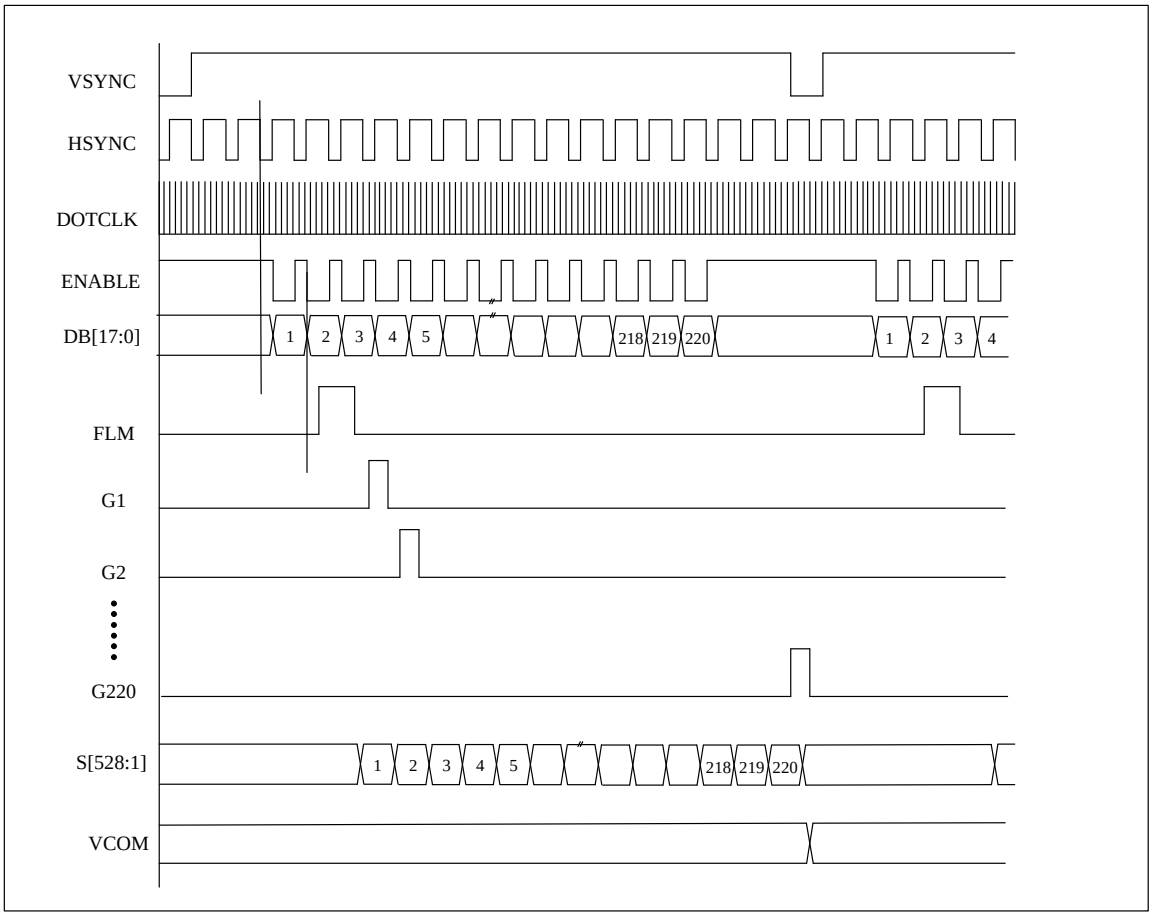


Figure17 Relationship between RGB I/F signals and LCD Driving Signals for Panel

6. Register Descriptions

6.1. Registers Access

GC9201 adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of GC9201 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of GC9201. The registers of the GC9201 are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ-correction (R30 ~ R39)

Normally, the display data (GRAM) is most often updated, and in order since the GC9201 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

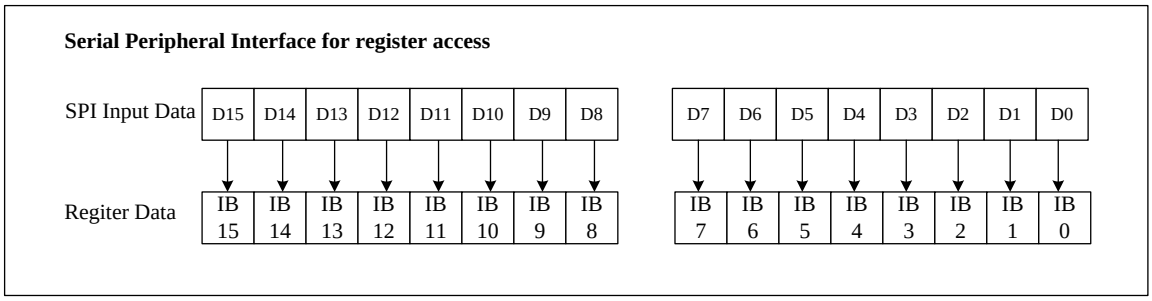


Figure18 Register Setting with Serial Peripheral Interface (SPI)

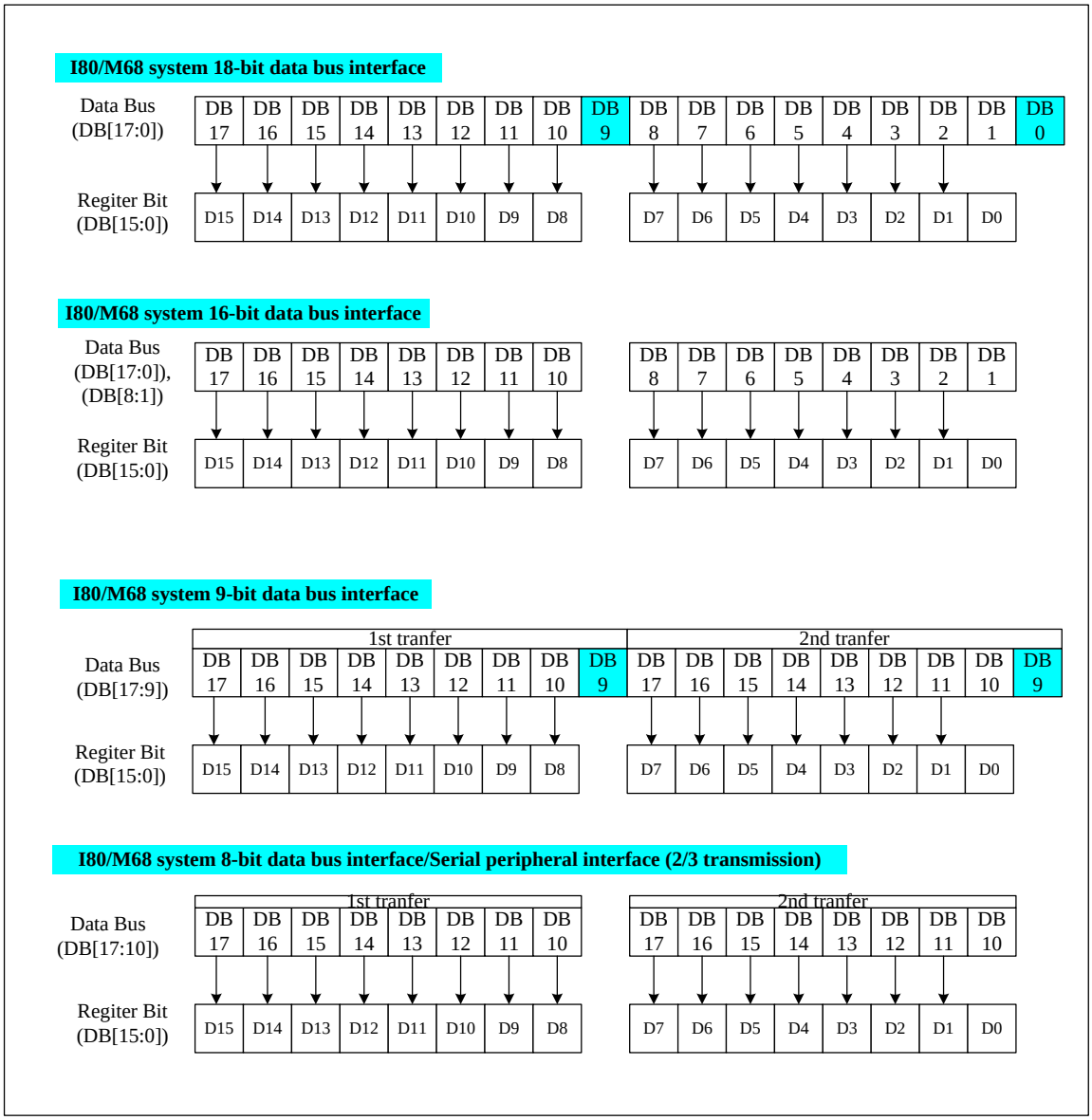
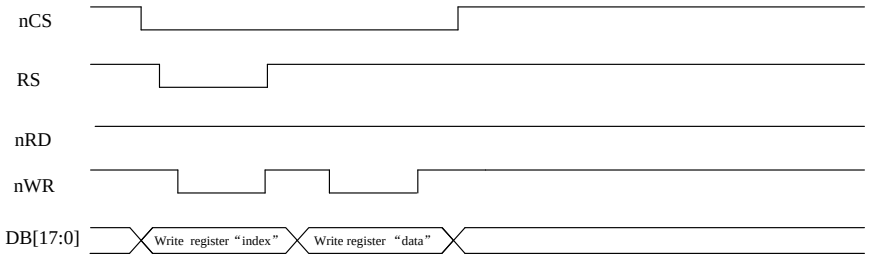


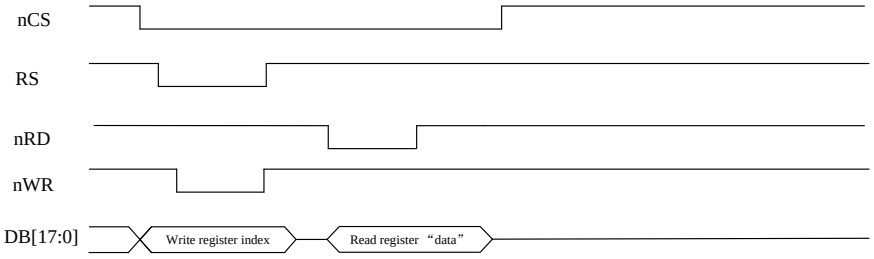
Figure19 Register setting with i80/M68 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

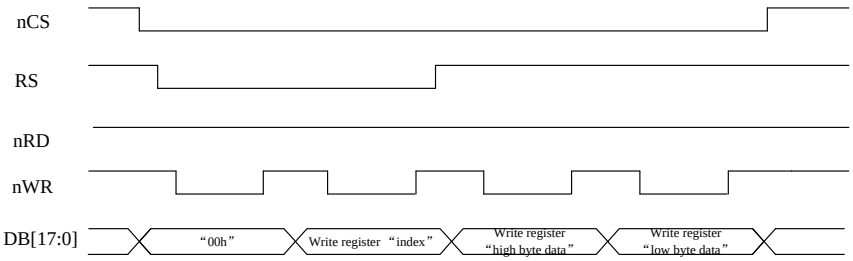


(b) Read from register



i80 9-/8-bit System Bus Interface Timing

(a) Write to register



(b) Read from regisster

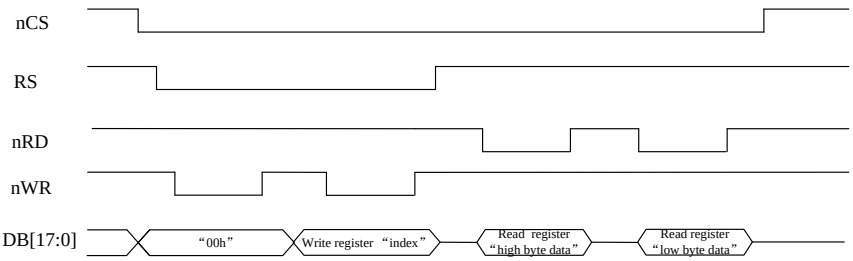
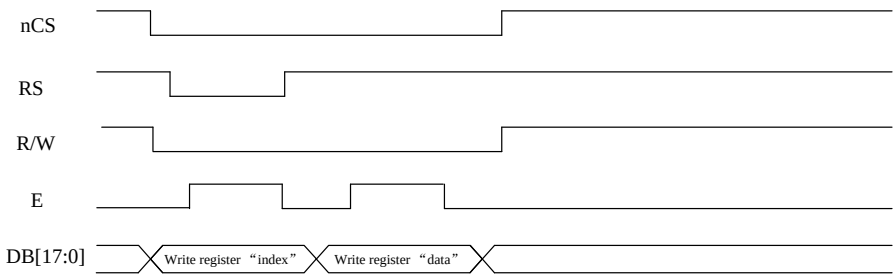


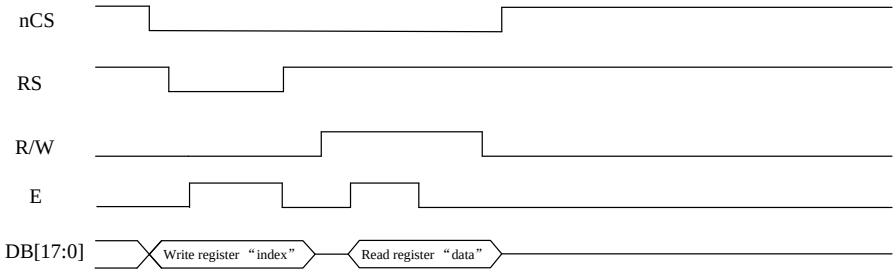
Figure20 Register Read/Write Timing of i80 System Interface

m68 18-/16-bit system Bus Interface Timing

(a) Write to register

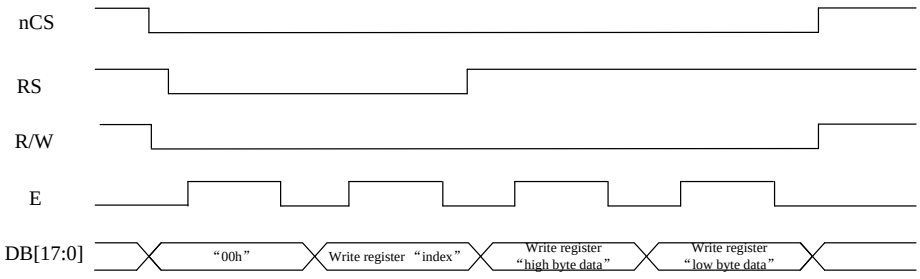


(b) Read from register



m68 9-/8-bit system Bus Interface Timing

(a) Write to register



(b) Read from register

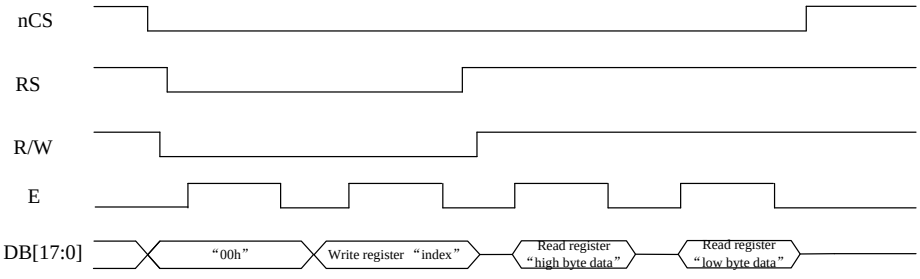


Figure21 Register Read/Write Timing of M68 System Interface

6.2. Instruction Description

NO	Register Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	index	w	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	W	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1
01h	Driver Output Control	W	1	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	0	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (0)
02h	LCD AC Driving Control	W	1	0	0	0	0	0	0	INV1 (0)	INV0 (1)	0	0	0	0	0	0	0	FLD (0)
03h	Entry Mode	W	1	0	0	0	BGR (0)	0	0	MDT1 (0)	MDT0 (0)	0	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0
07h	Display Control 1	W	1	0	0	0	TEMON (0)	0	0	0	0	0	0	0	GON (0)	CL (0)	REV (0)	D1 (0)	D0 (0)
08h	Blank Period Control 1	W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
0Bh	Frame Cycle Control	W	1	NO3 (0)	NO2 (0)	NO1 (1)	NO0 (1)	SDT3 (0)	SDT2 (0)	SDT1 (0)	SDT0 (0)	0	0	0		RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)
0Ch	nterface Control	W	1	0	0	0	0	0	0	0	RM(0)	0	0	0	DM (0)	0	0	RIM1 (0)	RIM0 (0)
0Fh	Oscillation Control	W	1	0	0	0	0	FOSC 3 (0)	FOSC 2 (1)	FOSC 1 (1)	FOSC 0 (1)	0	0	0	0	0	0	0	OSC_ ON(1)
10h	Power Control 1	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	STB (0)

11h	Power Control 2	W	1	0	0	0	APON (0)	0	0	0	0	0	0	0	0	0	0	0	0
12h	Power Control 3	W	1	0	BT2 (0)	BT1 (1)	BT0 (0)	0	0	0	0	0	0	0	0	0	0	0	0
13h	Power Control 4	W	1	0	0	0	0	0	0	0	0	0	GVD6 (1)	GVD5 (1)	GVD4 (0)	GVD3 (0)	GVD2 (1)	GVD1 (1)	GVGD 0(0)
14h	Power Control 5	W	1	VCO MG (0)	VCM6 (1)	VCM5 (0)	VCM4 (1)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (1)	0	VML6 (1)	VML5 (1)	VML4 (0)	VML3 (1)	VML2 (0)	VML1 (0)	VML0 (1)
20h	RAM Address Set 1	W	1	0	0	0	0	0	0	0	0	DA7 (0)	DA6 (0)	DA5 (0)	DA4 (0)	DA3 (0)	DA2 (0)	DA1 (0)	DA0 (0)
21h	RAM Address Set 2	W	1	0	0	0	0	0	0	0	0	DA15 (0)	DA14 (0)	DA13 (0)	DA12 (0)	DA11 (0)	DA10 (0)	DA9 (0)	DA8 (0)
22h	Write Data to GRAM	W	1	WD[17:0]: Pin assignment varies according to the interface method.															
22h	Read Data to GRAM	W	1	RD[17:0]: Pin assignment varies according to the interface method.															
30h	Gate Scan Control	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
31h	Vertical Scroll Control 1	W	1	0	0	0	0	0	0	0	0	SEA7 (1)	SEA6 (1)	SEA5 (0)	SEA4 (1)	SEA3 (1)	SEA2 (0)	SEA1 (1)	SEA0 (1)
32h	Vertical Scroll Control 2	W	1	0	0	0	0	0	0	0	0	SSA7 (0)	SSA6 (0)	SSA5 (0)	SSA4 (0)	SSA3 (0)	SSA2 (0)	SSA1 (0)	SSA0 (0)
33h	Vertical Scroll Control 3	W	1	0	0	0	0	0	0	0	0	SST7 (0)	SST6 (0)	SST5 (0)	SST4 (0)	SST3 (0)	SST2 (0)	SST1 (0)	SST0 (0)
34h	Partial Driving Position -1	W	1	0	0	0	0	0	0	0	0	SE17 (1)	SE16 (1)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (0)	SE11 (1)	SE10 (1)
35h	Partial Driving Position -2	W	1	0	0	0	0	0	0	0	0	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)

36h	Horizontal Window Address -1	W	1	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
37h	Horizontal Window Address -2	W	1	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
38h	Vertical Window Address -1	W	1	0	0	0	0	0	0	0	0	VEA7 (1)	VEA6 (1)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (0)	VEA1 (1)	VEA0 (1)
39h	Vertical Window Address -2	W	1	0	0	0	0	0	0	0	0	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
50h	Gamma Control 1	W	1	0	0	0	0	KP13 (0)	KP12 (0)	KP11 (0)	KP10 (0)	0	0	0	0	KP03 (0)	KP02 (0)	KP01 (0)	KP00 (0)
51h	Gamma Control 2	W	1	0	0	0	0	KP33 (1)	KP32 (0)	KP31 (0)	KP30 (0)	0	0	0	0	KP23 (1)	KP22 (0)	KP21 (0)	KP20 (0)
52h	Gamma Control 3	W	1	0	0	0	0	KP53 (1)	KP52 (0)	KP51 (0)	KP50 (0)	0	0	0	0	KP43 (1)	KP42 (0)	KP41	KP40 (0)
53h	Gamma Control 4	W	1	0	0	0	0	RP13 (0)	RP12 (0)	RP11 (0)	RP10 (0)	0	0	0	0	RP03 (1)	RP02 (0)	RP01	RP00 (0)
54h	Gamma Control 5	W	1	0	0	0	0	KN13 (1)	KN12 (0)	KN11 (1)	KN10 (0)	0	0	0	0	KN03 (1)	KN02 (0)	KN01 (0)	KN00 (0)
55h	Gamma Control 6	W	1	0	0	0	0	KN33 (1)	KN32 (0)	KN31 (0)	KN30 (0)	0	0	0	0	KN23 (1)	KN22 (0)	KN21 (0)	KN20 (0)
56h	Gamma Control 7	W	1	0	0	0	0	KN53 (0)	KN52 (0)	KN51 (0)	KN50 (0)	0	0	0	0	KN43 (0)	KN42 (0)	KN41 (0)	KN40 (0)
57h	Gamma Control 8	W	1	0	0	0	0	RN13 (1)	RN12 (0)	RN11 (1)	RN10 (0)	0	0	0	0	RN03 (0)	RN02 (0)	RN01 (0)	RN00 (0)
58h	Gamma Control 9	W	1	0	0	0	VRP14 (0)	VRP13 (0)	VRP12 (1)	VRP11 (1)	VRP10 (1)	0	0	0	VRP04 (1)	VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)
59h	Gamma Control 10	W	1	0	0	0	VRN14 (0)	VRN13 (0)	VRN12 (1)	VRN11 (1)	VRN10 (1)	0	0	0	VRN04 (1)	VRP03 (0)	VRN05 (0)	VRP04 (0)	VRN06 (0)

6.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	-	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ R4Fh) or RAM which will be accessed.

6.2.2. Device Code (R00h)

R	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1

The device code “9201h” is read out when read this register.

6.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VSPL	HSPL	DPL	EPL	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

VSPL: Inverts the polarity of signals from the VSYNC pin.
VSPL = ”0” : Low active.
VSPL = ”1” : High active.

HSPL: Inverts the polarity of signals from the HSYNC pin.
HSPL = ”0” : Low active.
HSPL = ”1” : High active.

DPL: Inverts the polarity of signals from the DOTCLK pin.
DPL = ”0” : Data are read on the rising edge of the DOTCLK.
DPL = ”1” : Data are read on the falling edge of the DOTCLK.

EPL: Set the polarity of the signal from the ENABLE pin in RGB interface mode.
EPL = “0”:
ENABLE = “Low” / Write data to DB[17:0]
ENABLE = “High” / Inhibit data write operation
EPL =”1”:
ENABLE = “High” / Write data to DB[17:0]
ENABLE = “Low” / Inhibit data write operation

The following table shows the relationship between the EPL, ENABLE bits, and RAM access

EPL	ENABLE	RAM write	RAM address
0	0	Enable	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enable	Updated

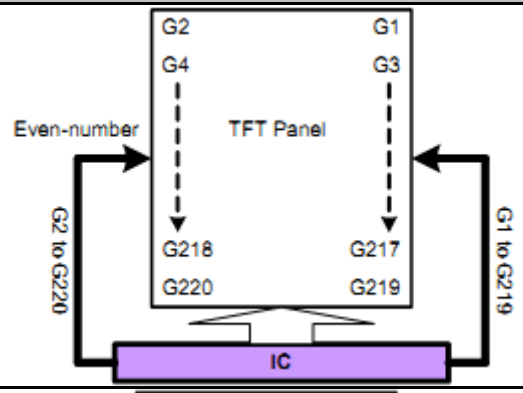
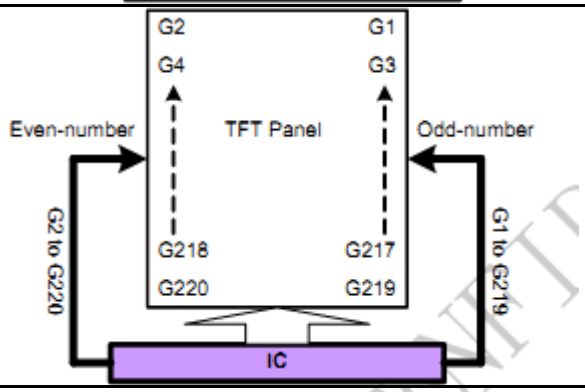
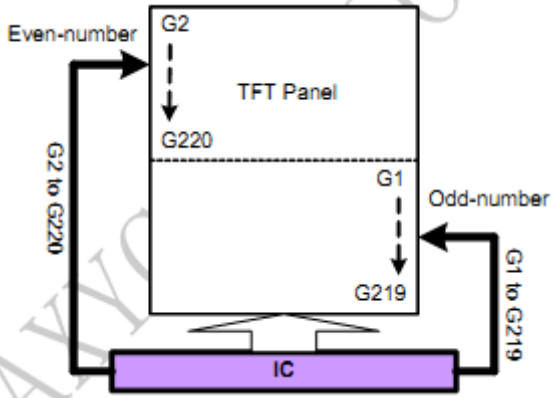
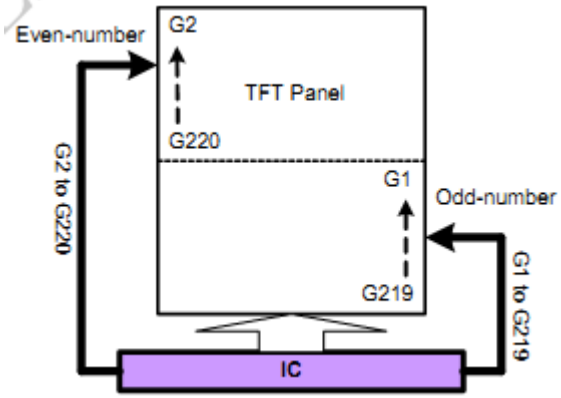
SS: Select the shift direction of outputs from the source driver.
When SS = 0, the shift direction of outputs is from S1 to S528
When SS = 1, the shift direction of outputs is from S528 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.
To assign R, G, B dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0.
To assign R, G, B dots to the source driver pins interchangeably from S528, set SS = 1, BGR = 1.

When changing SS or BGR bits, RAM data must be rewritten.

GS: Select the shift direction of outputs from the gate driver. The scan order is changeable in accordance to the scan mode by the gate driver. Select an optimum shift direction for the assembly.

SM: Set the scan order by the gate driver. Select an optimum scan order for the assembly

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4 ,…,G216, G217,G218, G219, G220
0	1		G220, G219, G218, … G6, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7 , … , G211 G213, G215,G217,G219 G2, G4, G6, G8, …, G212 G214, G216, G218, G220
1	1		G220, G318, G216, …., G10, G8, G6, G4, G2 G219, G217, G215, …, G9, G7, G5, G3, G1

NL[4:0] Set the active gate driver line to drive the liquid crystal display panel with 8 multiples as the following table. The GRAM address mapping is independent from the number of gate lines set with the NL[4:0] bits.

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD lines	Gate driver used
0	0	0	0	0	**Reserved**		
0	0	0	0	1	528*8 dots	8	G1~G8
0	0	0	1	0	528*16 dots	16	G1~G16
0	0	0	1	1	528*24 dots	24	G1~G24
0	0	1	0	0	528*32 dots	32	G1~G32
0	0	1	0	1	528*40 dots	40	G1~G40
0	0	1	1	0	528*48 dots	48	G1~G48
0	0	1	1	1	528*56 dots	56	G1~G56
0	1	0	0	0	528*64 dots	64	G1~G64
0	1	0	0	1	528*72 dots	72	G1~G72
0	1	0	1	0	528*80 dots	80	G1~G80
0	1	0	1	1	528*88 dots	88	G1~G88
0	1	1	0	0	528*96 dots	96	G1~G96
0	1	1	0	1	528*104 dots	104	G1~G104
0	1	1	1	0	528*112 dots	112	G1~G112
0	1	1	1	1	528*120 dots	120	G1~G120
1	0	0	0	0	528*128 dots	128	G1~G128
1	0	0	0	1	528*136 dots	136	G1~G136
1	0	0	1	0	528*144 dots	144	G1~G144
1	0	0	1	1	528*152 dots	152	G1~G152
1	0	1	0	0	528*160 dots	160	G1~G160
1	0	1	0	1	528*168 dots	168	G1~G168
1	1	1	1	0	528*176 dots	176	G1~G176
1	1	1	1	1	528*184 dots	184	G1~G184
1	1	0	0	0	528*192 dots	192	G1~G192
1	1	0	0	1	528*200 dots	200	G1~G200
1	1	0	1	0	528*208 dots	208	G1~G208
1	1	0	1	1	528*216 dots	216	G1~G216
1	1	1	0	0	528*220 dots	220	G1~G220

6.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	INV1	INV0	0	0	0	0	0	0	0	FLD

Set LCD inversion method as show below.
Enables or disables 3-field interlaced scanning function like below.

INV[1:0]	FLD	Description
00	0	Frame Inversion – 1 field interlace
	1	3 field interlace
01	0	Line Inversion – 1 field interlace
	1	Setting Disable
10	0	Two Line Inversion – 1 field interlace
	1	Setting Disable
11	0	No Inversion. Active with positive polarity (VCOM = Low)
	1	No Inversion. Active with negative polarity (VCOM = High)

GS = "0"						GS = "1"					
FLD	"0"	"1"				FLD	"0"	"1"			
Gate \ Field	*	1	2	3	4	Gate \ Field	*	1	2	3	4
G1	*	*			*	G220	*	*			*
G2	*		*			G219	*		*		
G3	*			*		G218	*			*	
G4	*	*			*	G217	*	*			*
G5	*		*			G216	*		*		
G6	*			*		G215	*			*	
G7	*	*			*	G214	*	*			*
G8	*		*			G213	*		*		
G9	*			*		G210	*			*	
G10	*	*			*	G211	*	*			*
	⋮	⋮	⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮
G217	*	*		*		G4	*	*		*	
G218	*		*		*	G3	*		*		*
G219	*			*		G2	*			*	
G220	*	*			*	G1	*	*			*

Figure22 Interlace Scan of AC Drive

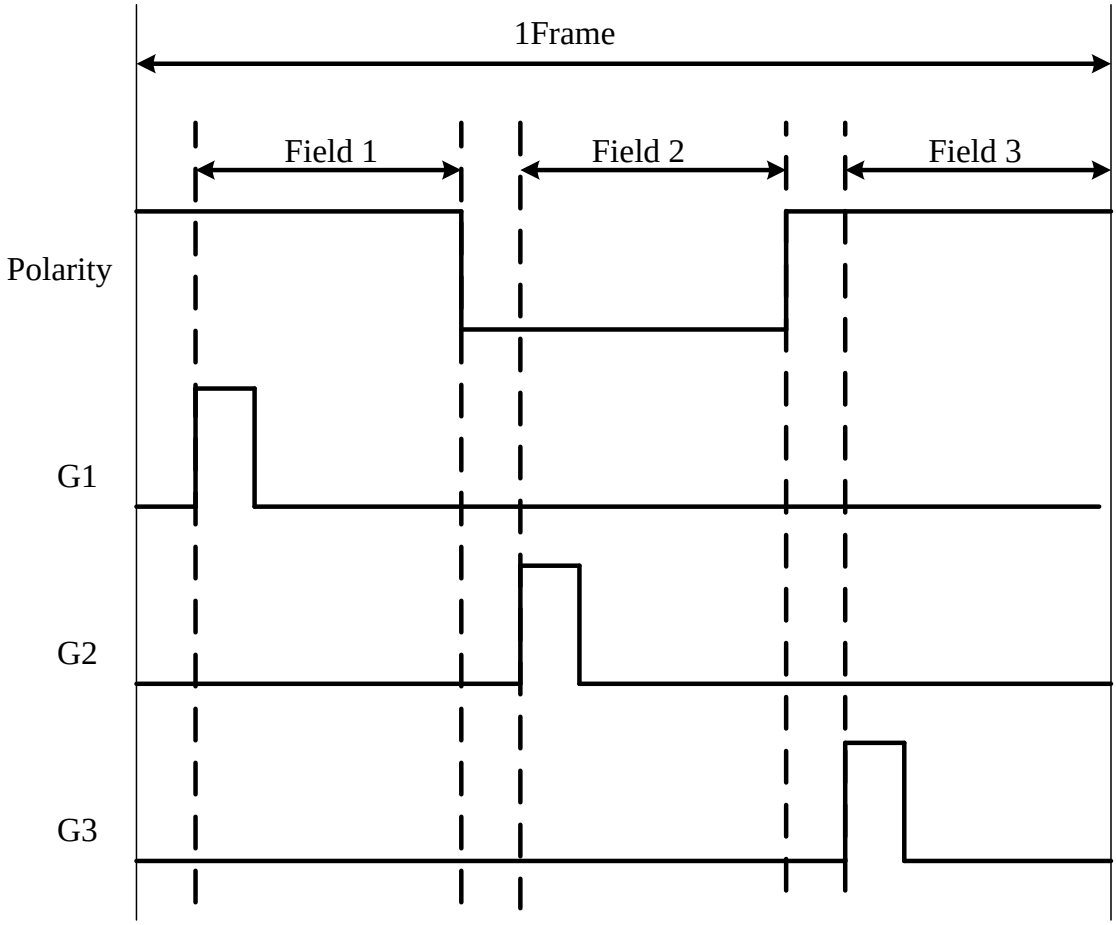


Figure23 Output Timing of Interlace Gate Signals (Three-field is selected)

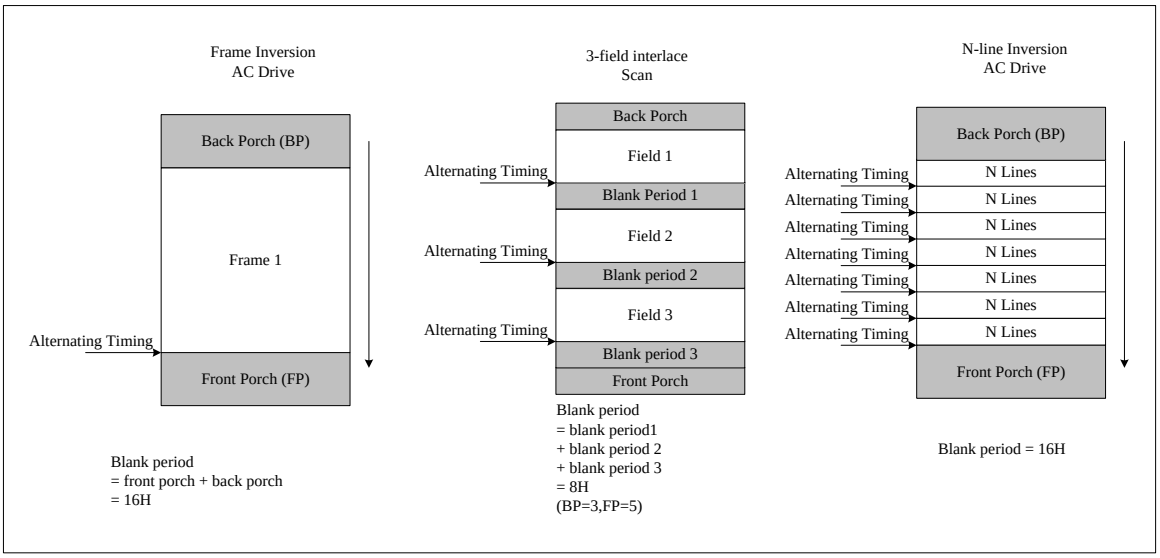


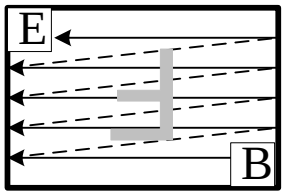
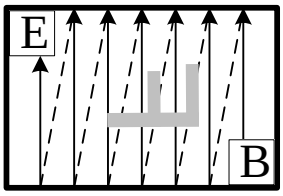
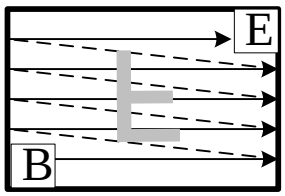
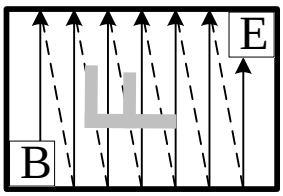
Figure24 AC Driving Alternating Timing

6.2.5. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	BGR	0	0	MDT 1	MDT 0	0	0	I/D1	I/D0	AM	0	0	0

AM Control the GRAM update direction. When AM = "0", the address is updated in horizontal writing direction. When AM = "1", the address is updated in vertical writing direction. When a window area is set by registers R44h and R45h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

	AM = 0 Horizontal	AM = 1 Vertical
I/D[1:0] = 00 Horizontal: decrement Vertical : decrement		
I/D[1:0] = 01 Horizontal : increment Vertical : decrement		

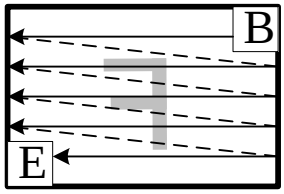
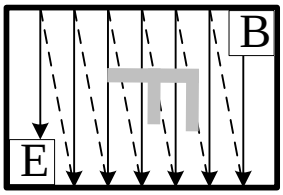
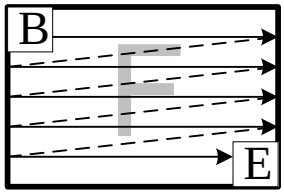
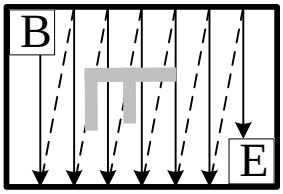
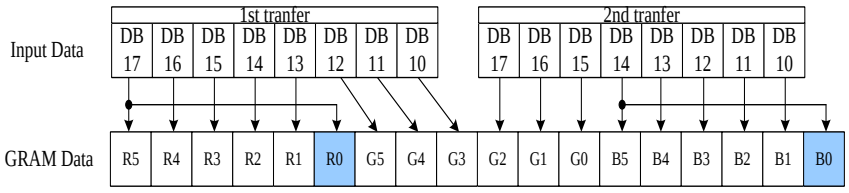
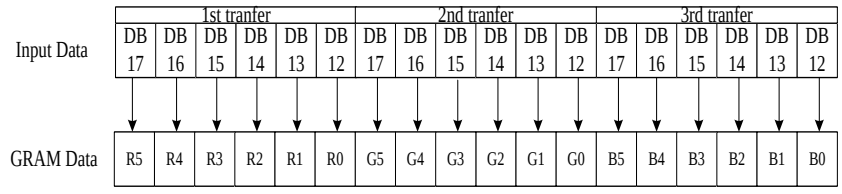
I/D[1:0] = 10 Horizontal : decreme Vertical : increment		
I/D[1:0] = 11 Horizontal : increment Vertical : increment		

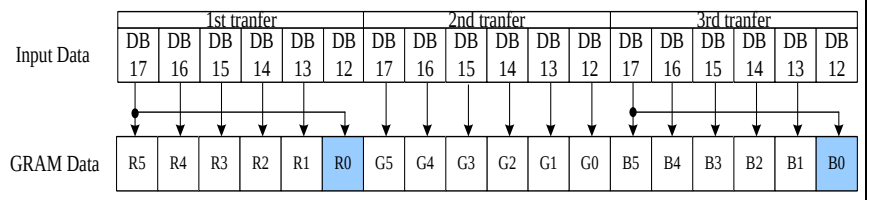
Figure25 GRAM Access Direction Setting

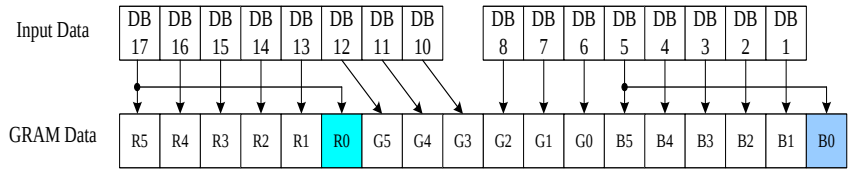
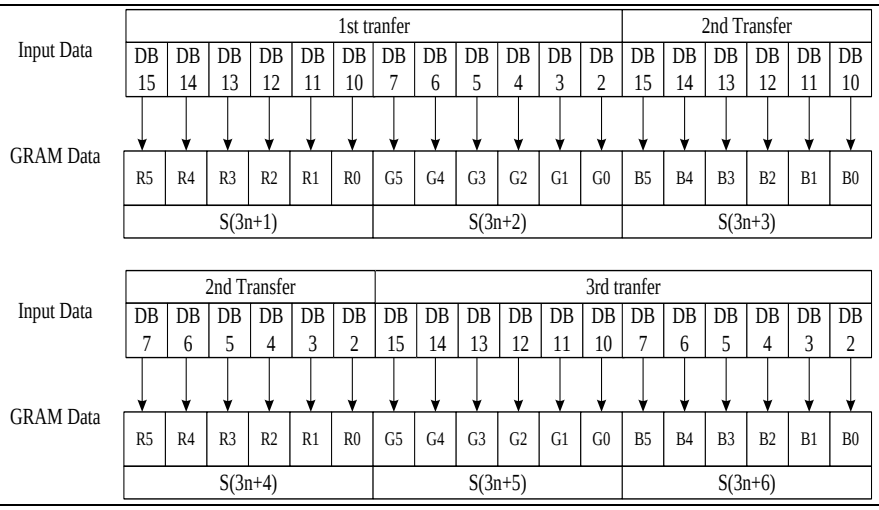
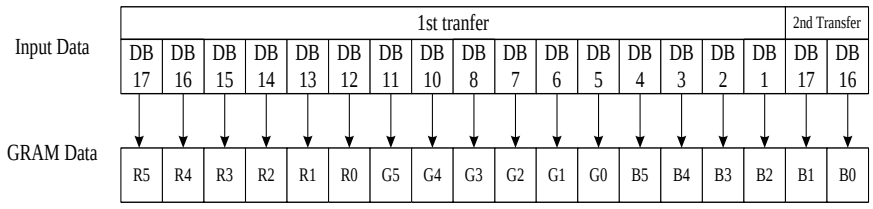
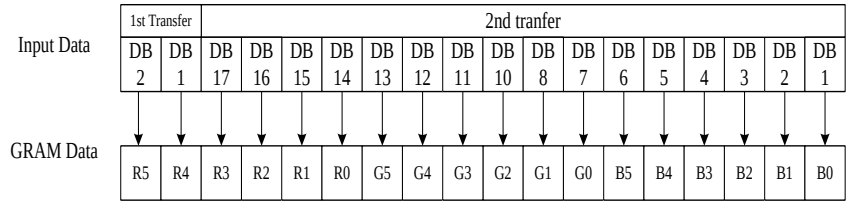
AM	I/D [1:0]	Register R20/R21 Start Address
0/1	00	DBAFh
	01	DB00h
	10	00AFh
	11	0000h

MDT[1:0]: These bits are used to set the data fromat for the 8/16-bit interface mode.

BGR Swap the R and B order of written data.

Interface	MDT[1:0]	Write Data to GRAM
8-bit Mode	00	
	01	Multiple data transfer (MDT[1:0]) function is not available.
	10	

	11	

Interface	MDT[1:0]	Write Data to GRAM
16-bit Mode	00	
	01	
	10	
	11	

6.2.6. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	TEMON	0	0	0	0	0	0	0	GON	CL	REV	D1	D0

D[1:0] Set D[1:0=”11” to turn on the display panel, and D[1:0]=”00” to turn off the display panel.

D1	D0	GON	Source Output	Gate Output	VCOM Output	Display
0	0	X	VSS	VGL	VSS	Off
0	1	0	VSS	VGL	VSS	Off
		1	VSS	Operate	VSS	Off
1	0	0	White on Normally WhitePanel Black on Normally BlackPanel	VGL	Operate	Off
		1	White on Normally WhitePanel Black on Normally BlackPanel	Operate	Operate	Off
1	1	0	Normal Display	VGL	Operate	Off
		1	Normal Display	Operate	Operate	On

Note: data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

GON Set the output level of gate driver G1 ~ G220 as follows

GON	G1~g220 Gate Output
0	VGL
1	**Normal Display**

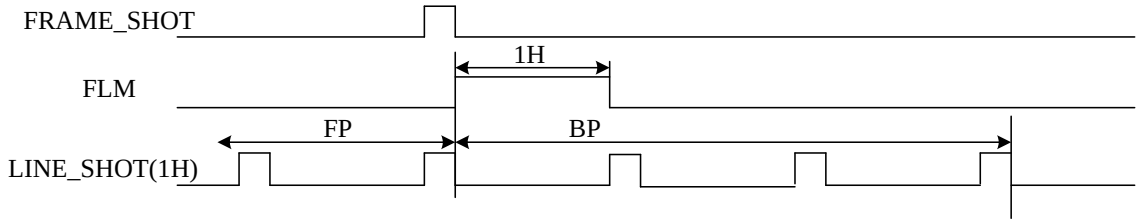
CL When CL = “1”, the 8-color display mode is selected. For details, see the “8-color Display Mode” section.

CL	Color
0	262144
1	8

REV When REV = “1”, the grayscale levels can be inverted.

REV	GRAM Data	Source output in positive polarity	Display Area negative polarity
0	18’h00000	V63	V0
	.	.	.
	.	.	.
	.	.	.
	18’h3FFFF	V0	V63
1	18’h00000	V0	V63
	.	.	.
	.	.	.
	.	.	.
	18’h3FFFF	V63	V0

TEMON:
TEMON = 1, Enable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.
TEMON = 0, Disable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.



6.2.7. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP[3:0]/BP[3:0]

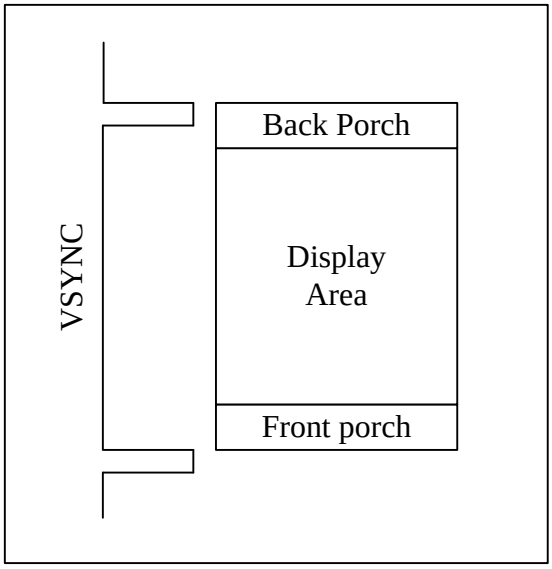
The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively. When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

FP[3:0]	Number of lines for Front Porch
BP[3:0]	Number of lines for Back Porch
0000	Setting prohibited
0001	Setting prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines
1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	Setting prohibited



Note: the output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal

Set the BP[3:0] and FP[3:0] bits as below for each operation mode

Operation mode	Number of interlace scan field	BP	FP	BP+FP
I80/M68 System Interface	FLD = "0"	BP≥2 lines	FP≥lines	FP+BP≤16 lines
	FLD = "1"	BP = 3 lines	FP = 5 lines	
RGB interface		BP≥2 lines	FP≥lines	FP+BP≤16 lines

6.2.8. Frame Cycle Control (R0Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	NO3	NO2	NO1	NO0	SDT3	SDT2	SDT1	SDT0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN[3:0] Set the clock cycle number of one display line

RTN[3:0]	Clock Cycle per lines
4'h0	16clocks
4'h1	17clocks
4'h2	18clocks
4'h3	19clocks
4'h4	20clocks
4'h5	21clocks
4'h6	22clocks
4'h7	23clocks
4'h8	24clocks
4'h9	25clocks
4'hA	26clocks
4'hB	27clocks
4'hC	28clocks
4'hD	29clocks
4'hE	30clocks
4'hF	31clocks

NO[3:0]: Set amount of non-overlay for the gate output.

	Gate output delay period		
NO[3:0]	System interface Mode	18/16-bit RGB Interface Mode	6-bit RGB Interface Mode
4'h0	Setting disable	Setting disable	Setting disable
4'h1	1 clock	8 clocks	8*3 clocks
4'h2	2 clock	16 clocks	16*3 clocks
4'h3	3 clock	24 clocks	24*3 clocks
4'h4	4 clock	32 clocks	32*3 clocks
4'h5	5 clock	40 clocks	40*3 clocks

4'h6	6 clock	48 clocks	48*3 clocks
4'h7	7 clock	56 clocks	56*3 clocks
4'h8	8 clock	64 clocks	64*3 clocks
4'h9	9 clock	72 clocks	72*3 clocks
4'hA	10 clock	80 clocks	80*3 clocks
4'hB	Setting disable	88 clocks	88*3 clocks
4'hC	Setting disable	96 clocks	96*3 clocks
4'Hd	Setting disable	104 clocks	104*3 clocks
4'hE	Setting disable	112 clocks	112*3 clocks
4'hF	Setting disable	120 clocks	120*3 clocks

SDT[3:0]: Set delay amount from gate edge (end) to source output.

Source output delay period			
NO[3:0]	**System interface Mode**	**18/16-bit RGB Interface Mode**	**6-bit RGB Interface Mode**
4'h0	Setting disable	Setting disable	Setting disable
4'h1	1 clock	8 clocks	8*3 clocks
4'h2	2 clock	16 clocks	16*3 clocks
4'h3	3 clock	24 clocks	24*3 clocks
4'h4	4 clock	32 clocks	32*3 clocks
4'h5	5 clock	40 clocks	40*3 clocks
4'h6	6 clock	48 clocks	48*3 clocks
4'h7	Setting disable	Setting disable	Setting disable
4'h8	Setting disable	Setting disable	Setting disable
4'h9	Setting disable	Setting disable	Setting disable
4'hA	Setting disable	Setting disable	Setting disable
4'hB	Setting disable	Setting disable	Setting disable
4'hC	Setting disable	Setting disable	Setting disable
4'Hd	Setting disable	Setting disable	Setting disable
4'hE	Setting disable	Setting disable	Setting disable
4'hF	Setting disable	Setting disable	Setting disable

6.2.9. RGB Input Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	RM	0	0	0	DM	0	0	RIM1	RIM0

RIM[1:0] Select the data bus width of RGB interface modes.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer/pixel)
1	0	6-bit RGB interface (three transfers/pixel)
1	1	Setting disabled

DM Select the display operation mode.

DM	Display interface
0	Internal system clock
1	RGB clock

RM Select the interface to access the GRAM

RM	Interface for RAM Access
0	Internal system clock interface
1	RGB interface (when writing display data by the RGB interface.)

Display state	Operation mode	RAM Access(RM)	Display operation Mode (DM)
Still picture	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM =0)
Moving picture	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM=1)
Rewrite still picture area while RGB interface Displaying moving pictures. RGB interface (2)		System interface (RM = 0)	RGB Interface (DM=1)

Note 1) Registers are set only via the system interface or SPI interface.
Note 2) Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

6.2.10. Oscillator Control (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FOSC[3]	FOSC[2]	FOSC[1]	FOSC[0]	0	0	0	0	0	0	0	OSC_EN

FOSC[3:0]: Select the oscillation frequency of internal oscillator.

FR_SEL[3:0]	Frame Rate	FR_SEL[3:0]	Frame Rate
0000	33Hz	1000	76 Hz
0001	41 Hz	1001	81 Hz
0010	46 Hz	1010	88 Hz
0011	50 Hz	1011	96 Hz
0100	56 Hz	1100	106 Hz
0101	62 Hz	1101	118 Hz
0110	66 Hz	1110	132 Hz
0111 (default)	71 Hz	1111	Setting prohibited

OSC_EN
This instruction starts the oscillator from the Halt State in the standby mode. After this instruction, Wait at least 10 ms for oscillation to stabilize before giving the next instruction.

OSC_EN	OSC Control
0	OSC. Off
1	OSC. On

6.2.11. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	STB

STB: When STB = 1, the GC9201 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal oscillator. Further, no external clock pulses are supplied.

Outputs	Congditions
VCOM	GND
Gate	GND
Source	GND

6.2.12. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	APON	0	0	0	0	0	0	0	0	0	0	0	0

APON: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the auto booster sequence circuit is stopped. In case of APON=1, booster circuits are automatically and sequentially operated.

6.2.13. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	BT2	BT1	BT0	0	0	0	0	0	0	0	1	0	0	1	0

BT[2:0] The output factor of step-up circuit is selected. Adjust scale factor of the step-up circuit by the voltage used. Lower amplification of the step-up circuit consumes less current.

BT2	BT1	BT0	Circuit1 AVDD	Circuit4 VCL	Circuit2 VGH	Circuit3 VGL
0	0	0	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
0	0	1	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
0	1	0	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
0	1	1	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
1	0	0	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
1	0	1	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
1	1	0	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI
1	1	1	2 x VCI	-1 x VCL	6 x VCI	-5 x VCI

Note : The condition of AVDD $\leqslant$ 5.5V and VGH $\leqslant$ 15.5V must be satisfied.

6.2.14. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0

GVD[6:0]: Set the amplifying factor of the GVDD voltage (the voltage for the Gamma voltage). It allows ranging from 2.66V to 5.5V.

GVD[6:0]	GVDD	GVD[6:0]	GVDD	GVD[6:0]	GVDD	GVD[6:0]	GVDD
7'h00	5.05V	7'h20	3.10V	7'h40	3.74V	7'h60	4.38V
7'h01	5.10V	7'h21	3.12V	7'h41	3.76V	7'h61	4.40V
7'h02	5.15V	7'h22	3.14V	7'h42	3.78V	7'h62	4.42V
7'h03	5.20V	7'h23	3.16V	7'h43	3.80V	7'h63	4.44V
7'h04	5.25V	7'h24	3.18V	7'h44	3.82V	7'h64	4.46V
7'h05	5.30V	7'h25	3.20V	7'h45	3.84V	7'h65	4.48V
7'h06	5.35V	7'h26	3.22V	7'h46	3.86V	7'h66	4.50V
7'h07	5.40V	7'h27	3.24V	7'h47	3.88V	7'h67	4.52V
7'h08	5.45V	7'h28	3.26V	7'h48	3.90V	7'h68	4.54V
7'h09	5.50V	7'h29	3.28V	7'h49	3.92V	7'h69	4.56V
7'hA	2.66V	7'h2A	3.30V	7'h4A	3.94V	7'h6A	4.58V
7'hB	2.68V	7'h2B	3.32V	7'h4B	3.96V	7'h6B	4.60V
7'hC	2.70V	7'h2C	3.34V	7'h4C	3.98V	7'h6C	4.62V
7'hD	2.72V	7'h2D	3.36V	7'h4D	4.00V	7'h6D	4.64V
7'hE	2.74V	7'h2E	3.38V	7'h4E	4.02V	7'h6E	4.66V
7'hF	2.76V	7'h2F	3.40V	7'h4F	4.04V	7'h6F	4.68V
7'h10	2.78V	7'h30	3.42V	7'h50	4.06V	7'h70	4.70V
7'h11	2.80V	7'h31	3.44V	7'h51	4.08V	7'h71	4.72V
7'h12	2.82V	7'h32	3.46V	7'h52	4.10V	7'h72	4.74V
7'h13	2.84V	7'h33	3.48V	7'h53	4.12V	7'h73	4.76V
7'h14	2.86V	7'h34	3.50V	7'h54	4.14V	7'h74	4.78V
7'h15	2.88V	7'h35	3.52V	7'h55	4.16V	7'h75	4.80V
7'h16	2.90V	7'h36	3.54V	7'h56	4.18V	7'h76	4.82V
7'h17	2.92V	7'h37	3.56V	7'h57	4.20V	7'h77	4.84V
7'h18	2.94V	7'h38	3.58V	7'h58	4.22V	7'h78	4.86V
7'h19	2.96V	7'h39	3.60V	7'h59	4.24V	7'h79	4.88V
7'h1A	2.98V	7'h3A	3.62V	7'h5A	4.26V	7'h7A	4.90V
7'h1B	3.00V	7'h3B	3.64V	7'h5B	4.28V	7'h7B	4.92V
7'h1C	3.02V	7'h3C	3.66V	7'h5C	4.30V	7'h7C	4.94V
7'h1D	3.04V	7'h3D	3.68V	7'h5D	4.32V	7'h7D	4.96V
7'h1E	3.06V	7'h3E	3.70V	7'h5E	4.34V	7'h7E	4.98V
7'h1F	3.08V	7'h3F	3.72V	7'h5F	4.36V	7'h7F	5.00V

6.2.15. Power Control 5 (R14h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VCOMG	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0

VCOMG: When VCOMG = 1, low level of VCOM signal is to be fixed at GND. Therefore, the amplitude of VCOM signal is determined as |VCOMH – GND| regardless of VML setting. In this case, VCOML pin can be open or connected to GND, because VCOML amp is off and VCOML output is floated. When VCOMG=0, the amplitude of VCOM signal is determined as |VCOMH – VCOML|.

VCM[6:0]: Set the VCOMH voltage (a high level voltage at the Vcom alternating drive), these bits amplify the VCOMH voltage from 0.4015 to 1.1000 times the GVDD voltage.

VCOM[6:0]	VCOMH voltage
7’h00	GVDD x 0.4015
7’h01	GVDD x 0.4070
7’h02	GVDD x 0.4125
7;h03	GVDD x 0.4180
:	:
7’h7A	GVDD x 1.0725
7’h7B	GVDD x 1.0780
7’h7C	GVDD x 1.0835
7’h7D	GVDD x 1.0890
7’h7E	GVDD x 1.0945
7’h7F	GVDD x 1.100

[NOTE]

1. **VCOMH = GVDD x (0.4015 + 0.0055 x VCM)**
2. When using VCI recycling function, VCOMH voltage should be higher than VCI.
3. VCM[6:0] register set is invalid when VCM_SEL=1.

VML[6:0]: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM from 0.534 to 1.20 times the GVDD voltage. When the VCOM alternation is not driven, the settings become invalid.

VML[6:0]	VCOMH Amplitude Voltage
7’h00 ~ 7’h0F	Setting prohibited
7’h10	GVDD x 0.534
7’h11	GVDD x 0.540
7’h12	GVDD x 0.546
:	:
7’h7A	GVDD x 1.170
7’h7B	GVDD x 1.176
7’h7C	GVDD x 1.182
7’h7D	GVDD x 1.188
7’h7E	GVDD x 1.194
7’h7F	GVDD x 1.200

[NOTE]

1**. VCOM amplitude = GVDD x (0.534 + 0.006(VML-16))**
2. Adjust the settings between GVDD and VML[6:0] so that the Vcom amplitudes are lower than 6.0 V.
3. VCOML voltage should be satisfied the following condition. : 0.0V > VCOML > VCL+0.5V

6.2.16. RAM Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	x	x	x	x	x	x	x	x	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	x	x	x	x	x	x	x	x	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD[15:0] Set the initial value of address counter (AC).
The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

Note1:GRAM address setting is not allowed in standby mode. Ensure that the address is set within the specified window area specified with VSA, VEA, HAS and HEA.
Note2: When the RGB interface is selected (RM = "1"), the address AD[15:0] is set to the address counter every frame on the falling edge of VSYNC.
Note3: When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD[15:0] is set upon the execution of an instruction.

AD[15:0]	Gram setting
"0000H" to "00AF" H	Bitmap data for G1
"0100H" to "01AF" H	Bitmap data for G2
"0200H" to "02AF" H	Bitmap data for G3
"0300H" to "03AF" H	Bitmap data for G4
:	:
:	:
:	:
"0800H" to "D8AF" H	Bitmap data for G217
"0900H" to "D9AF" H	Bitmap data for G218
"0A00H" to "DAAF" H	Bitmap data for G219
"0B00H" to "DBAF" H	Bitmap data for G220

6.2.17. Write Data to GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0]), the DB[17:0] pin assignment differs for each interface															

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

6.2.18. Read Data from GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM read data (RD[17:0]), the DB[17:0] pin assignment differs for each interface															

RD [17:0] Read 18-bit data from GRAM through the read data register (RDR).

6.2.19. Gate Scan Control (R30h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN [4:0] The GC9201 allows specifying the gate line from which the gate driver starts scan by setting the SCN[4:0] bits.

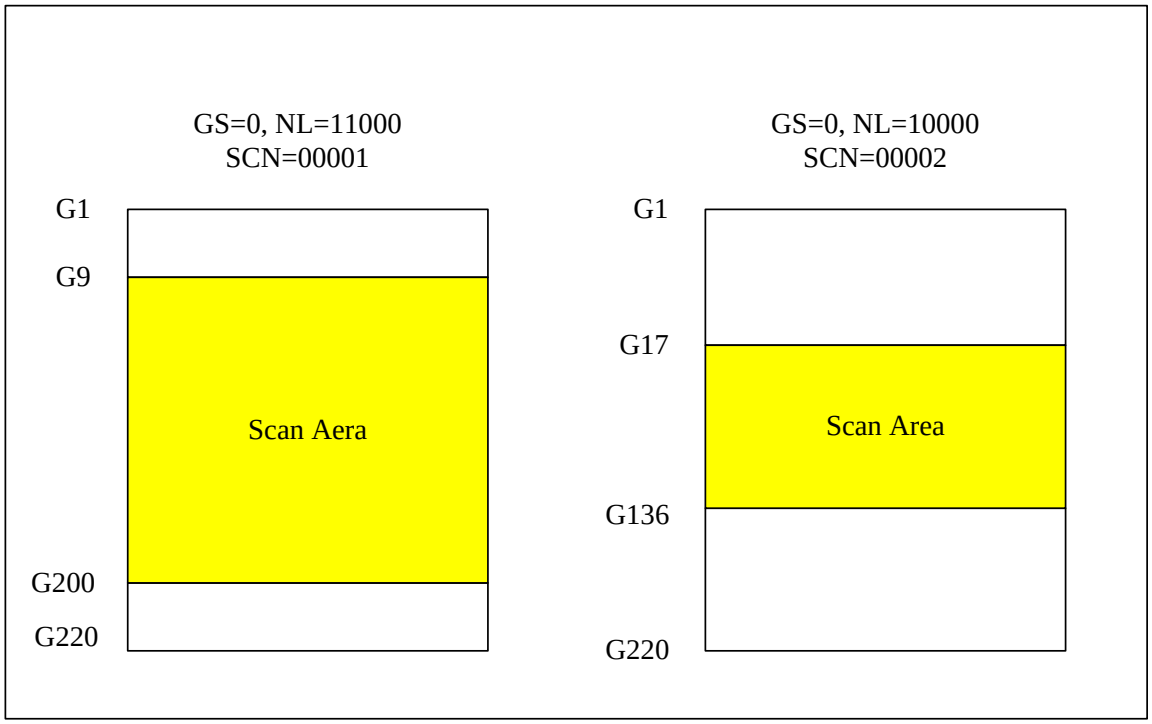


Figure28 Scanning Start Position for Gate Driver

Note: Don't set NL[4:0], SCN[4:0] over the end position of gate line (G220)
Note: Set NL[4:0] and SCN[4:0] to let the number for the end position of the gate line scans will not exceed 220.

SCN4	SCN3	SCN2	SCN1	SCN0	Scaning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G220	G1	G220
0	0	0	0	1	G9	G212	G17	G204
0	0	0	1	0	G17	G204	G33	G188
0	0	0	1	1	G25	G196	G49	G172

0	0	1	0	0	G33	G188	G65	G156
0	0	1	0	1	G41	G180	G81	G140
0	0	1	1	0	G49	G172	G97	G124
0	0	1	1	1	G57	G164	G113	G108
0	1	0	0	0	G65	G156	G129	G92
0	1	0	0	1	G73	G148	G145	G76
0	1	0	1	0	G81	G140	G161	G60
0	1	0	1	1	G89	G132	G177	G44
0	1	1	0	0	G97	G124	G193	G28
0	1	1	0	1	G105	G116	G209	G12
0	1	1	1	0	G113	G108	G2	G219
0	1	1	1	1	G121	G100	G18	G203
1	0	0	0	0	G129	G92	G34	G187
1	0	0	0	1	G137	G84	G50	G171
1	0	0	1	0	G145	G76	G66	G155
1	0	0	1	1	G153	G68	G82	G139
1	0	1	0	0	G161	G60	G98	G123
1	0	1	0	1	G169	G52	G114	G107
1	0	1	1	0	G177	G44	G130	G91
1	0	1	1	1	G185	G36	G146	G75
1	1	0	0	0	G193	G28	G162	G59
1	1	0	0	1	G201	G20	G178	G43
1	1	0	1	0	G209	G12	G194	G27
1	1	0	1	1	G217	G4	G210	G11

6.2.20. Vertical Scroll Control 1 (R31h, R32h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0
W	1	0	0	0	0	0	0	0	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0

SSA[7:0]: Specify scroll start address at the scroll display for vertical smooth scrolling.

SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0	Scroll Sart Line
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 linse
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

SEA[7:0]: Specify scroll end address at the scroll display for vertical smooth scrolling.

SEA7	SEA6	SEA5	SEA4	SEA3	SEA2	SEA1	SEA0	Scroll End Line
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 linse
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

[NOTE]
Do not set any higher raster-row than 219 (“DB”H).
Set SS17-10 ≤ SSA7-0, if set out of range, SSA7-0 = SS17-10.
Set SE17-10 ≥ SEA7-0, if set out of range, SEA7-0 = SE17-10

6.2.21. Vertical Scroll Control 1 (R33h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0

SST8-0: Specify scroll start and step at the scroll display for vertical smooth scrolling. Any line from the 1st to 220th can be scrolled for the number of the raster-row. After 219th line is displayed, the display restarts from the first raster-row. When SST7-0 = 00000000, Vertical Scroll Function is disabled.

SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0	Scroll Lines
0	0	0	0	0	0	0	0	0 lines
0	0	0	0	0	0	0	1	1 lines
0	0	0	0	0	0	1	0	2 linse
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

[NOTE]
Do not set any higher raster-row than 219 (“DB”H)
Set SS17-10 < SSA7-0 + SST7-0 ≤ SEA7-0 ≤ SE17-10, if set out of range, Scroll function is disabled

6.2.22. Partial Screen Driving Position (R34h, R35h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
W	1	0	0	0	0	0	0	0	0	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

SE1[7:0]: Specify the driving end position for the screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For example, when SS1[7:0] = 019h and SE1[7:0] = 029h are set, the LCD driving is performed from G26 to G42, and non-display driving is performed for G1 to G25, G43, and others. Ensure that SS1[7:0] ≤ SE1[7:0] ≤ DBh.

SS1[7:0]: Specify the drive starting position for the first screen in a line unit. The LCD driving starts from the 'set value +1' gate driver.

Note: Do not set the partial setting when the operation is in the normal display condition. Set this register only when in the partial display condition.

Ex) SS1[7:0]=07h and SE1[7:0]=10h are performed from G8 to G17.

6.2.23. Horizontal and Vertical RAM Address Position (R36h/R37h, R38h/R39h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	0	0	0	0	0	0	0	0	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
W	1	0	0	0	0	0	0	0	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA[7:0]/HEA[7:0]: HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure "00"h ≤ HSA[7:0]< HEA[7:0] ≤ "AF"h.

VSA[7:0]/VEA[7:0] VSA[7:0] and VEA[7:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure "00"h ≤ VSA[7:0]< VEA[7:0] ≤ "DB"h.

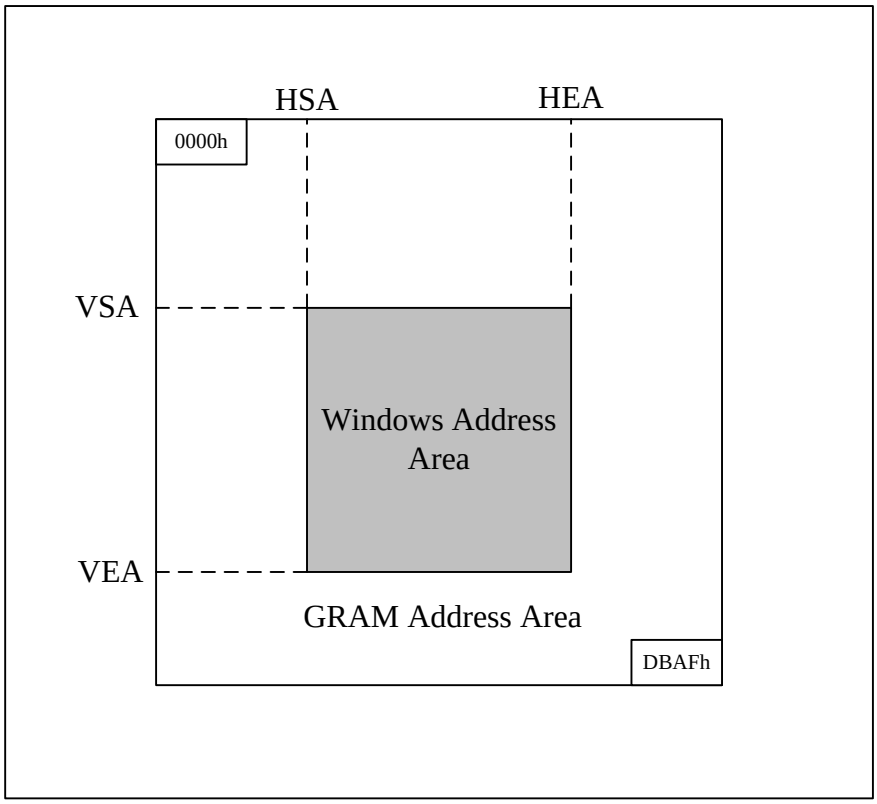


Figure29 GRAM Access Range configuration

“00”h ≤HAS[7:0] ≤HEA[7:0] ≤”AF”h
“00”h ≤VSA[7:0] ≤VEA[7:0] ≤”DB”h

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

6.2.24. Gamma Control (R50h ~ R59h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	KP13	KP12	KP11	KP10	0	0	0	0	KP03	KP02	KP01	KP00
R51h	W	1	0	0	0	0	KP33	KP32	KP31	KP30	0	0	0	0	KP23	KP22	KP21	KP20
R52h	W	1	0	0	0	0	KP53	KP52	KP51	KP50	0	0	0	0	KP43	KP42	KP41	KP40
R53h	W	1	0	0	0	0	RP13	RP12	RP11	RP10	0	0	0	0	RP02	RP02	RP01	RP00
R54h	W	1	0	0	0	0	KN13	KN12	KN11	KN10	0	0	0	0	KN03	KN02	KN01	KN00
R55h	W	1	0	0	0	0	KN33	KN32	KN31	KN30	0	0	0	0	KN23	KN22	KN21	KN20
R56h	W	1	0	0	0	0	KN53	KN52	KN51	KN50	0	0	0	0	KN43	KN42	KN41	KN40
R57h	W	1	0	0	0	0	RN13	RN12	RN11	RN10	0	0	0	0	RN03	RN02	RN01	RN00
R58h	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00
R59h	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00

KP53-00: The gamma fine adjustment register for the positive polarity output
*Initial Value: R50h = 0000
*Initial Value: R51h = 0808
*Initial Value: R52h = 080A

RP13-00: The gradient adjustment register for the positive polarity output.
*Initial Value: R53h = 000A

KN53-00: The gamma fine adjustment register for the negative polarity output.
*Initial Value: R54h = 0A08
*Initial Value: R55h = 0808
*Initial Value: R56h = 0000

RN13-00: The gradient adjustment register for the negative polarity output
*Initial Value: R57h= 0A00

VRP14-00: The amplitude adjustment register for the positive polarity output.
*Initial Value: R58h = 0710

VRN14-00: The amplitude adjustment register for the negative polarity output
*Initial Value: R59h = 0710

7. GRAM Address Map & Read/Write

GC9201 has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80/M68 system, SPI and RGB interfaces

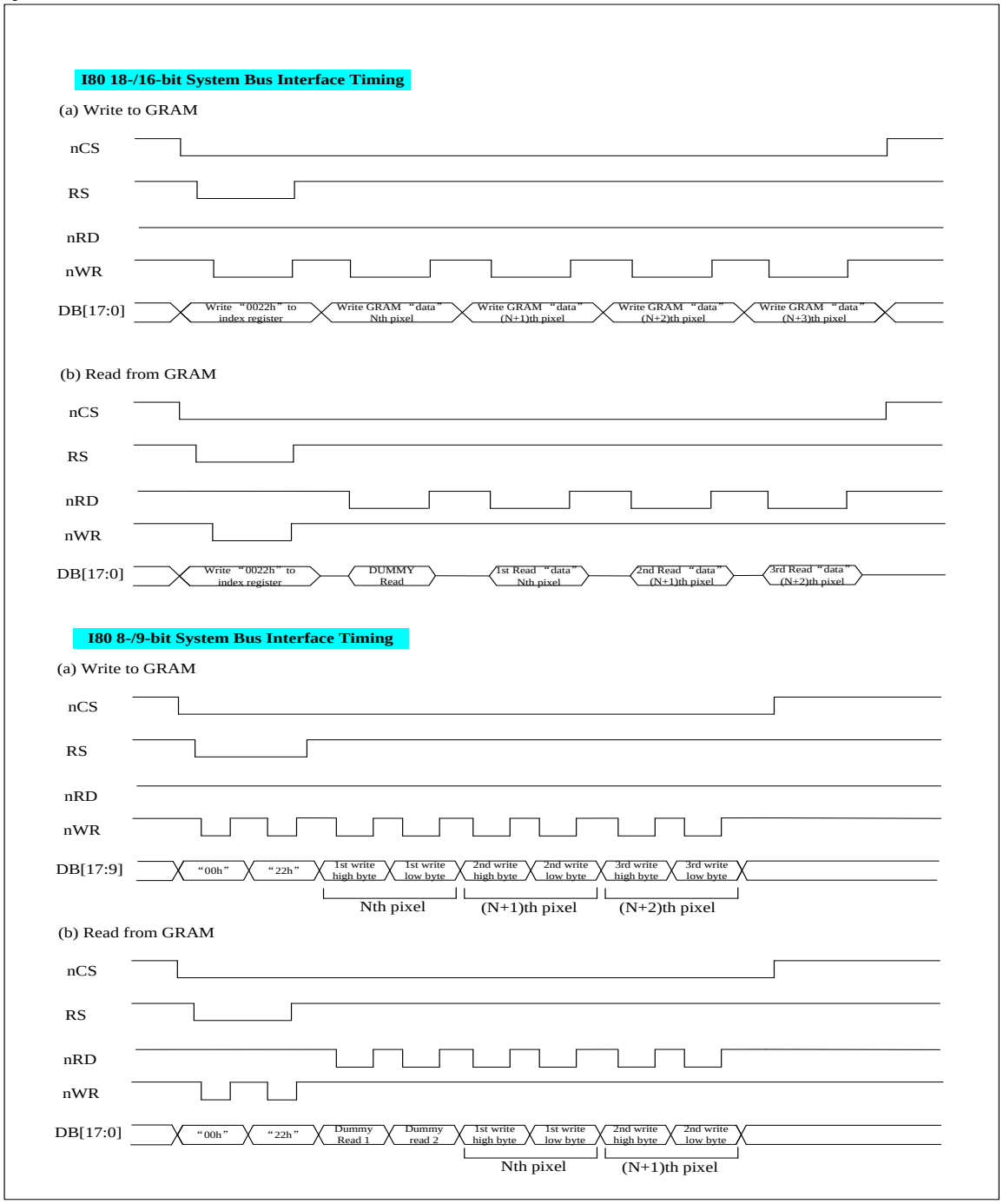
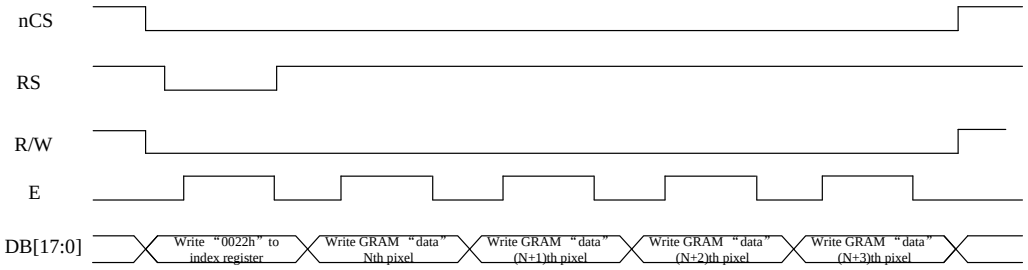


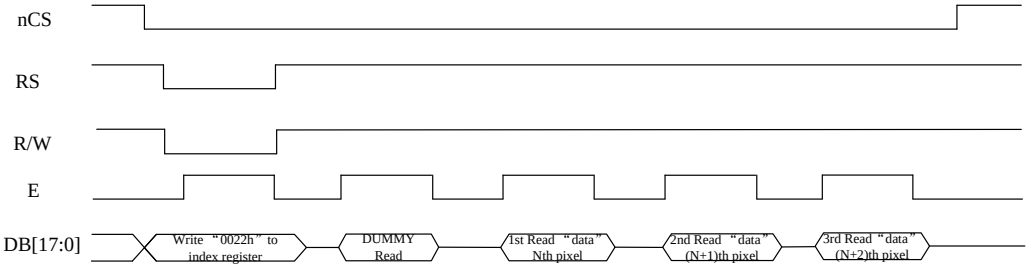
Figure30 GRAM Read/Write Timing of i80-System Interface

M68 18-/16-bit System Bus Interface Timing

(a) Write to GRAM

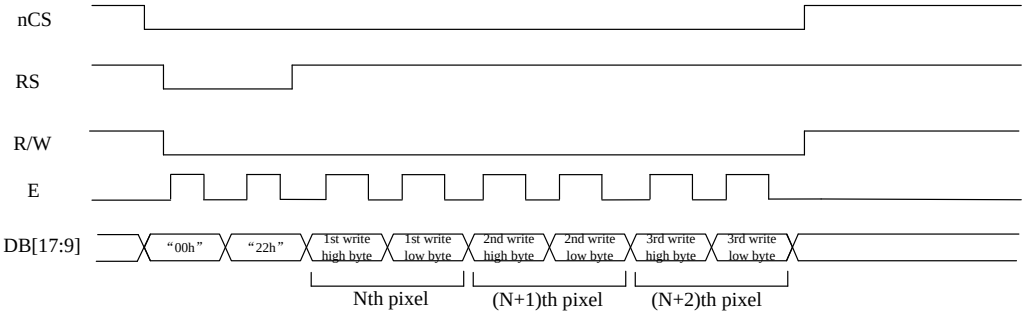


(b) Read from GRAM



M68 8-/9-bit System Bus Interface Timing

(a) Write to GRAM



(b) Read from GRAM

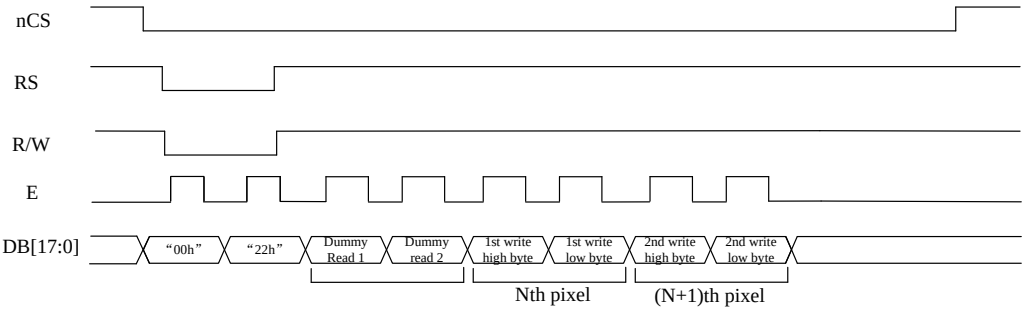


Figure31 GRAM Read/Write Timing of M68-System Interface

GRAM address map table of SS=0, BGR=0

SS=0,BGR=0		S1~S3	S4~S6	S7~S8	.	S520~S522	S523~S525	S526~S528
GS=0	GS=1	DB17~0	DB17~0	DB17~0	.	DB17~0	DB17~0	DB17~0
G1	G220	"0000h"	"0001h"	"0002h"	.	"00ADh"	"00AEh"	"00AFh"
G2	G219	"0100h"	"0101h"	"0102h"	.	"01ADh"	"01AEh"	"01AFh"
G3	G218	"0200h"	"0201h"	"0202h"	.	"02ADh"	"02AEh"	"02AFh"
G4	G217	"0300h"	"0301h"	"0302h"	.	"03ADh"	"03AEh"	"03AFh"
G5	G216	"0400h"	"0401h"	"0402h"	.	"04ADh"	"04AEh"	"04AFh"
G6	G215	"0500h"	"0501h"	"0502h"	.	"05ADh"	"05AEh"	"05AFh"
G7	G214	"0600h"	"0601h"	"0602h"	.	"06ADh"	"06AEh"	"06AFh"
G8	G213	"0700h"	"0701h"	"0702h"	.	"07ADh"	"07AEh"	"07AFh"
G9	G212	"0800h"	"0801h"	"0802h"	.	"08ADh"	"08AEh"	"08AFh"
G10	G211	"0900h"	"0901h"	"0902h"	.	"09ADh"	"09AEh"	"09AFh"
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
G211	G10	"D200h"	"D201h"	"D202h"	.	"D2ADh"	"D2AEh"	"D2AFh"
G212	G9	"D300h"	"D301h"	"D302h"	.	"D3ADh"	"D3AEh"	"D3AFh"
G213	G8	"D400h"	"D400h"	"D400h"	.	"D4ADh"	"D4AEh"	"D4AFh"
G214	G7	"D500h"	"D500h"	"D500h"	.	"D5ADh"	"D5AEh"	"D5AFh"
G215	G6	"D600h"	"D600h"	"D600h"	.	"D6ADh"	"D6AEh"	"D6AFh"
G216	G5	"D700h"	"D700h"	"D700h"	.	"D7ADh"	"D7AEh"	"D7AFh"
G217	G4	"D800h"	"D800h"	"D800h"	.	"D8ADh"	"D8AEh"	"D8AFh"
G218	G3	"D900h"	"D900h"	"D900h"	.	"D9ADh"	"D9AEh"	"D9AFh"
G219	G2	"DA00h"	"DA01h"	"DA02h"	.	"DAADh"	"DAAEh"	"DAAFh"
G220	G1	"DB00h"	"DB01h"	"DB02h"	.	"DBADh"	"DBAEh"	"DBAFh"

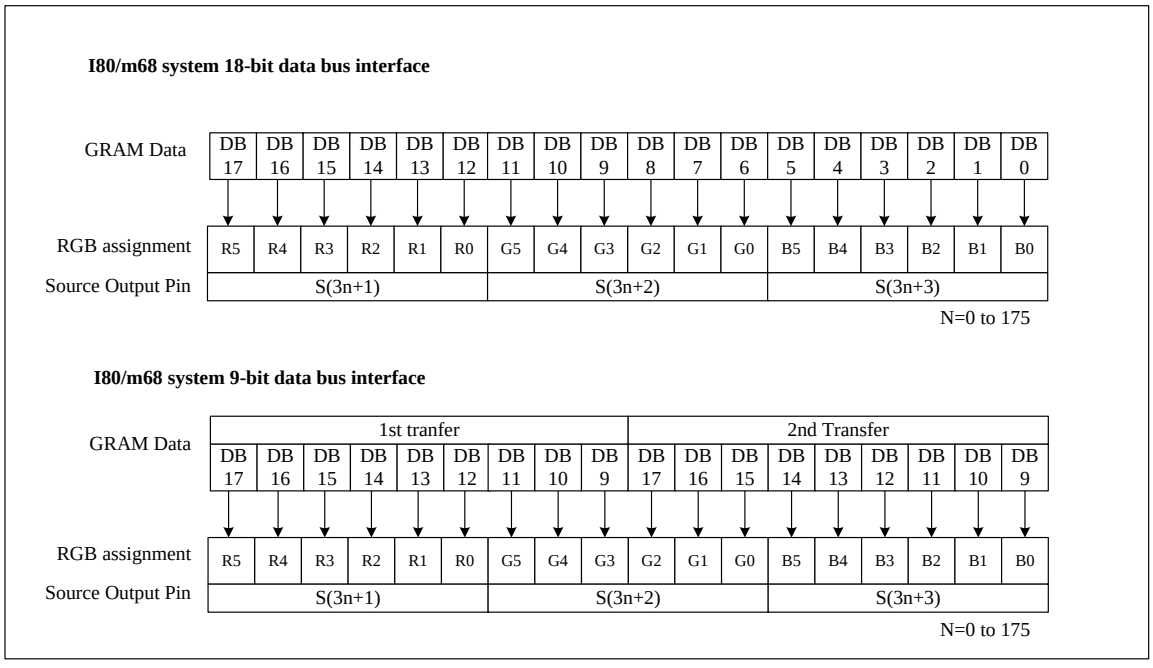


Figure32 i80-System Interface with 18-/9-bit Data Bus (SS="0", BGR="0")

GRAM address map table of SS=1, BGR=1

SS=0,BGR=0		S1~S3	S4~S6	S7~S8	.	S520~S522	S523~S525	S526~S528
GS=0	GS=1	DB17~0	DB17~0	DB17~0	.	DB17~0	DB17~0	DB17~0
G1	G220	"00AFh"	"00AEh"	"00ADh"	.	"0002h"	"0001h"	"0000h"
G2	G219	"01AFh"	"01AEh"	"01ADh"	.	"0102h"	"0101h"	"0100h"
G3	G218	"02AFh"	"02AEh"	"02ADh"	.	"0202h"	"0201h"	"0200h"
G4	G217	"03AFh"	"03AEh"	"03ADh"	.	"0302h"	"0301h"	"0300h"
G5	G216	"04AFh"	"04AEh"	"04ADh"	.	"0402h"	"0401h"	"0400h"
G6	G215	"05AFh"	"05AEh"	"05ADh"	.	"0502h"	"0501h"	"0500h"
G7	G214	"06AFh"	"06AEh"	"06ADh"	.	"0602h"	"0601h"	"0600h"
G8	G213	"07AFh"	"07AEh"	"07ADh"	.	"0702h"	"0701h"	"0700h"
G9	G212	"08AFh"	"08AEh"	"08ADh"	.	"0802h"	"0801h"	"0800h"
G10	G211	"09AFh"	"09AEh"	"09ADh"	.	"0902h"	"0901h"	"0900h"
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
G211	G10	"D2AFh"	"D2AEh"	"D2ADh"	.	"D202h"	"D201h"	"D200h"
G212	G9	"D3AFh"	"D3AEh"	"D3ADh"	.	"D302h"	"D301h"	"D300h"
G213	G8	"D4AFh"	"D4AEh"	"D4ADh"	.	"D400h"	"D400h"	"D400h"
G214	G7	"D5AFh"	"D5AEh"	"D5ADh"	.	"D500h"	"D500h"	"D500h"
G215	G6	"D6AFh"	"D6AEh"	"D6ADh"	.	"D600h"	"D600h"	"D600h"
G216	G5	"D7AFh"	"D7AEh"	"D7ADh"	.	"D700h"	"D700h"	"D700h"
G217	G4	"D8AFh"	"D8AEh"	"D8ADh"	.	"D800h"	"D800h"	"D800h"
G218	G3	"D9AFh"	"D9AEh"	"D9ADh"	.	"D900h"	"D900h"	"D900h"
G219	G2	"DAAFh"	"DAAEh"	"DAADh"	.	"DA02h"	"DA01h"	"DA00h"
G220	G1	"DBAFh"	"DBAEh"	"DBADh"	.	"DB02h"	"DB01h"	"DB00h"

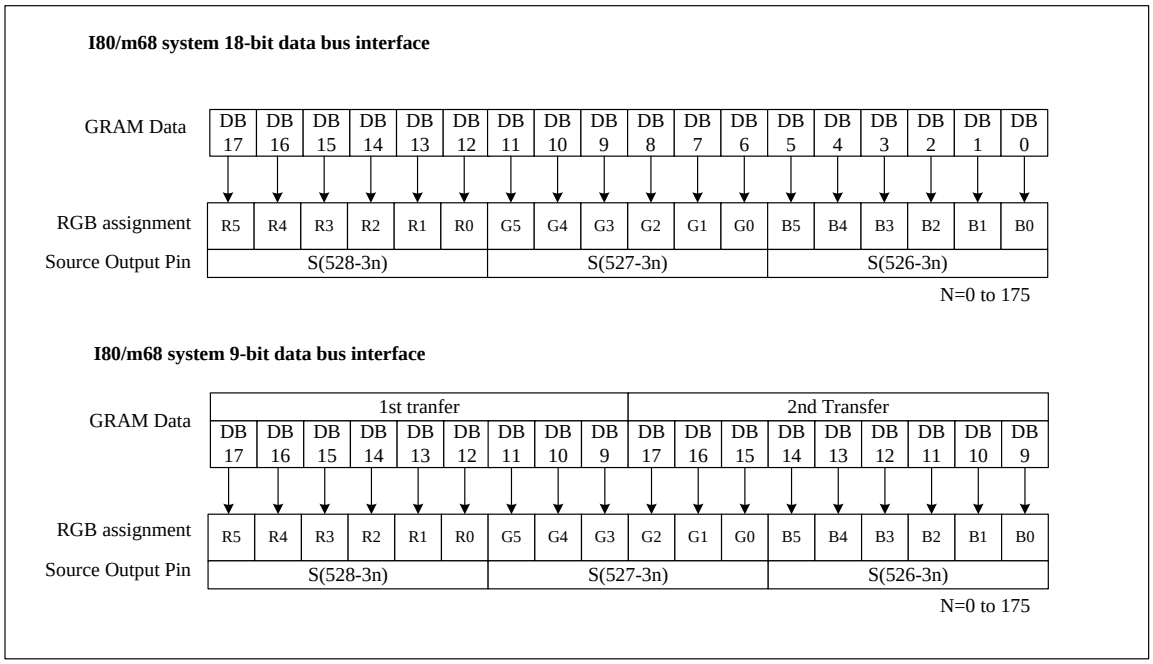


Figure33 i80-System Interface with 18-/9-bit Data Bus (SS="1", BGR="1")

8. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[7:0], end: VEA[7:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the GC9201 to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the AD[15:0] bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "AF" H

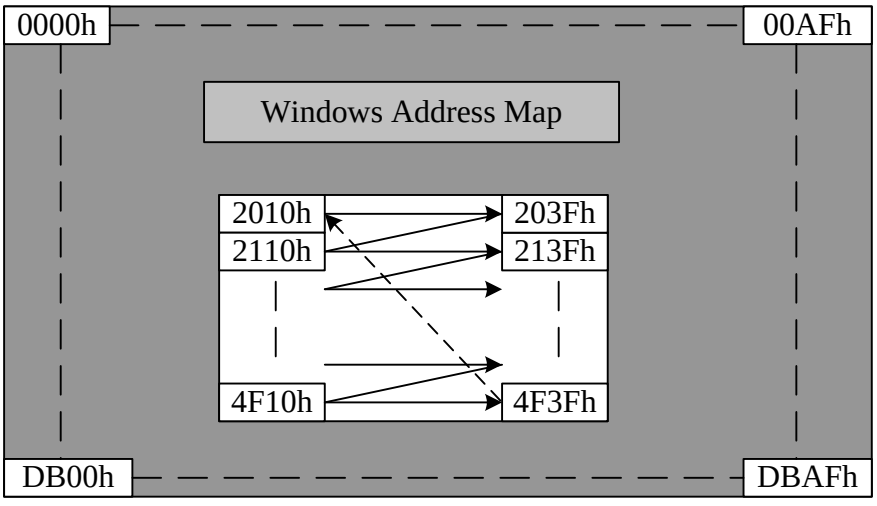
(Vertical direction) 00H ≤ VSA[7:0] ≤ VEA[7:0]≤ "DB" H

[RAM address, AD[15:0] (an address within a window address area)]]

RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]

VSA[7:0] ≤ AD[15:8] ≤ VEA[7:0]

GRAM Address Area



Windows address setting area

HSA[7:0] = 10h, HEA[7:0] = 3Fh, I/D = 1 (increment)
VSA[7:0] = 20h, VSA[7:0] = 4Fh, AM = 0 (horizontal writing)

Figure34 GRAM Access Window Map

9. Gamma Correction

GC9201 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ -correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9201 available with liquid crystal panels of various characteristics.

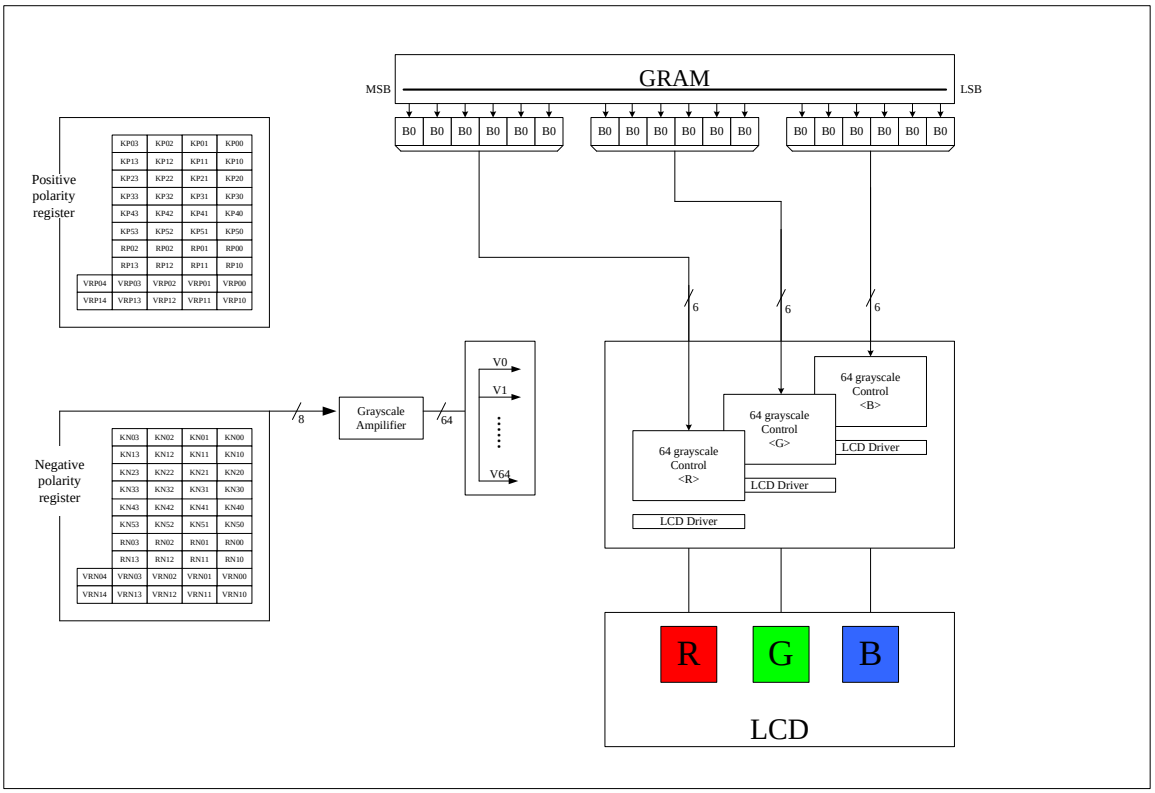


Figure35 Grayscale Mapping

Grayscale Voltage Generator Configuration

The following figure illustrates the grayscale voltage generator function of the GC9201. To generate 64 grayscale voltages (V0~V63), GC9201 first generates eight reference grayscale voltages (VgP/N0, VgP/N1, VgP/N8, VgP/N20, VgP/N43, VgP/N55, VgP/N62, VgP/N63) and the grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein. Total 64 grayscale levels are generated from the γ-correction function and used for the LCD source driver.

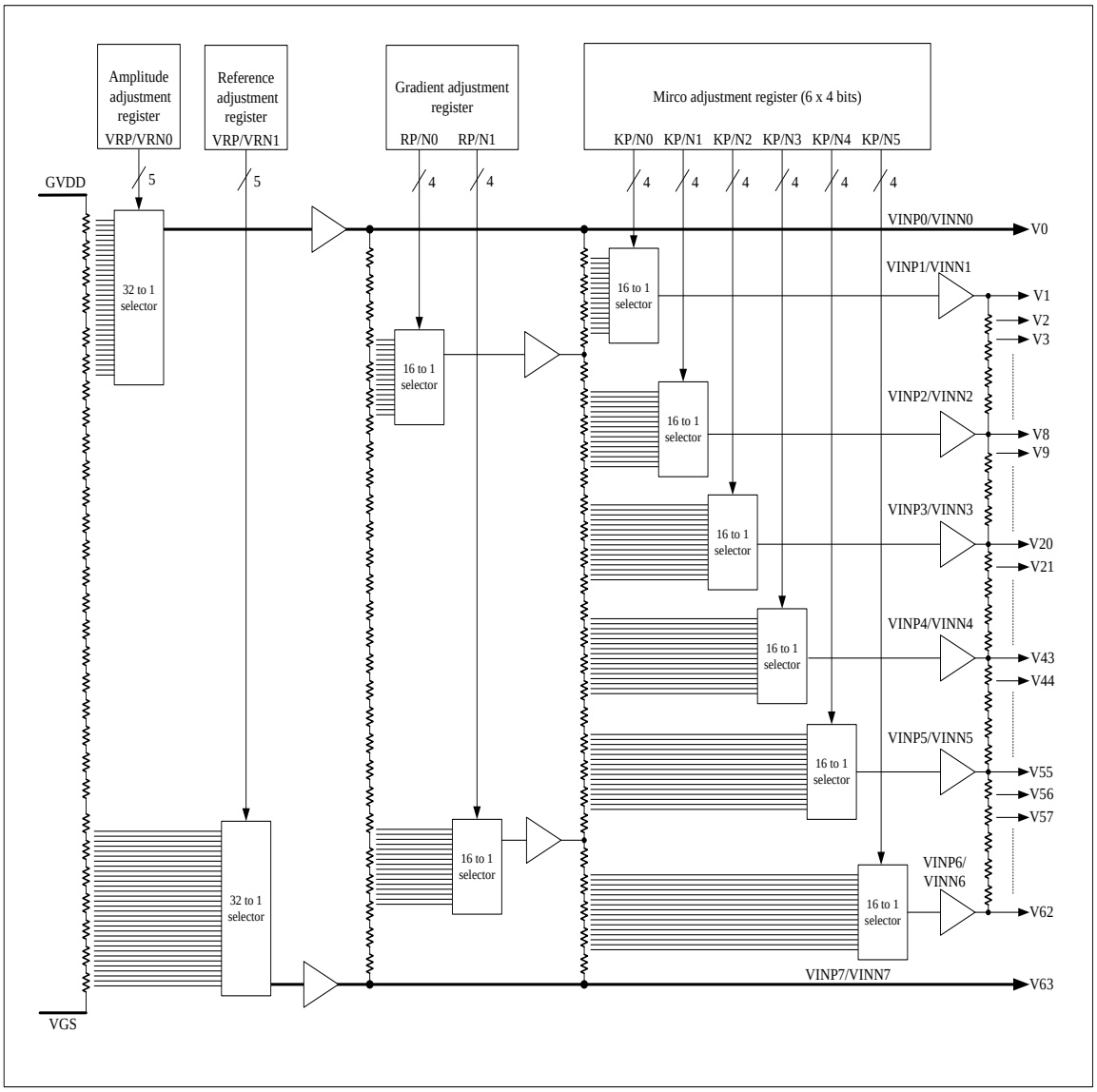


Figure36 Grayscale Voltage Generation

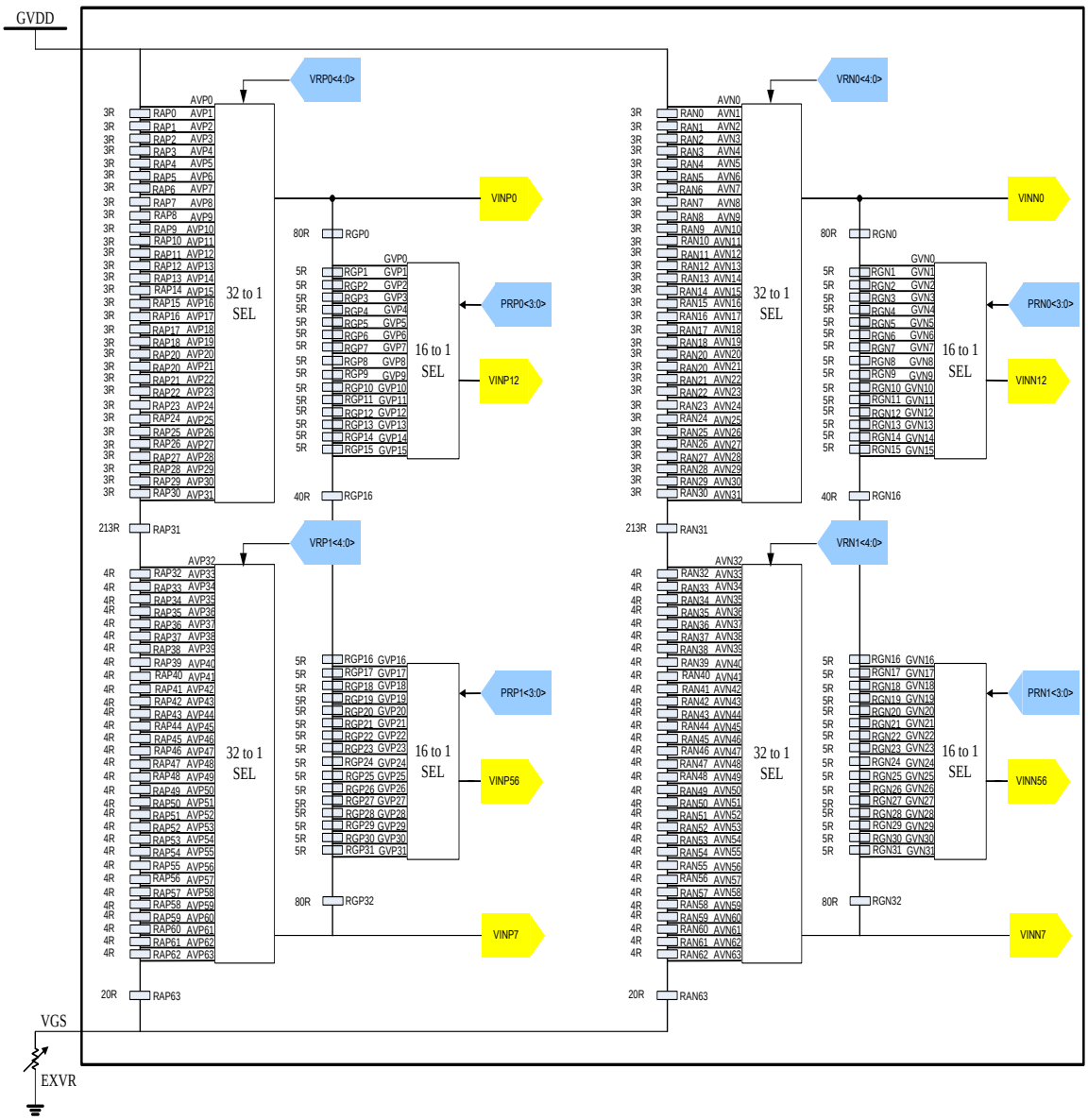


Figure37 Grayscale Voltage Adjustment 1

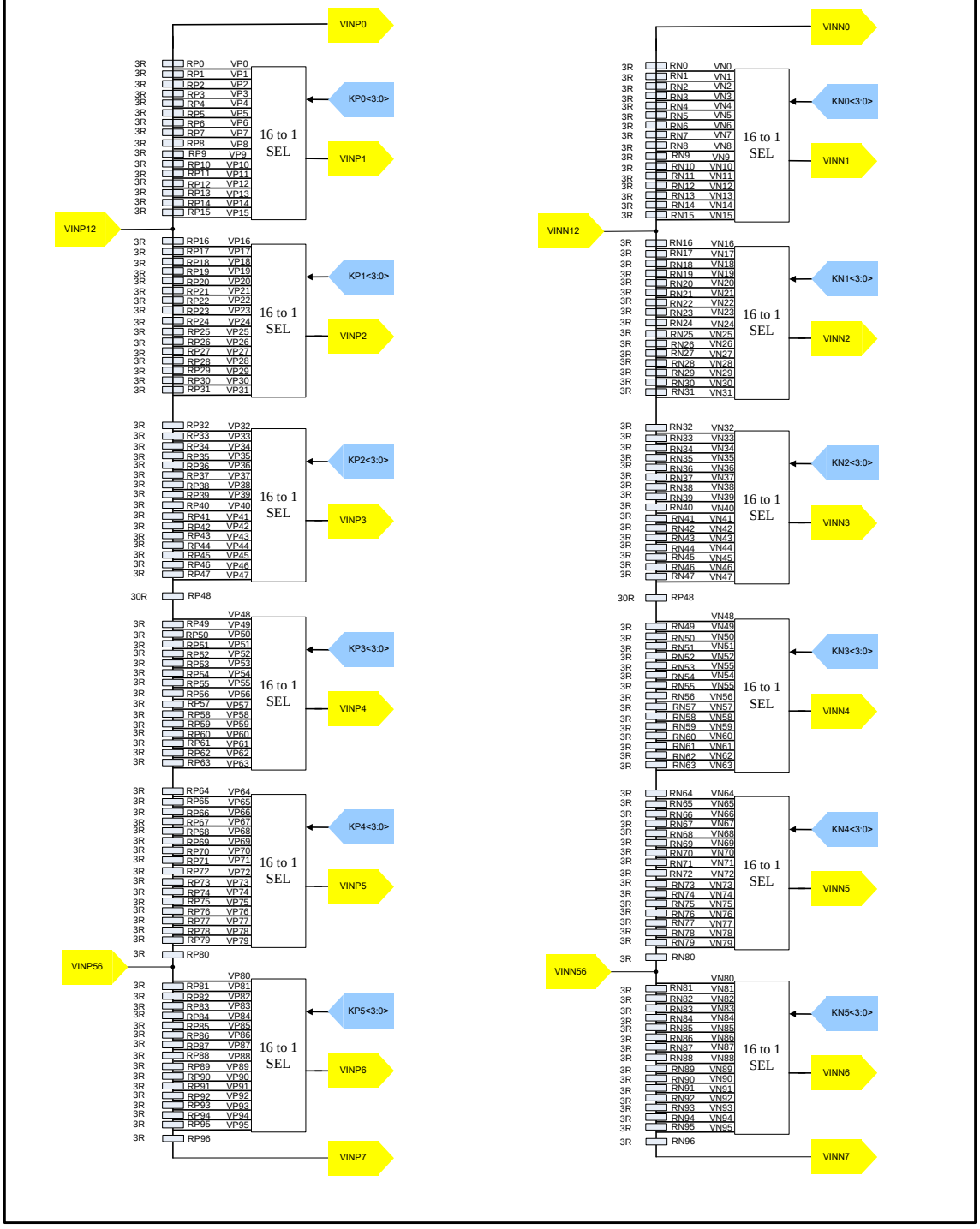


Figure38 Grayscale Voltage Adjustment 2

1. Gradient adjustment registers
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To accomplish the adjustment, it controls the VINP12/VINN12 and VINP56/VINN56 voltage level by the 16 to 1 selector towards the 16-leveled reference voltage generated from the resistor ladder between VINP0/VINN0 and VINP7/VINN7. Also, there is an independent register on the positive/negative polarities in order for corresponding to asymmetry drive.

2. Reference adjusting register
The Reference adjustment register is to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the VINP7/VINN7 voltage level by 32 to 1 selector towards the 32-leveled voltage generated from the resistor ladder between GVDD and VGS.

3. Amplitude adjustment registers
The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 32 to 1 selector towards the 32-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4. Fine adjustment registers
The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 16 levels for each register generated from the ladder resistor, in respective 16-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

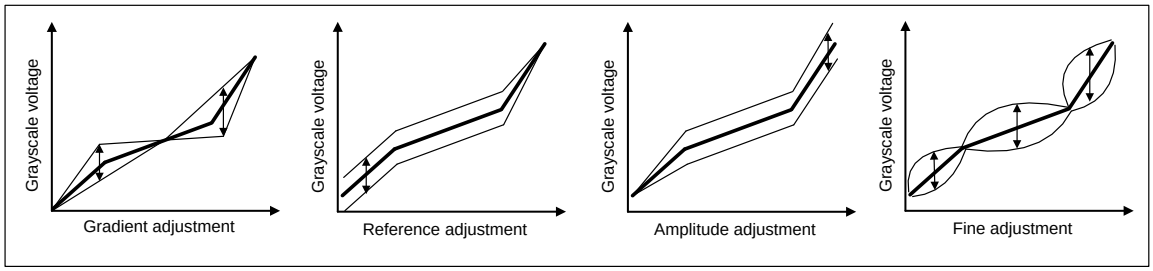


Figure39 Gamma Curve Adjustment

Gamma Adjustment Register

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[3:0]	PRN0[3:0]	The voltage of VINP12/VINN12 is elected by the 16 to 1 selector
	PRP1[3:0	PRN1[3:0]	The voltage of VINP56/VINN56 is elected by the 16 to 1 selector
Reference adjustment	VRP1[4:0]	VRN1[4:0]	The volateg of VINP7/VINN7 is elected by the 32 to 1 selector
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	The voltage of VINP0/VINN0 is elected by the 32 to 1 selector
Fine adjustment	PKP0[3:0]	PKN0[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector
	PKP1[3:0]	PKN1[3:0]	The voltage of grayscale number 20 is selected by the 16 to 1 selector
	PKP2[3:0]	PKN2[3:0]	The voltage of grayscale number 43 is selected by the 16 to 1 selector
	PKP3[3:0]	PKN3[3:0] T	The voltage of grayscale number 55 is selected by the 16 to 1 selector
	PKP4[3:0]	PKN4[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector

	PKP5[3:0]	PKN5[3:0]	The voltage of grayscale number 62 is selected by the 16 to 1 selector

RESISTOR LADDER NETWORK / SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are four ladder resistors including the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

Resistor ladder network 1 /selector

There are 4 adjustments that are for the gradient adjustment (VRHP(N)/VRLP(N)) and for the reference / amplitude adjustment(VRP(N)1 / VRP(N)0). The voltage level is set by the gradient adjustment register and the reference / amplitude adjustment registers as below.

Amplitude Adjustment

Register value VRP(N)0 [4:0]	Selected voltage VINP(N)0	Formula of VINP(N)0
00000	AVP(N)0	(450R/450R) * (GVDD-VGS) + VGS
00001	AVP(N)1	(447R/450R) * (GVDD-VGS) + VGS
00010	AVP(N)2	(444R/450R) * (GVDD-VGS) + VGS
00011	AVP(N)3	(441R/450R) * (GVDD-VGS) + VGS
00100	AVP(N)4	(438R/450R) * (GVDD-VGS) + VGS
00101	AVP(N)5	(435R/450R) * (GVDD-VGS) + VGS
00110	AVP(N)6	(432R/450R) * (GVDD-VGS) + VGS
00111	AVP(N)7	(429R/450R) * (GVDD-VGS) + VGS
01000	AVP(N)8	(426R/450R) * (GVDD-VGS) + VGS
01001	AVP(N)9	(423R/450R) * (GVDD-VGS) + VGS
01010	AVP(N)10	(420R/450R) * (GVDD-VGS) + VGS
01011	AVP(N)11	(417R/450R) * (GVDD-VGS) + VGS
01100	AVP(N)12	(414R/450R) * (GVDD-VGS) + VGS
01101	AVP(N)13	(411R/450R) * (GVDD-VGS) + VGS
01110	AVP(N)14	(408R/450R) * (GVDD-VGS) + VGS
01111	AVP(N)15	(405R/450R) * (GVDD-VGS) + VGS
10000	AVP(N)16	(402R/450R) * (GVDD-VGS) + VGS
10001	AVP(N)17	(399R/450R) * (GVDD-VGS) + VGS
10010	AVP(N)18	(396R/450R) * (GVDD-VGS) + VGS
10011	AVP(N)19	(393R/450R) * (GVDD-VGS) + VGS
10100	AVP(N)20	(390R/450R) * (GVDD-VGS) + VGS
10101	AVP(N)21	(387R/450R) * (GVDD-VGS) + VGS
10110	AVP(N)22	(384R/450R) * (GVDD-VGS) + VGS
10111	AVP(N)23	(381R/450R) * (GVDD-VGS) + VGS
11000	AVP(N)24	(378R/450R) * (GVDD-VGS) + VGS
11001	AVP(N)25	(375R/450R) * (GVDD-VGS) + VGS
11010	AVP(N)26	(372R/450R) * (GVDD-VGS) + VGS
11011	AVP(N)27	(369R/450R) * (GVDD-VGS) + VGS
11100	AVP(N)28	(366R/450R) * (GVDD-VGS) + VGS
11101	AVP(N)29	(363R/450R) * (GVDD-VGS) + VGS
11110	AVP(N)30	(360R/450R) * (GVDD-VGS) + VGS
11111	AVP(N)31	(357R/450R) * (GVDD-VGS) + VGS

Reference Adjustment

Register value VRP(N)0 [4:0]	Selected voltage VINP(N)7	Formula of VINP(N)7
00000	AVP(N)63	(20R/450R) * (GVDD-VGS) + VGS
00001	AVP(N)62	(24R/450R) * (GVDD-VGS) + VGS
00010	AVP(N)61	(28R/450R) * (GVDD-VGS) + VGS
00011	AVP(N)60	(32R/450R) * (GVDD-VGS) + VGS
00100	AVP(N)59	(36R/450R) * (GVDD-VGS) + VGS
00101	AVP(N)58	(40R/450R) * (GVDD-VGS) + VGS
00110	AVP(N)57	(44R/450R) * (GVDD-VGS) + VGS
00111	AVP(N)56	(48R/450R) * (GVDD-VGS) + VGS
01000	AVP(N)55	(52R/450R) * (GVDD-VGS) + VGS
01001	AVP(N)54	(56R/450R) * (GVDD-VGS) + VGS
01010	AVP(N)53	(60R/450R) * (GVDD-VGS) + VGS
01011	AVP(N)52	(64R/450R) * (GVDD-VGS) + VGS
01100	AVP(N)51	(68R/450R) * (GVDD-VGS) + VGS
01101	AVP(N)50	(72R/450R) * (GVDD-VGS) + VGS
01110	AVP(N)49	(76R/450R) * (GVDD-VGS) + VGS
01111	AVP(N)48	(80R/450R) * (GVDD-VGS) + VGS
10000	AVP(N)47	(84R/450R) * (GVDD-VGS) + VGS
10001	AVP(N)46	(88R/450R) * (GVDD-VGS) + VGS
10010	AVP(N)45	(92R/450R) * (GVDD-VGS) + VGS
10011	AVP(N)44	(96R/450R) * (GVDD-VGS) + VGS
10100	AVP(N)43	100R/450R) * (GVDD-VGS) + VGS
10101	AVP(N)42	104R/450R) * (GVDD-VGS) + VGS
10110	AVP(N)41	108R/450R) * (GVDD-VGS) + VGS
10111	AVP(N)40	112R/450R) * (GVDD-VGS) + VGS
11000	AVP(N)39	116R/450R) * (GVDD-VGS) + VGS
11001	AVP(N)38	120R/450R) * (GVDD-VGS) + VGS
11010	AVP(N)37	124R/450R) * (GVDD-VGS) + VGS
11011	AVP(N)36	128R/450R) * (GVDD-VGS) + VGS
11100	AVP(N)35	132R/450R) * (GVDD-VGS) + VGS
11101	AVP(N)34	136R/450R) * (GVDD-VGS) + VGS
11110	AVP(N)33	140R/450R) * (GVDD-VGS) + VGS
11111	AVP(N)32	144R/450R) * (GVDD-VGS) + VGS

Gradient Adjustment (1)

Register value PRP(N)0 [3:0]	Selected voltage VINP(N)12	Formula of VINP(N)12
0000	GVP(N)0	(270R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0001	GVP(N)1	(265R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0010	GVP(N)2	(260R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0011	GVP(N)3	(255R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0100	GVP(N)4	(250R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0101	GVP(N)5	(245R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0110	GVP(N)6	(240R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0111	GVP(N)7	(235R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1000	GVP(N)8	(230R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1001	GVP(N)9	(225R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1010	GVP(N)10	(220R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1011	GVP(N)11	(215R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1100	GVP(N)12	(210R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1101	GVP(N)13	(205R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7

1110	GVP(N)14	(200R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1111	GVP(N)15	(195R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7

Reference Adjustment (2)

Register value PRP(N)1 [3:0]	Selected voltage VINP(N)56	Formula of VINP(N)12
0000	GVP(N)0	80R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0001	GVP(N)1	85R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0010	GVP(N)2	90R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0011	GVP(N)3	95R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0100	GVP(N)4	100R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0101	GVP(N)5	105R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0110	GVP(N)6	110R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0111	GVP(N)7	115R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1000	GVP(N)8	120R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1001	GVP(N)9	125R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1010	GVP(N)10	130R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1011	GVP(N)11	135R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1100	GVP(N)12	140R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1101	GVP(N)13	145R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1110	GVP(N)14	150R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1111	GVP(N)15	155R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7

Resistor ladder network 2/selector

In the 16-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the six types of the reference voltage, VIN1 to VIN6. Following figure explains the relationship between the micro-adjustment register and the selected voltage.

Relationship between Fine-adjustment Register and Selected Voltage

Register Value PKP(N) [3:0]	Select Voltage					
	VINP(N)1	**VINP(N)2**	**VINP(N)3**	**VINP(N)4**	**VINP(N)5**	**VINP(N)6**
0000	KVP(N)0 K	KVP(N)16	KVP(N)32	KVP(N)63	KVP(N)79	KVP(N)95
0001	KVP(N)1 K	KVP(N)17	KVP(N)33	KVP(N)62	KVP(N)78	KVP(N)94
0010	KVP(N)2 K	KVP(N)18	KVP(N)34	KVP(N)61	KVP(N)77	KVP(N)93
0011	KVP(N)3 K	KVP(N)19	KVP(N)35	KVP(N)60	KVP(N)76	KVP(N)92
0100	KVP(N)4 K	KVP(N)20	KVP(N)36	KVP(N)59	KVP(N)75	KVP(N)91
0101	KVP(N)5 K	KVP(N)21	KVP(N)37	KVP(N)58	KVP(N)74	KVP(N)90
0110	KVP(N)6 K	KVP(N)22	KVP(N)38	KVP(N)57	KVP(N)73	KVP(N)89
0111	KVP(N)7 K	KVP(N)23	KVP(N)39	KVP(N)56	KVP(N)72	KVP(N)88
1000	KVP(N)8 K	KVP(N)24	KVP(N)40	KVP(N)55	KVP(N)71	KVP(N)87
1001	KVP(N)9 K	KVP(N)25	KVP(N)41	KVP(N)54	KVP(N)70	KVP(N)86
1010	KVP(N)10	KVP(N)26	KVP(N)42	KVP(N)53	KVP(N)69	KVP(N)85
1011	KVP(N)11	KVP(N)27	KVP(N)43	KVP(N)52	KVP(N)68	KVP(N)84
1100	KVP(N)12	KVP(N)28	KVP(N)44	KVP(N)51	KVP(N)67	KVP(N)83
1101	KVP(N)13	KVP(N)29	KVP(N)45	KVP(N)50	KVP(N)66	KVP(N)82
1110	KVP(N)14	KVP(N)30	KVP(N)46	KVP(N)49	KVP(N)65	KVP(N)81
1111	KVP(N)15	KVP(N)31	KVP(N)47	KVP(N)48	KVP(N)64	KVP(N)80

[NOTE] The grayscale levels are determined by the following formulas listed in the next pages.

Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pins	Formula	Fine-adjusting register value	Reference voltage
KVP0	(45R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0000”	VINP1
KVP1	(42R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0001”	
KVP2	(39R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0010”	
KVP3	(36R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0011”	
KVP4	(33R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0100”	
KVP5	(30R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0101”	
KVP6	(27R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0110”	
KVP7	(24R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0111”	
KVP8	(21R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1000”	
KVP9	(18R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1001”	
KVP10	(15R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1010”	
KVP11	(12R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1011”	
KVP12	(9R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1100”	
KVP13	(6R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1101”	
KVP14	(3R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1110”	
KVP15	VINP12	PKP0[3:0] = “1111”	
KVP16	(219R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0000”	VINP2
KVP17	(216R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0001”	
KVP18	(213R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0010”	
KVP19	(210R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0011”	
KVP20	(207R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0100”	
KVP21	(204R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0101”	
KVP22	(201R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0110”	
KVP23	(198R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0111”	
KVP24	(195R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1000”	
KVP25	(192R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1001”	
KVP26	(189R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1010”	
KVP27	(186R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1011”	
KVP28	(183R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1100”	
KVP29	(180R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1101”	
KVP30	(177R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1110”	
KVP31	(174R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1111”	
KVP32	(171R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0000”	VINP3
KVP33	(168R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0001”	
KVP34	(165R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0010”	
KVP35	(162R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0011”	
KVP36	(159R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0100”	
KVP37	(156R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0101”	
KVP38	(153R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0110”	
KVP39	(150R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0111”	
KVP40	(147R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1000”	
KVP41	(144R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1001”	
KVP42	(141R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1010”	
KVP43	(138R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1011”	

KVP44	(135R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1100”	
KVP45	(132R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1101”	
KVP46	(129R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1110”	
KVP47	(126R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1111”	
KVP48	(96R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1111"	VINP4
KVP49	(93R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1110"	
KVP50	(90R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1101"	
KVP51	(87R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1100"	
KVP52	(84R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1011"	
KVP53	(81R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1010"	
KVP54	(78R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1001"	
KVP55	(75R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1000"	
KVP56	(72R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0111"	
KVP57	(69R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0110"	
KVP58	(66R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0101"	
KVP59	(63R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0100"	
KVP60	(60R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0011"	
KVP61	(57R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0010"	
KVP62	(54R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0001"	
KVP63	(51R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0000"	
KVP64	(48R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1111"	VINP5
KVP65	(45R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1110"	
KVP66	(42R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1101"	
KVP67	(39R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1100"	
KVP68	(36R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1011"	
KVP69	(33R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1010"	
KVP70	(30R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1001"	
KVP71	(27R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1000"	
KVP72	(24R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0111"	
KVP73	(21R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0110"	
KVP74	(18R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0101"	
KVP75	(15R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0100"	
KVP76	(12R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0011"	
KVP77	(9R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0010"	
KVP78	(6R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0001"	
KVP79	(3R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0000"	
KVP80	VINP56	PKP5[3:0]="1111"	VINP6
KVP81	(45R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1110"	
KVP82	(42R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1101"	
KVP83	(39R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1100"	
KVP84	(36R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1011"	
KVP85	(33R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1010"	
KVP86	(30R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1001"	
KVP87	(27R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1000"	
KVP88	(24R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0111"	
KVP89	(21R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0110"	
KVP90	(18R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0101"	
KVP91	(15R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0100"	
KVP92	(12R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0011"	
KVP93	(9R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0010"	
KVP94	(6R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0001"	
KVP95	(3R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0000"	

Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(45/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(54/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 1

Pins	Formula	Fine-adjusting register value	Reference voltage
KVN0	(45R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0000”	VINN1
KVN1	(42R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0001”	
KVN2	(39R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0010”	
KVN3	(36R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0011”	
KVN4	(33R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0100”	
KVN5	(30R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0101”	
KVN6	(27R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0110”	
KVN7	(24R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0111”	
KVN8	(21R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1000”	
KVN9	(18R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1001”	
KVN10	(15R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1010”	
KVN11	(12R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1011”	
KVN12	(9R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1100”	

KVN13	(6R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1101”	
KVN14	(3R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1110”	
KVN15	VINN12	PKN0[3:0] = “1111”	
KVN16	(219R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0000”	VINN2
KVN17	(216R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0001”	
KVN18	(213R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0010”	
KVN19	(210R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0011”	
KVN20	(207R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0100”	
KVN21	(204R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0101”	
KVN22	(201R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0110”	
KVN23	(198R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0111”	
KVN24	(195R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1000”	
KVN25	(192R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1001”	
KVN26	(189R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1010”	
KVN27	(186R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1011”	
KVN28	(183R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1100”	
KVN29	(180R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1101”	
KVN30	(177R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1110”	
KVN31	(174R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1111”	
KVN32	(171R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0000”	VINN3
KVN33	(168R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0001”	
KVN34	(165R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0010”	
KVN35	(162R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0011”	
KVN36	(159R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0100”	
KVN37	(156R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0101”	
KVN38	(153R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0110”	
KVN39	(150R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0111”	
KVN40	(147R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1000”	
KVN41	(144R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1001”	
KVN42	(141R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1010”	
KVN43	(138R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1011”	
KVN44	(135R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1100”	
KVN45	(132R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1101”	
KVN46	(129R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1110”	
KVN47	(126R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1111”	
KVN48	(96R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1111"	VINN4
KVN49	(93R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1110"	
KVN50	(90R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1101"	
KVN51	(87R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1100"	
KVN52	(84R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1011"	
KVN53	(81R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1010"	
KVN54	(78R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1001"	
KVN55	(75R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="1000"	
KVN56	(72R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0111"	
KVN57	(69R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0110"	
KVN58	(66R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0101"	
KVN59	(63R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0100"	
KVN60	(60R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0011"	
KVN61	(57R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0010"	

KVN62	(54R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0001"	
KVN63	(51R/222R)*(VINN12-VINN56)+VINN56	PKN3[3:0]="0000"	
KVN64	(48R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1111"	VINN5
KVN65	(45R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1110"	
KVN66	(42R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1101"	
KVN67	(39R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1100"	
KVN68	(36R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1011"	
KVN69	(33R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1010"	
KVN70	(30R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1001"	
KVN71	(27R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="1000"	
KVN72	(24R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0111"	
KVN73	(21R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0110"	
KVN74	(18R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0101"	
KVN75	(15R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0100"	
KVN76	(12R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0011"	
KVN77	(9R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0010"	
KVN78	(6R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0001"	
KVN79	(3R/222R)*(VINN12-VINN56)+VINN56	PKN4[3:0]="0000"	
KVN80	VINN56	PKN5[3:0]="1111"	VINN6
KVN81	(45R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1110"	
KVN82	(42R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1101"	
KVN83	(39R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1100"	
KVN84	(36R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1011"	
KVN85	(33R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1010"	
KVN86	(30R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1001"	
KVN87	(27R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="1000"	
KVN88	(24R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0111"	
KVN89	(21R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0110"	
KVN90	(18R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0101"	
KVN91	(15R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0100"	
KVN92	(12R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0011"	
KVN93	(9R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0010"	
KVN94	(6R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0001"	
KVP95	(3R/48R)*(VINN56-VINN7)+VINN7	PKN5[3:0]="0000"	

Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)

V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(45/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(54/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7

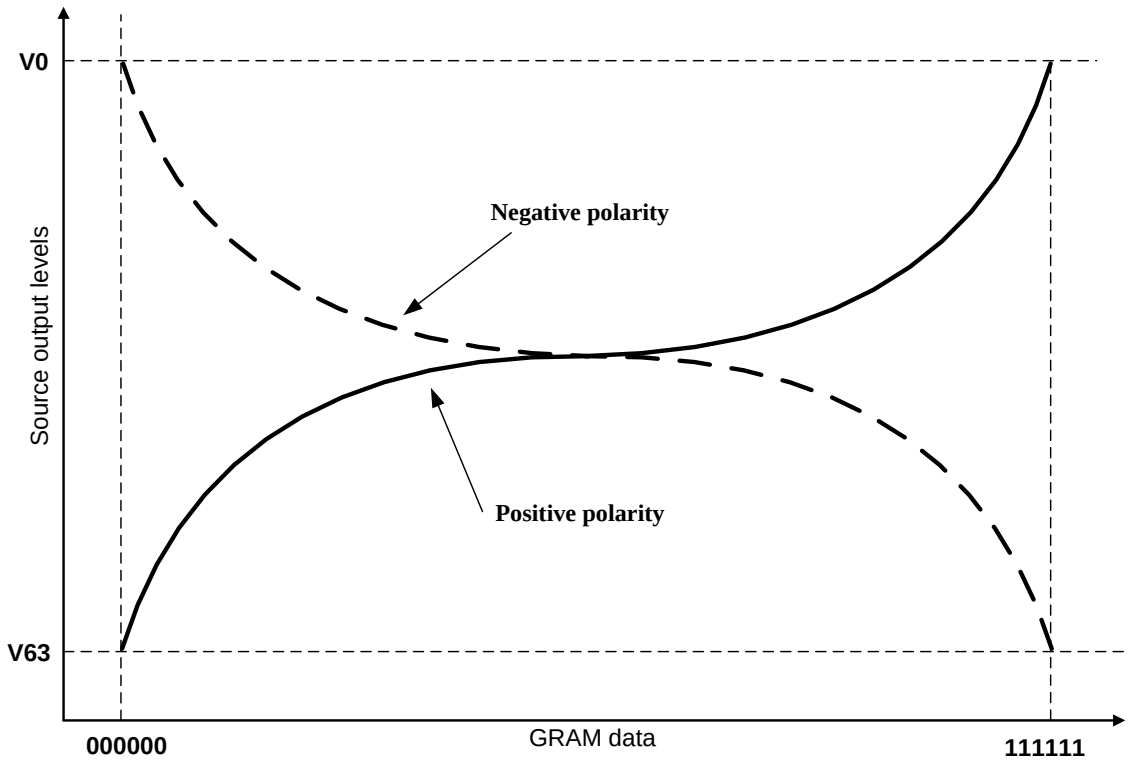


Figure40 Relationship between GRAM Data and Output Level

10. Application

10.1. Configuration of Power Supply Circuit

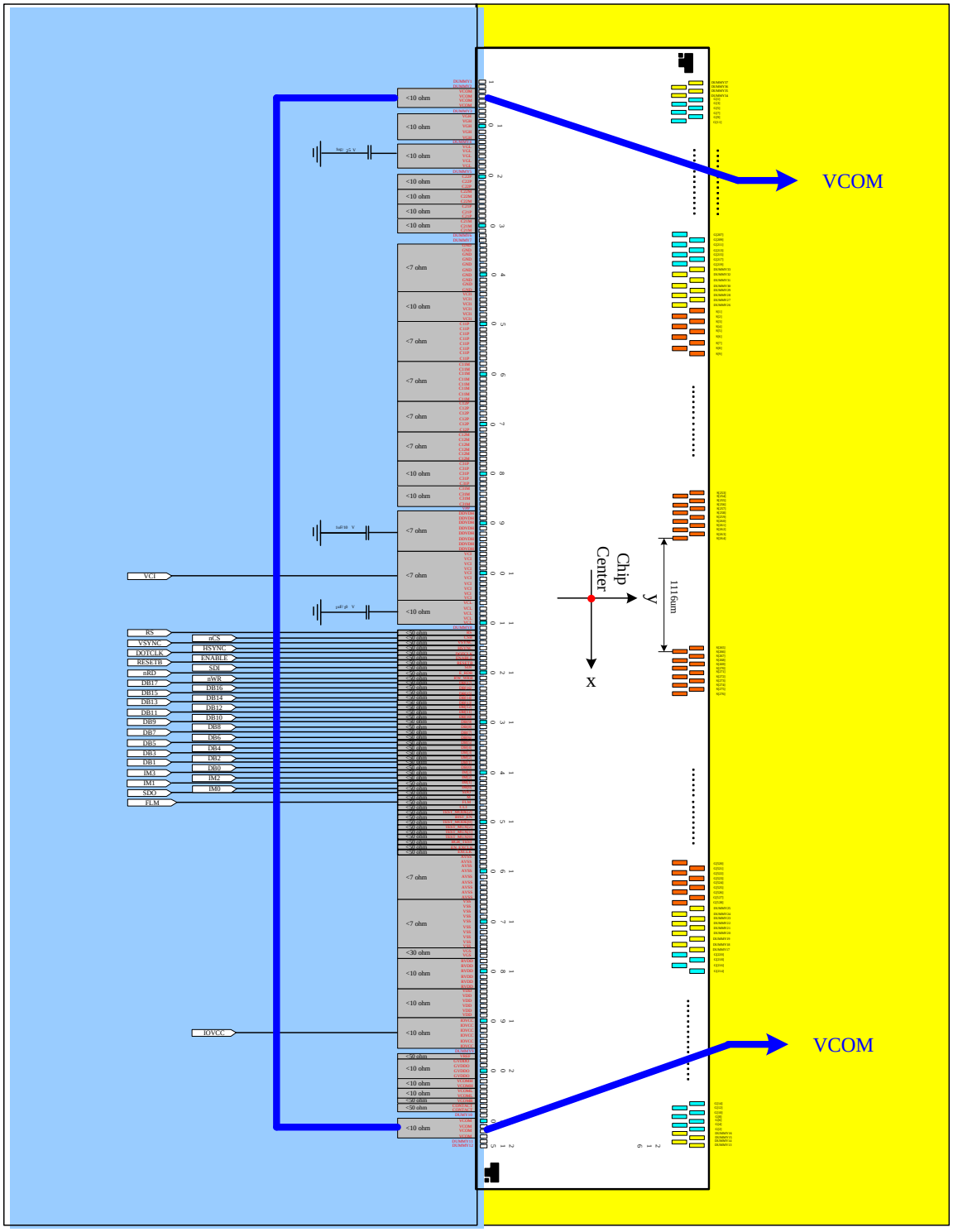


Figure41 Power Supply Circuit Block

Items	Recommended Specification	Pin connection
Capacity 1uF (B characteristics)	6.3V	VCL
	10V	DDVDH

10.2. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the GC9201 are as follows

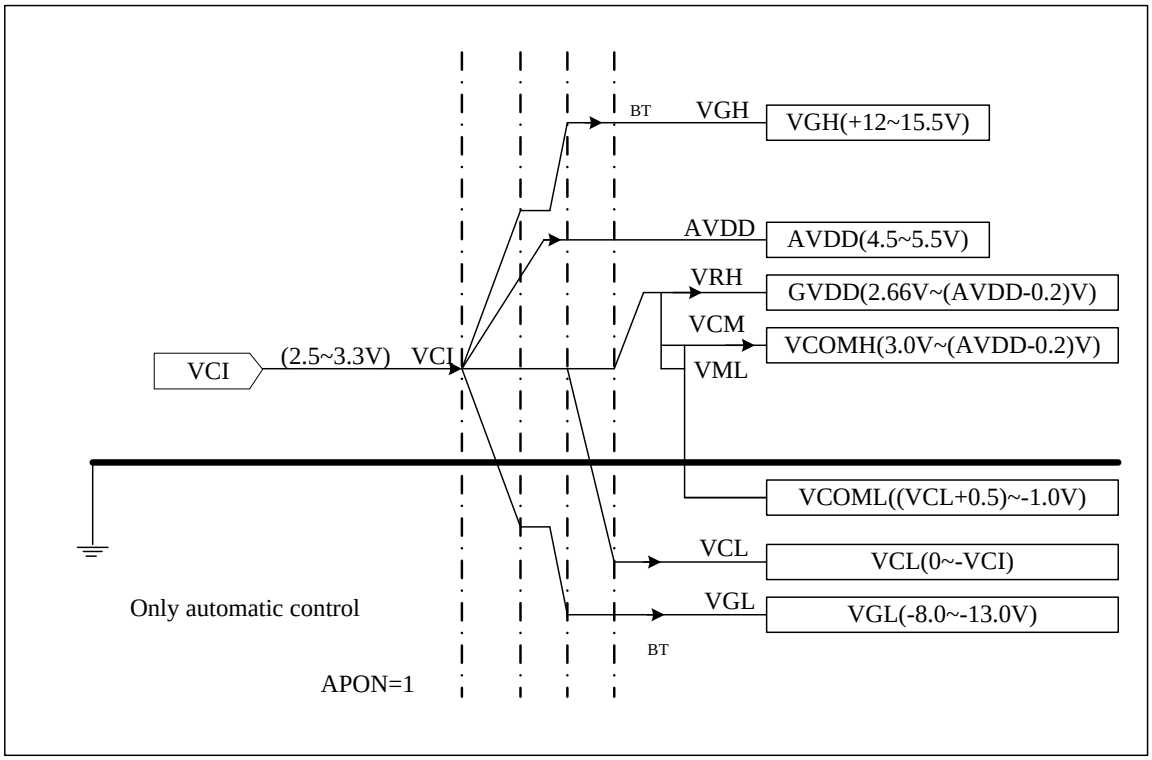


Figure42 Voltage Configuration Diagram

Note: The AVDD, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (AVDD – GVDD) > 0.2V, (VCOML – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use

10.3. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

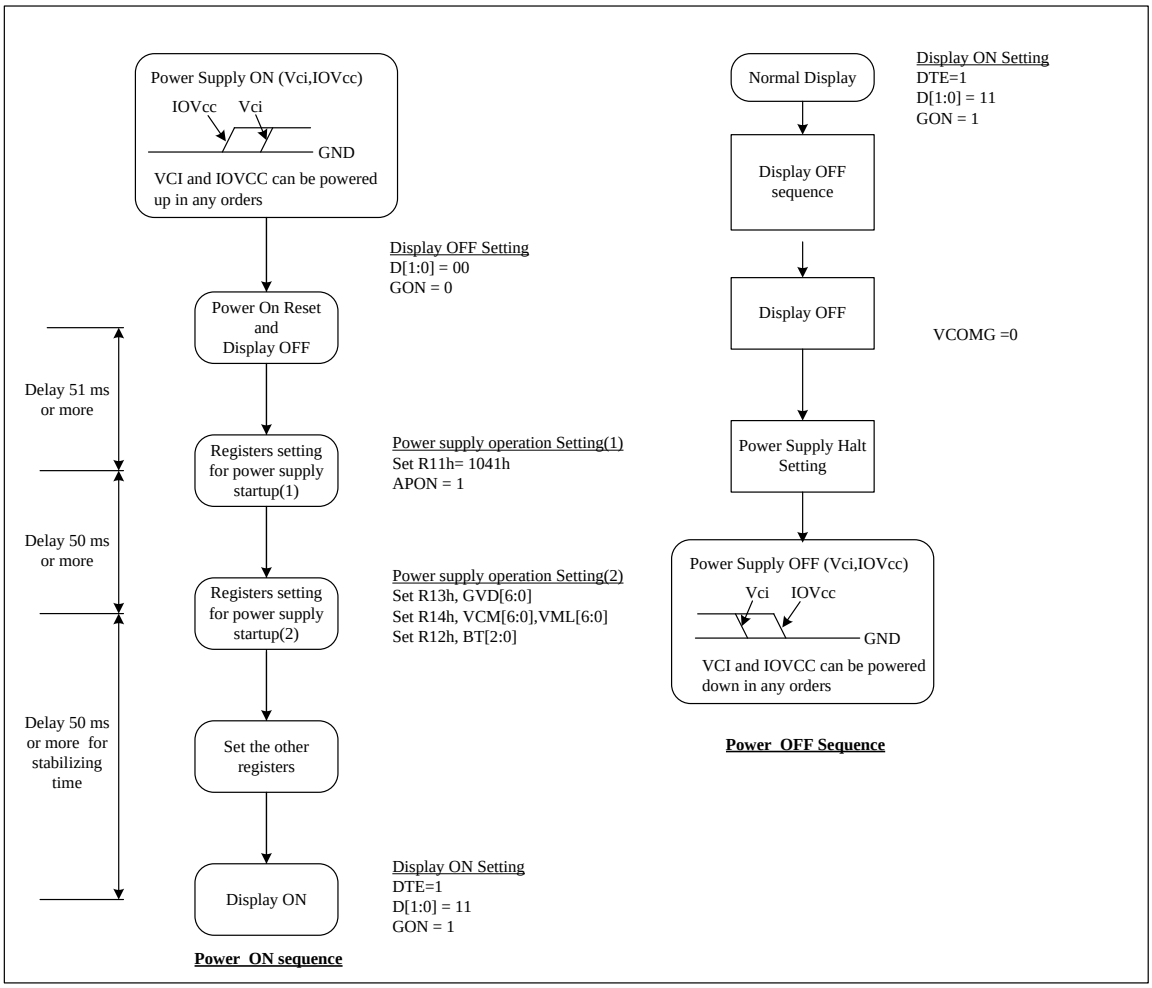


Figure43 Power On/Off Sequence

10.4. STB Mode

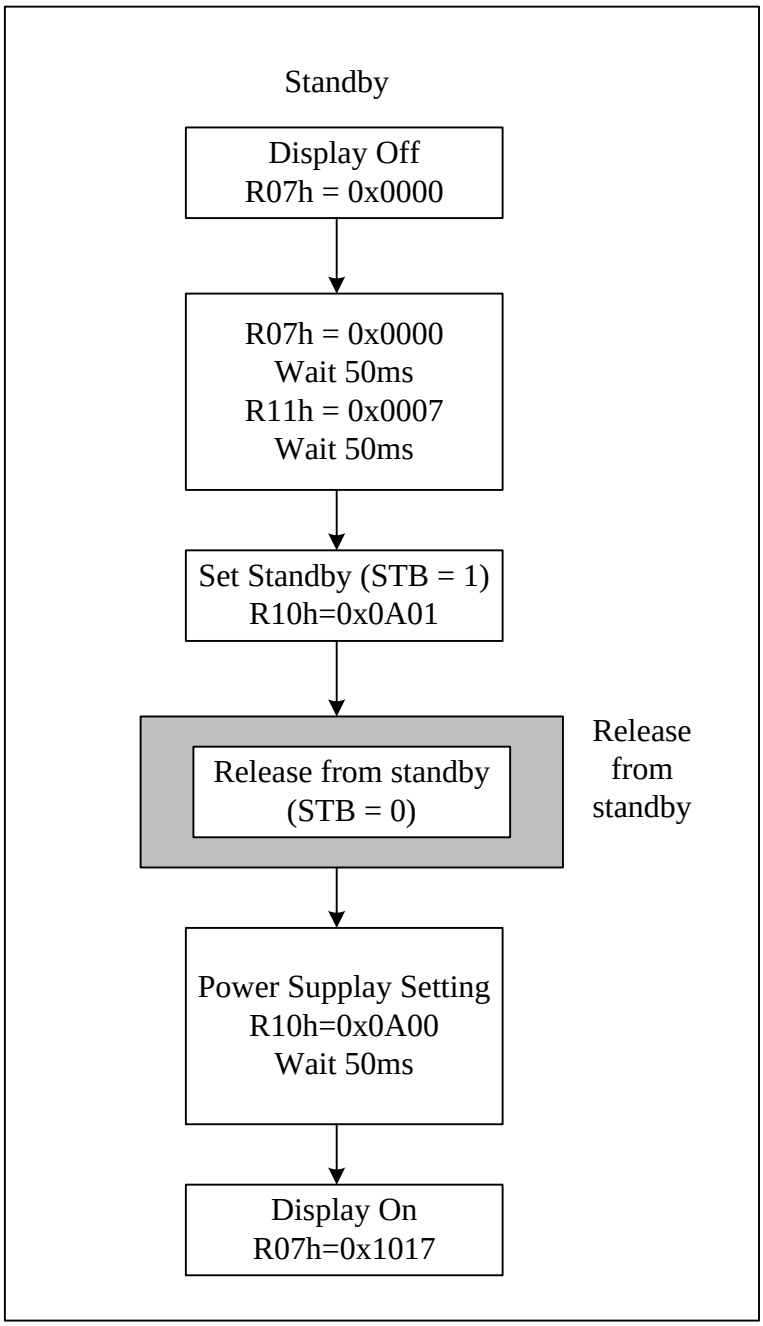


Figure44 STB Mode Register Setting Sequence

11. Electrical Characteristics

11.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9201 is used out of the absolute maximum ratings, the GC9201 may be permanently damaged. To use the GC9201 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the GC9201 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	IOVCC	V	-0.3 ~ +4.6	1, 2
Power supply voltage (1)	VCI – GND	V	-0.3 ~ +4.6	1, 4
Power supply voltage (1)	AVDD – GND	V	-0.3 ~ +6.0	1, 4
Power supply voltage (1)	GND – VCL	V	-0.3 ~ +4.6	1
Power supply voltage (1)	AVDD – VCL	V	-0.3 ~ +9.0	1, 5
Power supply voltage (1)	VGH – GND	V	-0.3 ~ +18.5	1, 5
Power supply voltage (1)	GND – VGL	V	-0.3 ~ +18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCI + 0.3	1
Operating temperature	Topr	℃	-40 ~ +85	8, 9
Storage temperature	Tstg	℃	-55 ~ +110	8, 9

Note:
1, VCI,GND must be maintained
2. (High) VCI ≥ GND (Low), (High) IOVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) AVDD ≥ ASSD (Low).
5. Make sure (High) AVDD ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85 ℃.
9. This temperature specifications apply to the TCP package

11.2. DC Characteristics

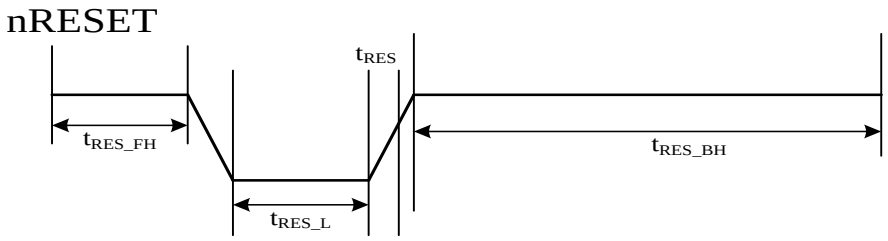
(VCI = 2.50 ~ 3.30V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 ℃)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Note
Input high voltage	V_{IH}	V	IOVCC= 1.65 ~ 3.3V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V_{IL}	V	IOVCC= 1.65 ~ 3.3V	0	-	0.2*IOVCC	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	IOVCC=1.65~3.3V VCI= 2.5 ~ 3.3V IOL = 0.1mA	-	-	0.2*IOVCC	-
I/O leakage current	I_{LI}	µA	Vin = 0 ~ IOVCC	-0.1		-0.1	-
Current consumption during standby mode (VCI – GND)	I_{ST}	µA	VCI=2.8V , Ta=25℃	-	5	30	-
LCD Driving Voltage (AVDD-GND)	AVDD	V	-	4.5	-	6	-
Output voltage deviation		mV	-		20	-	-
Dispersion of the Average Output Voltage	V	mV	-	-20	-	-20	-

11.3. Reset Timing Characteristics

Reset Timing Characteristics (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min	Typ	Max
Reset front high-level width	t_{RES_FH}	ms	1		
Reset low-level width	t_{RES_L}	us	10		
Reset back high-level width	t_{RES_BH}	Ms	50		
Reset rise time	t_{RES}	us			10



11.4. AC Characteristics

11.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Item		symbol	unit	min	max	Test Condition
Bus cycle time	**Write**	t_{CYCW}	ns	66	-	-
	Read	t_{CYCR}	ns	300	-	-
Write low-level pulse width		PW_{LW}	ns	35	500	-
Write high-level pulse width		PW_{HW}	ns	35	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	
Write/Read rise/fall time		t_{WRr}/t_{WRf}	ns	-	15	
Setup time	**Write(RS to nCS, E/nWR)**	t_{AS}	ns	10	-	
	Read(RS to nCS,RW/nRD)		ns	5	-	
Address hold time		t_{AH}	ns	5	-	
Write data set up time		t_{DSW}	ns	10	-	
Write data hold time		t_H	ns	15	-	
Read data delay time		t_{DDR}	ns	-	100	
Read data hold time		t_{DHR}	ns	5	-	

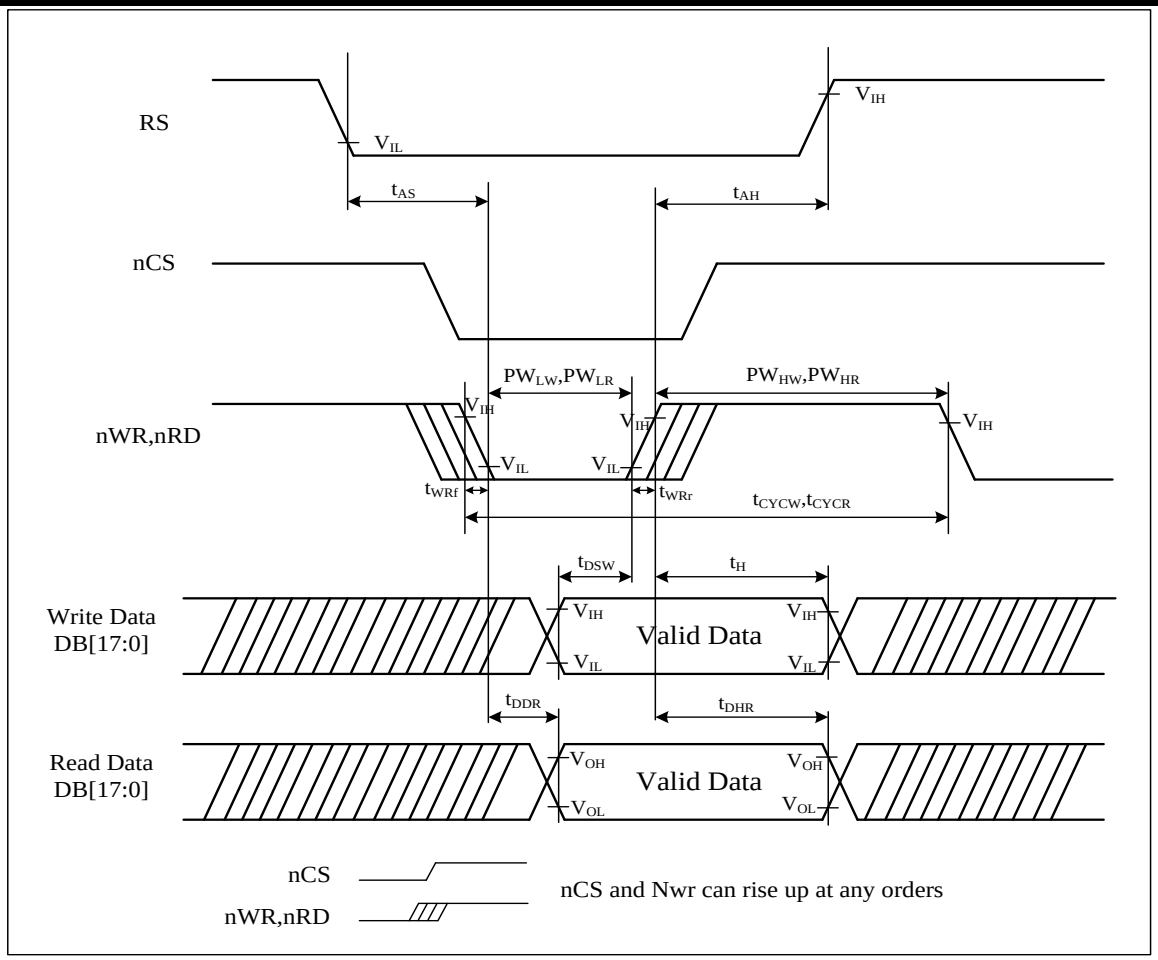


Figure45 i80-System Bus Timing

11.4.2. M68-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Item		symbol	unit	min	max	Test Condition
Bus cycle time	**Write**	t_{CYCEW}	ns	66	-	-
	Read	t_{CYCER}	ns	300	-	-
Write low-level pulse width		PW_{ELW}	ns	35	500	-
Write high-level pulse width		PW_{EHW}	ns	35	-	-
Read low-level pulse width		PW_{ELR}	ns	150	-	-
Read high-level pulse width		PW_{EHR}	ns	150	-	
Write/Read rise/fall time		t_{WRr}/t_{WRf}	ns	-	15	
Setup time	**Write(RS to nCS, E/nWR)**	t_{ASE}	ns	10	-	
	Read(RS to nCS,RW/nRD)		ns	10	-	
Address hold time		t_{AHE}	ns	5	-	
Write data set up time		t_{DSWE}	ns	10	-	
Write data hold time		t_{HE}	ns	15	-	
Read data delay time		t_{DDRE}	ns	-	100	
Read data hold time		t_{DHRE}	ns	5	-	

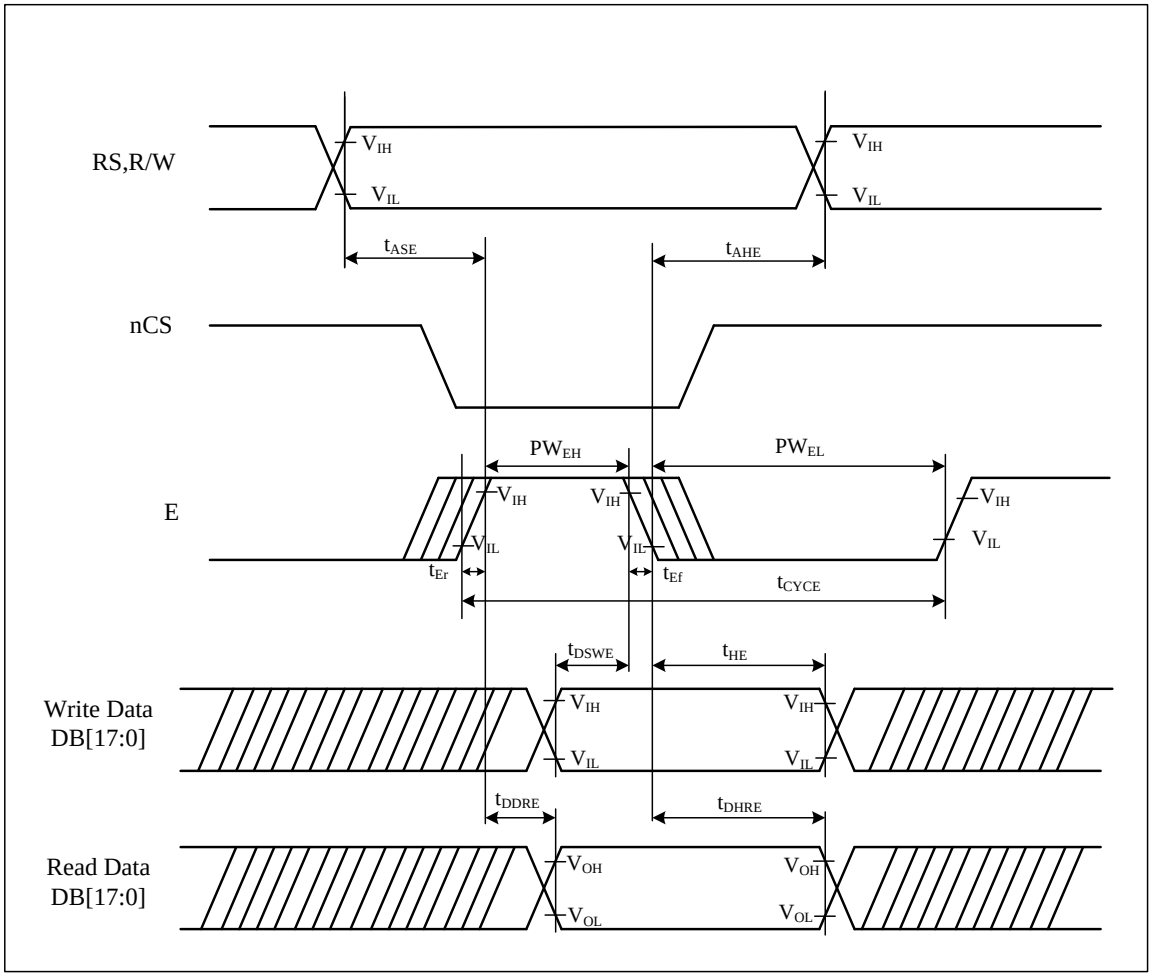


Figure47 M68-System Interface Timing

11.4.3. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.65~3.3V and VCI=2.5~3.3V)

Item		symbol	unit	min	max	Test Condition
Serial clock cycle time	**Write(received)**	t_{SCYC}	ns	80	-	IOVCC=1.65~2.8V
	Write(received)	t_{SCYC}	ns	25		IOVCC=2.8~3.3V
	Read(transmitted)	t_{SCYC}	ns	200	-	-
Serial clock high-level pulse width	**Write(received)**	t_{SCH}	ns	40		IOVCC=1.65~3.3V
	Read(transmitted)	t_{SCH}	ns	90		
Serial clock low-level pulse width	**Write(received)**	t_{SCL}	ns	40		IOVCC=1.65~3.3V
	Read(transmitted)	t_{SCL}	ns	90		
Write/Read rise/fall time		t_{SCr}, t_{SCf}	ns	-	5	
Chip select set up time		t_{CSU}	ns	10	-	
Chip select hold time		t_{CH}	ns	10	-	
Serial input data set up time		t_{SISU}	ns	5	-	
Serial input data hold time		t_{SIH}	ns	5	-	
Serial output data set up time		t_{SOD}	ns	-	200	
Serial output data hold time		t_{SOH}	ns	10	-	

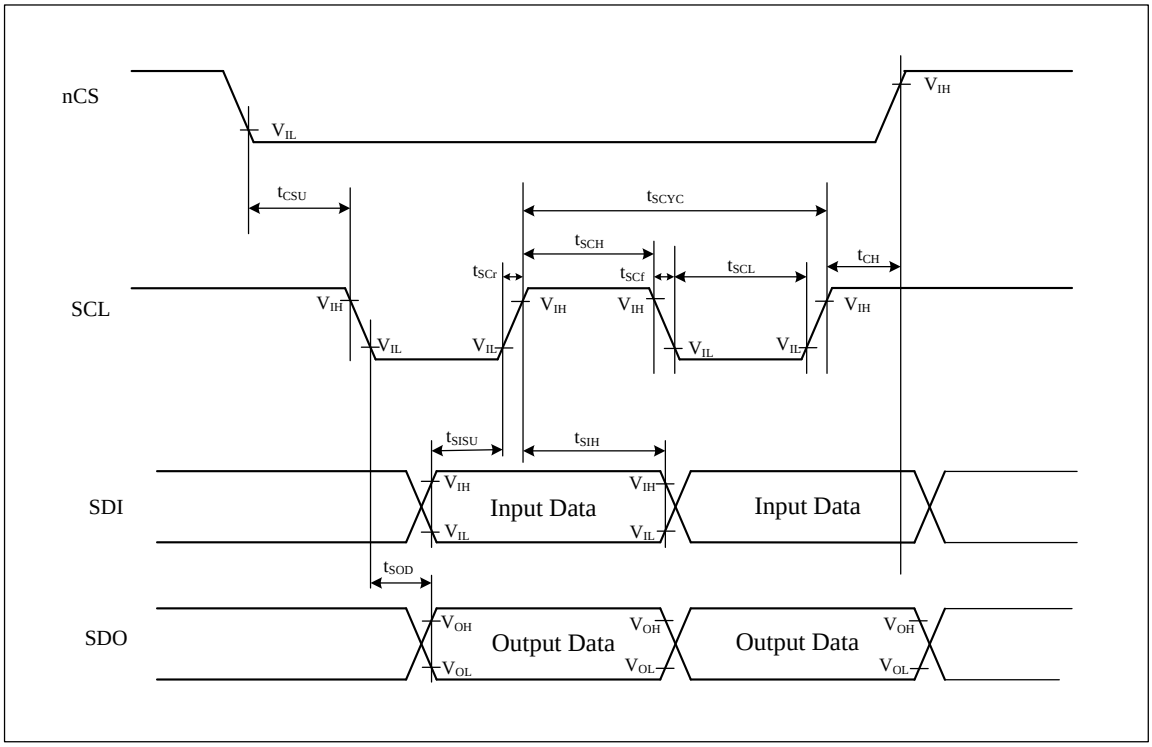


Figure48 SPI System Bus Timing

11.4.4. RGB Interface Timing Characteristics

8/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Item	symbol	unit	min	Type	max	Test Condition
VSYNC/HSYNC setup time	t_{SYNC}	ns	35	-	-	-
ENABLE setup time	t_{ENS}	ns	35	-	-	-
ENABLE hold time	t_{ENH}	ns	150	-	-	-
PD Data setup time	t_{PDS}	ns	150	-	-	-
PD Data hold time	t_{PDH}	ns	-	-	-	-
DOTCLK high-level pulse width	PWDH	ns	5	-	-	-
DOTCLK low-level pulse width	PWDL	ns	10	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	15	-	-	Frame rate under 100Hz
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr} , t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Item	symbol	unit	min	Type	max	Test Condition
VSYNC/HSYNC setup time	t_{SYNC}	ns	35	-	-	-
ENABLE setup time	t_{ENS}	ns	35	-	-	-
ENABLE hold time	t_{ENH}	ns	150	-	-	-
PD Data setup time	t_{PDS}	ns	150	-	-	-
PD Data hold time	t_{PDH}	ns	-	-	-	-
DOTCLK high-level pulse width	PWDH	ns	5	-	-	-
DOTCLK low-level pulse width	PWDL	ns	10	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	15	-	-	Frame rate under 100Hz
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rgbr} , t_{rgbf}	ns	-	-	25	-

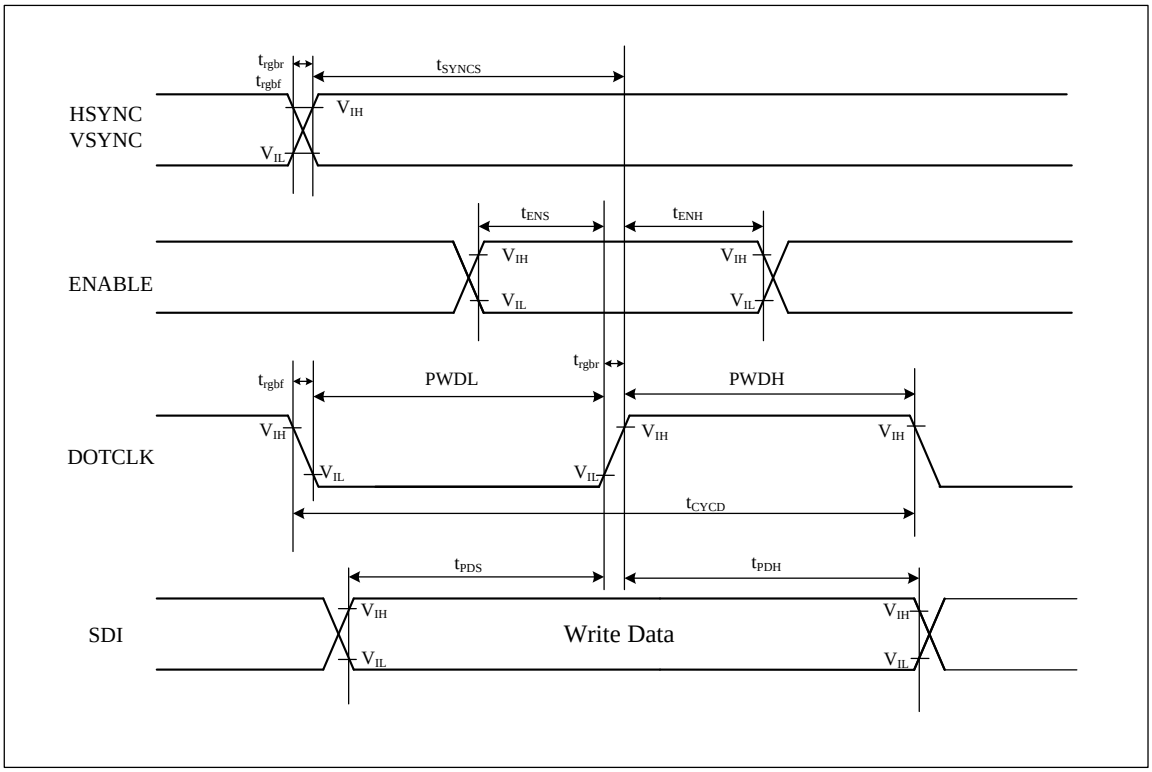


Figure49 RGB Interface Timing

12. Revision History

Version No.	Date	Page	Description
V1.00	2011-3-9	All	New Created
