a-Si TFT LCD Single Chip Driver 240RGBx320 Resolution and 262K color

Specification

Preliminary

Version: V1.02
Document No.: GC9301DS_V102.pdf

1. Introduction 6
2. Features 7
3. Block Diagram 8
3.1 Block diagram 8
3.2 Pin Descriptions 9
3.3 PAD coordinates 14
4. Interface setting 23
4.1. MCU interfaces 23
4.1.1. MCU interface selection 23
4.1.2. 8080-Ⅰ Series Parallel Interface 24
4.1.3. Write Cycle Sequence 25
4.1.4. Read Cycle Sequence 26
4.1.5. 8080-Ⅱ Series Parallel Interface 27
4.1.6. Write Cycle Sequence 28
4.1.7. Read Cycle Sequence 29
4.1.8. Serial Interface 30
4.1.9. Write Cycle Sequence 30
4.1.10. Read Cycle Sequence 33
4.1.11. Data Transfer Break and Recovery 36
4.1.12. Data Transfer Pause 38
4.1.13. Serial Interface Pause (3_wire) 39
4.1.14 .Parallel Interface Pause 39
4.1.15 . Data Transfer Mode 40
4.1.16 . Data Transfer Method 1 40
4.1.17 . Data Transfer Method 2 40
4.2. RGB Interface 41
4.2.1. RGB Interface Selection 41
4.2.2. RGB Interface Timing 43
4.3. VSYNC Interface 45
4.4. Display Data RAM (DDRAM) 47
4.5. Display Data Format 48
4.5.1 3-line Serial Interface 48
4.5.2 4-line Serial Interface 50
4.5.3. 8-bit Parallel MCU Interface 52
4.5.4. 9-bit Parallel MCU Interface 54
4.5.5. 16-bit Parallel MCU Interface 56
4.5.6. 18-bit Parallel MCU Interface 62
4.5.7. 6-bit Parallel RGB Interface 66
4.5.8. 16-bit Parallel RGB Interface 68
4.5.9. 18-bit Parallel RGB Interface 68
5. Function Description 69
5.1 Display data GRAM mapping 69
5.2 Address Counter (AC) of GRAM 69

5.3 GRAM to display address mapping 73
5.3.1 Normal display on or partial mode on, vertical scroll off 75
5.3.2 Vertical scroll display mode 76
5.3.3 Updating order on display active area in RGB interface mode 80
5.4 Tearing effect output line 82
5.4.1 Tearing effect line modes 82
5.4.2 Tearing effect line timing 83
5.5 Source driver 84
5.6 Gate driver 84
5.7 Scan mode setting 85
5.8 LCD power generation circuit 86
5.9 Gamma Correction 88
5.10 Power Level Definition 94
5.10.1 Power Levels 94
5.10.2 Power Flow Chart 95
5.11 Brightness control block 96
5.12 Input/output pin state 97
5.12.1 Output pins 97
5.12.2 Input pins 97
6. Command 98
6.1. Command List 98
6.2. Description of Level 1 Command 103
6.2.1. Read display identification information 1 (00h) 103
6.2.2. Software Reset (01h) 105
6.2.3. Read display identification information 2 (04h) 106
6.2.4. Read Display Status (09h) 108
6.2.5. Read Display Power Mode (0Ah) 110
6.2.6. Read Display MADCTL (0Bh) 112
6.2.7. Read Display Pixel Format (0Ch) 114
6.2.8. Read Display Image Format (0Dh) 116
6.2.9. Read Display Signal Mode (0Eh) 118
6.2.10. Read Display Self-Diagnostic Result (0Fh) 120
6.2.11. Enter Sleep Mode (10h) 121
6.2.12. Sleep Out Mode (11h) 123
6.2.13. Partial Mode ON (12h) 125
6.2.14. Normal Display Mode ON (13h) 126
6.2.15. Display Inversion OFF (20h) 127
6.2.16. Display Inversion ON (21h) 129
6.2.17. Display OFF (28h) 131
6.2.18. Display ON (29h) 133
6.2.19. Column Address Set (2Ah) 135
6.2.20. Row Address Set (2Bh) 137
6.2.21. Memory Write (2Ch) 139

6.2.22. Memory Read (2Eh) 141
6.2.23. Partial Area (30h) 143
6.2.24. Vertical Scrolling Definition (33h) 146
6.2.25. Tearing Effect Line OFF (34h) 150
6.2.26. Tearing Effect Line ON (35h) 151
6.2.27. Tearing Effect Line ON (36h) 153
6.2.28. Vertical Scrolling Start Address (37h) 156
6.2.29. Idle Mode OFF (38h) 158
6.2.30. Idle Mode ON (39h) 159
6.2.31. COLMOD: Pixel Format Set (3Ah) 161
6.2.32. write_memory_continue (3Ch) 163
6.2.33. Set_Tear_Scanline (44h) 165
6.2.34. Get_Scanline (45h) 167
6.2.35. Write Display Brightness (51h) 169
6.2.36. Read Display Brightness (52h) 170
6.2.37. Write CTRL Display (53h) 171
6.2.38. Read CTRL Display (54h) 173
6.2.39. Read ID1 (DAh) 175
6.2.40. Read ID2 (DBh) 176
6.2.41. Read ID3 (DCh) 177
6.3. Description of Level 2 Command 178
6.3.1. RGB Interface Signal Control (B0h) 178
6.3.2. Display Inversion Control (B4h) 179
6.3.3.Blanking Porch Control (B5h) 180
6.3.4. Display Function Control (B6h) 182
6.3.5. Read ID4 (D3h) 185
6.3.6. Interface Control (F6h) 186
6.4. Description of Level 3 Command 188
6.4.1. Frame Rate and Display Inversion Control (A3h) 188
6.4.2. Power control 1 (A4h) 190
6.4.3. Power control 2 (EDh) 191
6.4.4. Inter register enable 2 (EFh) 192
6.4.5. SET_GAMMA1 (F0h) 193
6.4.6. SET_GAMMA2 (F1h) 194
8.4.7. SET_GAMMA3 (F2h) 195
6.4.8. SET_GAMMA4 (F3h) 196
6.4.9. SET_GAMMA5 (F4h) 197
6.4.10. SET_GAMMA6 (F5h) 198
6.4.11. SET_GAMMA7(F7h) 199
6.4.12. SET_GAMMA8(F8h) 200
6.4.13. SET_GAMMA9(F9h) 201
6.4.14. SET_GAMMA10(FAh) 202
6.4.15. SET_GAMMA11(FBh) 203

6.4.16. SET_GAMMA12(FCh) 204
6.4.17. Power control 3 (FDh) 205
6.4.18. Inter register enable 1 (FEh) 207
6.4.19. Power control 4 (FFh) 208
7. Application 209
8. Electrical Characteristics 211
8.1 Absolute Maximum Ratings 211
8.2 DC Characteristics 212
8.3 AC Characteristics 214
8.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ) 214
8.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ) 216
8.3.3 Display Serial Interface Timing Characteristics (3-line SPI system) 219
8.3.4 Display Serial Interface Timing Characteristics (4-line SPI system) 220
8.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics 221
9. Revision History 222

1. Introduction

The GC9301 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

The GC9301 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

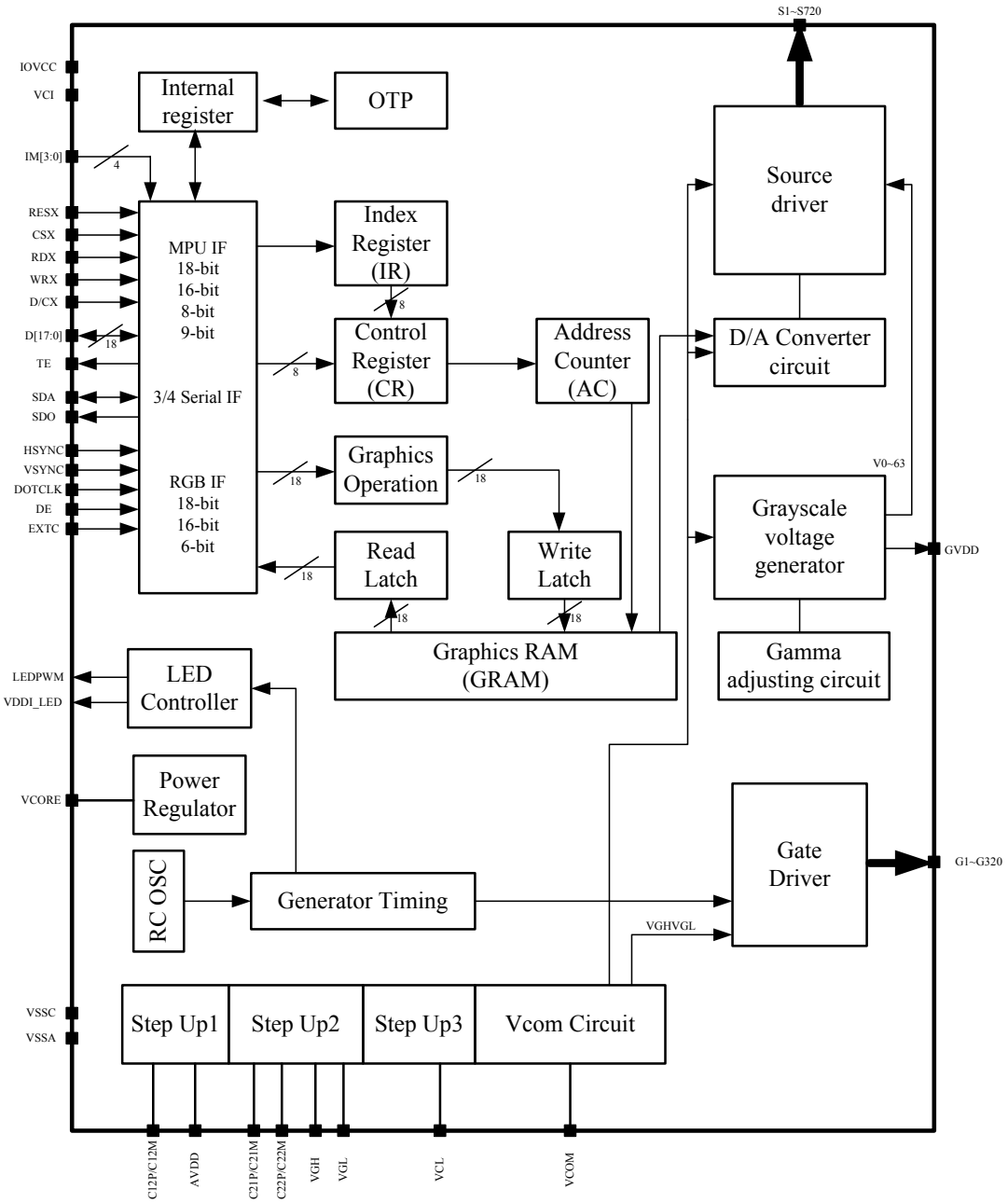
The GC9301 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9301 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9301 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- Display resolution: [240xRGB](H) x 320(V)
- Output:
  - 720 source outputs
  - 320 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-Ⅰ/8080-Ⅱ series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - VDDI = 1.65V ~ 3.3V (logic)
    - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/VCOM power supply voltage
    - AVDD - GND = 4.5V ~ 5.5V
    - VCL - GND = -1.5V ~ -3.0V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 20.0V
    - VGL - GND = -5.0V ~ -15.0V
    - VGH - VGL ≦32V
  - VCOM driver output voltage
    - VCOMH = 3.0V ~ (AVDD – 0.5)V
    - VCOML = (VCL+0.5)V ~ 0V
    - VCOMH - VCOML≦6.0V
- Operate temperature range: -40℃to 85℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1 Block diagram



3.2 Pin Descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDDI	I	P	Low voltage power supply for interface logic circuits(1.65~3.3V)
VDDI_LED	I		Power supply for LED driver interface.(1.65~3.3V) If LED driver is not used, fix this pin at VDDI.
VCI	I	Analog Power	High voltage power supply for analog circuit blocks(2.5~3.3V)
Vcore	O	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I	I/O Ground	System ground level for I/O circuits.
VSS	I	Digital Ground	System ground level for logic blocks.
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(VDDI/VSS)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅱ</td><td colspan="2">SDI:In
SDO:Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅱ</td><td colspan="2">SDI:In
SDO:Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
*:Fix this pin at VDDI or VSS.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>EXTC</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>Extended command set enable.
Low: extended command set is discarded.
High: extended command set is accepted.
Please connect EXTC to VDDI to read/write extended registers
(RB0h~RCFh,RE0h~RFFh)</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(VDDI/VSS)</td><td>Chip select input pin("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only. *note1,2</td></tr>
</table>

D/CX	I	MCU (VDDI/VSS)	This pin is used to select "Data or Command" in the parallel interface or 4-wire 8-bit serial data interface. When DCX='1', data is selected. When DCX='0', command is selected. If not used, this pin should be connected to VDDI or VSS.
RDX	I	MCU (VDDI/VSS)	8080-I/8080-II system (RDX):Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use
WRX(SCL)	I	MCU (VDDI/VSS)	8080-I/8080-II system (WRX): Serves ad a write signal and writes data at the rising edge. This pin is used serial interface clock in 3-wire 9-bit/4-write 8-bit serial data interface. Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use
SDI/SDA	I/O	MCU (VDDI/VSS)	When IM[3]:Low, Serial in/out signal. When IM[3]:High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
SDO	O	MCU (VDDI/VSS)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/VSS)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.

Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S720~S1	O	Source	Source output signals.. Leave the pin to open when not in use.
G320~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
AVDD	O	Power Stabilizing capacitor	Output voltage of 1st step up circuit(2*VCI).Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VGL	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VCL	O	Power stabilizing capacitor	Power supply for VCOML. VCL=0~-VCI Connect this pad with a stabilizing capacitor.
C12P,C12M	P		Connect the charge-pumping capacitor for generating AVDD level.
C21P,C21M C22P,C22M	P		Connect the charge-pumping capacitor for generating VGH,VGL level.
C31P,C31M	P		Floating
GVDD	O		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VGS	I		Low reference voltage for grayscale voltage generator. Connect an external resistor or to system ground.
VCOM	O		Power supply pad for the TFT-display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
LEDPWM	O		Output pin for PWM(Pulse width Modulation) signal of LED driving. If not used ,open this pad.

Test Pins			
Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation ,leave these pads open.

Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		720 pins (240*RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S720	V0~V63 grayscales
		G1~G320	VGH-VGL
		VCOM	VCOMH-VCOML :Amplitude = electronic volumes
5	Input Voltage	VDDI	1.65~3.30V
		VCI	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	4.5~5.5V
		VGH	10.0~20.0V
		VGL	-5.0~-15.0V
		VCL	-1.9~-3.0V
		VGH-VGL	Max. 32.0V
7	Internal Step-up Circuits	AVDD	VCI*2
		VGH	VCI*5
		VGL	VCI*-4
		VCL	VCI*-1

3.3 PAD coordinates

	Pad name	X	Y
1	DUMMY	-7292.5	-285
2	DUMMY	-7232.5	-285
3	VCOM	-7172.5	-285
4	VCOM	-7112.5	-285
5	VCOM	-7052.5	-285
6	VCOM	-6992.5	-285
7	VCOM	-6932.5	-285
8	VCOM	-6872.5	-285
9	VCOM	-6812.5	-285
10	VCOM	-6752.5	-285
11	DUMMY	-6692.5	-285
12	C22P	-6632.5	-285
13	C22P	-6572.5	-285
14	C22M	-6512.5	-285
15	C22M	-6452.5	-285
16	C21P	-6392.5	-285
17	C21P	-6332.5	-285
18	C21M	-6272.5	-285
19	C21M	-6212.5	-285
20	VGH	-6152.5	-285
21	VGH	-6092.5	-285
22	VGH	-6032.5	-285
23	VGH	-5972.5	-285
24	VGH	-5912.5	-285
25	DUMMY	-5852.5	-285
26	VGL	-5792.5	-285
27	VGL	-5732.5	-285
28	VGL	-5672.5	-285
29	VGL	-5612.5	-285
30	VGL	-5552.5	-285
31	VGL	-5492.5	-285
32	AVDD	-5432.5	-285
33	AVDD	-5372.5	-285
34	AVDD	-5312.5	-285
35	AVDD	-5252.5	-285
36	AVDD	-5192.5	-285
37	AVDD	-5132.5	-285
38	AVDD	-5072.5	-285
39	C12P	-5012.5	-285
40	C12P	-4952.5	-285
41	C12P	-4892.5	-285
42	C12P	-4832.5	-285
43	C12P	-4772.5	-285
44	C12P	-4712.5	-285
45	C12P	-4652.5	-285
46	C12M	-4592.5	-285
47	C12M	-4532.5	-285
48	C12M	-4472.5	-285
49	C12M	-4412.5	-285
50	C12M	-4352.5	-285

No.	Pad name	X	Y
51	C12M	-4292.5	-285
52	C12M	-4232.5	-285
53	C11P	-4172.5	-285
54	C11P	-4112.5	-285
55	C11P	-4052.5	-285
56	C11P	-3992.5	-285
57	C11P	-3932.5	-285
58	C11P	-3872.5	-285
59	C11P	-3812.5	-285
60	C11M	-3752.5	-285
61	C11M	-3692.5	-285
62	C11M	-3632.5	-285
63	C11M	-3572.5	-285
64	C11M	-3512.5	-285
65	C11M	-3452.5	-285
66	C11M	-3392.5	-285
67	DUMMY	-3332.5	-285
68	DUMMY	-3272.5	-285
69	DUMMY	-3212.5	-285
70	DUMMY	-3152.5	-285
71	DUMMY	-3092.5	-285
72	DUMMY	-3032.5	-285
73	DUMMY	-2972.5	-285
74	VCI	-2912.5	-285
75	VCI	-2842.5	-285
76	VCI	-2792.5	-285
77	VCI	-2732.5	-285
78	VCI	-2672.5	-285
79	VCI	-2612.5	-285
80	VCI	-2552.5	-285
81	VCI	-2492.5	-285
82	VSS3	-2432.5	-285
83	VSS3	-2372.5	-285
84	VSS3	-2312.5	-285
85	VSS	-2252.5	-285
86	VSS	-2192.5	-285
87	VSS	-2132.5	-285
88	VSS	-2072.5	-285
89	VSS	-2012.5	-285
90	VSS	-1952.5	-285
91	VSSC	-1892.5	-285
92	VSSC	-1832.5	-285
93	VSSC	-1772.5	-285
94	VSSC	-1712.5	-285
95	VSSC	-1652.5	-285
96	VSSC	-1592.5	-285
97	VSSC	-1532.5	-285
98	VSSA	-1472.5	-285
99	VSSA	-1412.5	-285
100	VSSA	-1352.5	-285

No.	Pad name	X	Y
101	VSSA	-1292.5	-285
102	VSSA	-1232.5	-285
103	VSSA	-1172.5	-285
104	VSSA	-1112.5	-285
105	VSSA	-1052.5	-285
106	DUMMY	-992.5	-285
107	VGS	-932.5	-285
108	VGS	-872.5	-285
109	EXTC	-812.5	-285
110	IM<3>	-752.5	-285
111	IM<2>	-692.5	-285
112	IM<1>	-632.5	-285
113	IM<0>	-572.5	-285
114	RESX	-512.5	-285
115	CSX	-452.5	-285
116	DCX	-392.5	-285
117	WRX	-332.5	-285
118	RDX	-272.5	-285
119	DUMMY	-212.5	-285
120	VSYNC	-152.5	-285
121	HSYNC	-92.5	-285
122	ENABL	-32.5	-285
123	DOTCLK	27.5	-285
124	DUMMY	87.5	-285
125	SDA	160	-285
126	DB[0]	245	-285
127	DB[1]	330	-285
128	DB[2]	415	-285
129	DB[3]	500	-285
130	DUMMY	572.5	-285
131	DB[4]	645	-285
132	DB[5]	730	-285
133	DB[6]	815	-285
134	DB[7]	900	-285
135	DUMMY	972.5	-285
136	DB[8]	1045	-285
137	DB[9]	1130	-285
138	DB[10]	1215	-285
139	DB[11]	1300	-285
140	DUMMY	1372.5	-285
141	DB[12]	1445	-285
142	DB[13]	1530	-285
143	DB[14]	1615	-285
144	DB[15]	1700	-285
145	DUMMY	1772.5	-285
146	DB[16]	1845	-285
147	DB[17]	1930	-285
148	DUMMY	2002.5	-285
149	TE	2075	-285
150	SDO	2160	-285

No.	Pad name	X	Y
151	LEDPWM	2245	-285
152	LEDON	2330	-285
153	VDDI_LED	2402.5	-285
154	VDDI_LED	2462.5	-285
155	DB[18]_Dummy	2535	-285
156	DB[19]_Dummy	2620	-285
157	DB[20]_Dummy	2705	-285
158	DB[21]_Dummy	2790	-285
159	DB[22]_Dummy	2875	-285
160	DB[23]_Dummy	2960	-285
161	DUMMY	3032.5	-285
162	VDDI	3092.5	-285
163	VDDI	3152.5	-285
164	VDDI	3212.5	-285
165	VDDI	3272.5	-285
166	VDDI	3332.5	-285
167	VDDI	3392.5	-285
168	VDDI	3452.5	-285
169	Vcore	3512.5	-285
170	Vcore	3572.5	-285
171	Vcore	3632.5	-285
172	Vcore	3692.5	-285
173	Vcore	3752.5	-285
174	Vcore	3812.5	-285
175	Vcore	3872.5	-285
176	Vcore	3932.5	-285
177	Vcore	3992.5	-285
178	Vcore	4052.5	-285
179	Vcore	4112.5	-285
180	Vcore	4172.5	-285
181	Vcore	4232.5	-285
182	Vcore	4292.5	-285
183	DUMMY	4352.5	-285
184	GVDD	4412.5	-285
185	GVDD	4472.5	-285
186	GVDD	4532.5	-285
187	GVDD	4592.5	-285
188	DUMMY	4652.5	-285
189	DUMMY	4712.5	-285
190	VCL	4772.5	-285
191	VCL	4832.5	-285
192	VCL	4892.5	-285
193	VCL	4952.5	-285
194	VCL	5012.5	-285
195	VCL	5072.5	-285
196	VCL	5132.5	-285
197	VCL	5192.5	-285
198	C13P	5252.5	-285
199	C13P	5312.5	-285
200	C13P	5372.5	-285

No.	Pad name	X	Y
201	C13P	5432.5	-285
202	C13P	5492.5	-285
203	C13P	5552.5	-285
204	C13P	5612.5	-285
205	C13P	5672.5	-285
206	C31M	5732.5	-285
207	C31M	5792.5	-285
208	C31M	5852.5	-285
209	C31M	5912.5	-285
210	C31M	5972.5	-285
211	C31M	6032.5	-285
212	C31M	6092.5	-285
213	C31M	6152.5	-285
214	DUMMY	6212.5	-285
215	DUMMY	6272.5	-285
216	DUMMY	6332.5	-285
217	DUMMY	6392.5	-285
218	DUMMY	6452.5	-285
219	DUMMY	6512.5	-285
220	DUMMY	6572.5	-285
221	DUMMY	6632.5	-285
222	DUMMY	6692.5	-285
223	VCOM	6752.5	-285
224	VCOM	6812.5	-285
225	VCOM	6872.5	-285
226	VCOM	6932.5	-285
227	VCOM	6992.5	-285
228	VCOM	7052.5	-285
229	VCOM	7112.5	-285
230	VCOM	7172.5	-285
231	DUMMY	7232.5	-285
232	DUMMY	7292.5	-285
233	DUMMY	7399	261
234	DUMMY	7385	126
235	DUMMY	7371	261
236	G2	7357	126
237	G4	7343	261
238	G6	7329	126
239	G8	7315	261
240	G10	7301	126
241	G12	7287	261
242	G14	7273	126
243	G16	7259	261
244	G18	7245	126
245	G20	7231	261
246	G22	7217	126
247	G24	7203	261
248	G26	7189	126
249	G28	7175	261
250	G30	7161	126

No.	Pad	X	Y
251	G32	7147	261
252	G34	7133	126
253	G36	7119	261
254	G38	7105	126
255	G40	7091	261
256	G42	7077	126
257	G44	7063	261
258	G46	7049	126
259	G48	7035	261
260	G50	7021	126
261	G52	7007	261
262	G54	6993	126
263	G56	6979	261
264	G58	6965	126
265	G60	6951	261
266	G62	6937	126
267	G64	6923	261
268	G66	6909	126
269	G68	6895	261
270	G70	6881	126
271	G72	6867	261
272	G74	6853	126
273	G76	6839	261
274	G78	6825	126
275	G80	6811	261
276	G82	6797	126
277	G84	6783	261
278	G86	6769	126
279	G88	6755	261
280	G90	6741	126
281	G92	6727	261
282	G94	6713	126
283	G96	6699	261
284	G98	6685	126
285	G100	6671	261
286	G102	6657	126
287	G104	6643	261
288	G106	6629	126
289	G108	6615	261
290	G110	6601	126
291	G112	6587	261
292	G114	6573	126
293	G116	6559	261
294	G118	6545	126
295	G120	6531	261
296	G122	6517	126
297	G124	6503	261
298	G126	6489	126
299	G128	6475	261
300	G130	6461	126

No.	Pad name	X	Y
301	G132	6447	261
302	G134	6433	126
303	G136	6419	261
304	G138	6405	126
305	G140	6391	261
306	G142	6377	126
307	G144	6363	261
308	G146	6349	126
309	G148	6335	261
310	G150	6321	126
311	G152	6307	261
312	G154	6293	126
313	G156	6279	261
314	G158	6265	126
315	G160	6251	261
316	G162	6237	126
317	G164	6223	261
318	G166	6209	126
319	G168	6195	261
320	G170	6181	126
321	G172	6167	261
322	G174	6153	126
323	G176	6139	261
324	G178	6125	126
325	G180	6111	261
326	G182	6097	126
327	G184	6083	261
328	G186	6069	126
329	G188	6055	261
330	G190	6041	126
331	G192	6027	261
332	G194	6013	126
333	G196	5999	261
334	G198	5985	126
335	G200	5971	261
336	G202	5957	126
337	G204	5943	261
338	G206	5929	126
339	G208	5915	261
340	G210	5901	126
341	G212	5887	261
342	G214	5873	126
343	G216	5859	261
344	G218	5845	126
345	G220	5831	261
346	G222	5817	126
347	G224	5803	261
348	G226	5789	126
349	G228	5775	261
350	G230	5761	126

No.	Pad name	X	Y
351	G232	5747	261
352	G234	5733	126
353	G236	5719	261
354	G238	5705	126
355	G240	5691	261
356	G242	5677	126
357	G244	5663	261
358	G246	5649	126
359	G248	5635	261
360	G250	5621	126
361	G252	5607	261
362	G254	5593	126
363	G256	5579	261
364	G258	5565	126
365	G260	5551	261
366	G262	5537	126
367	G264	5523	261
368	G266	5509	126
369	G268	5495	261
370	G270	5481	126
371	G272	5467	261
372	G274	5453	126
373	G276	5439	261
374	G278	5425	126
375	G280	5411	261
376	G282	5397	126
377	G284	5383	261
378	G286	5369	126
379	G288	5355	261
380	G290	5341	126
381	G292	5327	261
382	G294	5313	126
383	G296	5299	261
384	G298	5285	126
385	G300	5271	261
386	G302	5257	126
387	G304	5243	261
388	G306	5229	126
389	G308	5215	261
390	G310	5201	126
391	G312	5187	261
392	G314	5173	126
393	G316	5159	261
394	G318	5145	126
395	G320	5131	261
396	S720	5075	126
397	S719	5061	261
398	S718	5047	126
399	S717	5033	261
400	S716	5019	126

No.	Pad name	X	Y
401	S715	5005	261
402	S714	4991	126
403	S713	4977	261
404	S712	4963	126
405	S711	4949	261
406	S710	4935	126
407	S709	4921	261
408	S708	4907	126
409	S707	4893	261
410	S706	4879	126
411	S705	4865	261
412	S704	4851	126
413	S703	4837	261
414	S702	4823	126
415	S701	4809	261
416	S700	4795	126
417	S699	4781	261
418	S698	4767	126
419	S697	4753	261
420	S696	4739	126
421	S695	4725	261
422	S694	4711	126
423	S693	4697	261
424	S692	4683	126
425	S691	4669	261
426	S690	4655	126
427	S689	4641	261
428	S688	4627	126
429	S687	4613	261
430	S686	4599	126
431	S685	4585	261
432	S684	4571	126
433	S683	4557	261
434	S682	4543	126
435	S681	4529	261
436	S680	4515	126
437	S679	4501	261
438	S678	4487	126
439	S677	4473	261
440	S676	4459	126
441	S675	4445	261
442	S674	4431	126
443	S673	4417	261
444	S672	4403	126
445	S671	4389	261
446	S670	4375	126
447	S669	4361	261
448	S668	4347	126
449	S667	4333	261
450	S666	4319	126

No.	Pad	X	Y
451	S665	4305	261
452	S664	4291	126
453	S663	4277	261
454	S662	4263	126
455	S661	4249	261
456	S660	4235	126
457	S659	4221	261
458	S658	4207	126
459	S657	4193	261
460	S656	4179	126
461	S655	4165	261
462	S654	4151	126
463	S653	4137	261
464	S652	4123	126
465	S651	4109	261
466	S650	4095	126
467	S649	4081	261
468	S648	4067	126
469	S647	4053	261
470	S646	4039	126
471	S645	4025	261
472	S644	4011	126
473	S643	3997	261
474	S642	3983	126
475	S641	3969	261
476	S640	3955	126
477	S639	3941	261
478	S638	3927	126
479	S637	3913	261
480	S636	3899	126
481	S635	3885	261
482	S634	3871	126
483	S633	3857	261
484	S632	3843	126
485	S631	3829	261
486	S630	3815	126
487	S629	3801	261
488	S628	3787	126
489	S627	3773	261
490	S626	3759	126
491	S625	3745	261
492	S624	3731	126
493	S623	3717	261
494	S622	3703	126
495	S621	3689	261
496	S620	3675	126
497	S619	3661	261
498	S618	3647	126
499	S617	3633	261
500	S616	3619	126

No.	Pad name	X	Y
501	S615	3605	261
502	S614	3591	126
503	S613	3577	261
504	S612	3563	126
505	S611	3549	261
506	S610	3535	126
507	S609	3521	261
508	S608	3507	126
509	S607	3493	261
510	S606	3479	126
511	S605	3465	261
512	S604	3451	126
513	S603	3437	261
514	S602	3423	126
515	S601	3409	261
516	S600	3395	126
517	S599	3381	261
518	S598	3367	126
519	S597	3353	261
520	S596	3339	126
521	S595	3325	261
522	S594	3311	126
523	S593	3297	261
524	S592	3283	126
525	S591	3269	261
526	S590	3255	126
527	S589	3241	261
528	S588	3227	126
529	S587	3213	261
530	S586	3199	126
531	S585	3185	261
532	S584	3171	126
533	S583	3157	261
534	S582	3143	126
535	S581	3129	261
536	S580	3115	126
537	S579	3101	261
538	S578	3087	126
539	S577	3073	261
540	S576	3059	126
541	S575	3045	261
542	S574	3031	126
543	S573	3017	261
544	S572	3003	126
545	S571	2989	261
546	S570	2975	126
547	S569	2961	261
548	S568	2947	126
549	S567	2933	261
550	S566	2919	126

No.	Pad name	X	Y
551	S565	2905	261
552	S564	2891	126
553	S563	2877	261
554	S562	2863	126
555	S561	2849	261
556	S560	2835	126
557	S559	2821	261
558	S558	2807	126
559	S557	2793	261
560	S556	2779	126
561	S555	2765	261
562	S554	2751	126
563	S553	2737	261
564	S552	2723	126
565	S551	2709	261
566	S550	2695	126
567	S549	2681	261
568	S548	2667	126
569	S547	2653	261
570	S546	2639	126
571	S545	2625	261
572	S544	2611	126
573	S543	2597	261
574	S542	2583	126
575	S541	2569	261
576	S540	2555	126
577	S539	2541	261
578	S538	2527	126
579	S537	2513	261
580	S536	2499	126
581	S535	2485	261
582	S534	2471	126
583	S533	2457	261
584	S532	2443	126
585	S531	2429	261
586	S530	2415	126
587	S529	2401	261
588	S528	2387	126
589	S527	2373	261
590	S526	2359	126
591	S525	2345	261
592	S524	2331	126
593	S523	2317	261
594	S522	2303	126
595	S521	2289	261
596	S520	2275	126
597	S519	2261	261
598	S518	2247	126
599	S517	2233	261
600	S516	2219	126

No.	Pad name	X	Y
601	S515	2205	261
602	S514	2191	126
603	S513	2177	261
604	S512	2163	126
605	S511	2149	261
606	S510	2135	126
607	S509	2121	261
608	S508	2107	126
609	S507	2093	261
610	S506	2079	126
611	S505	2065	261
612	S504	2051	126
613	S503	2037	261
614	S502	2023	126
615	S501	2009	261
616	S500	1995	126
617	S499	1981	261
618	S498	1967	126
619	S497	1953	261
620	S496	1939	126
621	S495	1925	261
622	S494	1911	126
623	S493	1897	261
624	S492	1883	126
625	S491	1869	261
626	S490	1855	126
627	S489	1841	261
628	S488	1827	126
629	S487	1813	261
630	S486	1799	126
631	S485	1785	261
632	S484	1771	126
633	S483	1757	261
634	S482	1743	126
635	S481	1729	261
636	S480	1715	126
637	S479	1701	261
638	S478	1687	126
639	S477	1673	261
640	S476	1659	126
641	S475	1645	261
642	S474	1631	126
643	S473	1617	261
644	S472	1603	126
645	S471	1589	261
646	S470	1575	126
647	S469	1561	261
648	S468	1547	126
649	S467	1533	261
650	S466	1519	126

No.	Pad	X	Y
651	S465	1505	261
652	S464	1491	126
653	S463	1477	261
654	S462	1463	126
655	S461	1449	261
656	S460	1435	126
657	S459	1421	261
658	S458	1407	126
659	S457	1393	261
660	S456	1379	126
661	S455	1365	261
662	S454	1351	126
663	S453	1337	261
664	S452	1323	126
665	S451	1309	261
666	S450	1295	126
667	S449	1281	261
668	S448	1267	126
669	S447	1253	261
670	S446	1239	126
671	S445	1225	261
672	S444	1211	126
673	S443	1197	261
674	S442	1183	126
675	S441	1169	261
676	S440	1155	126
677	S439	1141	261
678	S438	1127	126
679	S437	1113	261
680	S436	1099	126
681	S435	1085	261
682	S434	1071	126
683	S433	1057	261
684	S432	1043	126
685	S431	1029	261
686	S430	1015	126
687	S429	1001	261
688	S428	987	126
689	S427	973	261
690	S426	959	126
691	S425	945	261
692	S424	931	126
693	S423	917	261
694	S422	903	126
695	S421	889	261
696	S420	875	126
697	S419	861	261
698	S418	847	126
699	S417	833	261
700	S416	819	126

No.	Pad name	X	Y
701	S415	805	261
702	S414	791	126
703	S413	777	261
704	S412	763	126
705	S411	749	261
706	S410	735	126
707	S409	721	261
708	S408	707	126
709	S407	693	261
710	S406	679	126
711	S405	665	261
712	S404	651	126
713	S403	637	261
714	S402	623	126
715	S401	609	261
716	S400	595	126
717	S399	581	261
718	S398	567	126
719	S397	553	261
720	S396	539	126
721	S395	525	261
722	S394	511	126
723	S393	497	261
724	S392	483	126
725	S391	469	261
726	S390	455	126
727	S389	441	261
728	S388	427	126
729	S387	413	261
730	S386	399	126
731	S385	385	261
732	S384	371	126
733	S383	357	261
734	S382	343	126
735	S381	329	261
736	S380	315	126
737	S379	301	261
738	S378	287	126
739	S377	273	261
740	S376	259	126
741	S375	245	261
742	S374	231	126
743	S373	217	261
744	S372	203	126
745	S371	189	261
746	S370	175	126
747	S369	161	261
748	S368	147	126
749	S367	133	261
750	S366	119	126

No.	Pad name	X	Y
751	S365	105	261
752	S364	91	126
753	S363	77	261
754	S362	63	126
755	S361	49	261
756	S360	-49	126
757	S359	-63	261
758	S358	-77	126
759	S357	-91	261
760	S356	-105	126
761	S355	-119	261
762	S354	-133	126
763	S353	-147	261
764	S352	-161	126
765	S351	-175	261
766	S350	-189	126
767	S349	-203	261
768	S348	-217	126
769	S347	-231	261
770	S346	-245	126
771	S345	-259	261
772	S344	-273	126
773	S343	-287	261
774	S342	-301	126
775	S341	-315	261
776	S340	-329	126
777	S339	-343	261
778	S338	-357	126
779	S337	-371	261
780	S336	-385	126
781	S335	-399	261
782	S334	-413	126
783	S333	-427	261
784	S332	-441	126
785	S331	-455	261
786	S330	-469	126
787	S329	-483	261
788	S328	-497	126
789	S327	-511	261
790	S326	-525	126
791	S325	-539	261
792	S324	-553	126
793	S323	-567	261
794	S322	-581	126
795	S321	-595	261
796	S320	-609	126
797	S319	-623	261
798	S318	-637	126
799	S317	-651	261
800	S316	-665	126

No.	Pad name	X	Y
801	S315	-679	261
802	S314	-693	126
803	S313	-707	261
804	S312	-721	126
805	S311	-735	261
806	S310	-749	126
807	S309	-763	261
808	S308	-777	126
809	S307	-791	261
810	S306	-805	126
811	S305	-819	261
812	S304	-833	126
813	S303	-847	261
814	S302	-861	126
815	S301	-875	261
816	S300	-889	126
817	S299	-903	261
818	S298	-917	126
819	S297	-931	261
820	S296	-945	126
821	S295	-959	261
822	S294	-973	126
823	S293	-987	261
824	S292	-1001	126
825	S291	-1015	261
826	S290	-1029	126
827	S289	-1043	261
828	S288	-1057	126
829	S287	-1071	261
830	S286	-1085	126
831	S285	-1099	261
832	S284	-1113	126
833	S283	-1127	261
834	S282	-1141	126
835	S281	-1155	261
836	S280	-1169	126
837	S279	-1183	261
838	S278	-1197	126
839	S277	-1211	261
840	S276	-1225	126
841	S275	-1239	261
842	S274	-1253	126
843	S273	-1267	261
844	S272	-1281	126
845	S271	-1295	261
846	S270	-1309	126
847	S269	-1323	261
848	S268	-1337	126
849	S267	-1351	261
850	S266	-1365	126

No.	Pad	X	Y
851	S265	-1379	261
852	S264	-1393	126
853	S263	-1407	261
854	S262	-1421	126
855	S261	-1435	261
856	S260	-1449	126
857	S259	-1463	261
858	S258	-1477	126
859	S257	-1491	261
860	S256	-1505	126
861	S255	-1519	261
862	S254	-1533	126
863	S253	-1547	261
864	S252	-1561	126
865	S251	-1575	261
866	S250	-1589	126
867	S249	-1603	261
868	S248	-1617	126
869	S247	-1631	261
870	S246	-1645	126
871	S245	-1659	261
872	S244	-1673	126
873	S243	-1687	261
874	S242	-1701	126
875	S241	-1715	261
876	S240	-1729	126
877	S239	-1743	261
878	S238	-1757	126
879	S237	-1771	261
880	S236	-1785	126
881	S235	-1799	261
882	S234	-1813	126
883	S233	-1827	261
884	S232	-1841	126
885	S231	-1855	261
886	S230	-1869	126
887	S229	-1883	261
888	S228	-1897	126
889	S227	-1911	261
890	S226	-1925	126
891	S225	-1939	261
892	S224	-1953	126
893	S223	-1967	261
894	S222	-1981	126
895	S221	-1995	261
896	S220	-2009	126
897	S219	-2023	261
898	S218	-2037	126
899	S217	-2051	261
900	S216	-2065	126

No.	Pad name	X	Y
901	S215	-2079	261
902	S214	-2093	126
903	S213	-2107	261
904	S212	-2121	126
905	S211	-2135	261
906	S210	-2149	126
907	S209	-2163	261
908	S208	-2177	126
909	S207	-2191	261
910	S206	-2205	126
911	S205	-2219	261
912	S204	-2233	126
913	S203	-2247	261
914	S202	-2261	126
915	S201	-2275	261
916	S200	-2289	126
917	S199	-2303	261
918	S198	-2317	126
919	S197	-2331	261
920	S196	-2345	126
921	S195	-2359	261
922	S194	-2373	126
923	S193	-2387	261
924	S192	-2401	126
925	S191	-2415	261
926	S190	-2429	126
927	S189	-2443	261
928	S188	-2457	126
929	S187	-2471	261
930	S186	-2485	126
931	S185	-2499	261
932	S184	-2513	126
933	S183	-2527	261
934	S182	-2541	126
935	S181	-2555	261
936	S180	-2569	126
937	S179	-2583	261
938	S178	-2597	126
939	S177	-2611	261
940	S176	-2625	126
941	S175	-2639	261
942	S174	-2653	126
943	S173	-2667	261
944	S172	-2681	126
945	S171	-2695	261
946	S170	-2709	126
947	S169	-2723	261
948	S168	-2737	126
949	S167	-2751	261
950	S166	-2765	126

No.	Pad name	X	Y
951	S165	-2779	261
952	S164	-2793	126
953	S163	-2807	261
954	S162	-2821	126
955	S161	-2835	261
956	S160	-2849	126
957	S159	-2863	261
958	S158	-2877	126
959	S157	-2891	261
960	S156	-2905	126
961	S155	-2919	261
962	S154	-2933	126
963	S153	-2947	261
964	S152	-2961	126
965	S151	-2975	261
966	S150	-2989	126
967	S149	-3003	261
968	S148	-3017	126
969	S147	-3031	261
970	S146	-3045	126
971	S145	-3059	261
972	S144	-3073	126
973	S143	-3087	261
974	S142	-3101	126
975	S141	-3115	261
976	S140	-3129	126
977	S139	-3143	261
978	S138	-3157	126
979	S137	-3171	261
980	S136	-3185	126
981	S135	-3199	261
982	S134	-3213	126
983	S133	-3227	261
984	S132	-3241	126
985	S131	-3255	261
986	S130	-3269	126
987	S129	-3283	261
988	S128	-3297	126
989	S127	-3311	261
990	S126	-3325	126
991	S125	-3339	261
992	S124	-3353	126
993	S123	-3367	261
994	S122	-3381	126
995	S121	-3395	261
996	S120	-3409	126
997	S119	-3423	261
998	S118	-3437	126
999	S117	-3451	261
1000	S116	-3465	126

No.	Pad name	X	Y
1001	S115	-3479	261
1002	S114	-3493	126
1003	S113	-3507	261
1004	S112	-3521	126
1005	S111	-3535	261
1006	S110	-3549	126
1007	S109	-3563	261
1008	S108	-3577	126
1009	S107	-3591	261
1010	S106	-3605	126
1011	S105	-3619	261
1012	S104	-3633	126
1013	S103	-3647	261
1014	S102	-3661	126
1015	S101	-3675	261
1016	S100	-3689	126
1017	S99	-3703	261
1018	S98	-3717	126
1019	S97	-3731	261
1020	S96	-3745	126
1021	S95	-3759	261
1022	S94	-3773	126
1023	S93	-3787	261
1024	S92	-3801	126
1025	S91	-3815	261
1026	S90	-3829	126
1027	S89	-3843	261
1028	S88	-3857	126
1029	S87	-3871	261
1030	S86	-3885	126
1031	S85	-3899	261
1032	S84	-3913	126
1033	S83	-3927	261
1034	S82	-3941	126
1035	S81	-3955	261
1036	S80	-3969	126
1037	S79	-3983	261
1038	S78	-3997	126
1039	S77	-4011	261
1040	S76	-4025	126
1041	S75	-4039	261
1042	S74	-4053	126
1043	S73	-4067	261
1044	S72	-4081	126
1045	S71	-4095	261
1046	S70	-4109	126
1047	S69	-4123	261
1048	S68	-4137	126
1049	S67	-4151	261
1050	S66	-4165	126

No.	Pad	X	Y
1051	S65	-4179	261
1052	S64	-4193	126
1053	S63	-4207	261
1054	S62	-4221	126
1055	S61	-4235	261
1056	S60	-4249	126
1057	S59	-4263	261
1058	S58	-4277	126
1059	S57	-4291	261
1060	S56	-4305	126
1061	S55	-4319	261
1062	S54	-4333	126
1063	S53	-4347	261
1064	S52	-4361	126
1065	S51	-4375	261
1066	S50	-4389	126
1067	S49	-4403	261
1068	S48	-4417	126
1069	S47	-4431	261
1070	S46	-4445	126
1071	S45	-4459	261
1072	S44	-4473	126
1073	S43	-4487	261
1074	S42	-4501	126
1075	S41	-4515	261
1076	S40	-4529	126
1077	S39	-4543	261
1078	S38	-4557	126
1079	S37	-4571	261
1080	S36	-4585	126
1081	S35	-4599	261
1082	S34	-4613	126
1083	S33	-4627	261
1084	S32	-4641	126
1085	S31	-4655	261
1086	S30	-4669	126
1087	S29	-4683	261
1088	S28	-4697	126
1089	S27	-4711	261
1090	S26	-4725	126
1091	S25	-4739	261
1092	S24	-4753	126
1093	S23	-4767	261
1094	S22	-4781	126
1095	S21	-4795	261
1096	S20	-4809	126
1097	S19	-4823	261
1098	S18	-4837	126
1099	S17	-4851	261
1100	S16	-4865	126

No.	Pad name	X	Y
1101	S15	-4879	261
1102	S14	-4893	126
1103	S13	-4907	261
1104	S12	-4921	126
1105	S11	-4935	261
1106	S10	-4949	126
1107	S9	-4963	261
1108	S8	-4977	126
1109	S7	-4991	261
1110	S6	-5005	126
1111	S5	-5019	261
1112	S4	-5033	126
1113	S3	-5047	261
1114	S2	-5061	126
1115	S1	-5075	261
1116	G319	-5131	126
1117	G317	-5145	261
1118	G315	-5159	126
1119	G313	-5173	261
1120	G311	-5187	126
1121	G309	-5201	261
1122	G307	-5215	126
1123	G305	-5229	261
1124	G303	-5243	126
1125	G301	-5257	261
1126	G299	-5271	126
1127	G297	-5285	261
1128	G295	-5299	126
1129	G293	-5313	261
1130	G291	-5327	126
1131	G289	-5341	261
1132	G287	-5355	126
1133	G285	-5369	261
1134	G283	-5383	126
1135	G281	-5397	261
1136	G279	-5411	126
1137	G277	-5425	261
1138	G275	-5439	126
1139	G273	-5453	261
1140	G271	-5467	126
1141	G269	-5481	261
1142	G267	-5495	126
1143	G265	-5509	261
1144	G263	-5523	126
1145	G261	-5537	261
1146	G259	-5551	126
1147	G257	-5565	261
1148	G255	-5579	126
1149	G253	-5593	261
1150	G251	-5607	126

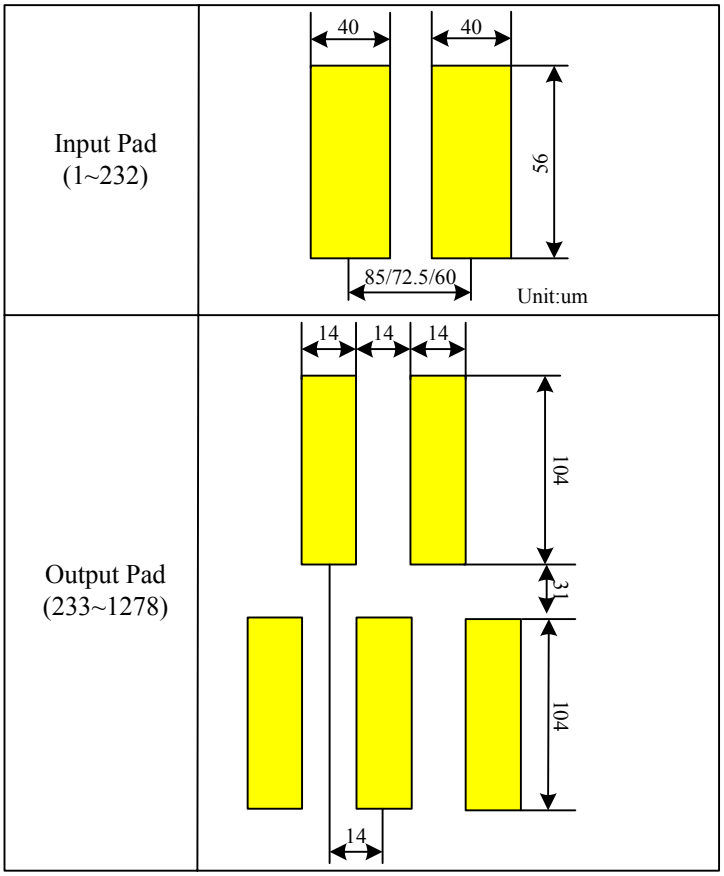
No.	Pad name	X	Y
1151	G249	-5621	261
1152	G247	-5635	126
1153	G245	-5649	261
1154	G243	-5663	126
1155	G241	-5677	261
1156	G239	-5691	126
1157	G237	-5705	261
1158	G235	-5719	126
1159	G233	-5733	261
1160	G231	-5747	126
1161	G229	-5761	261
1162	G227	-5775	126
1163	G225	-5789	261
1164	G223	-5803	126
1165	G221	-5817	261
1166	G219	-5831	126
1167	G217	-5845	261
1168	G215	-5859	126
1169	G213	-5873	261
1170	G211	-5887	126
1171	G209	-5901	261
1172	G207	-5915	126
1173	G205	-5929	261
1174	G203	-5943	126
1175	G201	-5957	261
1176	G199	-5971	126
1177	G197	-5985	261
1178	G195	-5999	126
1179	G193	-6013	261
1180	G191	-6027	126
1181	G189	-6041	261
1182	G187	-6055	126
1183	G185	-6069	261
1184	G183	-6083	126
1185	G181	-6097	261
1186	G179	-6111	126
1187	G177	-6125	261
1188	G175	-6139	126
1189	G173	-6153	261
1190	G171	-6167	126
1191	G169	-6181	261
1192	G167	-6195	126
1193	G165	-6209	261
1194	G163	-6223	126
1195	G161	-6237	261
1196	G159	-6251	126
1197	G157	-6265	261
1198	G155	-6279	126
1199	G153	-6293	261
1200	G151	-6307	126

No.	Pad name	X	Y
1201	G149	-6321	261
1202	G147	-6335	126
1203	G145	-6349	261
1204	G143	-6363	126
1205	G141	-6377	261
1206	G139	-6391	126
1207	G137	-6405	261
1208	G135	-6419	126
1209	G133	-6433	261
1210	G131	-6447	126
1211	G129	-6461	261
1212	G127	-6475	126
1213	G125	-6489	261
1214	G123	-6503	126
1215	G121	-6517	261
1216	G119	-6531	126
1217	G117	-6545	261
1218	G115	-6559	126
1219	G113	-6573	261
1220	G111	-6587	126
1221	G109	-6601	261
1222	G107	-6615	126
1223	G105	-6629	261
1224	G103	-6643	126
1225	G101	-6657	261
1226	G99	-6671	126
1227	G97	-6685	261
1228	G95	-6699	126
1229	G93	-6713	261
1230	G91	-6727	126
1231	G89	-6741	261
1232	G87	-6755	126
1233	G85	-6769	261
1234	G83	-6783	126
1235	G81	-6797	261
1236	G79	-6811	126
1237	G77	-6825	261
1238	G75	-6839	126
1239	G73	-6853	261
1240	G71	-6867	126
1241	G69	-6881	261
1242	G67	-6895	126
1243	G65	-6909	261
1244	G63	-6923	126
1245	G61	-6937	261
1246	G59	-6951	126
1247	G57	-6965	261
1248	G55	-6979	126
1249	G53	-6993	261
1250	G51	-7007	126

No.	Pad name	X	Y
1251	G49	-7021	261
1252	G47	-7035	126
1253	G45	-7049	261
1254	G43	-7063	126
1255	G41	-7077	261
1256	G39	-7091	126
1257	G37	-7105	261
1258	G35	-7119	126
1259	G33	-7133	261
1260	G31	-7147	126
1261	G29	-7161	261
1262	G27	-7175	126
1263	G25	-7189	261
1264	G23	-7203	126
1265	G21	-7217	261
1266	G19	-7231	126
1267	G17	-7245	261
1268	G15	-7259	126
1269	G13	-7273	261
1270	G11	-7287	126
1271	G9	-7301	261
1272	G7	-7315	126
1273	G5	-7329	261
1274	G3	-7343	126
1275	G1	-7357	261
1276	DUMMY	-7371	126
1277	DUMMY	-7385	261
1278	DUMMY	-7399	126

Alignment mark	X	Y
Left COG Align	-7480	260
Right COG Align	7480	260

BUMP Size


Input Pad
(1~232)
40
40
56
85/72.5/60
Unit:um
Output Pad
(233~1278)
14
14
14
104
31
104
14

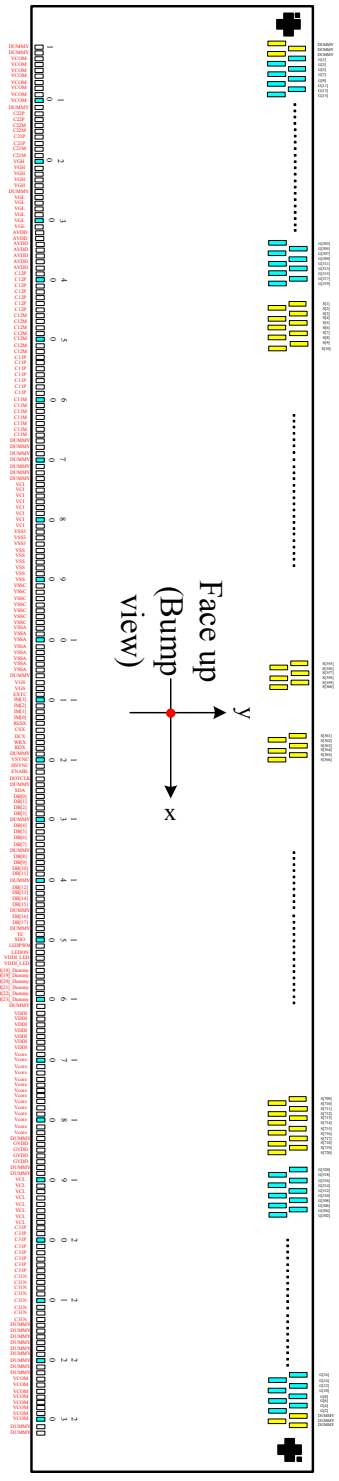
Chip Size: 15310um x 725um

Chip thickness: 280um(typ.)

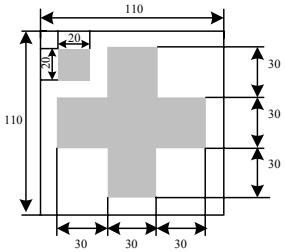
Pad Location: Pad Center.

Coordinate Origin: Chip center

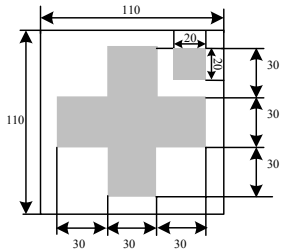
Au bump height: 12um(typ.)



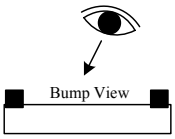
Alignment Marks



Alignment Mark:A1



Alignment Mark:A2



4. Interface setting

4.1. MCU interfaces

GC9301 provides the 8-/9-/16-/18-bit parallel system interface for 8080-Ⅰ/8080-Ⅱ series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface Ⅱ	SCL,SDI,SDO,CSX	
1	1	1	0	4-wire 8-bit data serial interface Ⅱ	SCL,SDI,SDO,D/CX,CSX	

4.1.2. 8080-Ⅰ Series Parallel Interface

GC9301 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅰ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9301 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9301 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX=’1’, D [17:0] bits are display RAM data or command’s parameters. When D/CX=’0’, D[17:0] bits are commands.

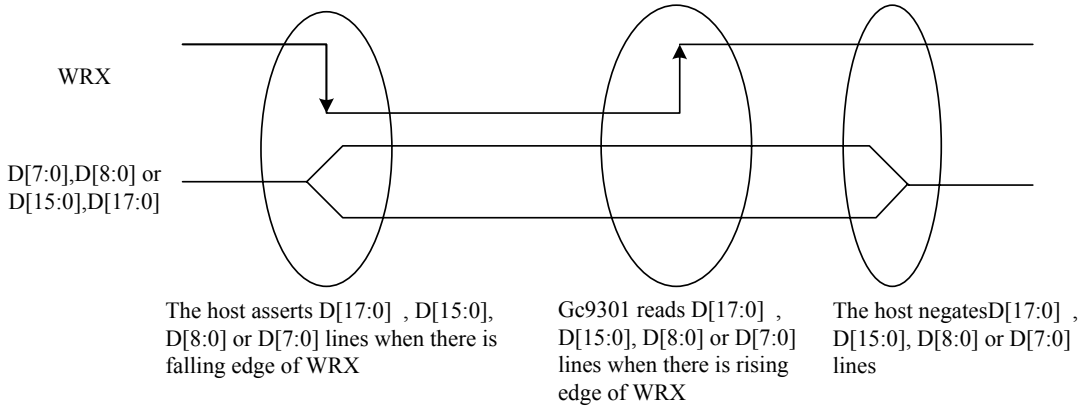
The 8080-Ⅰ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅰ Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.
The selection of 8080-Ⅰ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 8-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
0	0	0	1	8080 MCU 16-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
0	0	1	0	8080 MCU 9-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface I	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.

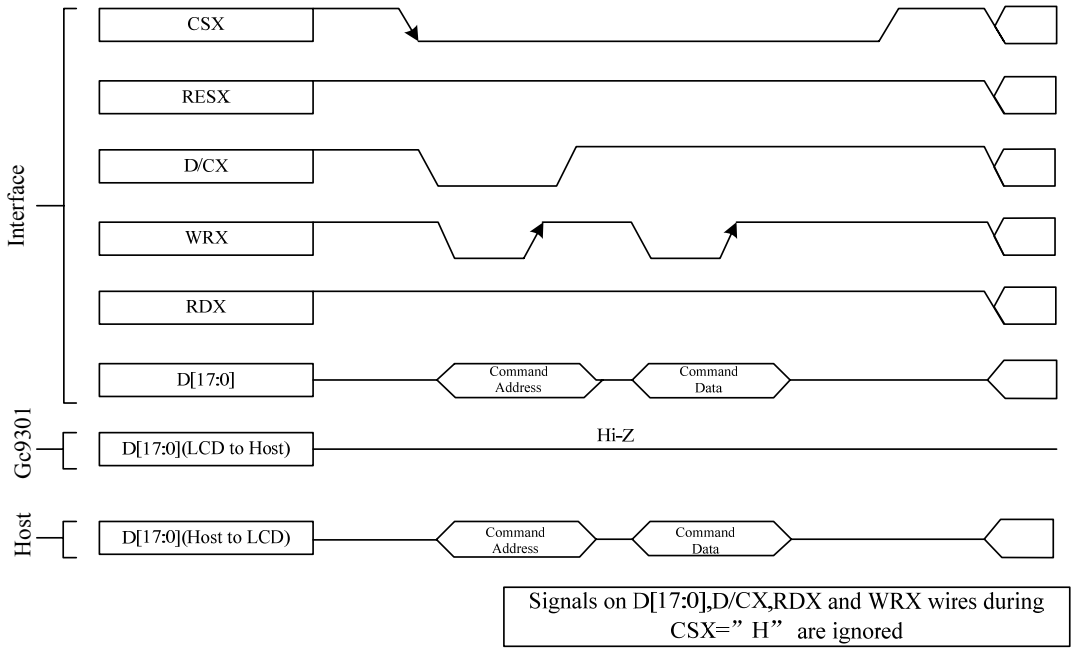
4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅰ MCU interface.



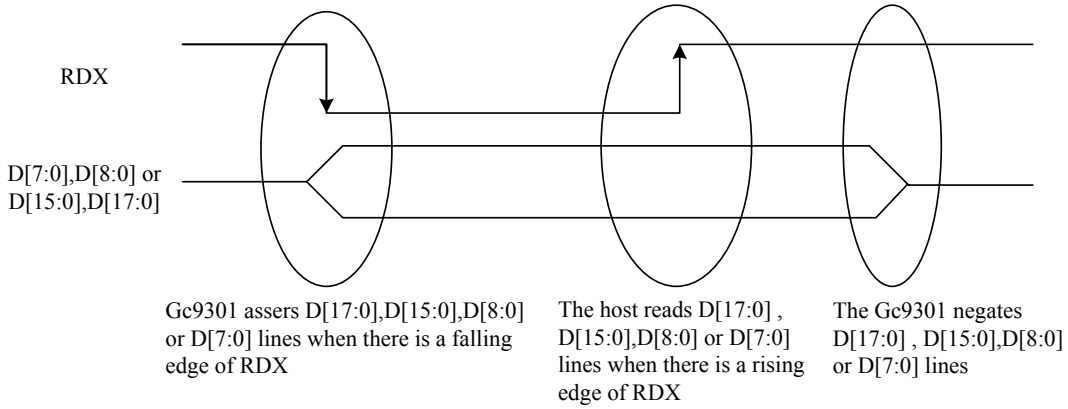
Note: WRX is an unsynchronized signal (It can be stopped)



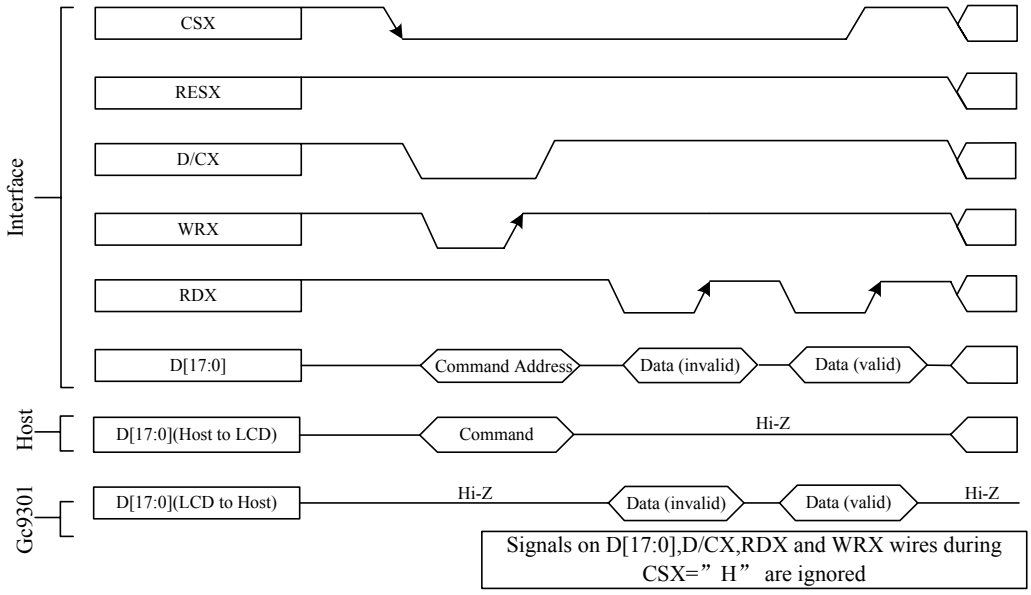
4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅰ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Series Parallel Interface

GC9301 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9301 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9301 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX=’1’, D [17:0] bits are display RAM data or command’s parameters. When D/CX=’0’, D[17:0] bits are commands.

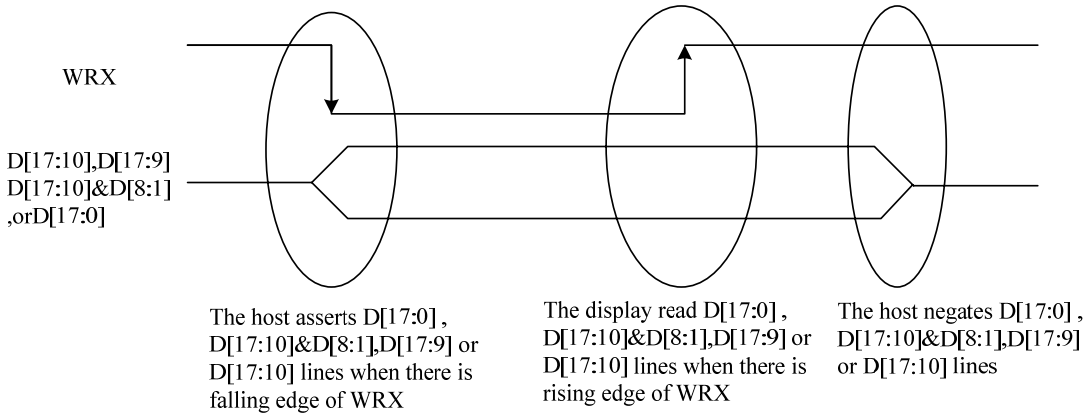
The 8080-Ⅱ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅱ Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.
The selection of 8080-Ⅱ series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface Ⅱ	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	0	1	8080 MCU 8-bit bus interface Ⅱ	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bit bus interface Ⅱ	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface Ⅱ	“L”	↑	“H”	“L”	Write command code.
					“L”	“H”	↑	“H”	Read internal status.
					“L”	↑	“H”	“H”	Write parameter or display data.
					“L”	“H”	↑	“H”	Reads parameter or display data.

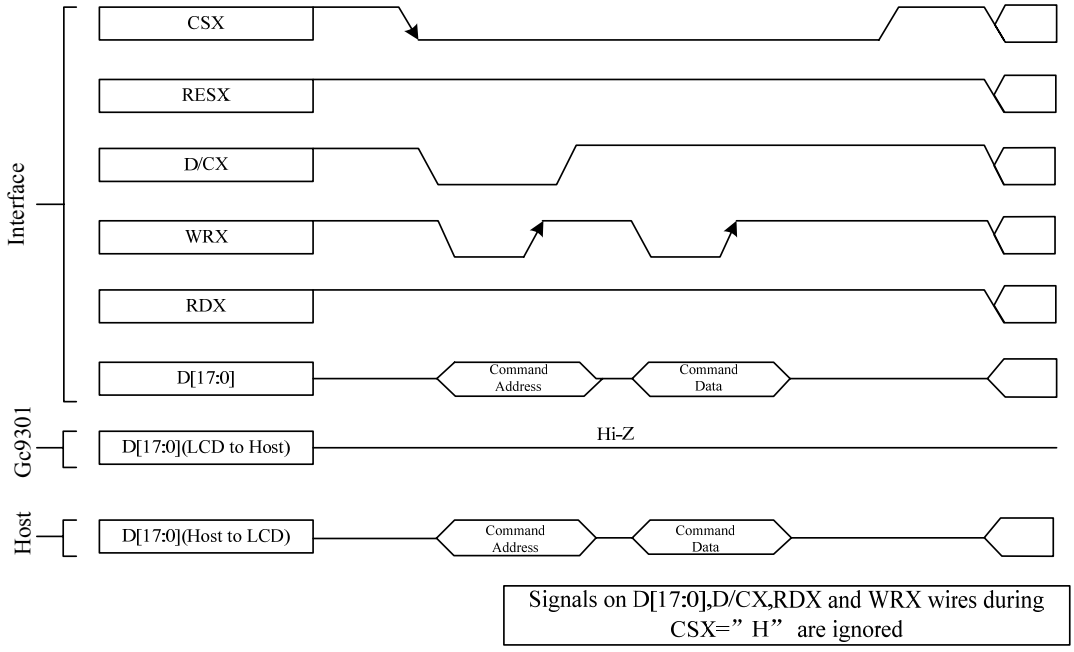
4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-Ⅱ MCU interface.



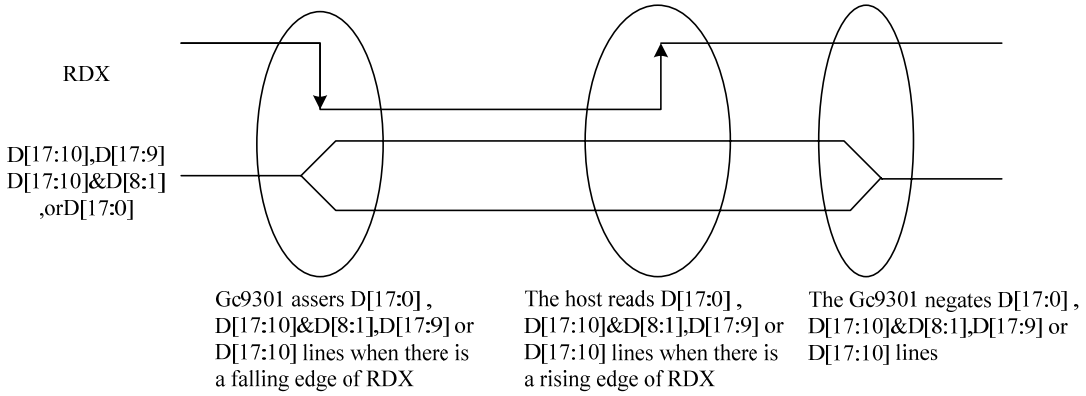
Note: WRX is an unsynchronized signal (It can be stopped)



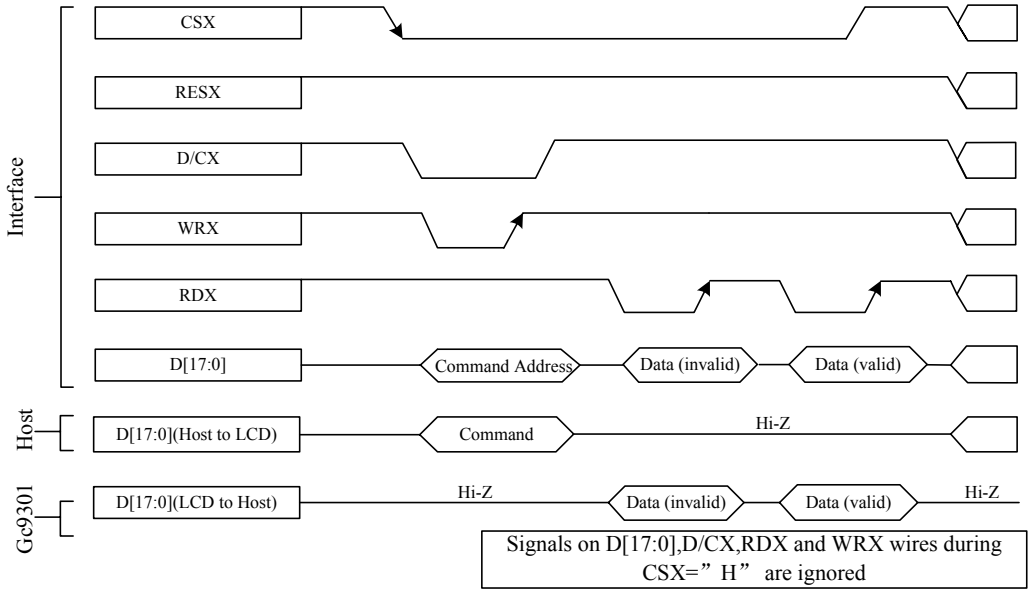
4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-Ⅱ MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	“L”	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	“L”	"H/L"		Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	“L”	-		Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	“L”	"H/L"		Read/Write command, parameter or display data.

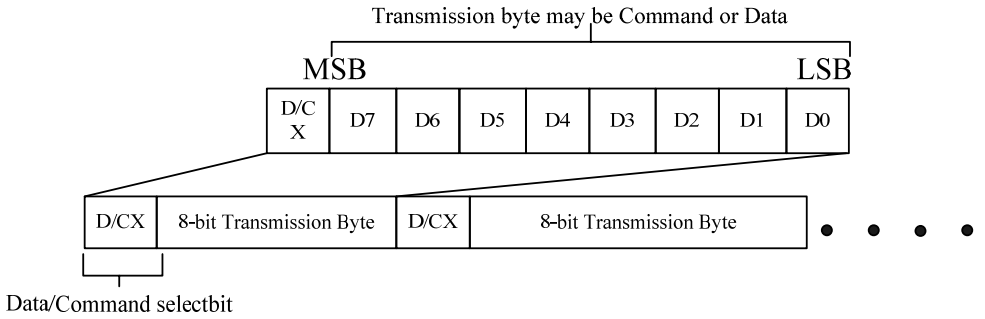
GC9301 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9301. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

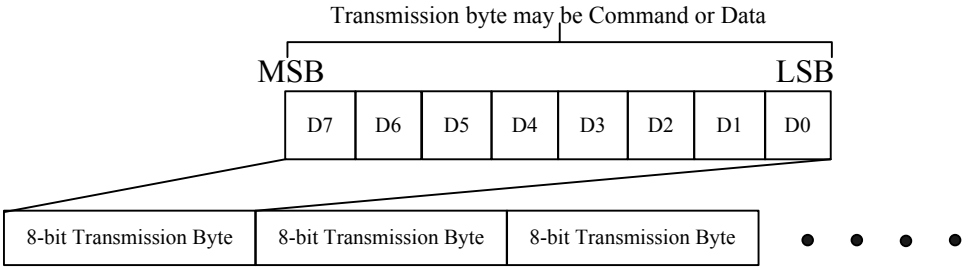
The write mode of the interface means that host writes commands or data to GC9301. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9301 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

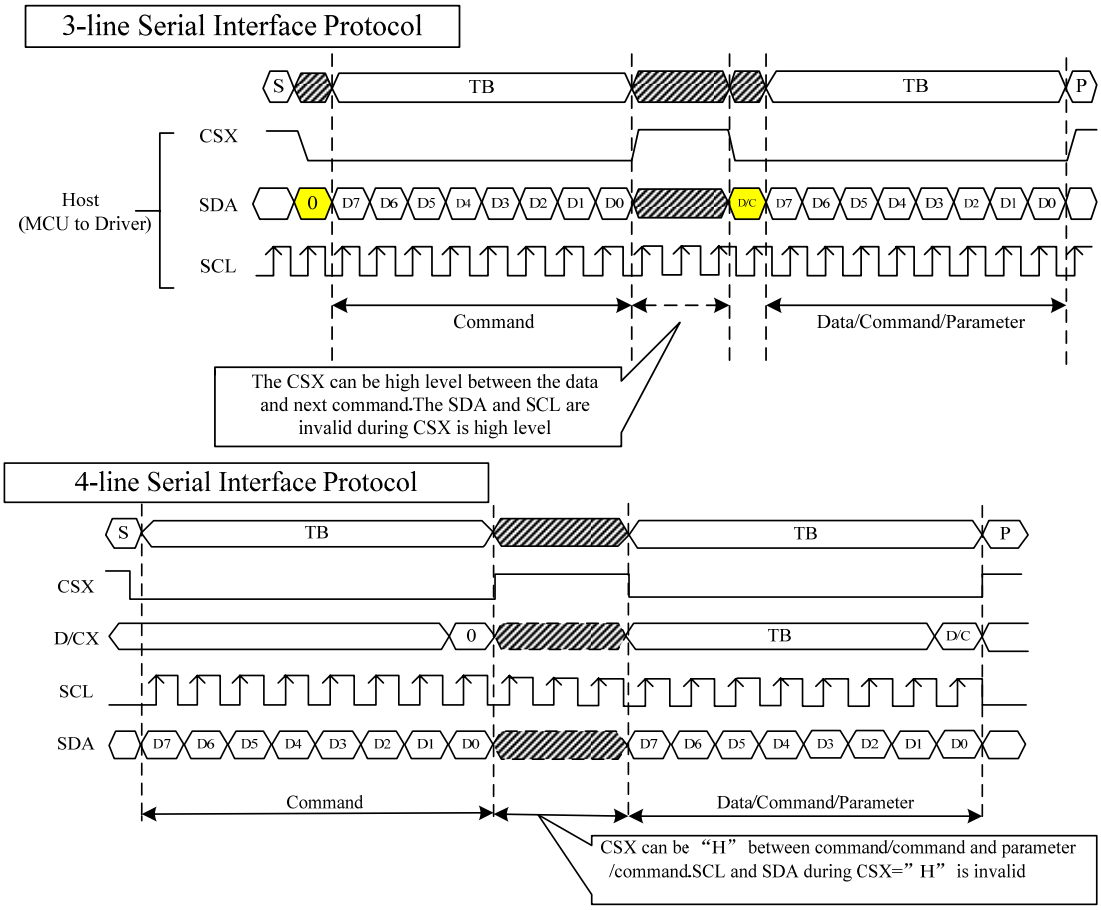
Data Format for 3-line Serial Interface



Data Format for 4-line Serial Interface



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9301 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

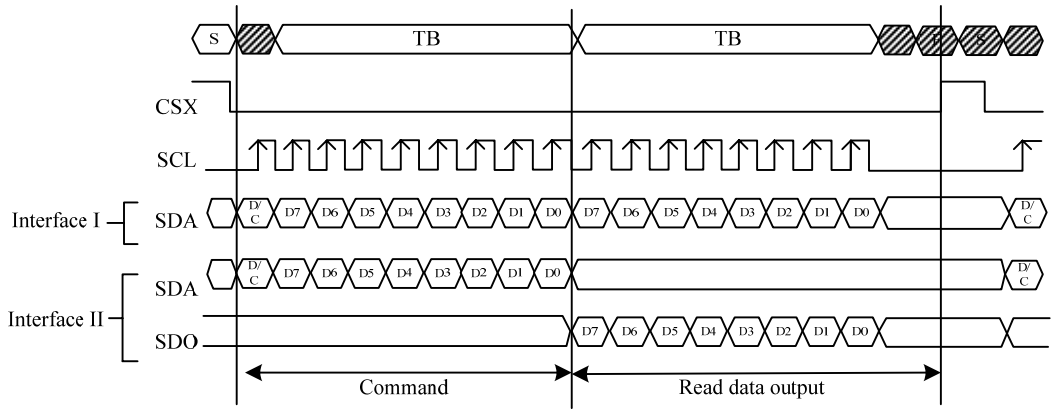


4.1.10. Read Cycle Sequence

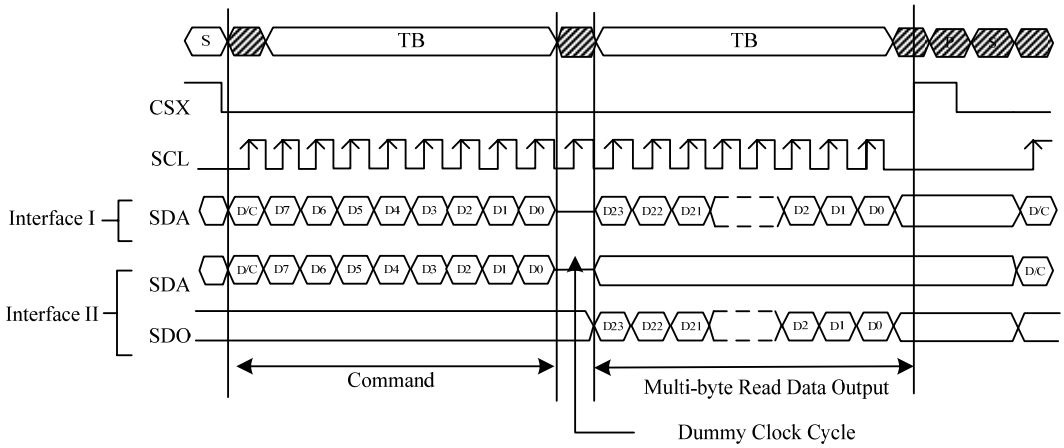
The read mode of interface means that the host reads register's parameter from GC9301. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9301 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol

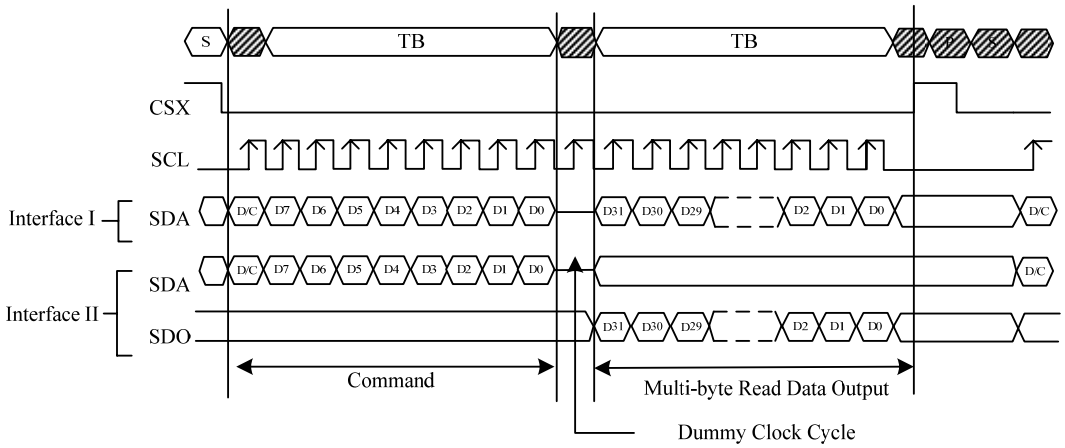
3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



3-wire Serial Protocol (for RDDID command:24-bit read)

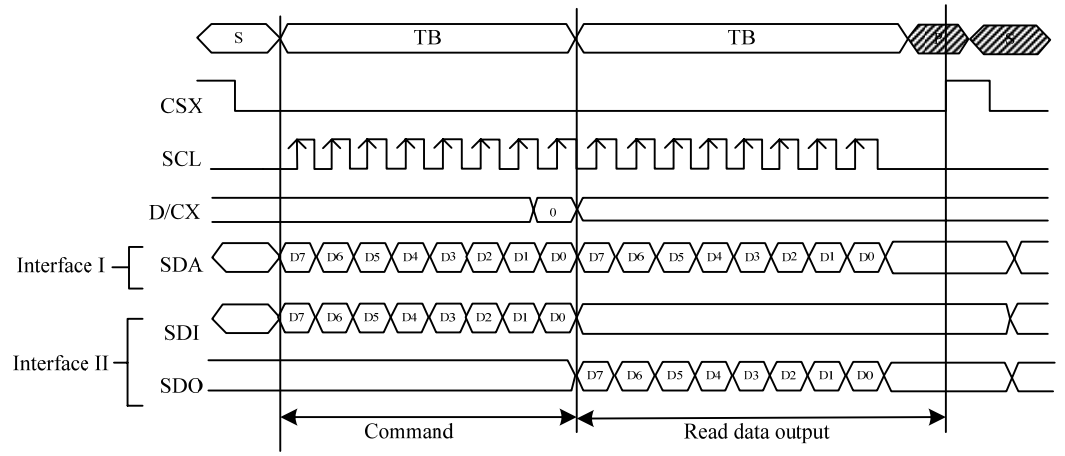


3-wire Serial Protocol (for RDDST command:32-bit read)

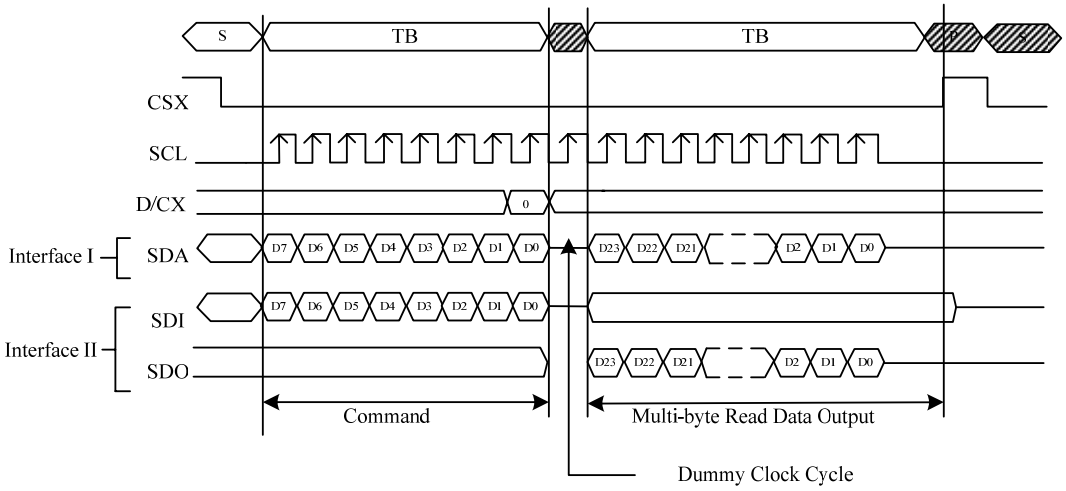


4-wire Serial Interface Protocol

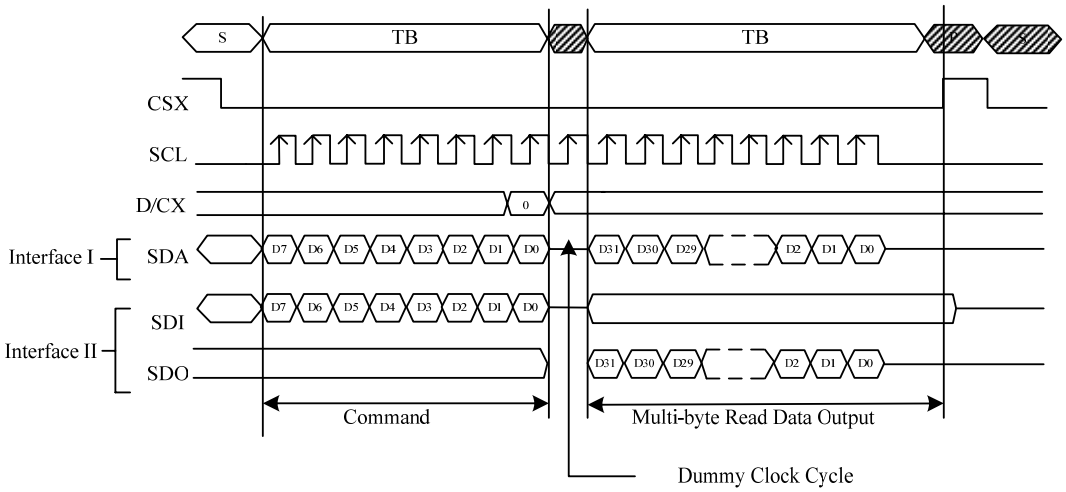
4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



4-wire Serial Protocol (for RDDID command:24-bit read)

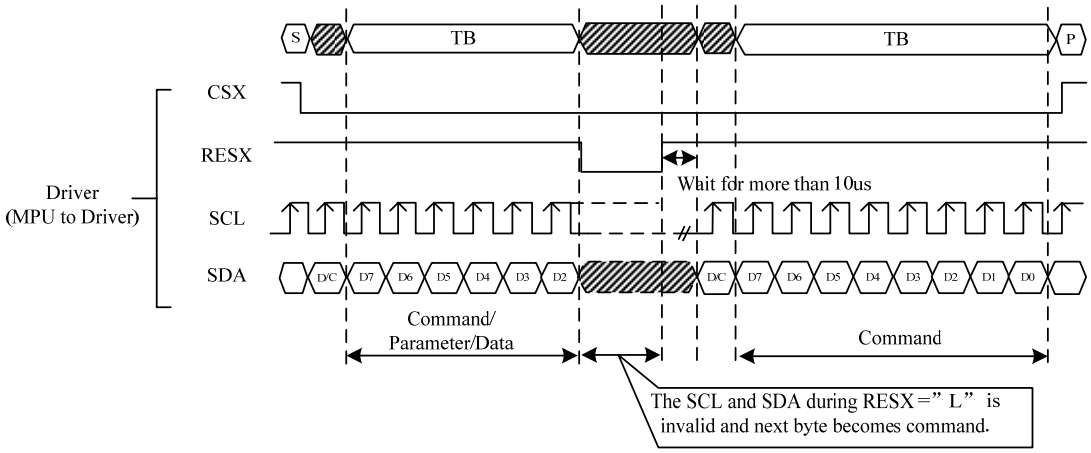


4-wire Serial Protocol (for RDDST command:32-bit read)

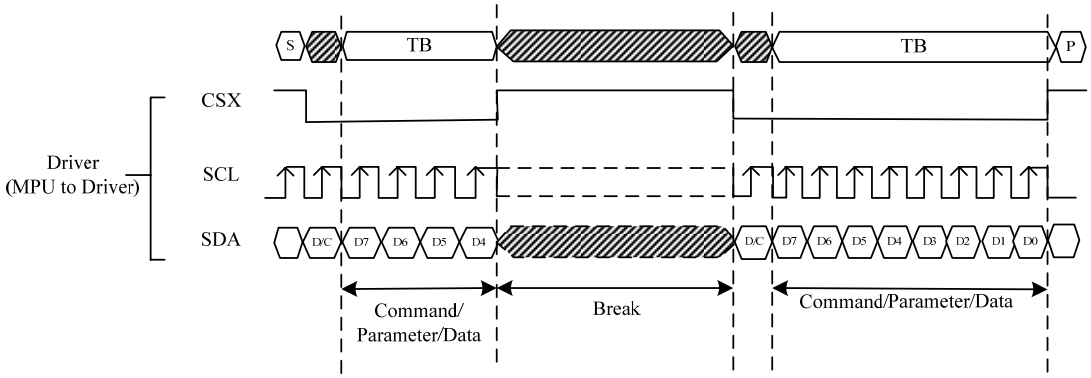


4.1.11. Data Transfer Break and Recovery

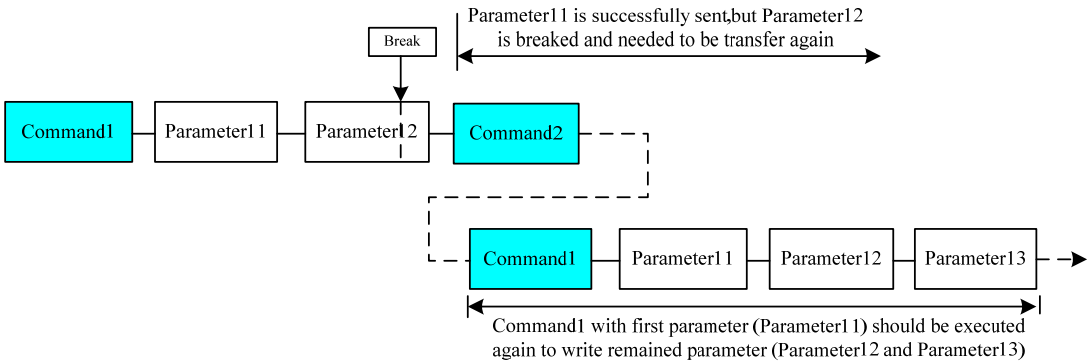
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



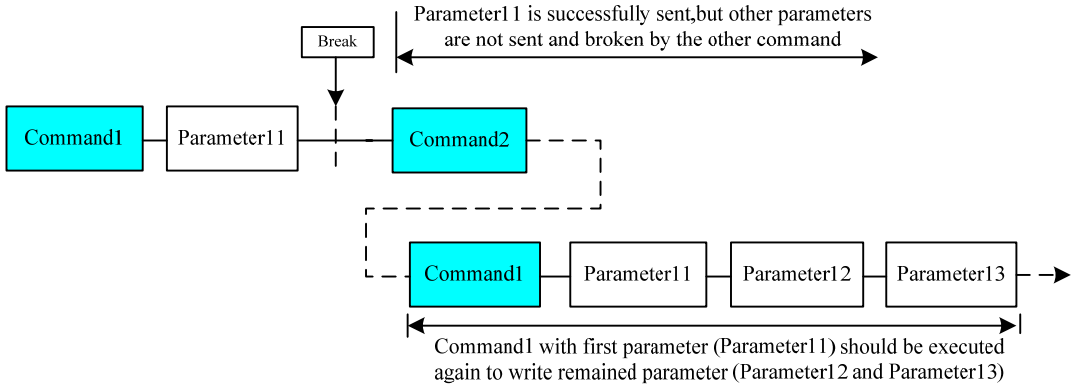
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



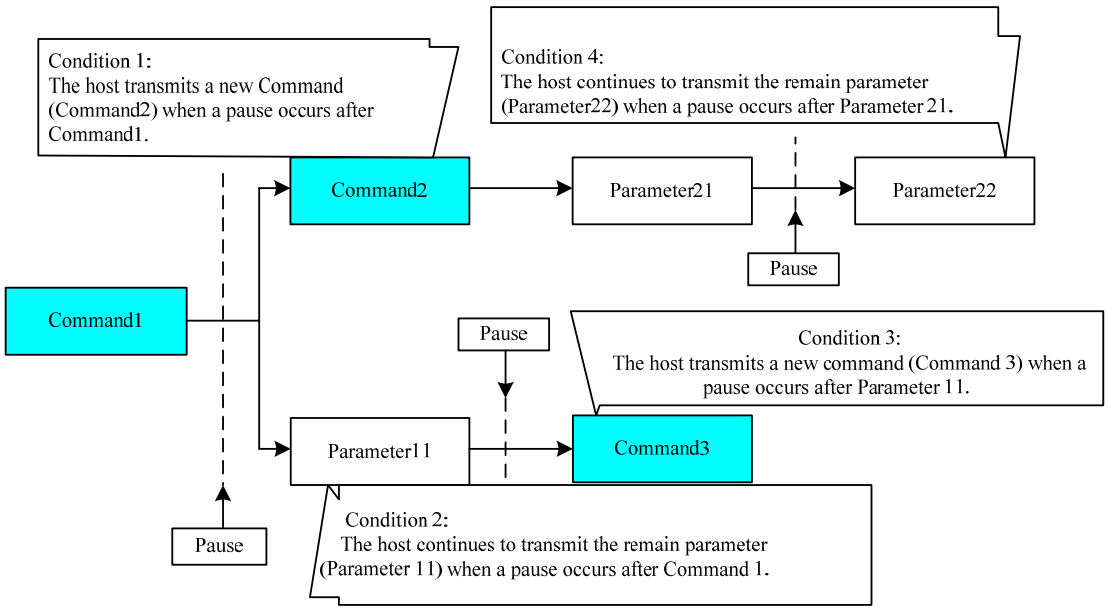
If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



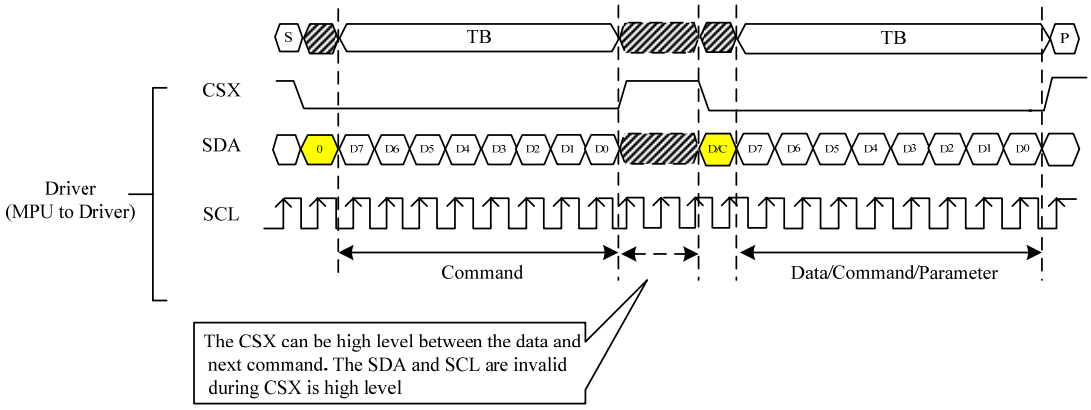
4.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9301 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

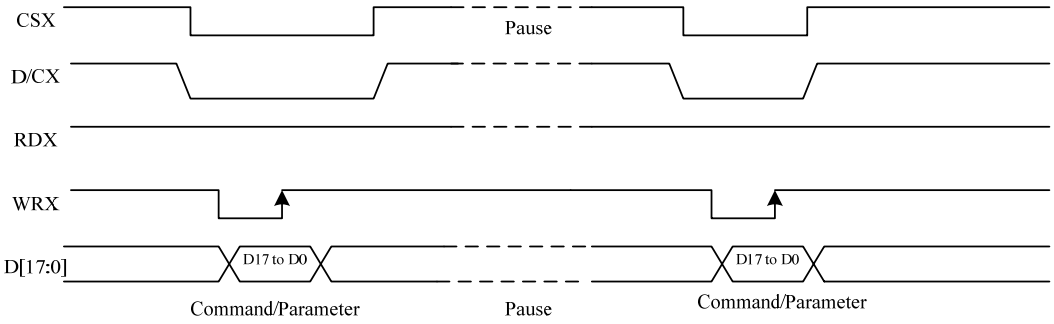
This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter



4.1.13. Serial Interface Pause (3_wire)



4.1.14 .Parallel Interface Pause

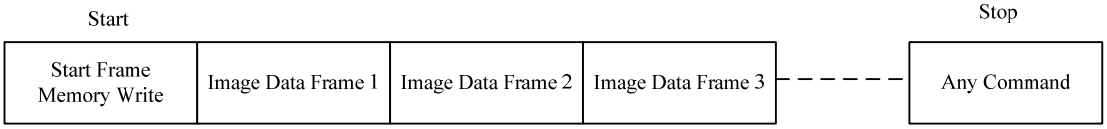


4.1.15 . Data Transfer Mode

GC9301 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

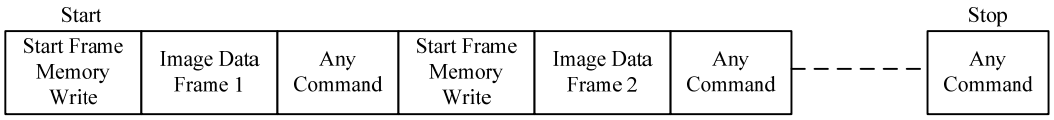
4.1.16 . Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



4.1.17 . Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. RGB Interface

4.2.1. RGB Interface Selection

GC9301 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC,DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.
GC9301 supports several pixel formats that can be selected by RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] as show in the following table.

RCM[1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE,DOTCLK, D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK, D[15:0]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK, D[5:0]
1	1	0	1	0	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode,DE signal is ignored;blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK,D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK,D[15:0]

18-bit data bus interface (D[17:0] is used) , RIM=0

	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[15:0] is used) , DPI[2:0] = 101, and RIM=0

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color are same as MSB data.

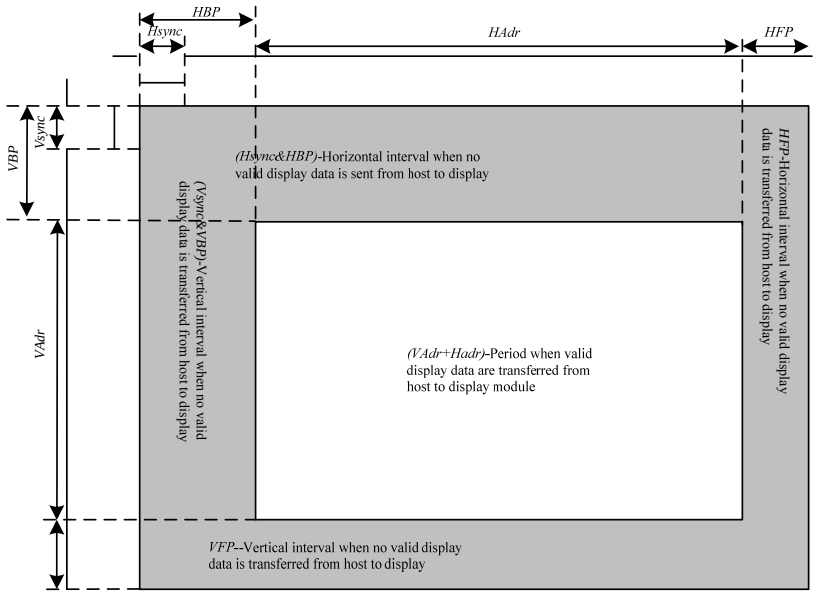
6-bit data bus interface (D[5:0] is used) , RIM=1

	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D[17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= ’0’ (low) and there is a rising edge of DOTCLK). D [17:0] can be ‘0’ (low) or ‘1’ (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Notes:

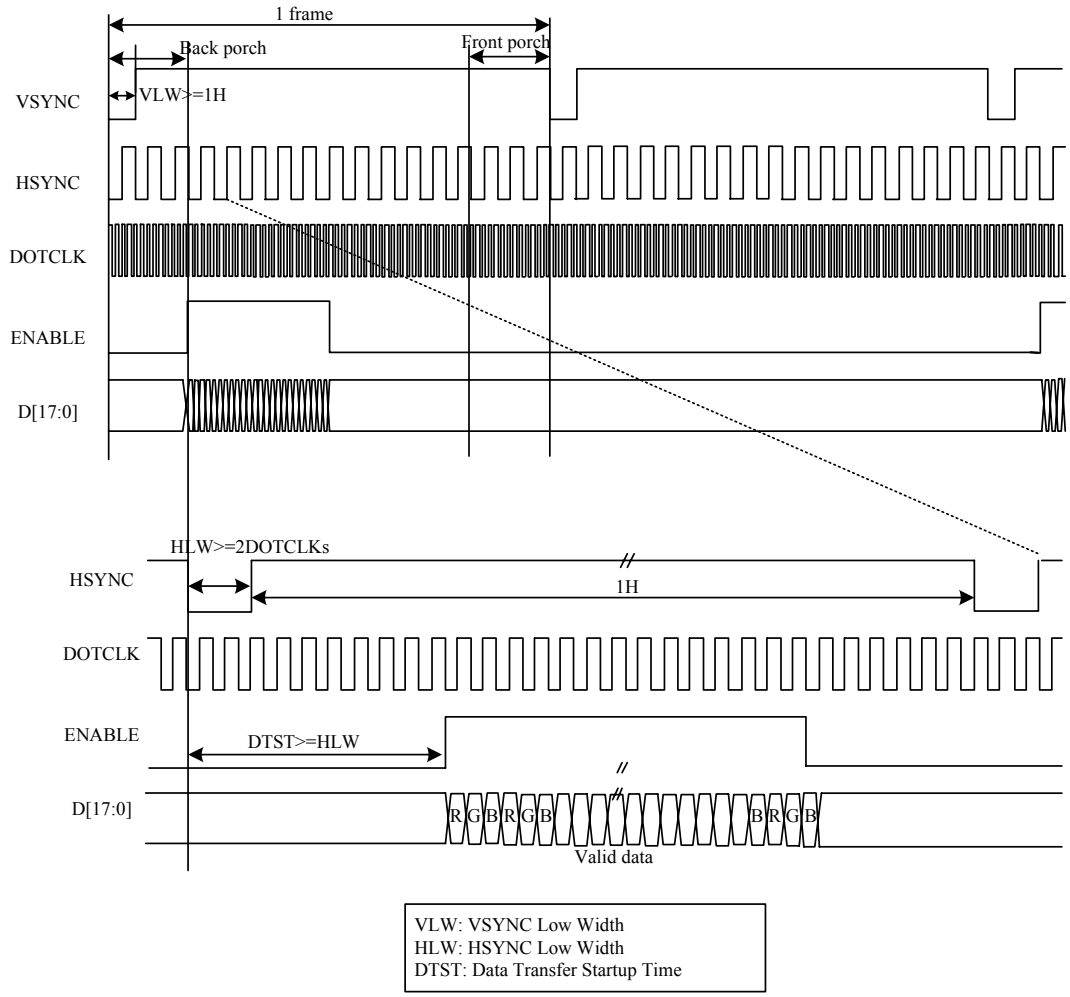
1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

4.2.2. RGB Interface Timing

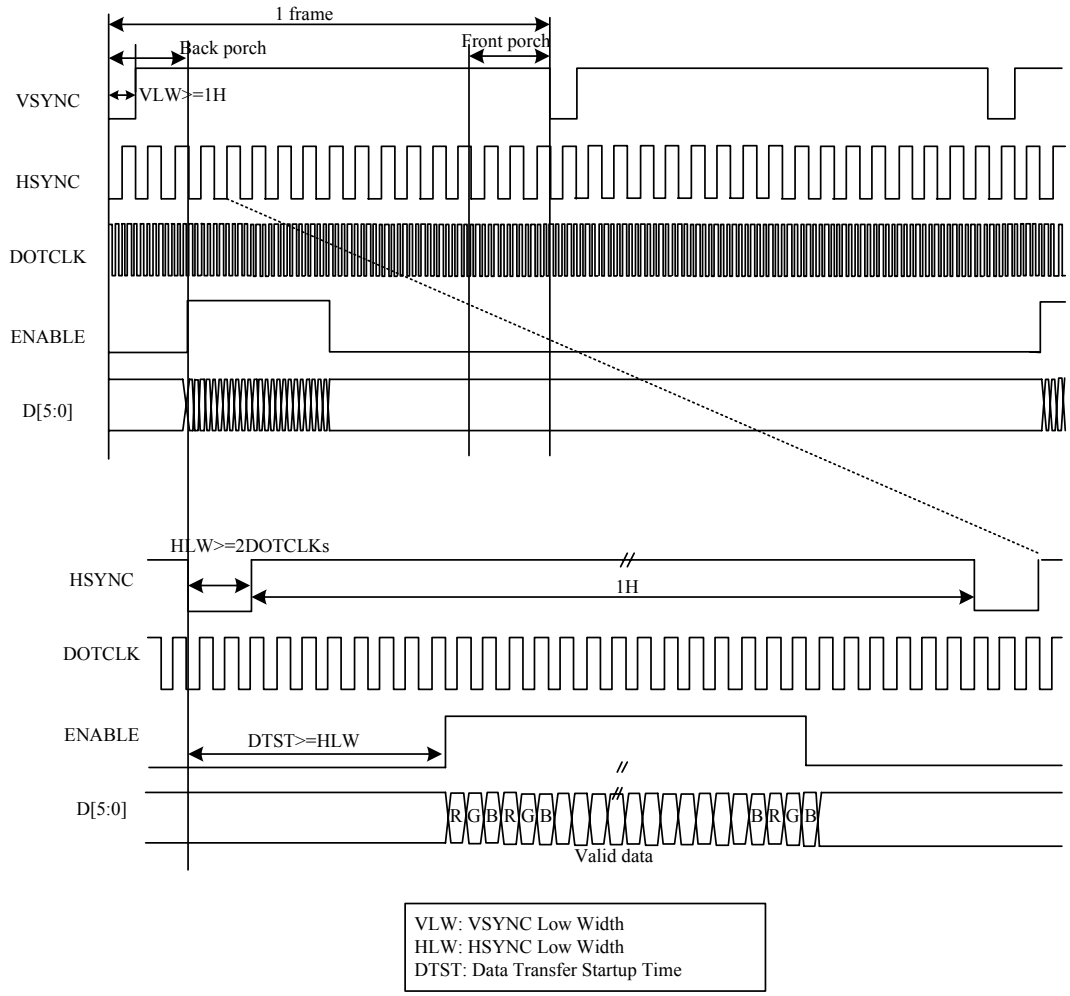
The timing chart of 18-/16-bit RGB interface mode is shown as below.



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



Note 1: 6-bit RGB interface mode only used in the DE interface.

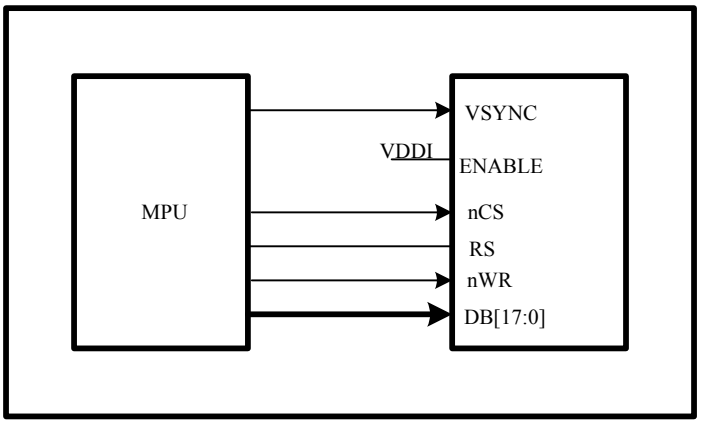
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

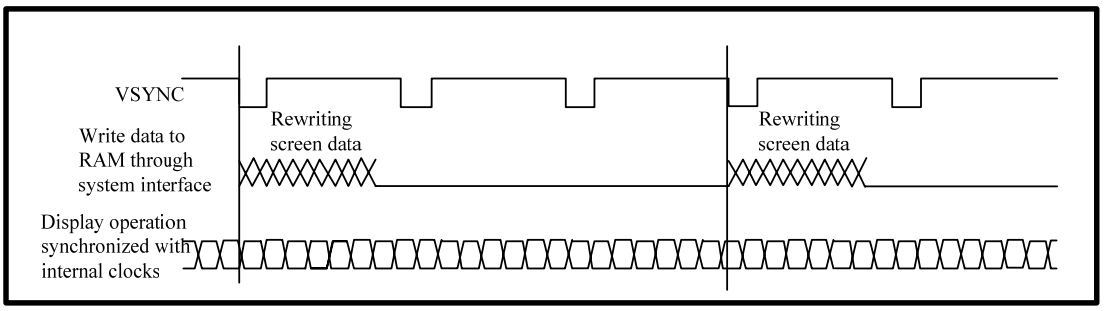
4.3. VSYNC Interface

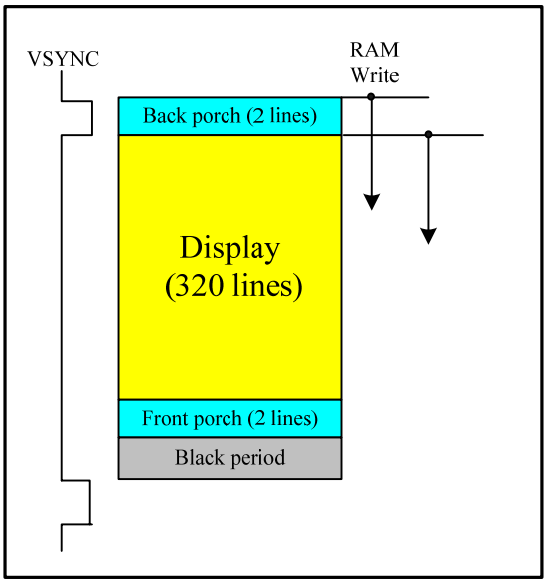
GC9301 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".



Note 1:In the VSYNC mode,the pin ENABLE should connect to VDDI.

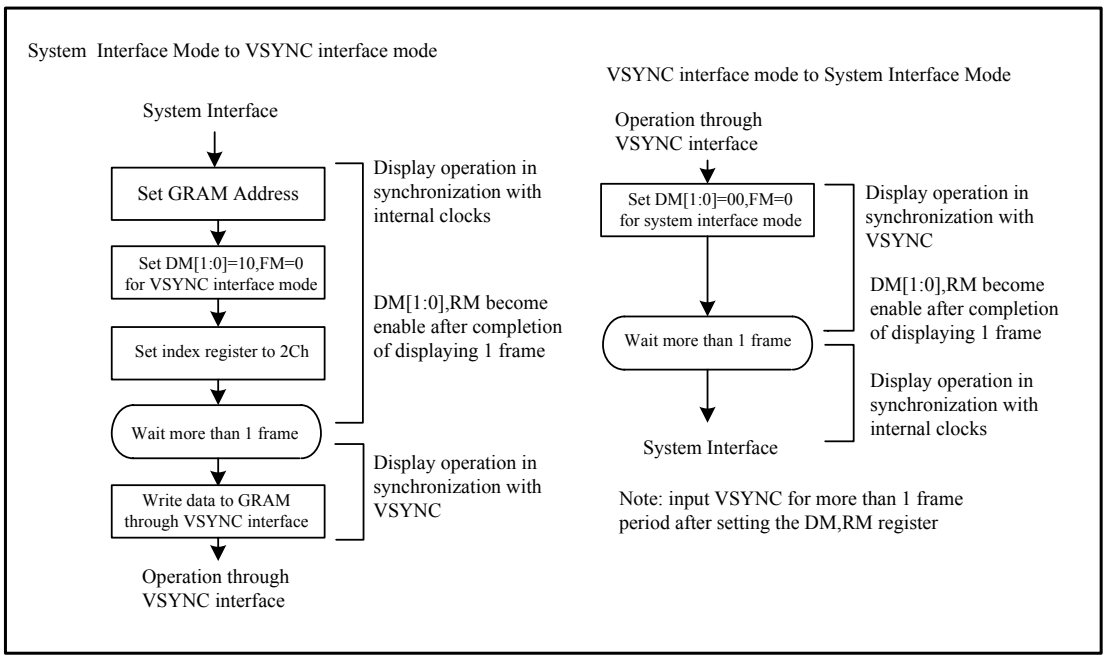
In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = "00") to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



4.4. Display Data RAM (DDRAM)

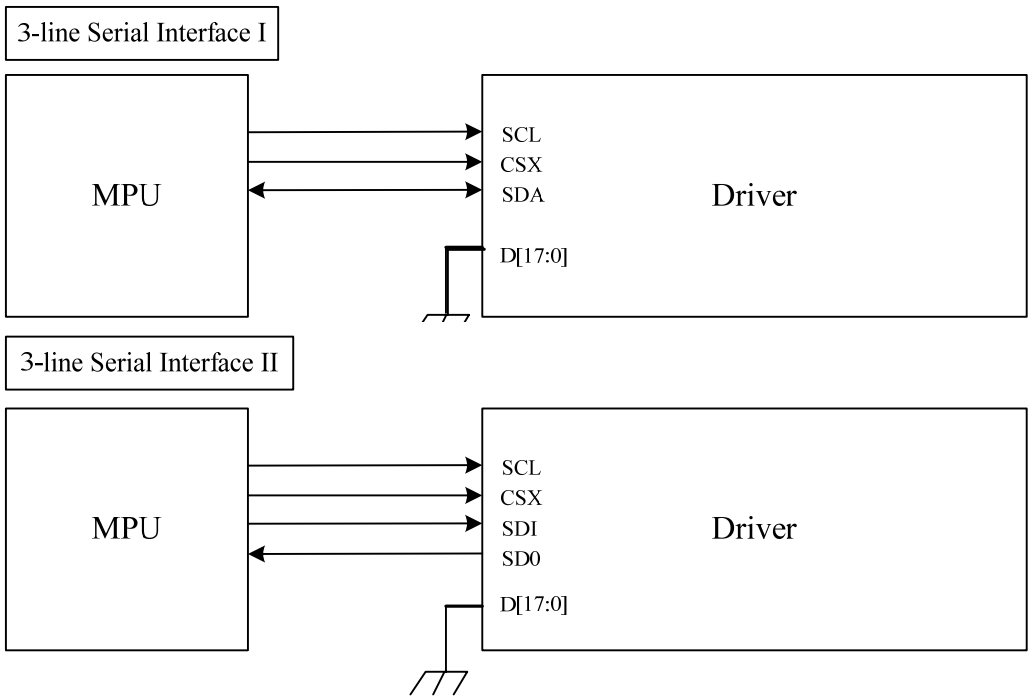
GC9301 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.5. Display Data Format

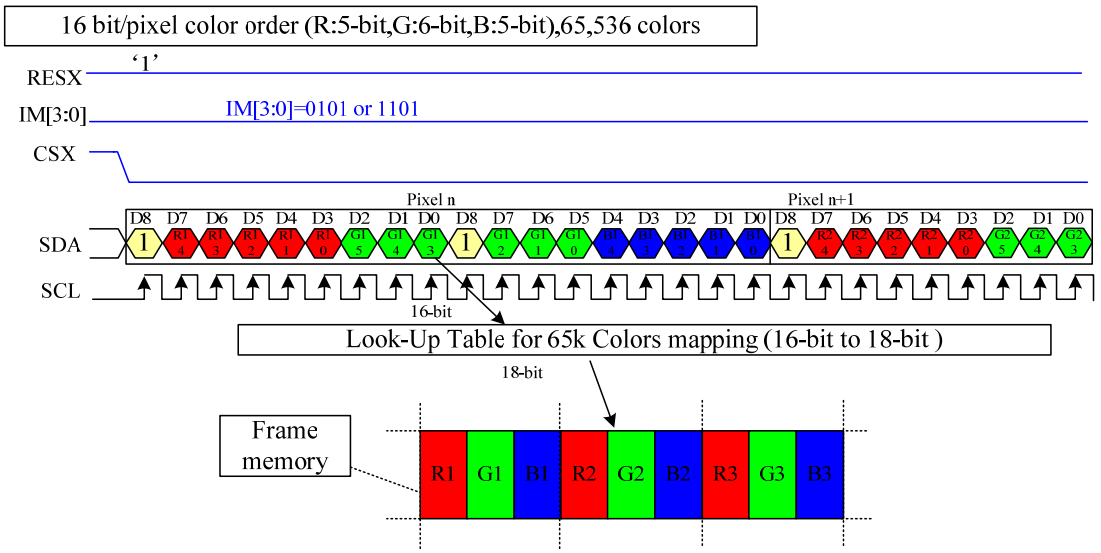
GC9301 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

4.5.1 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9301 can be used by setting external pin as IM [3:0] to "0101" for serial interface I or IM [3:0] to "1101" for serial interface II. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.
-65k colors, RGB 5, 6, 5 -bits input
-262k colors, RGB 6, 6, 6 -bits input.

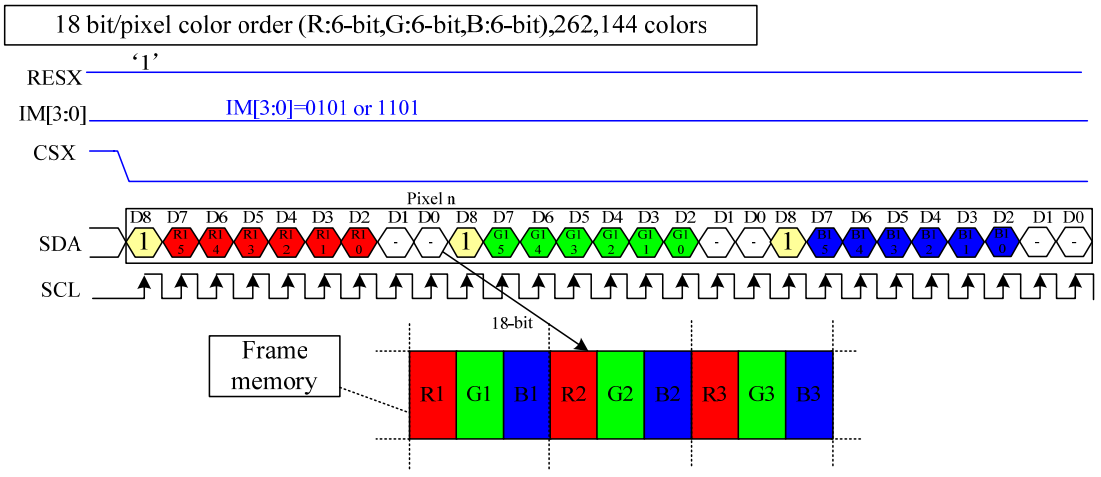


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.

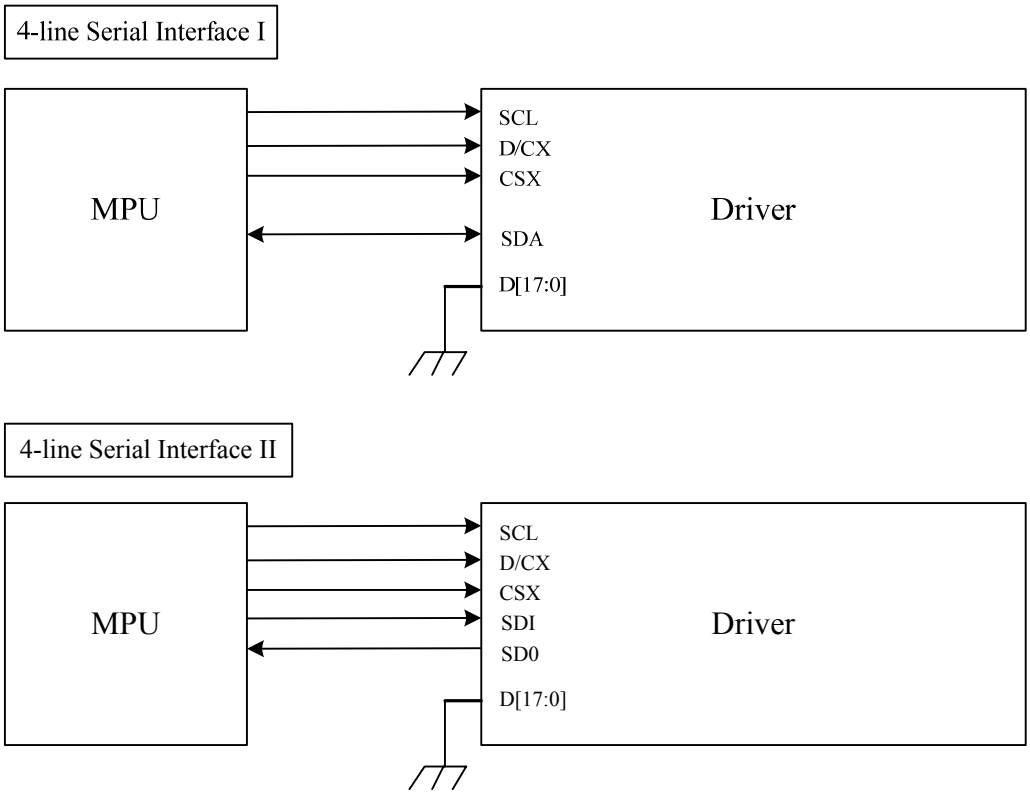
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

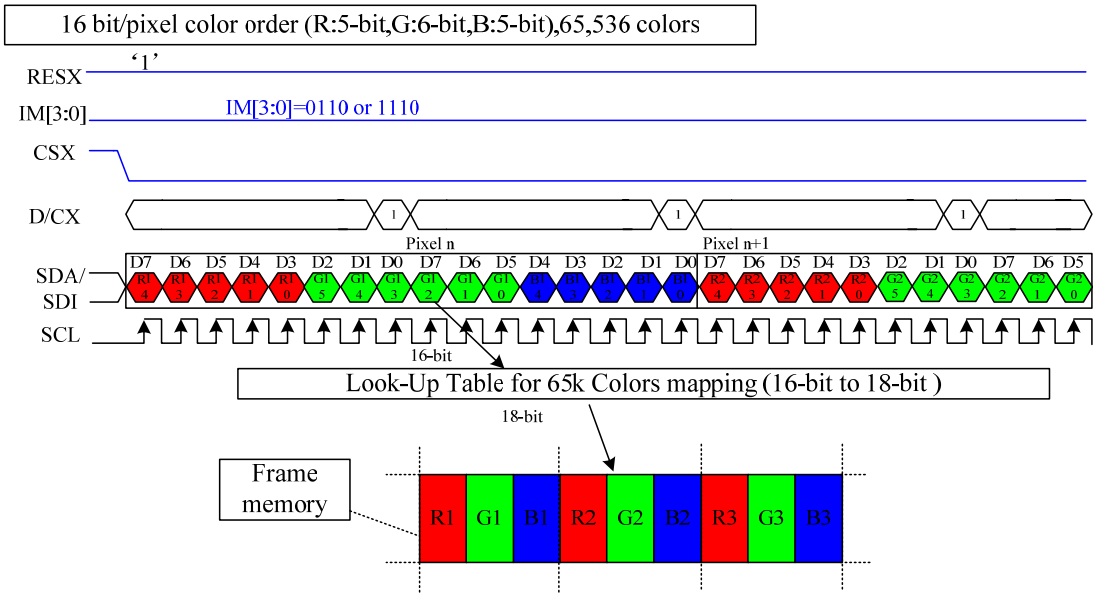
Note 4: '-'= Don't care - Can be set "0" or "1".

4.5.2 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9301 can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM
listed below.
-65k colors, RGB 5, 6, 5 -bits input.
-262k colors, RGB 6, 6, 6 -bits input.

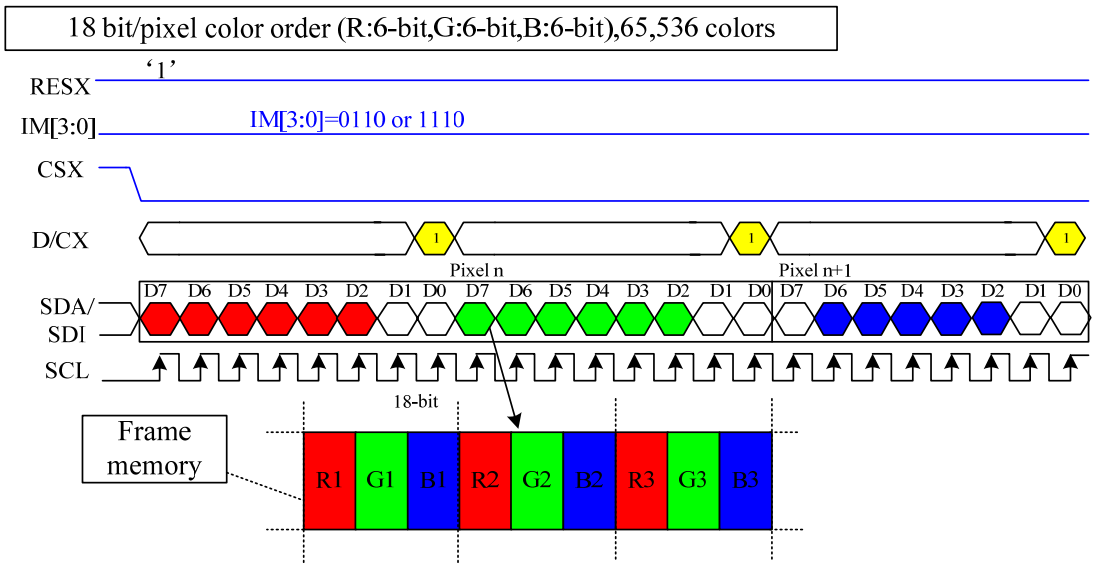


Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".



Note 1: The pixel data with 18-bit color depth information.

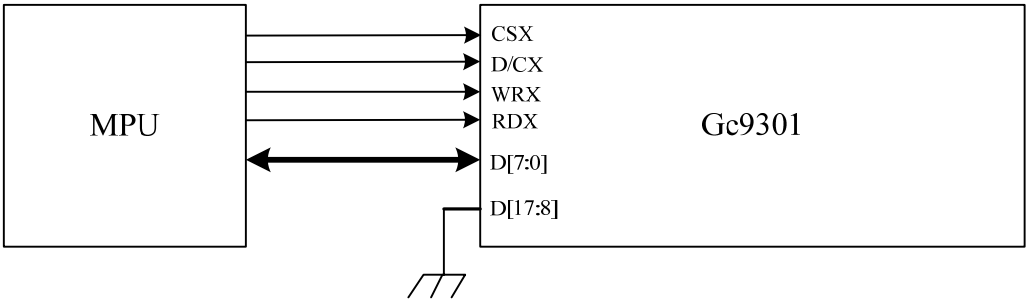
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

4.5.3. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of GC9301 can be used by setting external pin as IM [3:0] to"0000".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

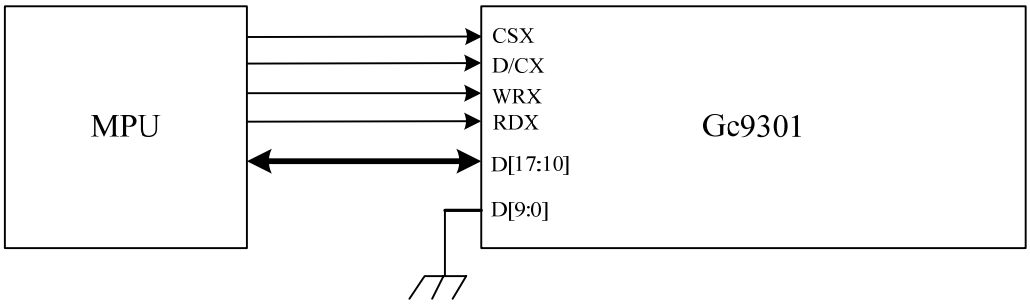
Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-Ⅱ system 8-bit parallel bus interface of GC9301 can be used by settings as IM [3:0] =”1001”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

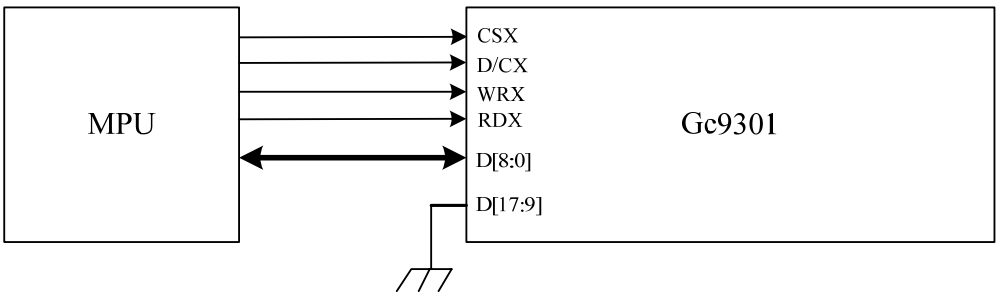
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

4.5.4. 9-bit Parallel MCU Interface

The 8080-Ⅰsystem 9-bit parallel bus interface of GC9301 can be selected by setting hardware pin IM [3:0] to “0010”. The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

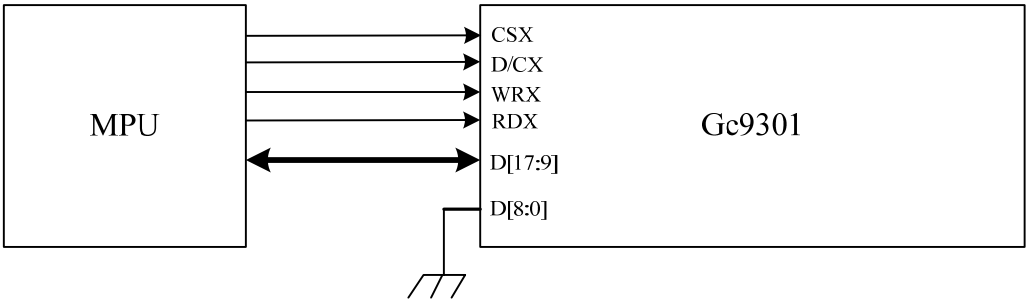


262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

The 8080- Ⅱ system 9-bit parallel bus interface of GC9301 can be selected by setting hardware pin IM [3:0] to “1011”. The following shown figure is the example of interface with 8080- MCU system interface.



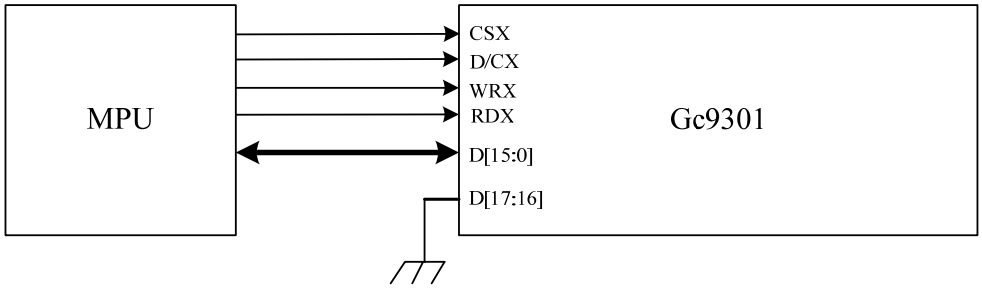
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

4.5.5. 16-bit Parallel MCU Interface

The 8080-Ⅰ system 16-bit parallel bus interface of GC9301 can be selected by setting hardware pin IM[3:0] to "0001".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for two colors depth supported by listed below.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah

register are set to “110”.

MDT[1:0]=” 00”

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1							
D0	C0							

MDT[1:0]=” 01”

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

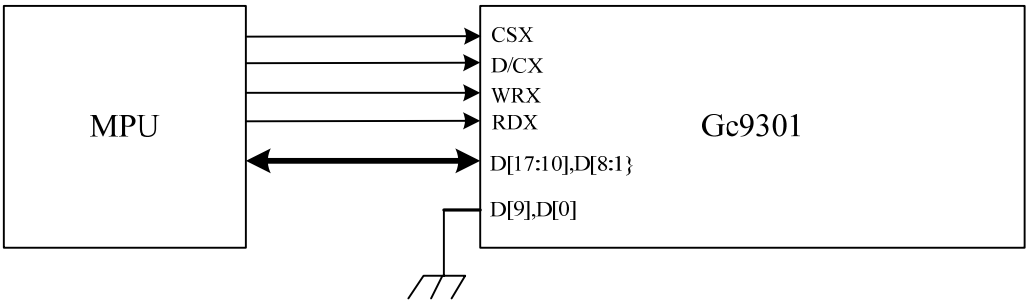
MDT[1:0]=" 10"

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=" 11"

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-Ⅱ system 16-bit parallel bus interface of GC9301 can be selected by settings IM [3:0] ="1000". The following shown figure is the example of interface with 8080-MCU system interface.



Different display data format is available for two colors depth supported by listed below.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0]=" 00"

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	0B5	1G5	…	238R5	238B5	239G5
D16		0R4	0B4	1G4	…	238R4	238B4	239G4
D15		0R3	0B3	1G3	…	238R3	238B3	239G3
D14		0R2	0B2	1G2	…	238R2	238B2	239G2
D13		0R1	0B1	1G1	…	238R1	238B1	239G1
D12		0R0	0B0	1G0	…	238R0	238B0	239G0
D11								
D10								
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D2	C1							
D1	C0							

MDT[1:0]=" 01"

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

MDT[1:0]=" 10"

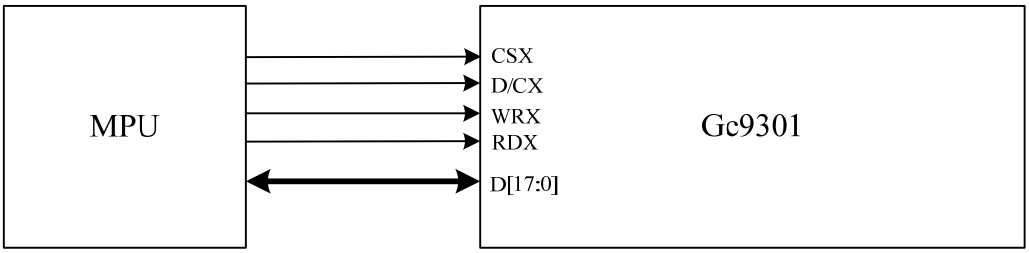
Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

MDT[1:0]=" 11"

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

4.5.6. 18-bit Parallel MCU Interface

The 8080-Ⅰ system 18-bit parallel bus interface of GC9301 can be selected by setting hardware pin IM[3:0] to "0011".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

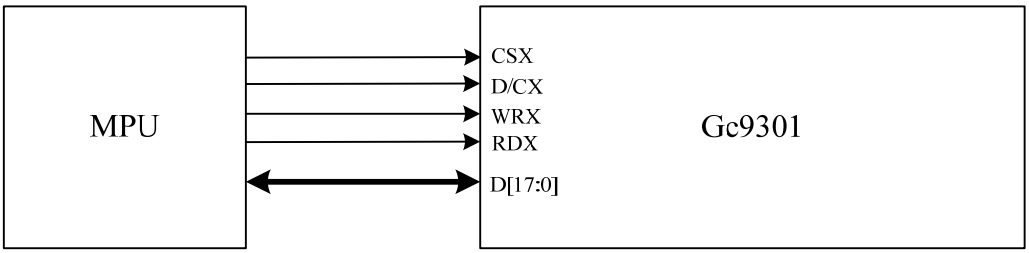
Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-Ⅱ system 18-bit parallel bus interface mode can be selected by settings IM [3:0] =”1010”. The following shown figure is the example of interface with 8080- MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

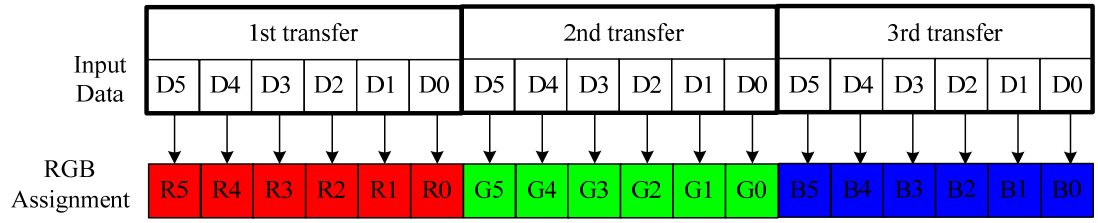
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

4.5.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the RIM bit to “1”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

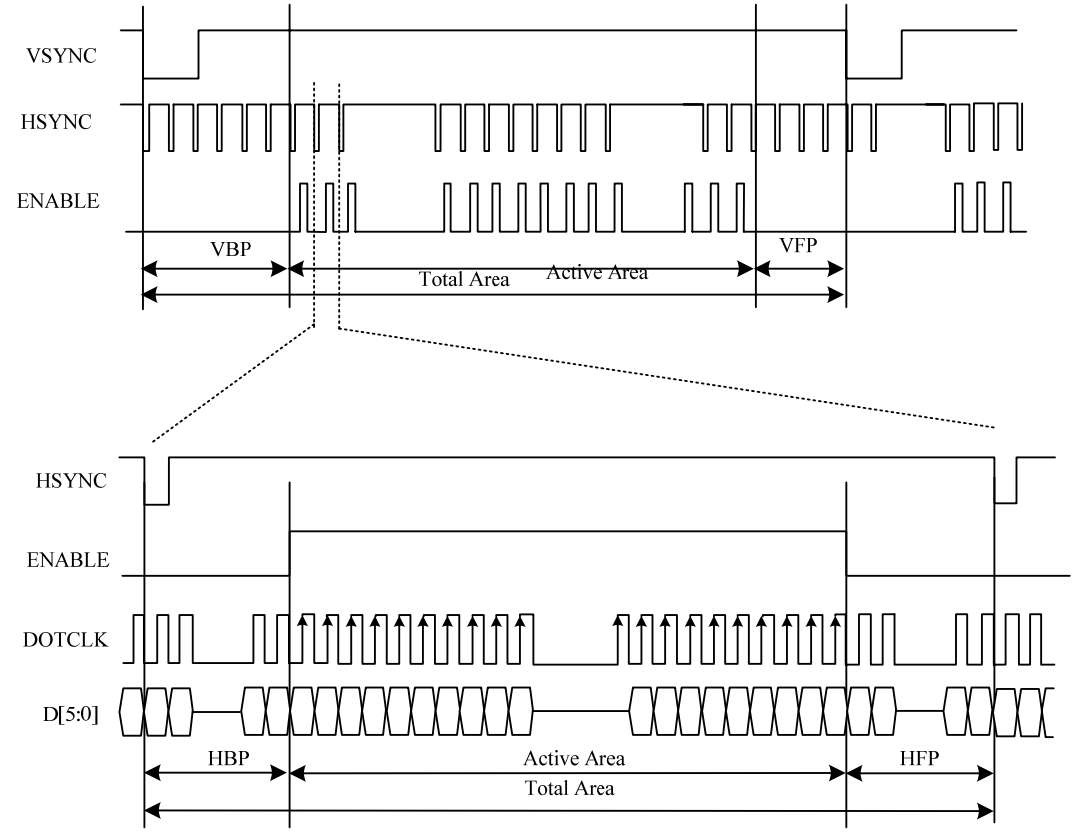
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



GC9301 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

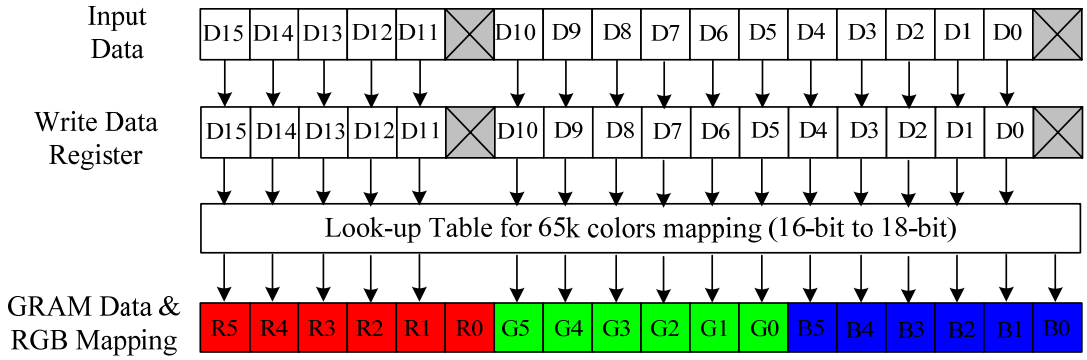
Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK).Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode.RCM[1:0]=” 10”



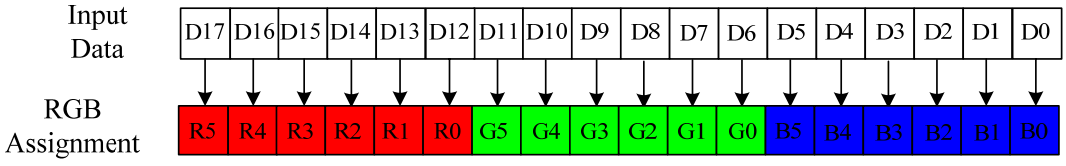
4.5.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [15:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [15:0] according to the VFP/VBP and HFP/HBP settings. The unused D16 and D17 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



4.5.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



5. Function Description

5.1 Display data GRAM mapping

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

GRAM address for display panel position as shown in the following table

(00,00)h	(00,01)h	…… …	(00,ED)h	(00,EE)h	(00,EF)h
(01,00)h	(01,01)h	…… …	(01,ED)h	(01,EE)h	(01,EF)h
(02,00)h	(02,01)h	…… …	(02,ED)h	(02,EE)h	(02,EF)h
(03,00)h	(03,01)h	…… …	(03,ED)h	(03,EE)h	(03,EF)h
. . .	. . .	. . .	. . .	. . .	. . .
(13D,00)h	(13D,01)h	…… …	(13D,ED)h	(13D,EE)h	(13D,EF)h
(13E,00)h	(13E,01)h	…… …	(13E,ED)h	(13E,EE)h	(13E,EF)h
(13F,00)h	(13F,01)h	…… …	(13F,ED)h	(13F,EE)h	(13F,EF)h

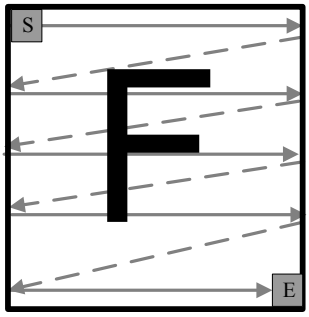
5.2 Address Counter (AC) of GRAM

The GC9301 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being

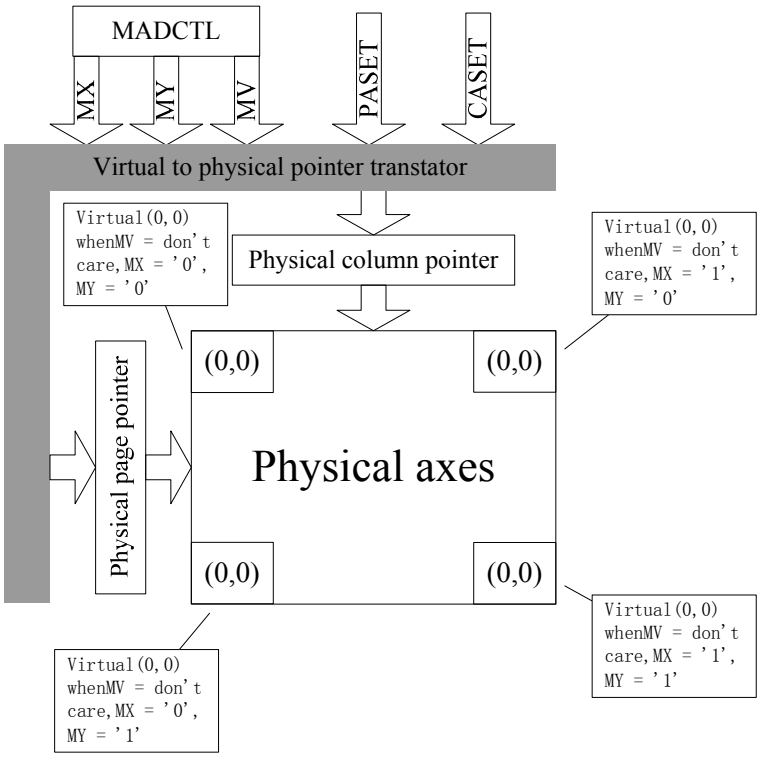
written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

Image data sending order from host and data stream update as shown in the following figure



The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

Image data writing control:

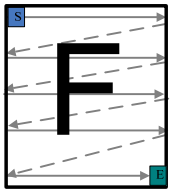
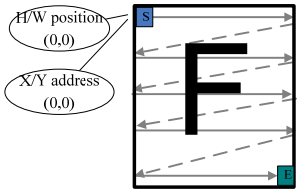
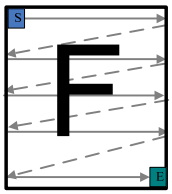
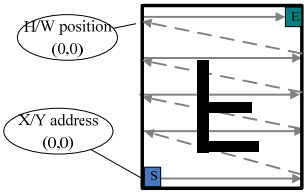
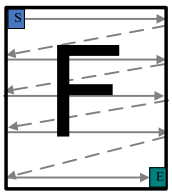
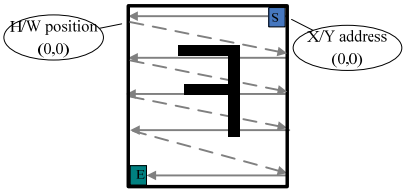
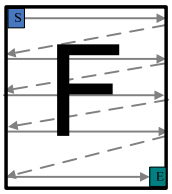
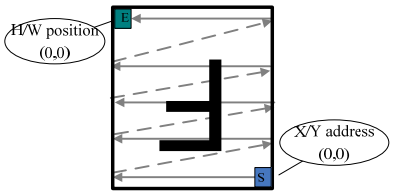
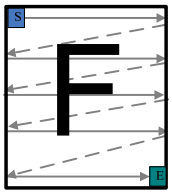
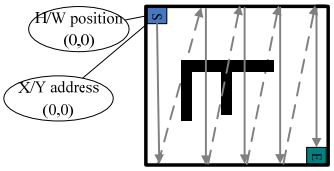
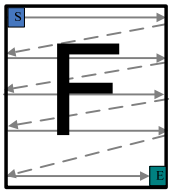
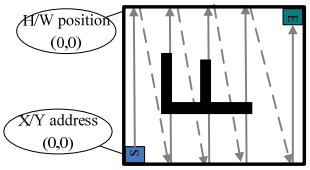
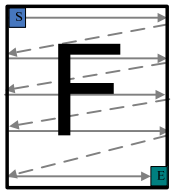
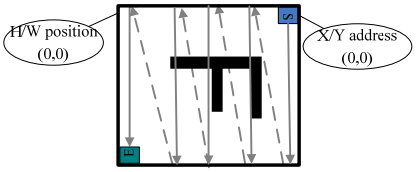
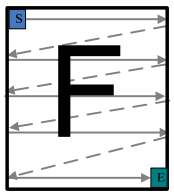
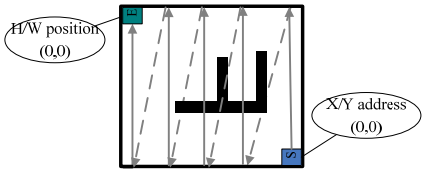


CASET and PASET control for physical column/page pointers:

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319 - Physical Page Pointer)
0	1	0	Direct to (239 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239 - Physical Column Pointer)	Direct to (319 - Physical Page Pointer)
0	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
0	0	1	Direct to (319 - Physical Page Pointer)	Direct to Physical Column Pointer
0	1	0	Direct to Physical Page Pointer	Direct to (239 - Physical Column Pointer)
0	1	1	Direct to (319 - Physical Page Pointer)	Direct to (239 - Physical Column Pointer)

condition	**Column Counter**	**Page Counter**
When RAMWR/RAMRD command is accepted	Return to “Start Column”	Return to “Start Page”
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than “End column.”	Return to “Start Column”	Increment by 1
The Page counter value is larger than “End page”.	Return to “Start column”	Return to “Start Page”

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Display data direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
normal	0	0	0		
Y-invert	0	0	1		
X-ivert	0	1	0		
Y-invert X-invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-invert	1	0	1		
X-Y exchange X-invert	1	1	0		
X-Y exchange Y-invert X-invert	1	1	1		

5.3 GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement.
The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

BGR="0"														
Source	**SS="0"**	S1	S2	S3	S4	S5	S6	------	S715	S716	S717	S718	S719	S720
Output	**SS="1"**	S718	S719	S720	S715	S716	S717	------	S4	S5	S6	S1	S2	S3
GRAM X address		"00"h			"01"h			------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	------	R	G	B	R	G	B
Pixel		Pixel1			Pixel2			------	Pixel239			Pixel240		
BGR="1"														
Source	**SS="0"**	S3	S2	S1	S6	S5	S4	------	S717	S716	S715	S720	S719	S718
Output	**SS="1"**	S720	S719	S718	S717	S716	S715	------	S6	S5	S4	S3	S2	S1
GRAM X address		"00"h			"01"h			------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	------	R	G	B	R	G	B
Pixel		Pixel1			Pixel2			------	Pixel239			Pixel240		

GRAM address and display panel position (GS_Panel =’0’):

S/G pins	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**S9**	**----**	**S712**	**S713**	**S714**	**S715**	**S716**	**S717**	**S718**	**S719**	**S720**
G1	0000h			0001h			0002h			----	00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			----	01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			----	02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			----	03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			----	04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			----	05EDh			05EEh			05EFh		
⋮	⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G315	13A00h			13A01h			13A02h			----	13AEDh			13AEEh			13AEFh		
G316	13B00h			13B01h			13B02h			----	13BEDh			13BEEh			13BEFh		
G317	13C00h			13C01h			13C02h			----	13CEDh			13CEEh			13CEFh		
G318	13D00h			13D01h			13D02h			----	13DEDh			13DEEh			13DEFh		
G319	13E00h			13E01h			13E02h			----	13EEDh			13EEEh			13EEFh		
G320	13F00h			13F01h			13F02h			----	13FEDh			13FEEh			13FEFh		

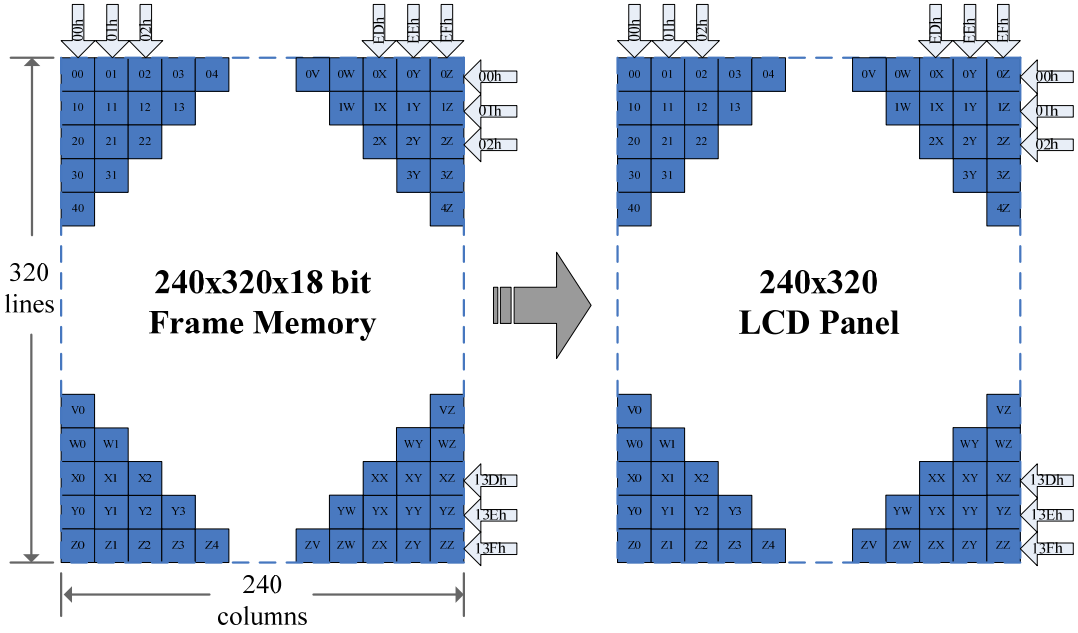
GRAM address and display panel position (GS_Panel =’1’):

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	----	S712	S713	S714	S715	S716	S717	S718	S719	S720
G320	0000h			0001h			0002h			----	00EDh			00EEh			00EFh		
G319	0100h			0101h			0102h			----	01EDh			01EEh			01EFh		
G318	0200h			0201h			0202h			----	02EDh			02EEh			02EFh		
G317	0300h			0301h			0302h			----	03EDh			03EEh			03EFh		
G316	0400h			0401h			0402h			----	04EDh			04EEh			04EFh		
G315	0500h			0501h			0502h			----	05EDh			05EEh			05EFh		
⋮	⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G6	13A00h			13A01h			13A02h			----	13AEDh			13AEEh			13AEFh		
G5	13B00h			13B01h			13B02h			----	13BEDh			13BEEh			13BEFh		
G4	13C00h			13C01h			13C02h			----	13CEDh			13CEEh			13CEFh		
G3	13D00h			13D01h			13D02h			----	13DEDh			13DEEh			13DEFh		
G2	13E00h			13E01h			13E02h			----	13EEDh			13EEEh			13EEFh		
G1	13F00h			13F01h			13F02h			----	13FEDh			13FEEh			13FEFh		

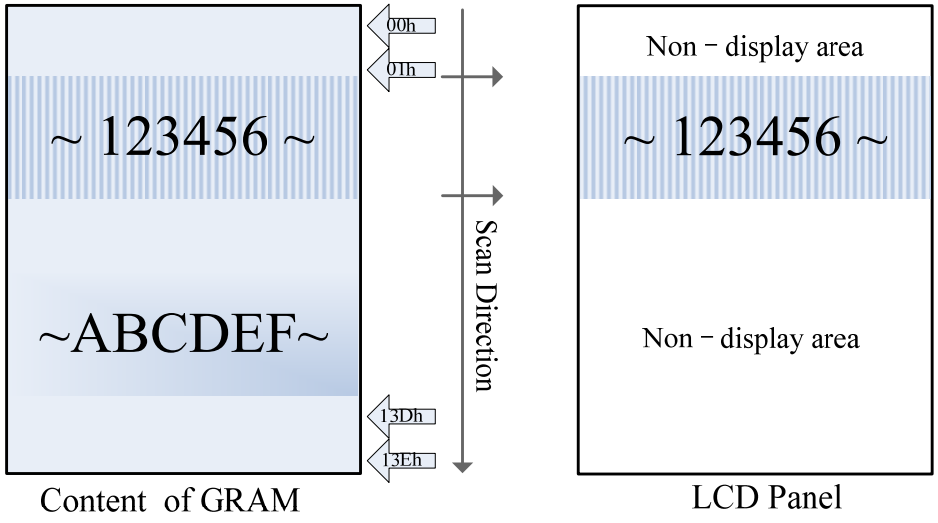
GC9301 supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

5.3.1 Normal display on or partial mode on, vertical scroll off

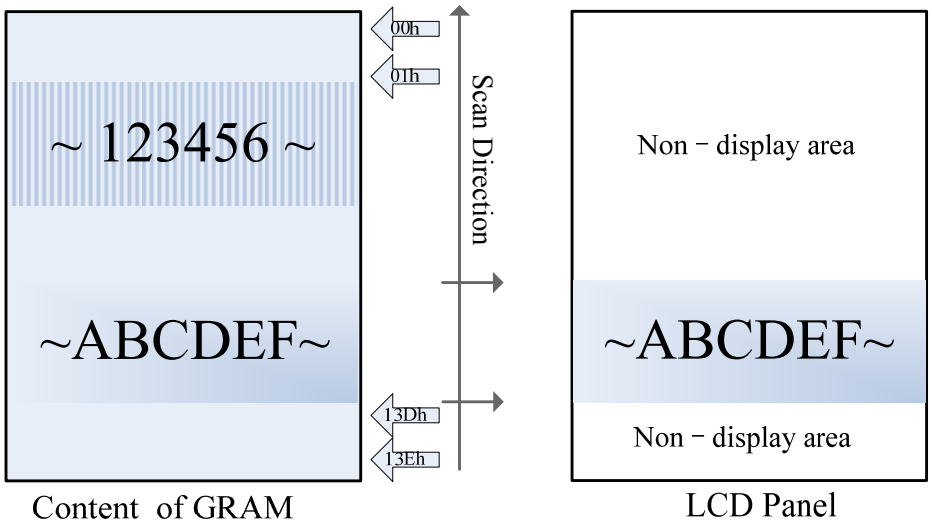
In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer)
= (0,0)



Example1:
(1) partial mode on (setting 12h)
(2) SR [15:0] =50DEC, ER [15:0] =150DEC, MADCTL's **B4(ML)='0'** (GS='0').

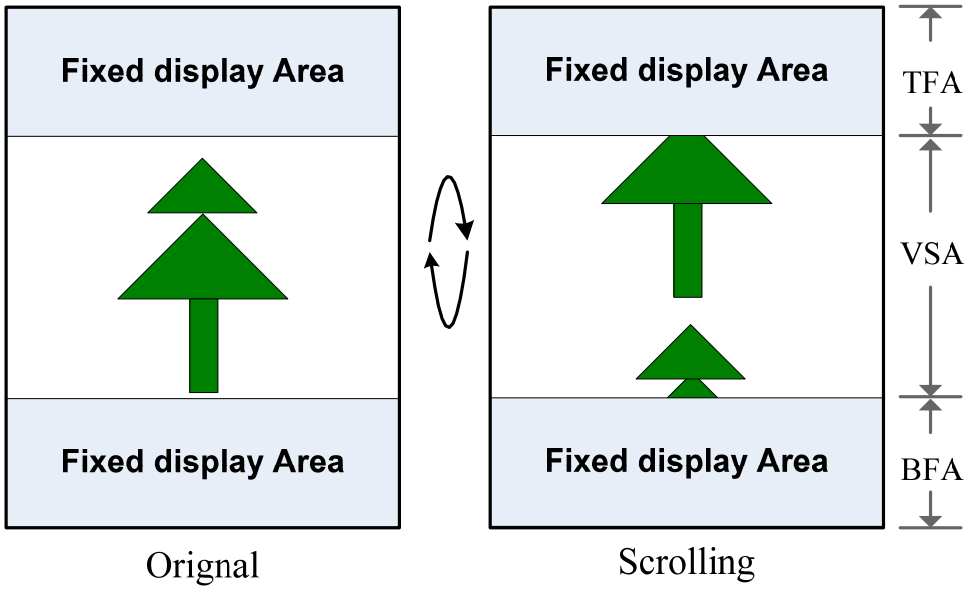


Example2:
(1) partial mode on (setting 12h)
(2) SR [15:0] =50DEC, ER [15:0] =150DEC, MADCTL's **B4(ML)='1'** (GS='0').



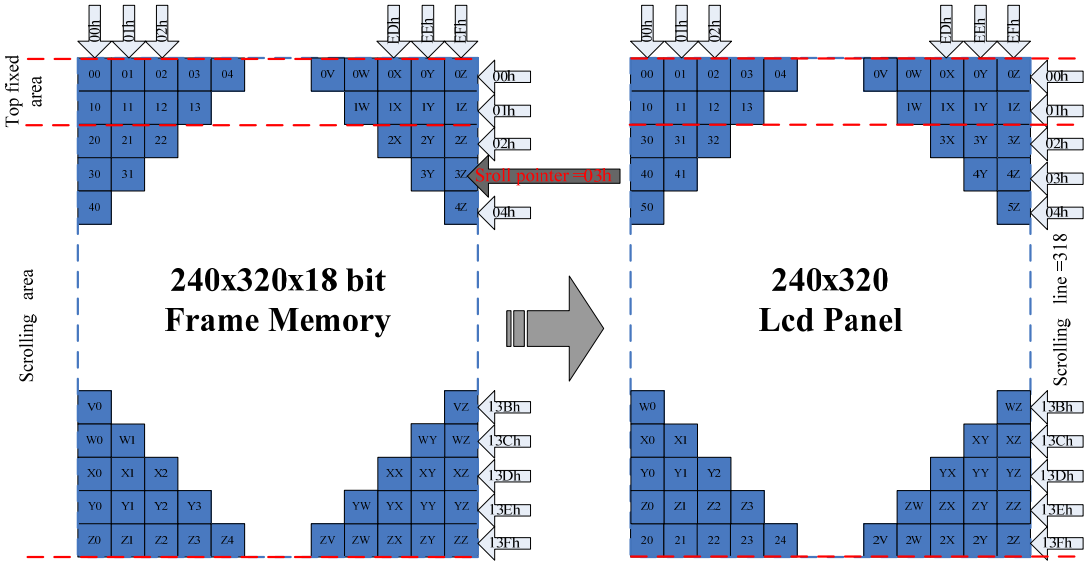
5.3.2 Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).

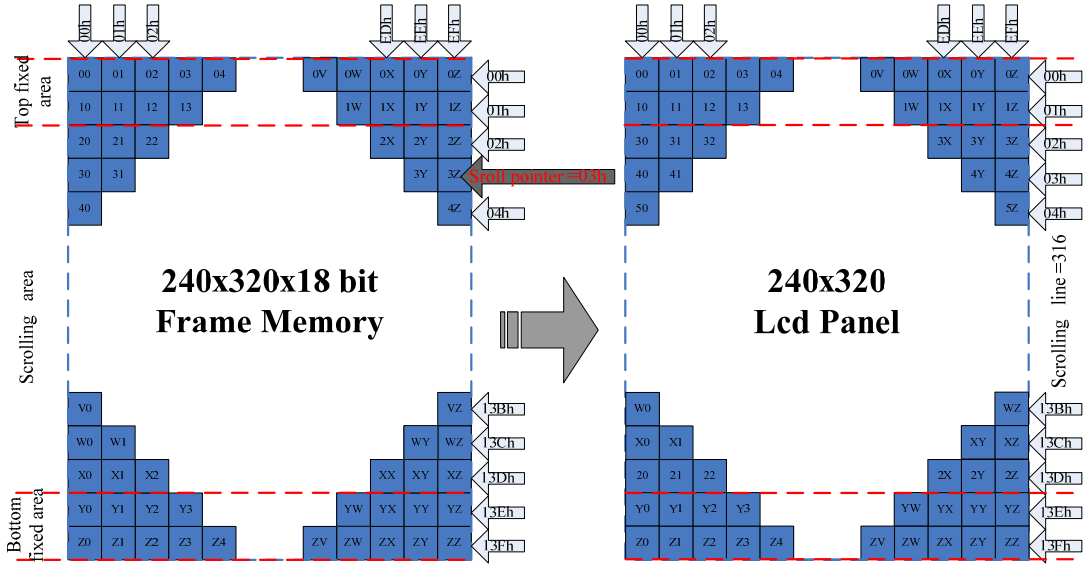


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =320. In this case, scrolling is applied as shown below.

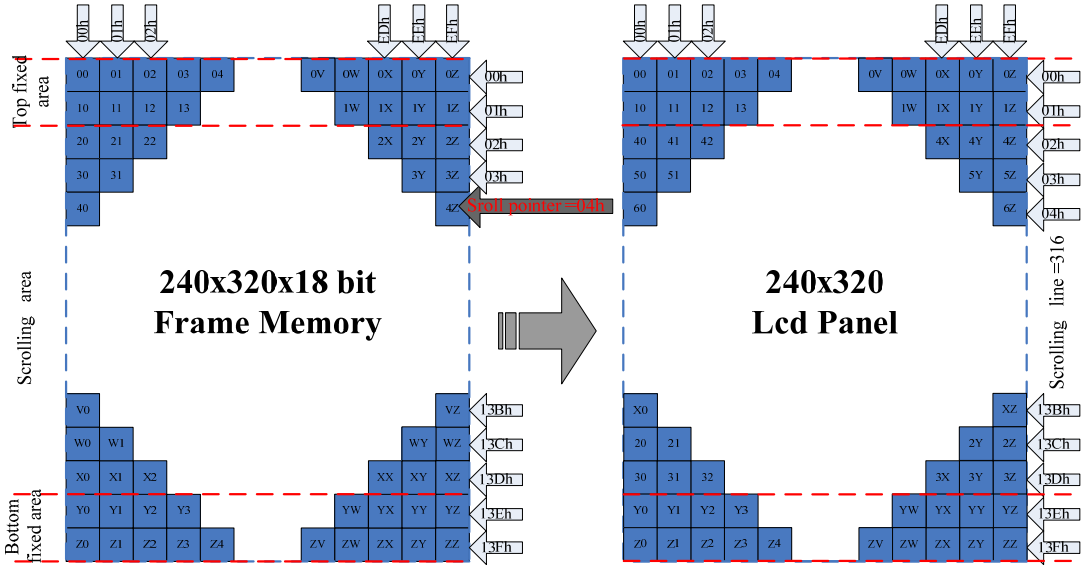
Example 1 .TFA=’2d’, VSA=’318d’, BFA=’0d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 1:



Example 2 .TFA=’2d’, VSA=’316d’, BFA=’2d’, VSP=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 2:



Example 3 .TFA=’2d’, VSA=’316d’, BFA=’2d’, VSP=’4d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 3:



Vertical scroll example

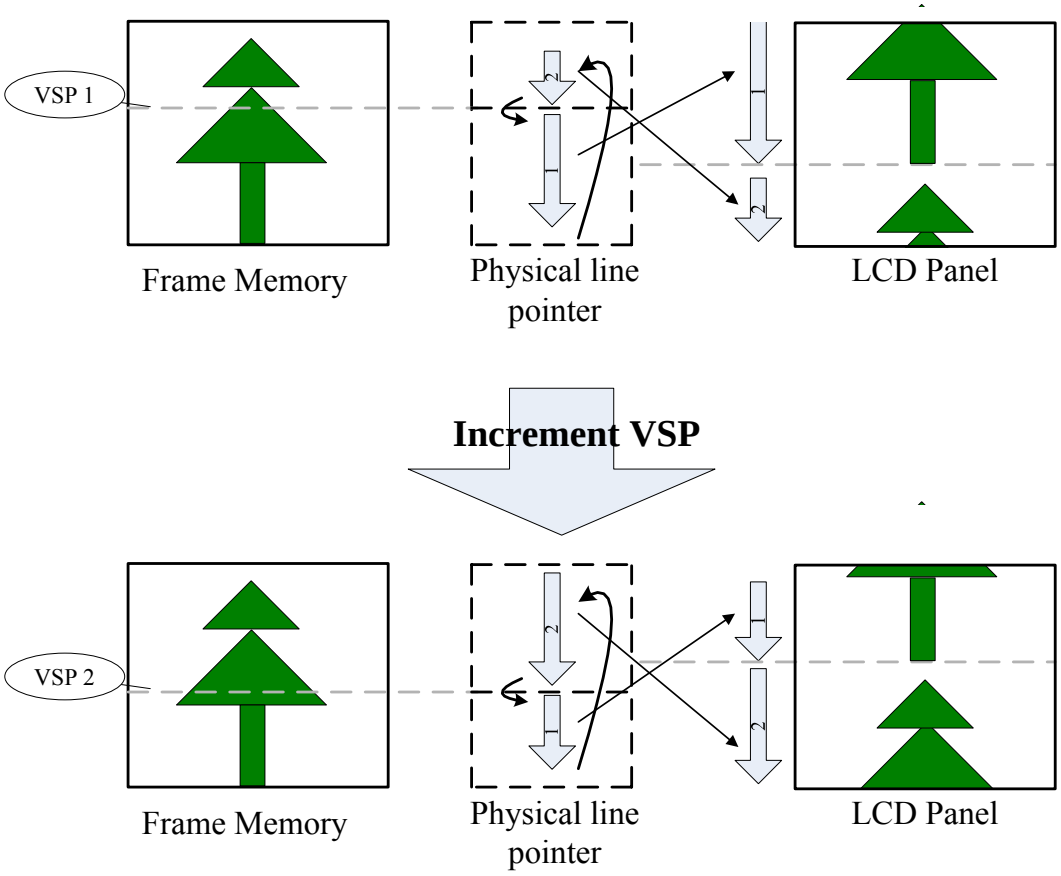
There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits and **VSP** bits

Case 1: TFA + VSA + BFA ≠ '320d'

N/A. Do not set TFA + VSA + BFA ≠ '320d'. In that case, unexpected picture will be shown.

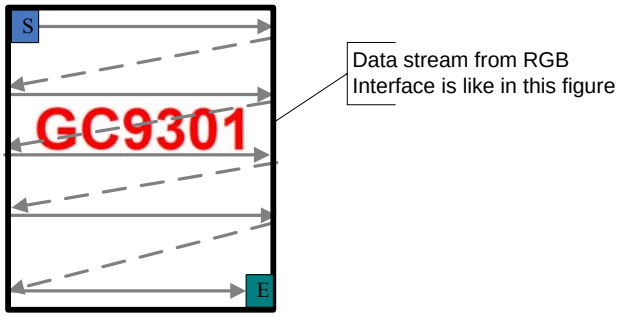
Case 2: TFA + VSA + BFA = '320d' (Scrolling)

Example (1) When TFA='0d', VSA='320d', BFA='0d' and VSP1='40d' & VSP2='140d' (SS ='0',GS='0')

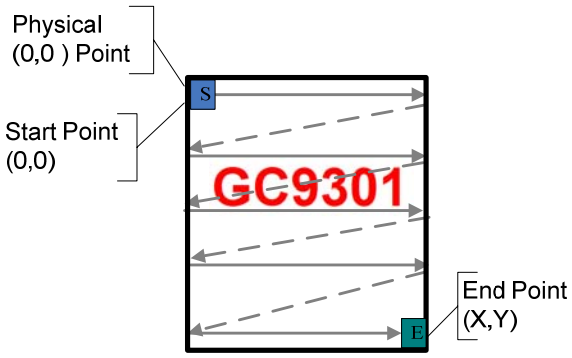


5.3.3 Updating order on display active area in RGB interface mode

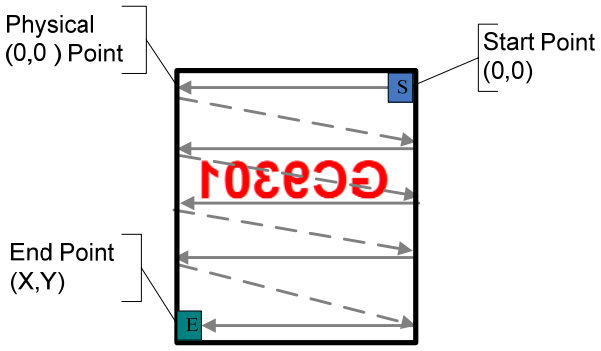
There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’).
These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.



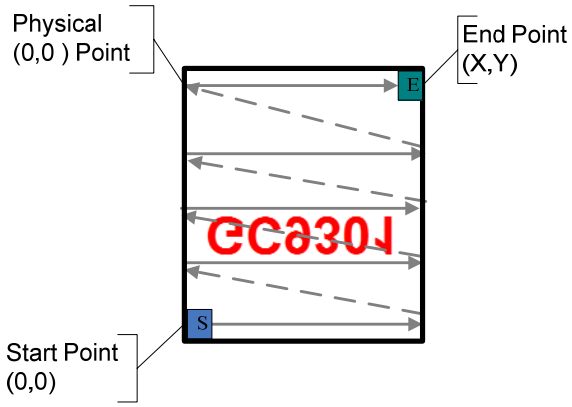
Updating order when MY = '0' and MX = '0'



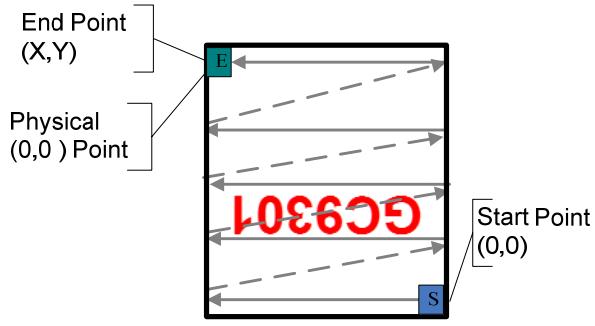
Updating order when MY = '0' and MX = '1'



Updating order when MY = '1' and MX = '0'



Updating order when MY = '1' and MX = '1'



Rules for updating order on display active area in RGB interface display mode:

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 “Start Column”	Return to “Start Page”

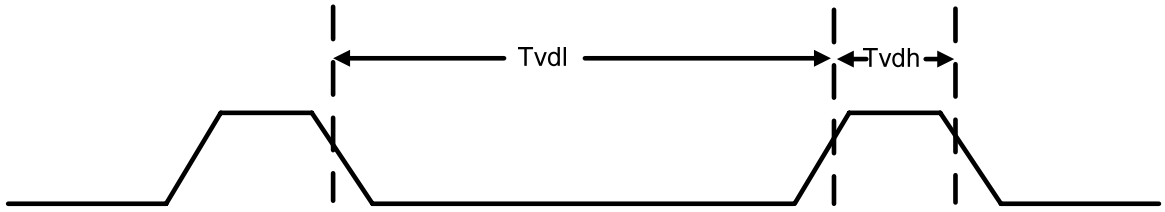
Note: Pixel order is RGB on the display.

5.4 Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing
when displaying video images.

5.4.1 Tearing effect line modes

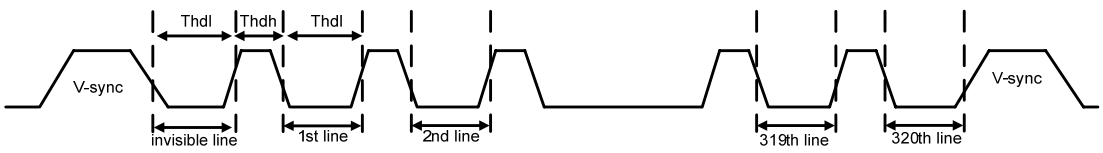
Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:



t_{Vdh}= The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.

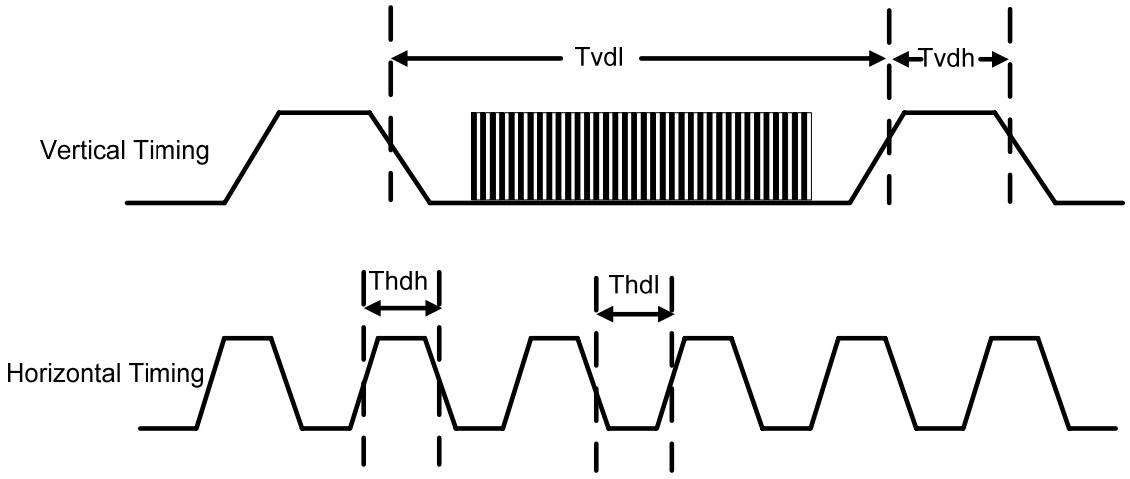


t_{hdh}= The LCD display is not updated from the Frame Memory

t_{hdl}= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2 Tearing effect line timing

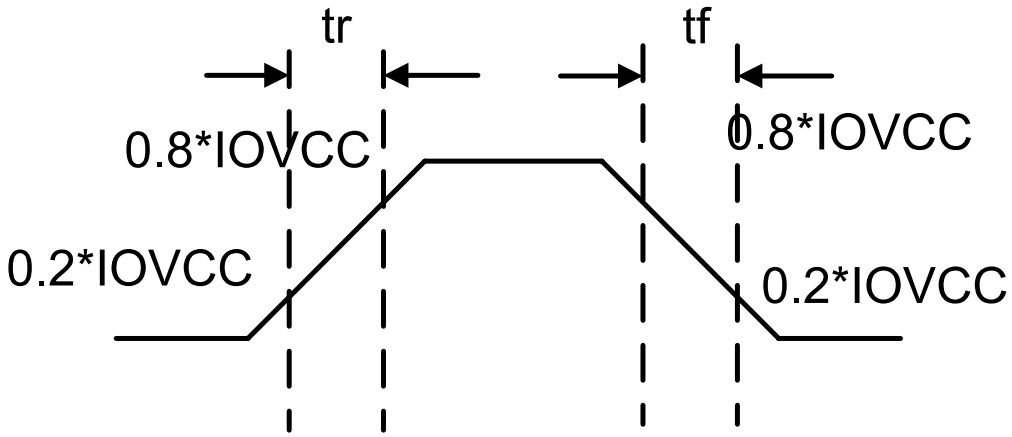
The Tearing Effect signal is described below.



Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5 Source driver

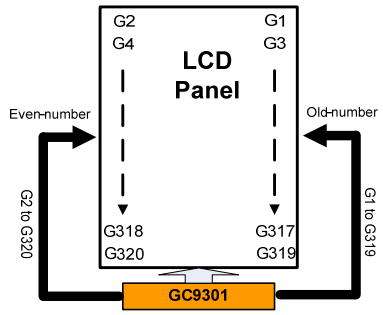
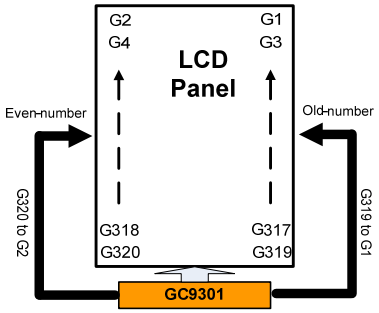
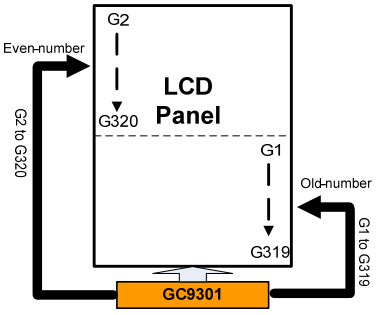
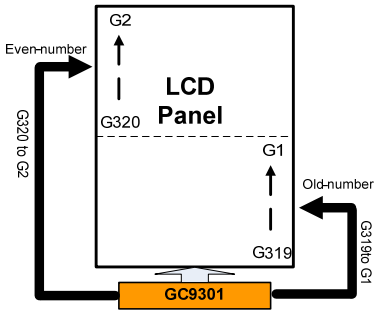
The GC9301 contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6 Gate driver

The GC9301 contains a 320 gate channels of gate driver (G1~G320) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7 Scan mode setting

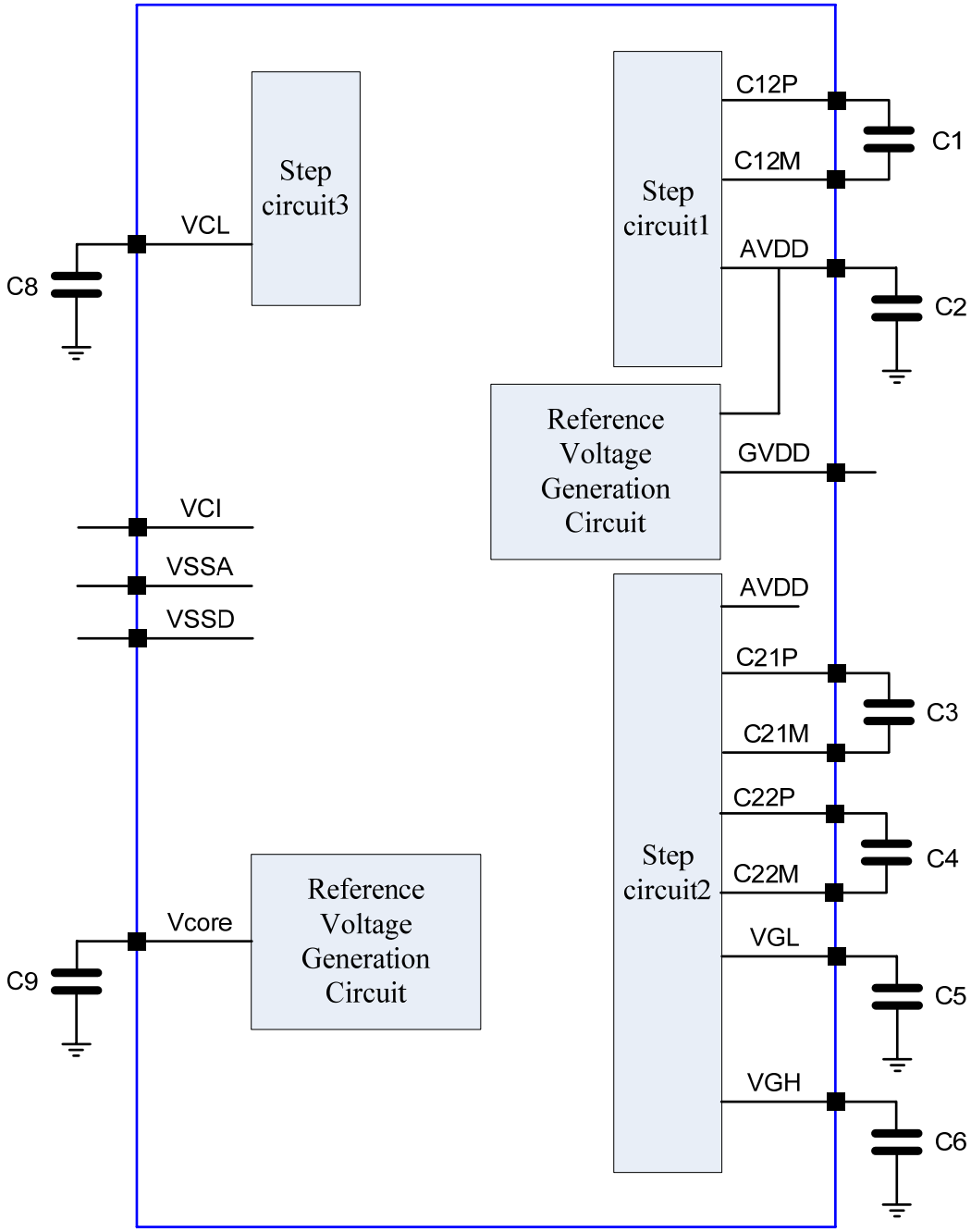
GS: Sets the direction of scan by the gate driver, The scan direction determined by GS = 0 can be reversed by setting GS = 1.
SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1 G2 G3 G4 ---> G317 G318 G319 G320
0	1		G320 G319 G 318 G317 ---> G4 G3 G2 G1
1	0		G1 G3 ---> G317 G319 --> G2 G4 ---> G318 G320
1	1		G320 G318 ---> G4 G2 --> G319 G317 ---> G3 G1

5.8 LCD power generation circuit

5.8.1 Power supply circuit

The power circuit of GC9301 is used to generate supply voltages for LCD panel driving.



Block diagram of GC9301 power circuit

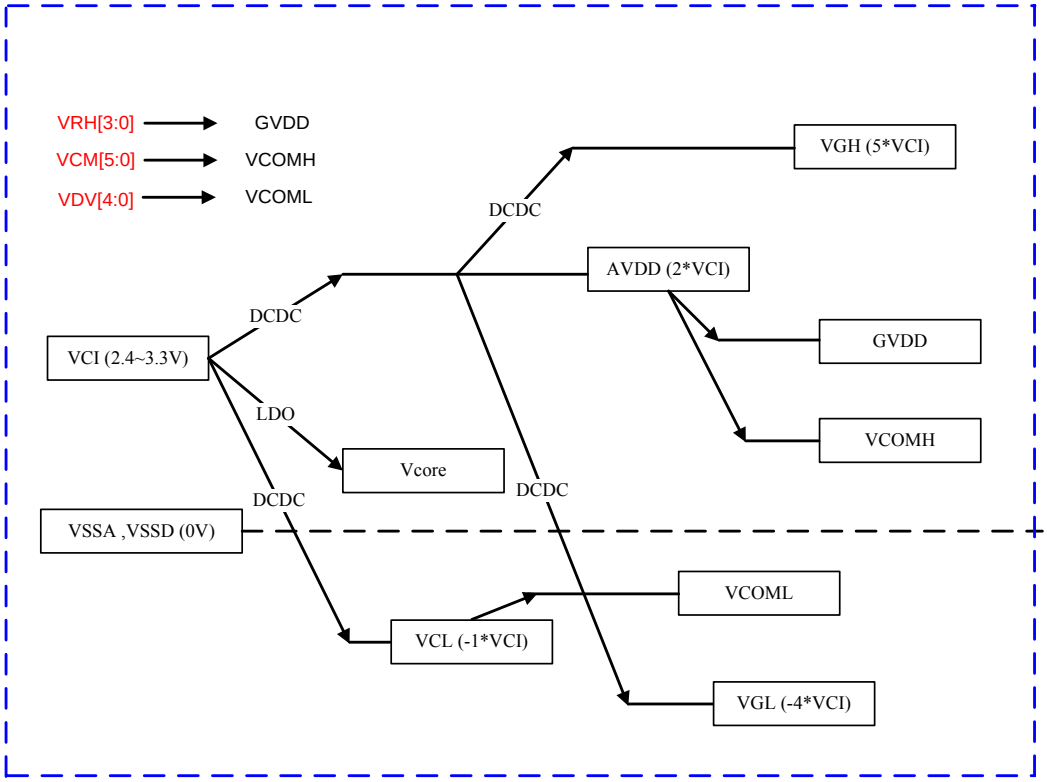
Specification of connected passive component

Capacitor	Recommended voltage	Capacity
C1(C12P/M)	6V	1μF (B characteristics)
C2(AVDD)	10V	1μF (B characteristics)
C3(C21P/M)	10V	1μF (B characteristics)
C4(C22P/M)	10V	1μF (B characteristics)
C5(VGL)	16V	1μF (B characteristics)
C6(VGH)	25V	1μF (B characteristics)
C8(VCL)	6V	1μF (B characteristics)
C9(Vcore)	6V	1μF (B characteristics)

Adoptability of capacitor

5.8.2 LCD power generation scheme

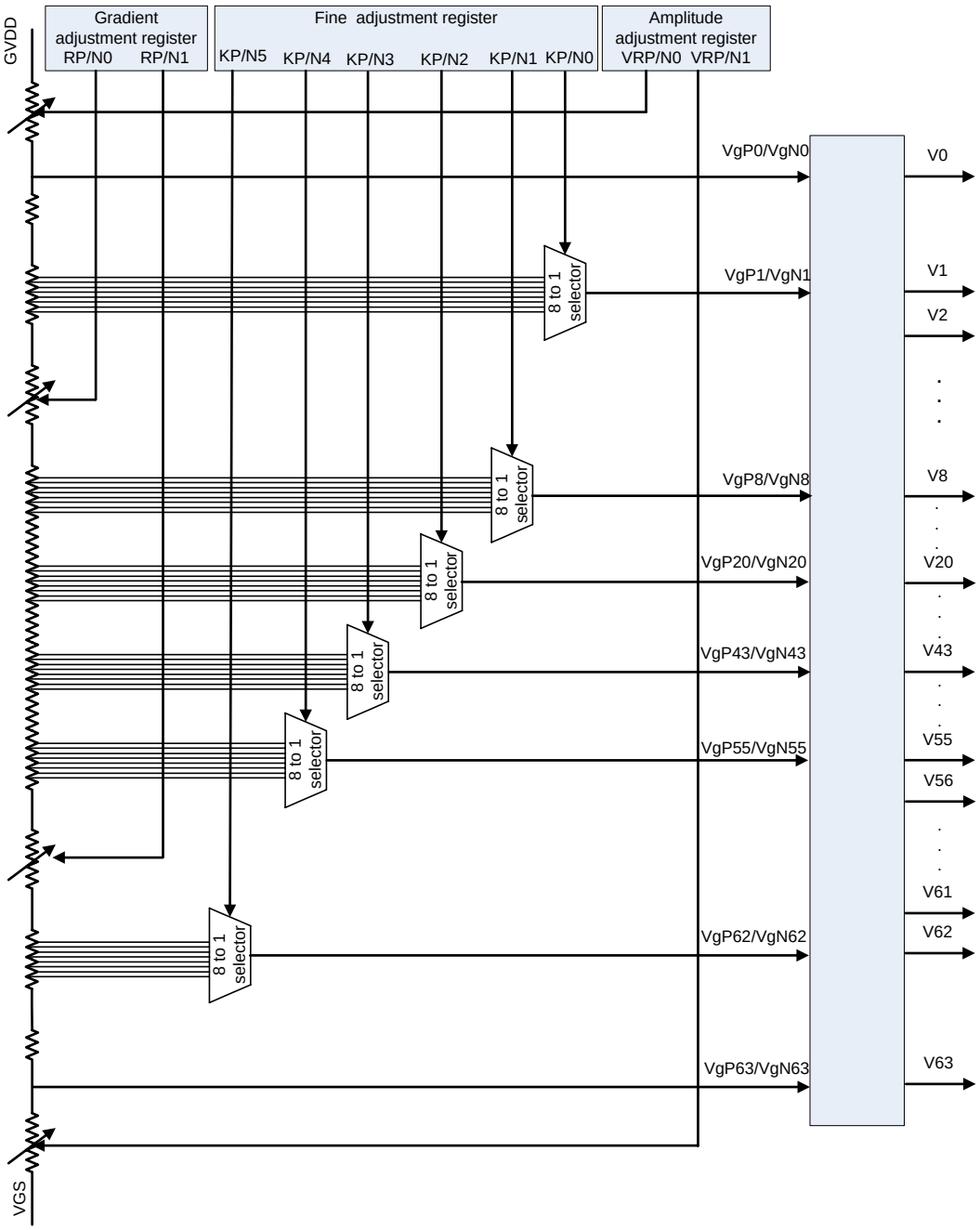
The boost voltage generated is shown as below.



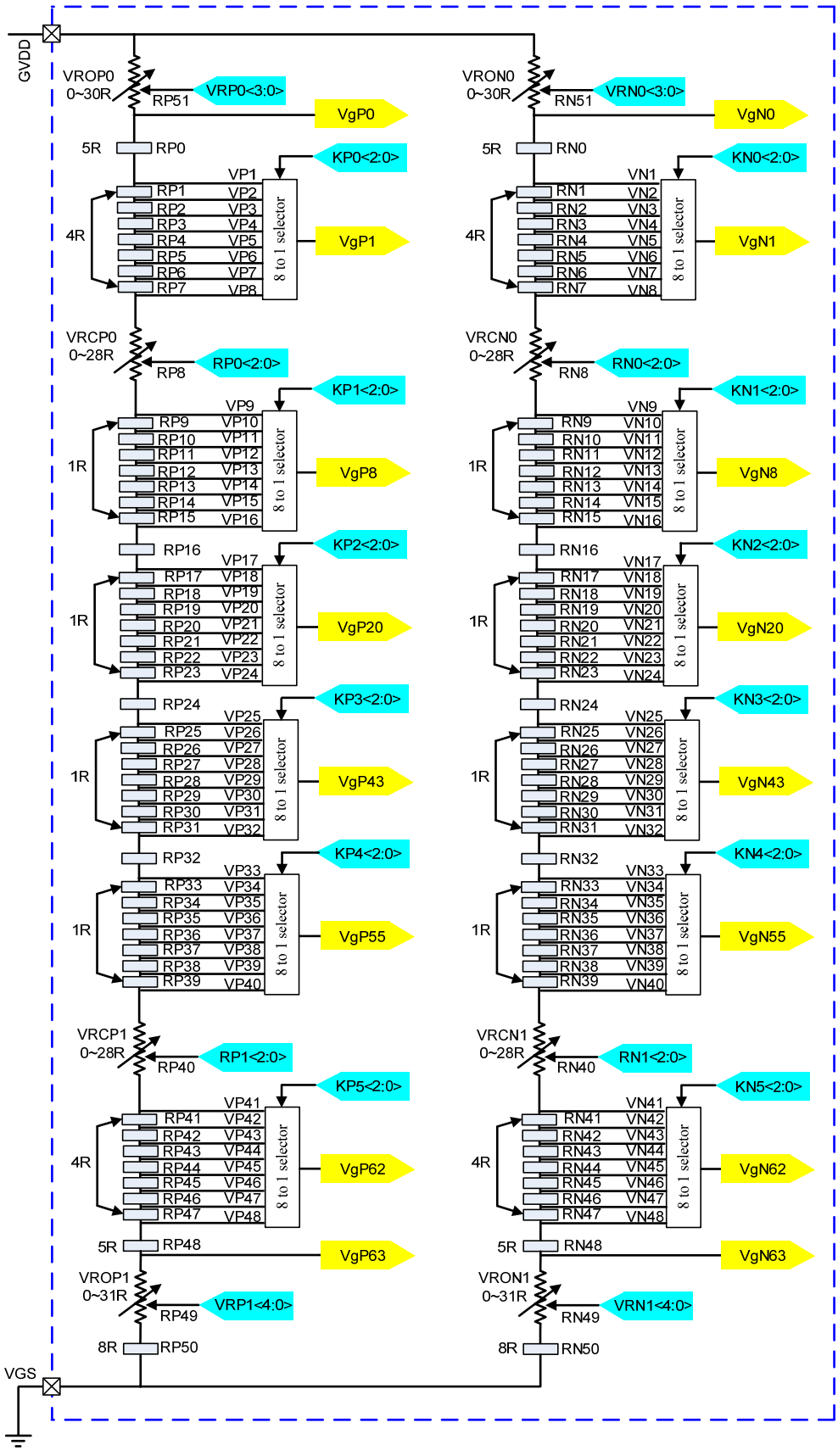
LCD power generation scheme

5.9 Gamma Correction

GC9301 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9301 available with liquid crystal panels of various characteristics.



Grayscale Voltage Generation



Grayscale Voltage Adjustment

1. Gradient adjustment registers

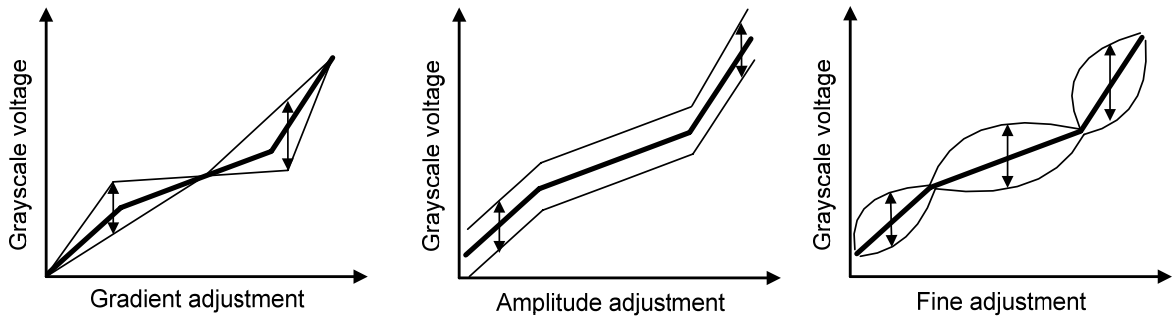
The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers RP0[2:0]/RN0[2:0], RP1[2:0]/RN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.



Gamma Curve Adjustment

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	RP0[2:0]	RN0[2:0]	Variable resistor VRCP0, VRCN0
	RP1[2:0]	RN1[2:0]	Variable resistor VRCP1, VRCN1
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VROP0, VRON0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0[2:0]	KN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	KP1[2:0]	KN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	KP2[2:0]	KN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	KP3[2:0]	KN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	KP4[2:0]	KN4[2:0]	8-to-1 selector (voltage level of grayscale 55)
	KP5[2:0]	KN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable resistors

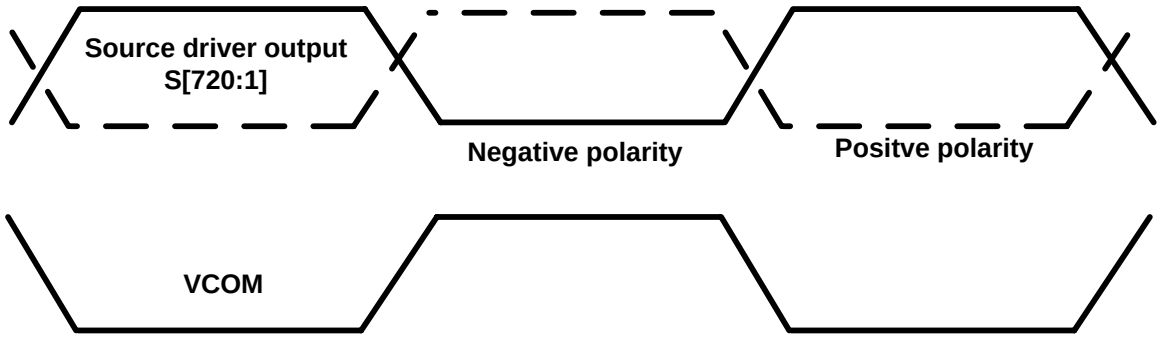
GC9301 uses variable resistors of the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment		**Amplitude adjustment (1)**		**Amplitude adjustment (2)**	
RP(N)0/1[2:0]	**VRCP(N)0 Resistance**	**VRP(N)0[3:0] Register**	**VROP(N)0 Resistance**	**VRP(N)1[4:0] Register**	**VROP(N)1 Resistance**
000	0R	0000	0R	00000	0R
001	4R	0001	2R	00001	1R
010	8R	0010	4R	00010	2R
011	12R				
100	16R	• • • •	• • • •	• • • •	• • • •
101	20R	1101	26R	11101	29R
110	24R	1110	28R	11110	30R
111	28R	1111	30R	11111	31R

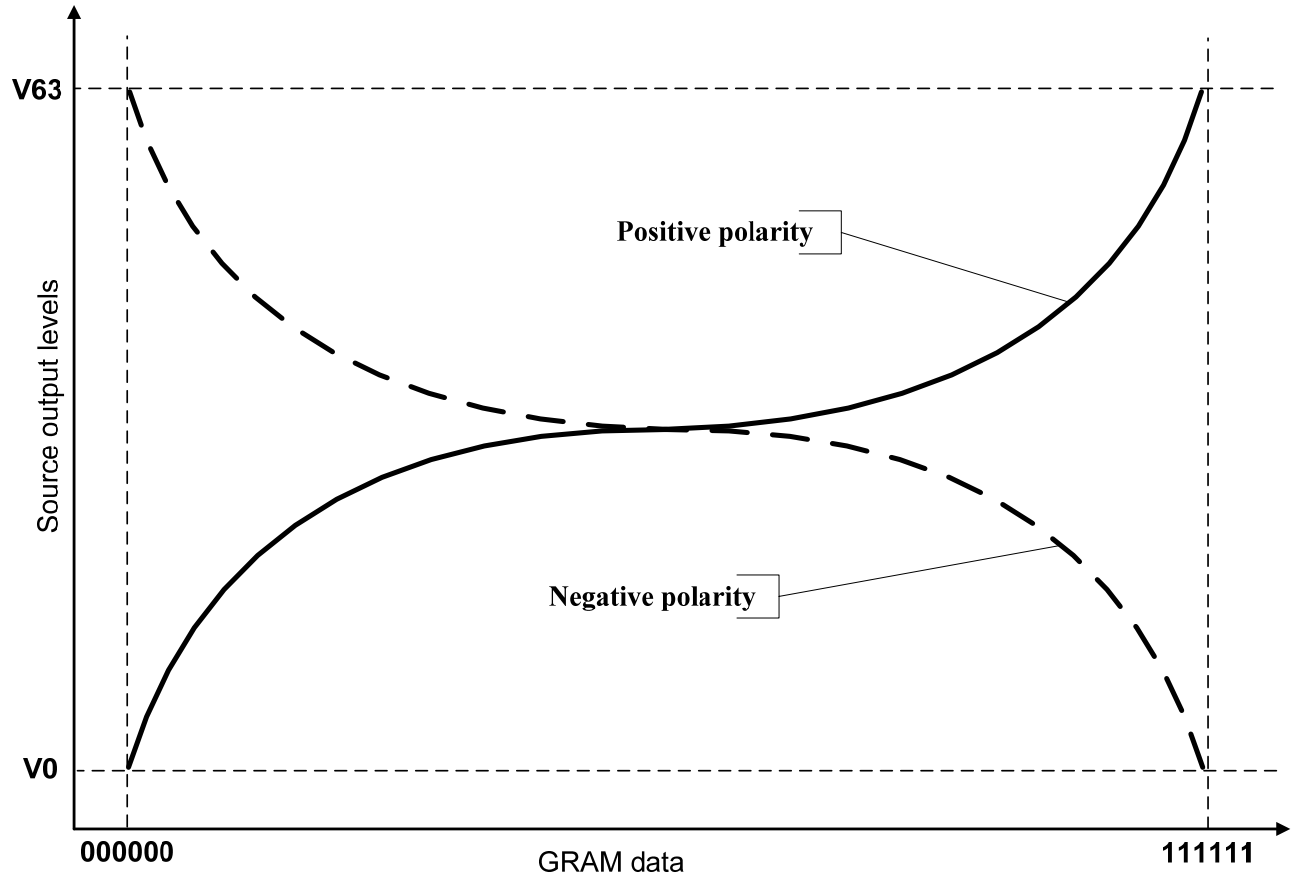
8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine adjustment registers and selected voltage						
Register	**Selected Voltage**					
KP/N[2:0]	**VgP/N1**	**VgP/N8**	**VgP/N20**	**VgP/N43**	**VgP/N55**	**VgP/N62**
000	VP/N1	VP/N9	VP/N17	VP/N25	VP/N33	VP/N41
001	VP/N2	VP/N10	VP/N18	VP/N26	VP/N34	VP/N42
010	VP/N3	VP/N11	VP/N19	VP/N27	VP/N35	VP/N43
011	VP/N4	VP/N12	VP/N20	VP/N28	VP/N36	VP/N44
100	VP/N5	VP/N13	VP/N21	VP/N29	VP/N37	VP/N45
101	VP/N6	VP/N14	VP/N22	VP/N30	VP/N38	VP/N46
110	VP/N7	VP/N15	VP/N23	VP/N31	VP/N39	VP/N47
111	VP/N8	VP/N16	VP/N24	VP/N32	VP/N40	VP/N48



Relationship between Source Output and VCOM


V63
V0
Source output levels
Positive polarity
Negative polarity
000000
GRAM data
111111

5.10 Power Level Definition

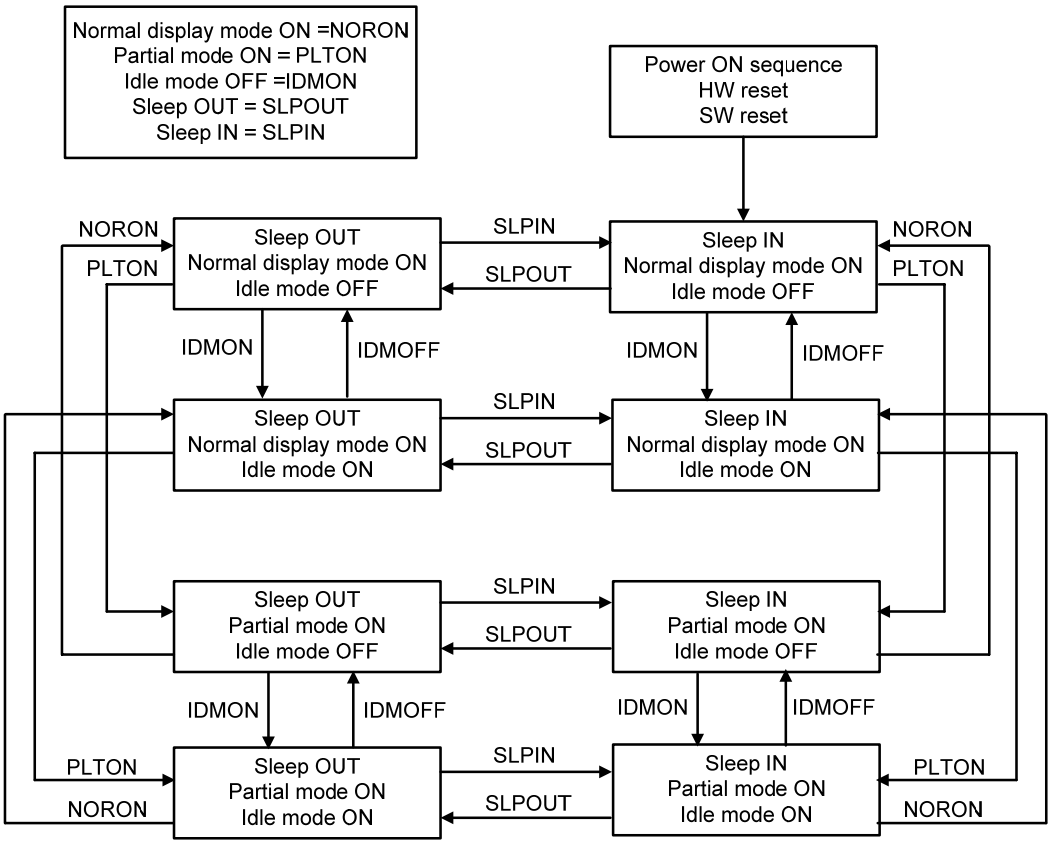
5.10.1 Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

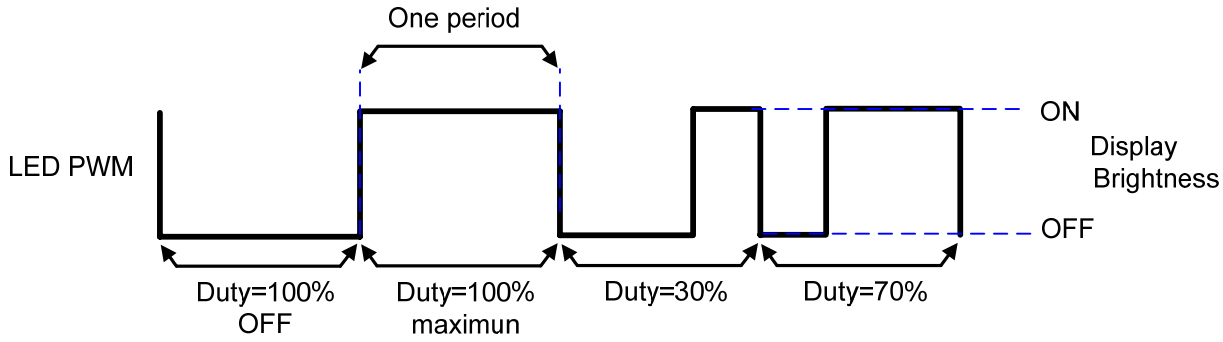
5.10.2 Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.
Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

5.11 Brightness control block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC
in order to control display brightness.
There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).
For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty =
200 / 255=78.1%. Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM
(high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.



LEDPWM output duty

5.12 Input/output pin state

5.12.1 Output pins

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

5.12.2 Input pins

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
IM[3:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6. Command

6.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 1	0	1	↑	XX	0	0	0	0	0	1	0	0	00h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID1_1[7:0]								XX
	1	↑	1	XX	ID1_2[7:0]								XX
	1	↑	1	XX	ID1_3[7:0]								XX
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2_1[7:0]								XX
	1	↑	1	XX	ID2_2[7:0]								XX
	1	↑	1	XX	ID2_3[7:0]								XX
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:2]						0	0	08
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:2]						0	0	00
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	RIM	DPI [2:0]			X	DBI [2:0]			06
Read Display Image Format	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	D [2:0]			00
Read Display Signal Mode	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:2]						0	0	00

Read Display Self-Diagnostic Result	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[7:6]		X	X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								XX
	1	1	↑	XX	SC[7:0]								XX
	1	1	↑	XX	EC[15:8]								XX
	1	1	↑	XX	EC[7:0]								XX
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								XX
	1	1	↑	XX	SP[7:0]								XX
	1	1	↑	XX	EP[15:8]								XX
	1	1	↑	XX	EP[7:0]								XX
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	D [17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								01
	1	1	↑	XX	ER[7:0]								3F
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								01
	1	1	↑	XX	VSA[7:0]								40

Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X	GTS [9:8]		00
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Module's Manufacture [7:0]								XX
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver Version [7:0]								XX
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								XX

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	X	RCM[1:0]		X	VSPL	HSPL	DPL	EPL	40
Display Inversion Control	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
	1	1	↑	XX	X	X	X	X	X	NLA	X	X	00
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	VFP[6:0]							02
	1	1	↑	XX	0	VBP[6:0]							02
	1	1	↑	XX	0	0	0	HFP[4:0]					0A
	1	1	↑	XX	0	0	0	HBP[4:0]					14
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	XX
	1	1	1	XX	REV	GS	SS	SM	ISC[3:0]				82
	1	1	1	XX	X	X	NL[5:0]						27
Read ID4	0	↑	1	XX	1	1	0	1	0	0	1	1	D3h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	0	0	0	00
	1	↑	1	XX	1	0	0	1	0	0	1	1	93
	1	↑	1	XX	0	1	0	0	0	0	0	0	40
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	X	X	X	X	BGR_EOR	X	X	WEMODE	01
	1	1	↑	XX	X	X	X	X	X	X	MDT[1:0]		00
	1	1	↑	XX	X	X	X	X	DM[1:0]		RM	RIM	00

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Frame Rate and Display Inversion	0	1	↑	XX	1	0	1	0	0	0	1	1	A3h
	1	1	↑	XX	Inv_ctl	0	0	0	frs[3:0]				84
Power control 1	0	1	↑	XX	1	0	1	0	0	1	0	0	A4h
	1	1	↑	XX	VCIRE	X	X	X	VRH[3:0]				8C
Power control 2	0	1	↑	XX	1	1	1	0	1	1	0	1	EDh
	1	1	↑	XX	X	X	dc1[2:0]			dc0[2:0]			0A
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	X	KP1[2:0]			X	KP0[2:0]			00
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	X	KP3[2:0]			X	KP2[2:0]			55
SET_GAMMA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	X	KP5[2:0]			X	KP4[2:0]			07
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
	1	1	↑	XX	X	RP1[2:0]			X	RP0[2:0]			52
SET_GAMMA5	0	1	↑	XX	1	1	1	1	0	1	0	0	F4h
	1	1	↑	XX	X	X	X	X	VRP0[3:0]				00
SET_GAMMA6	0	1	↑	XX	1	1	1	1	0	1	0	1	F5h
	1	1	↑	XX	X	X	X	VRP1[4:0]					00
SET_GAMMA7	0	1	↑	XX	1	1	1	1	0	1	1	1	F7h
	1	1	↑	XX	X	KN1[2:0]			X	KN0[2:0]			07
SET_GAMMA8	0	1	↑	XX	1	1	1	1	1	0	0	0	F8h
	1	1	↑	XX	X	KN3[2:0]			X	KN2[2:0]			22
SET_GAMMA9	0	1	↑	XX	1	1	1	1	1	0	0	1	F9h
	1	1	↑	XX	X	KN5[2:0]			X	KN4[2:0]			77
SET_GAMMA10	0	1	↑	XX	1	1	1	1	1	0	1	0	FAh
	1	1	↑	XX	X	RN1[2:0]			X	RN0[2:0]			25
SET_GAMMA11	0	1	↑	XX	1	1	1	1	1	0	1	1	FBh
	1	1	↑	XX	X	X	X	X	VRN0[3:0]				00
SET_GAMMA12	0	1	↑	XX	1	1	1	1	1	1	0	0	FCh
	1	1	↑	XX	X	X	X	VRN1[4:0]					00
Power control 3	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh
	1	1	↑	XX	X	X	VCM[5:0]						1C
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Power control 4	0	1	↑	XX	1	1	1	1	1	1	1	1	FFh
	1	1	↑	XX	X	X	X	VDV[4:0]					16

6.2. Description of Level 1 Command

6.2.1. Read display identification information 1 (00h)

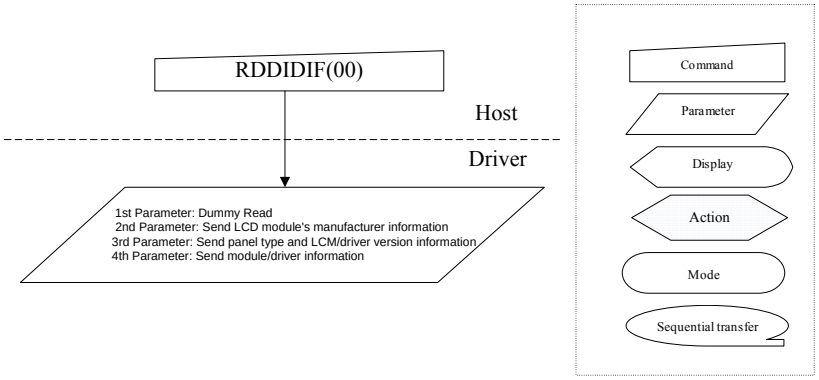
00h	Read display identification information 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1_1[7:0]								00
3rd Parameter	1	↑	1	XX	ID1_2[7:0]								03
4th Parameter	1	↑	1	XX	ID1_3[7:0]								01
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID1_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID1_2 [7:0]): LCD module/driver version ID. The 4th parameter (ID1_3 [7:0]): LCD module/driver ID.												
Restriction													

Register Availability

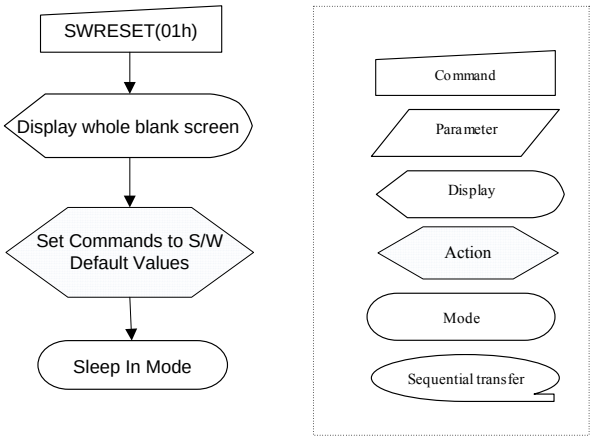
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h000301h
SW Reset	24'h000301h
HW Reset	24'h000301h

Flow Chart	 RDDIDIF(00) Host Driver 1st Parameter: Dummy Read 2nd Parameter: Send LCD module's manufacturer information 3rd Parameter: Send panel type and LCM/driver version information 4th Parameter: Send module/driver information Command Parameter Display Action Mode Sequential transfer

6.2.2. Software Reset (01h)

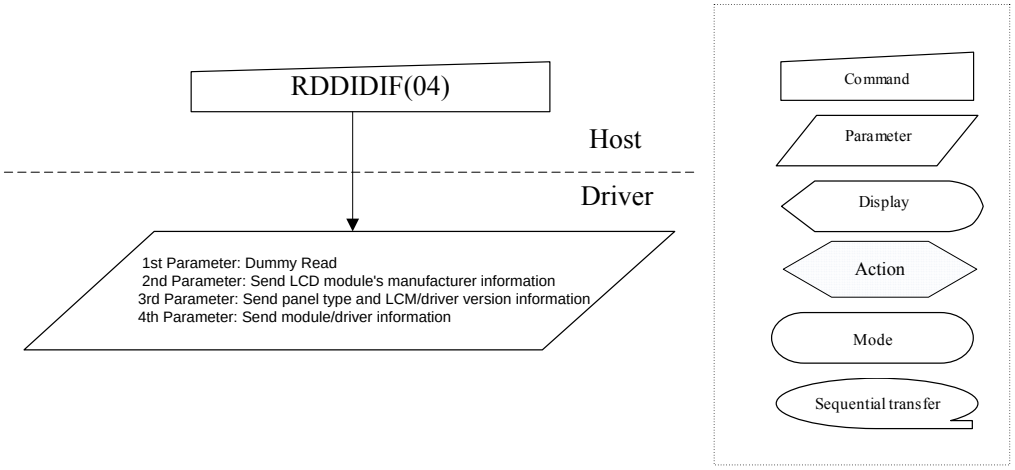
<table>
<tr><td>01h</td><td colspan="13">Software Reset</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)
Note: The Frame Memory contents are unaffected by this command
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>N/A</td></tr><tr><td>SW Reset</td><td>N/A</td></tr><tr><td>HW Reset</td><td>N/A</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.3. Read display identification information 2 (04h)

04h	Read display identification information 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID2_1[7:0]								X X
3rd Parameter	1	↑	1	XX	ID2_1[7:0]								X X
4th Parameter	1	↑	1	XX	ID2_1[7:0]								X X
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID2_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID. The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.												
Restriction													
Register Availability													
Default													
Flow Chart													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description


RDDIDIF(04)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send LCD module's manufacturer information
3rd Parameter: Send panel type and LCM/driver version information
4th Parameter: Send module/driver information
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.4. Read Display Status (09h)

<table>
<tr><td>09h</td><td colspan="13">Read Display Status</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>09h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="8">D[31:25]</td><td>X</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td colspan="3">D[22:20]</td><td colspan="4">D[19:16]</td><td>61</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">D[10:8]</td><td>00</td></tr>
<tr><td>5th Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td colspan="3">D[7:5]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th><th>Status</th></tr>
<tr><td>D31</td><td>Booster voltage status</td><td>O</td><td>Booster OFF</td></tr>
<tr><td></td><td></td><td>1</td><td>Booster ON</td></tr>
<tr><td>D30</td><td>Row address order</td><td>O</td><td>Top to Bottom (When MADCTL B7='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>Bottom to Top (When MADCTL B7='1')</td></tr>
<tr><td>D29</td><td>Column address order</td><td>O</td><td>Left to Right (When MADCTL B6='0').</td></tr>
<tr><td></td><td></td><td>1</td><td>Right to Left (When MADCTL B6='1').</td></tr>
<tr><td>D28</td><td>Row/column exchange</td><td>O</td><td>Normal Mode (When MADCTL B5='0').</td></tr>
<tr><td></td><td></td><td>1</td><td>Reverse Mode (When MADCTL B5='1').</td></tr>
<tr><td>D27</td><td>Vertical refresh</td><td>O</td><td>LCD Refresh Top to BoUom (When MADCTL B4='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>LCD Refresh BoUom to Top (When MADCTL B4='1').</td></tr>
<tr><td>D26</td><td>RGB/BGR order</td><td>O</td><td>RGB (When MADCTL B3='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>BGR (When MADCTL B3='1')</td></tr>
<tr><td>D25</td><td>Horizontal refresh order</td><td>O</td><td>LCD Refresh Left to Right (When MADCTL B2='0')</td></tr>
<tr><td></td><td></td><td>1</td><td>LCD Refresh Right to Left (When MADCTL B2='1')</td></tr>
<tr><td>D24</td><td>Not used</td><td>O</td><td>-</td></tr>
<tr><td>D23</td><td>Not used</td><td>O</td><td>-</td></tr>
<tr><td>D22</td><td rowspan="3">Interface color pixel format definition</td><td rowspan="2">101</td><td rowspan="2">16-bit/pixel</td></tr>
<tr><td>D21</td></tr>
<tr><td>D20</td><td>110</td><td>18-bit/pixel</td></tr>
<tr><td>D19</td><td>Idle mode ON/OFF</td><td>O</td><td>Idle Mode OFF</td></tr>
<tr><td></td><td></td><td>1</td><td>Idle Mode ON</td></tr>
<tr><td>D18</td><td>Partial mode ON/OFF</td><td>O</td><td>Partial Mode OFF</td></tr>
<tr><td></td><td></td><td>1</td><td>Partial Mode ON</td></tr>
<tr><td>D17</td><td>Sleep IN/OUT</td><td>O</td><td>Sleep IN Mode</td></tr>
<tr><td></td><td></td><td>1</td><td>Sleep OUT Mode</td></tr>
<tr><td>D16</td><td>Display normal mode ON/OFF</td><td>O</td><td>Display Normal Mode OFF.</td></tr>
</table></td></tr>
</table>

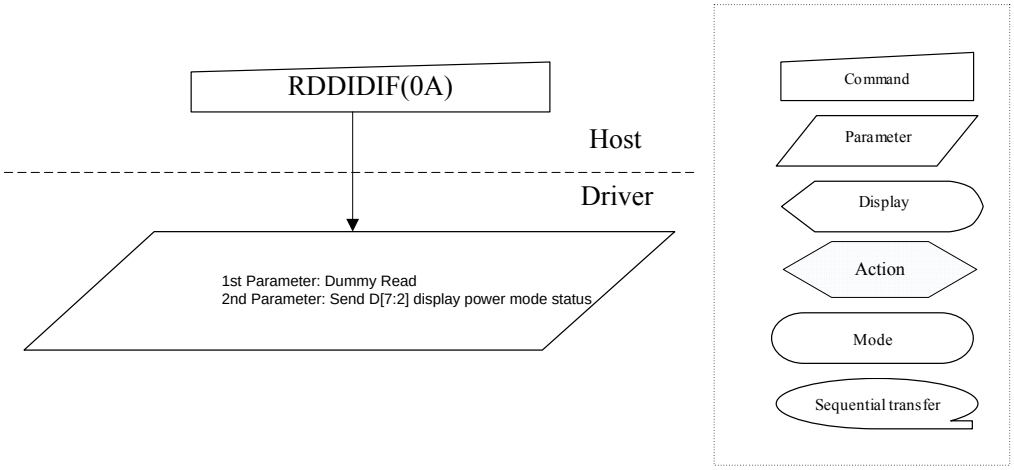
				1	Display Normal Mode ON.	
		D15	Vertical scrolling status	O	Scroll OFF	
		D14	Not used	O	-	
		D13	Inversion status	O	Not defined	
		D12	All pixel ON	O	Not defined	
		D11	All pixel OFF	O	Not defined	
		D10	Display ON/OFF	O		
				1	Display is ON	
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF	
				1	Tearing Effect ON	
		D[8:6]	Gamma curve selection	000	GC0	
				001	GC1	
				010	GC2	
				011	GC3	
				other	Not defined	
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only	
				1	Mode 2, both H-Blanking and V-Blanking	
		D4	Not used	O	-	
		D3	Not used	O	-	
		D2	Not used	O	-	
		D1	Not used	O	-	
		D0	Not used	O	-	
Restriction						

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.5. Read Display Power Mode (0Ah)

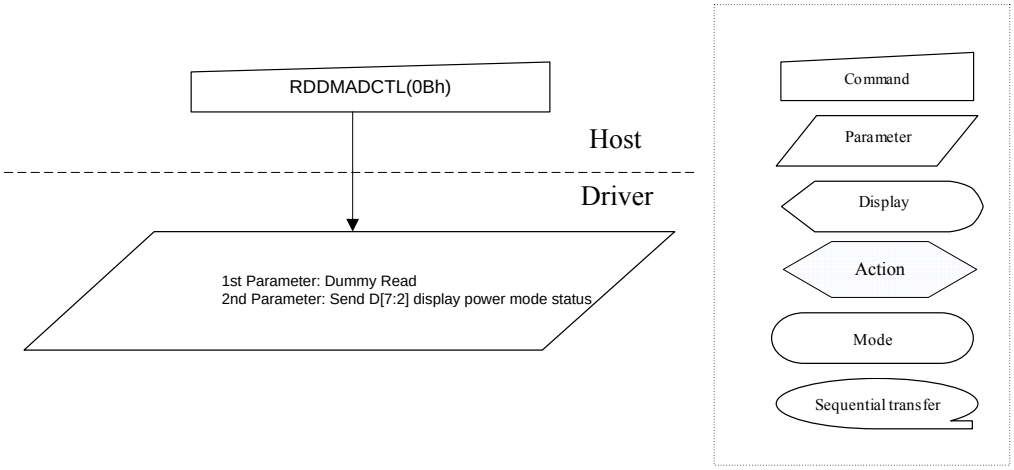
<table>
<tr><td>0Ah</td><td colspan="13">Read Display Power Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th><th>Comment</th></tr>
<tr><td rowspan="2">D7</td><td>0</td><td>Booster Off or has a fault.</td><td>---</td></tr>
<tr><td>1</td><td>Booster On and working OK.</td><td>---</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td>Idle Mode Off.</td><td>---</td></tr>
<tr><td>1</td><td>Idle Mode On.</td><td>---</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td>Partial Mode Off.</td><td>---</td></tr>
<tr><td>1</td><td>Partial Mode On.</td><td>---</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td>Sleep In Mode</td><td>---</td></tr>
<tr><td>1</td><td>Sleep Out Mode</td><td>---</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td>Display Normal Mode Off.</td><td>---</td></tr>
<tr><td>1</td><td>Display Normal Mode On</td><td>---</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td>Display is Off.</td><td>---</td></tr>
<tr><td>1</td><td>Display is On</td><td>---</td></tr>
<tr><td>D1</td><td>--</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>--</td><td>Not Defined</td><td>Set to ‘0’</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>See description</td></tr>
<tr><td>SW Reset</td><td>See description</td></tr>
<tr><td>HW Reset</td><td>See description</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDIDIF(0A)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.6. Read Display MADCTL (0Bh)

<table>
<tr><td>0Bh</td><td colspan="13">Read Display MADCTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th><th>Comment</th></tr>
<tr><td rowspan="2">D7</td><td>0</td><td>Top to Bottom (When MADCTL B7=’0’).</td><td>---</td></tr>
<tr><td>1</td><td>Bottom to Top(When MADCTL B7=’1’).</td><td>---</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td>Left to Right (When MADCTL B6=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>Right to Left (When MADCTL B6=’1’)</td><td>---</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td>Normal Mode (When MADCTL B5=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>Reverse Mode (When MADCTL B5=’1’)</td><td>---</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td>LCD Refresh Top to Bottom (When MADCTL B4=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>LCD Refresh Bottom to Top (When MADCTL B4=’1’).</td><td>---</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td>RGB (When MADCTL B3=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>BGR (When MADCTL B3=’1’).</td><td>---</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td>LCD Refresh Left to Right (When MADCTL B2=’0’)</td><td>---</td></tr>
<tr><td>1</td><td>LCD Refresh Right to Left (When MADCTL B2=’1’)</td><td>---</td></tr>
<tr><td>D1</td><td>--</td><td>Switching between Segment outputs and RAM</td><td>Set to ‘0’</td></tr>
<tr><td>D0</td><td>--</td><td>Switching between Segment outputs and RAM</td><td>Set to ‘0’</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

Flow Chart	

RDDMADCTL(0Bh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.7. Read Display Pixel Format (0Ch)

0Ch	Read Display Pixel Format												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00

Description

This command indicates the current status of the display as described in the table below:

RIM	DPI [2:0]			RGB Interface Format		DBI [2:0]			MCU Interface Format
0	0	0	0	Reserved		0	0	0	Reserved
0	0	0	1	Reserved		0	0	1	Reserved
0	0	1	0	Reserved		0	1	0	Reserved
0	0	1	1	Reserved		0	1	1	Reserved
0	1	0	0	Reserved		1	0	0	Reserved
0	1	0	1	16 bits / pixel		1	0	1	16 bits / pixel
0	1	1	0	18 bits / pixel		1	1	0	18 bits / pixel
0	1	1	1	Reserved		1	1	1	Reserved
1	1	0	1	16 bits / pixel (6-bit 3 times data transfer)					
1	1	1	0	16 bits / pixel (6-bit 3 times data transfer)					

X = Don't care

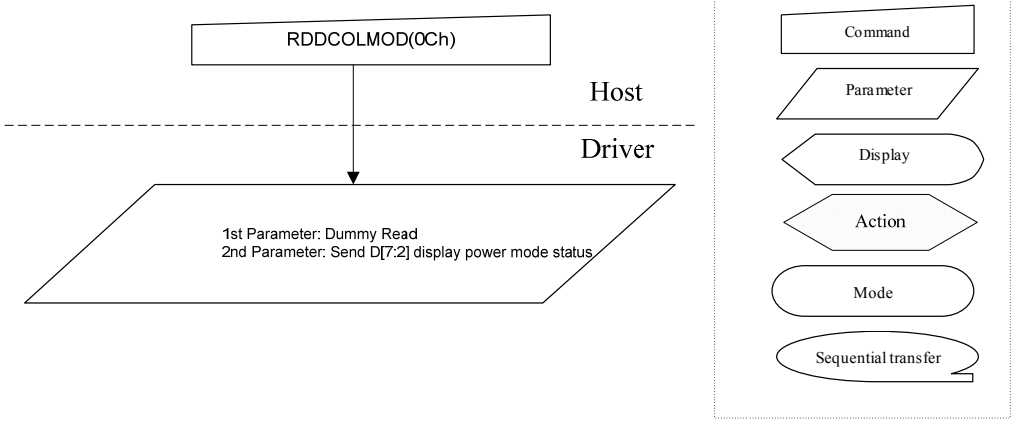
Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

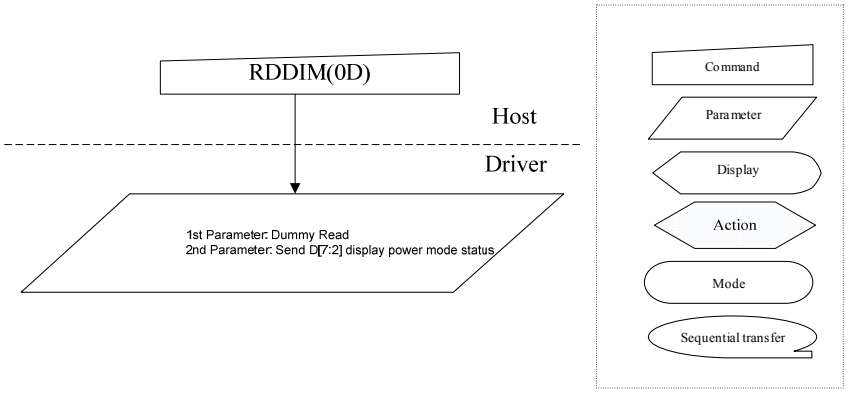
Default

Status	Default Value		
	RIM	DPI [2:0]	DBI [2:0]
Power On Sequence	1'b0	3'b000	3'b110

		SW Reset	No Chang	No Chang	No Chang	
		HW Reset	1'b0	3'b000	3'b110	
Flow Chart						

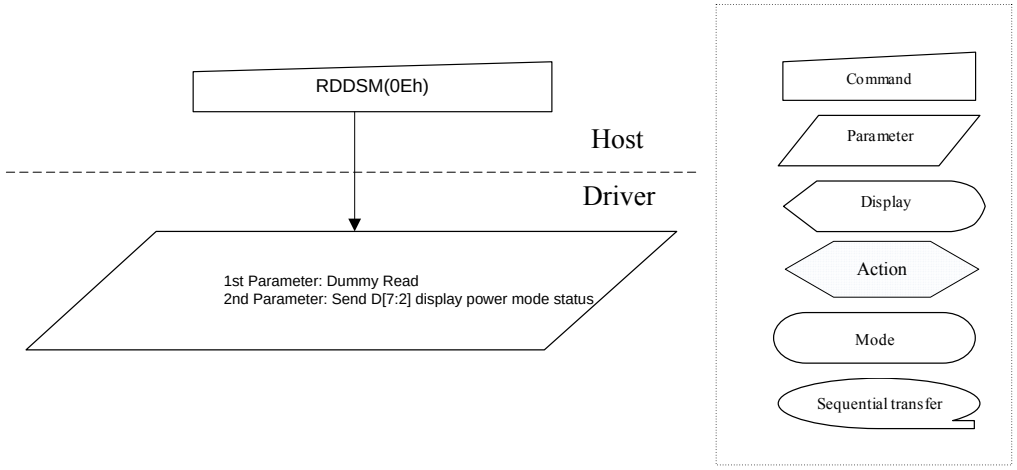
6.2.8. Read Display Image Format (0Dh)

<table>
<tr><td>0Dh</td><td colspan="13">Read Display Image Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0Dh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">D[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table><tr><th>D [2:0]</th><th>Description</th></tr><tr><td>000</td><td>Gamma curve 1 (G2.2)</td></tr><tr><td>001</td><td>Gamma curve 2 (G1.8)</td></tr><tr><td>010</td><td>Gamma curve 3 (G2.5)</td></tr><tr><td>011</td><td>Gamma curve 4 (G1.0)</td></tr><tr><td>Other</td><td>Not defined</td></tr></table>X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>3’b000</td></tr><tr><td>SW Reset</td><td>3’b000</td></tr><tr><td>HW Reset</td><td>3’b000</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDIM(0D)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.9. Read Display Signal Mode (0Eh)

<table>
<tr><td>0Eh</td><td colspan="13">Read Display Signal Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0Eh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">D7</td><td>0</td><td>Tearing effect line OFF</td></tr>
<tr><td>1</td><td>Tearing effect line ON</td></tr>
<tr><td rowspan="2">D6</td><td>0</td><td>Tearing effect line mode 1</td></tr>
<tr><td>1</td><td>Tearing effect line mode 2</td></tr>
<tr><td rowspan="2">D5</td><td>0</td><td>Horizontal sync. (RGB interface) OFF</td></tr>
<tr><td>1</td><td>Horizontal sync. (RGB interface) ON</td></tr>
<tr><td rowspan="2">D4</td><td>0</td><td>Vertical sync. (RGB interface) OFF</td></tr>
<tr><td>1</td><td>Vertical sync. (RGB interface) ON</td></tr>
<tr><td rowspan="2">D3</td><td>0</td><td>Pixel clock (DOTCLK, RGB interface) OFF</td></tr>
<tr><td>1</td><td>Pixel clock (DOTCLK, RGB interface) ON</td></tr>
<tr><td rowspan="2">D2</td><td>0</td><td>Data enable (DE,RGB interface) OFF</td></tr>
<tr><td>1</td><td>Data enable (DE,RGB interface) ON</td></tr>
<tr><td>D1</td><td>0</td><td>Reserved</td></tr>
<tr><td>D0</td><td>1</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>SW Reset</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"></td></tr>
</table>


RDDSM(0Eh)
Host
Driver
1st Parameter: Dummy Read
2nd Parameter: Send D[7:2] display power mode status
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.10. Read Display Self-Diagnostic Result (0Fh)

0Fh	Read Display Self-Diagnostic Result												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	1	F	1	0Fh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Action
D7	Register Loading Detection	Invert the D7 bit if register values loading work properly.
D6	Functionality Detection	Invert the D6 bit if the display is functionality

X = Don't care

Restriction

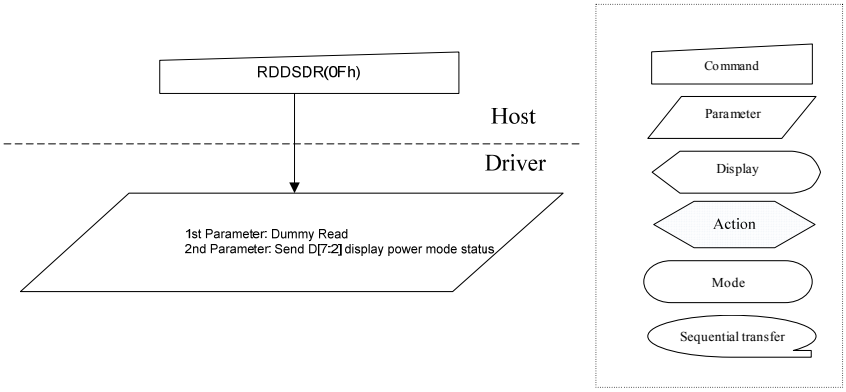
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

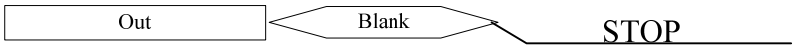
Default

Status	Default Value
Power On Sequence	3'b000
SW Reset	3'b000
HW Reset	3'b000

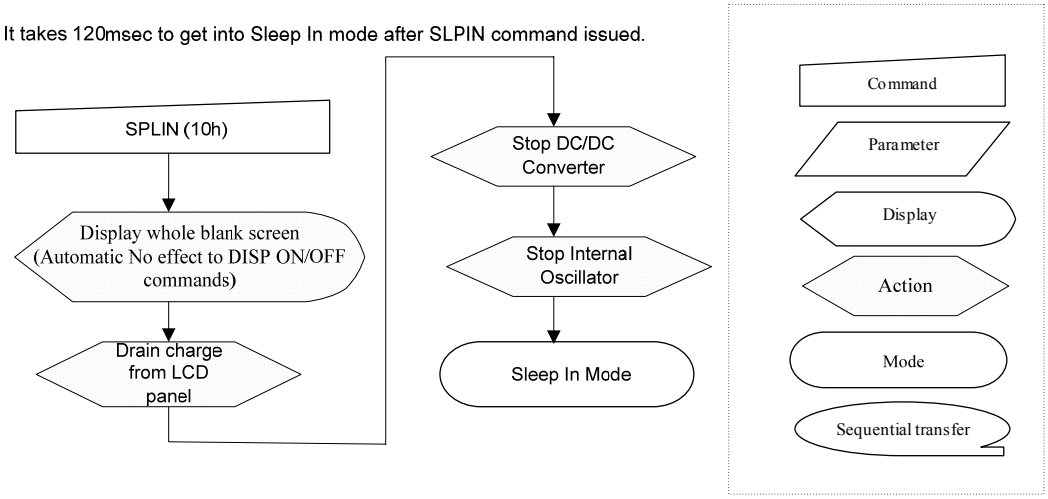
Flow Chart



6.2.11. Enter Sleep Mode (10h)

<table>
<tr><td>10h</td><td colspan="13">Enter Sleep Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped
 

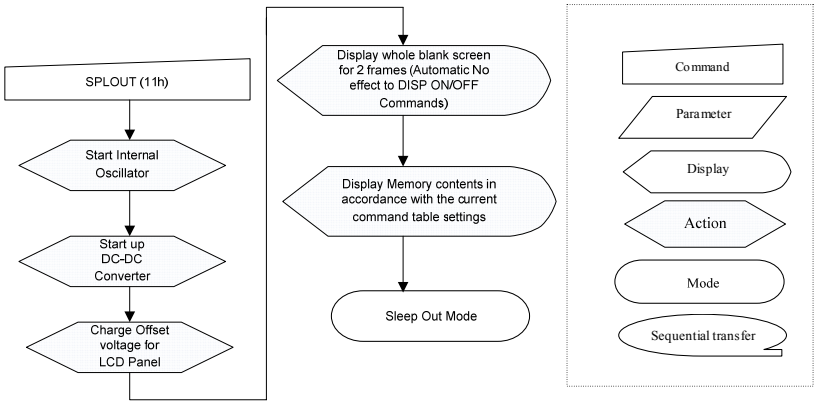
MCU interface and memory are still working and the memory keeps its contents.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

It takes 120msec to get into Sleep In mode after SLPIN command issued.
SPLIN (10h)
Display whole blank screen (Automatic No effect to DISP ON/OFF commands)
Drain charge from LCD panel
Stop DC/DC Converter
Stop Internal Oscillator
Sleep In Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.12. Sleep Out Mode (11h)

<table>
<tr><td>11h</td><td colspan="13">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	 SPLOUT (11h) Start Internal Oscillator Start up DC-DC Converter Charge Offset voltage for LCD Panel Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands) Display Memory contents in accordance with the current command table settings Sleep Out Mode Command Parameter Display Action Mode Sequential transfer

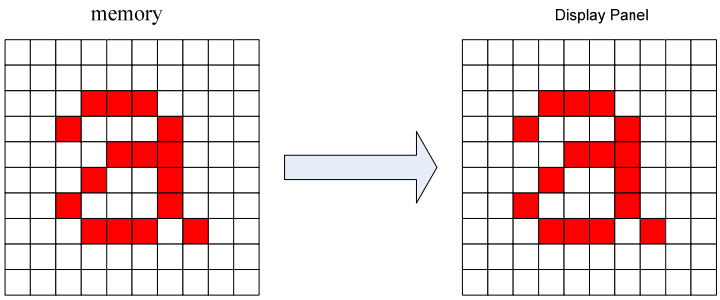
6.2.13. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

6.2.14. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

6.2.15. Display Inversion OFF (20h)

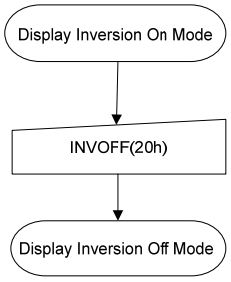
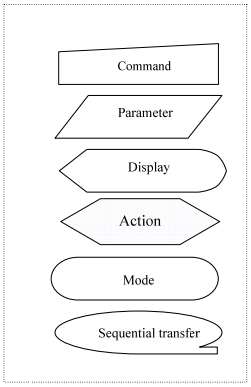
20h	Display Inversion OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status.  X = Don't care												
Restriction	This command has no effect when module already is inversion OFF mode.												

Register Availability

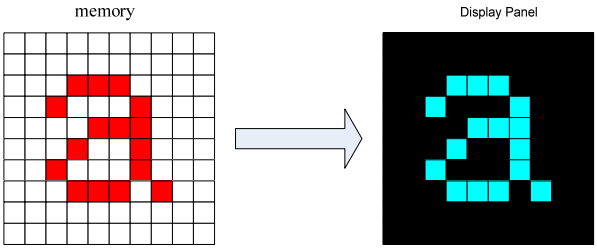
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

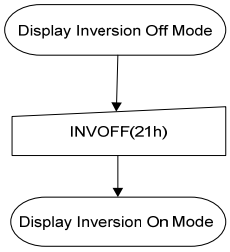
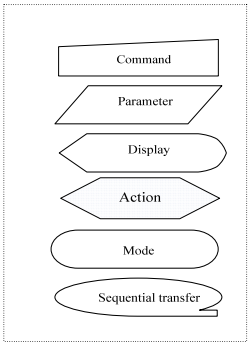
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

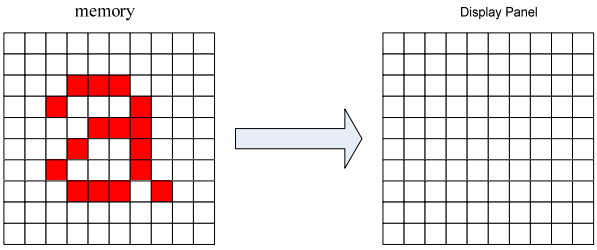
Flow Chart	 Display Inversion On Mode INVOFF(20h) Display Inversion Off Mode  Command Parameter Display Action Mode Sequential transfer

6.2.16. Display Inversion ON (21h)

<table>
<tr><td>21h</td><td colspan="13">Display Inversion ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn’t change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>SW Reset</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
</table>

Flow Chart	 Display Inversion Off Mode INVOFF(21h) Display Inversion On Mode  Command Parameter Display Action Mode Sequential transfer

6.2.17. Display OFF (28h)

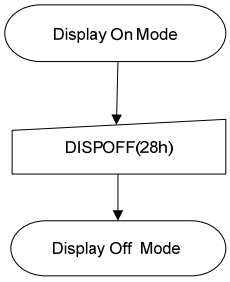
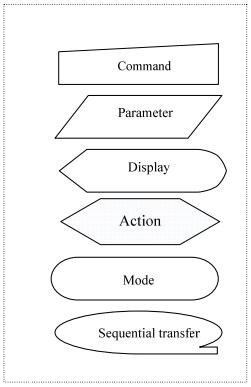
28h	Display OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care												
Restriction	This command has no effect when module is already in display off mode.												

Register Availability

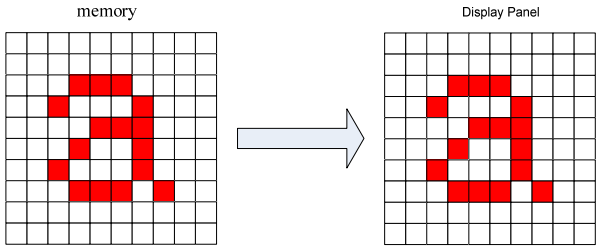
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

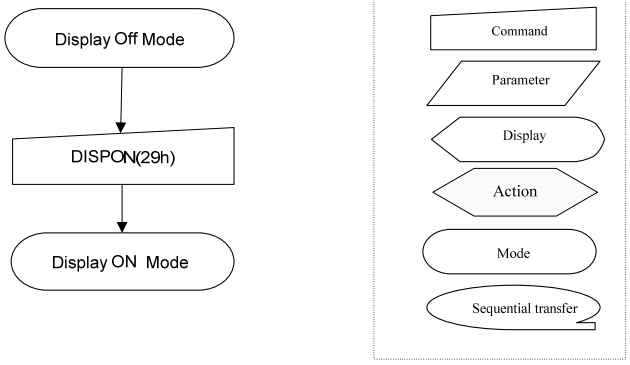
Default

Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart	 Display On Mode DISPOFF(28h) Display Off Mode  Command Parameter Display Action Mode Sequential transfer

6.2.18. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="12">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>SW Reset</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
</table>

Flow Chart	

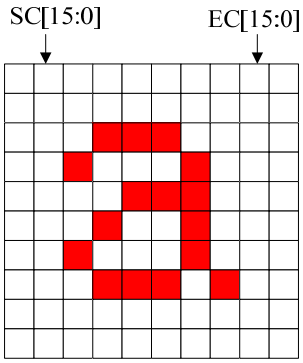
Display Off Mode
DISPON(29h)
Display ON Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.19. Column Address Set (2Ah)

2Ah	Column Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
1st Parameter	1	1	↑	XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2nd Parameter	1	1	↑	XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3rd Parameter	1	1	↑	XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory..



X = Don't care

Restriction

SC [15:0] always must be equal to or less than EC [15:0].

Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored

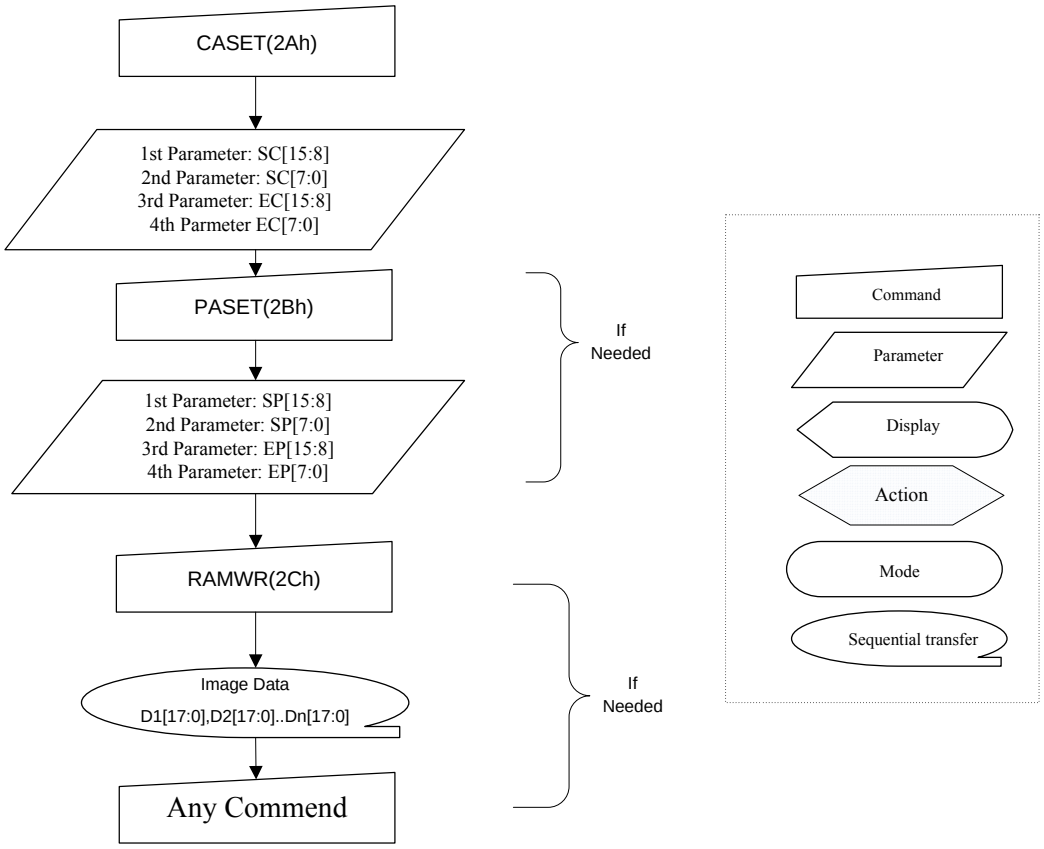
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh
SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=00EFh
		If MADCTL's B5 = 1: EC [15:0]=013Fh
HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh

Flow Chart

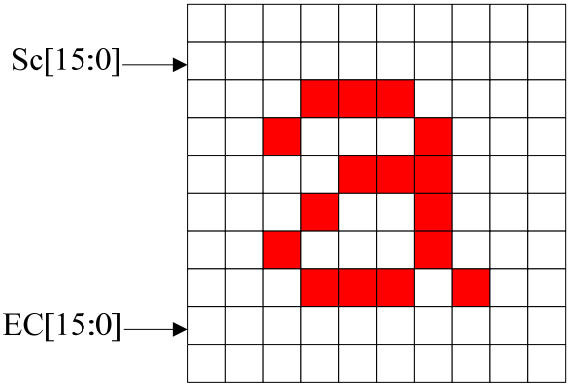

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
If Needed
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
If Needed
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.20. Row Address Set (2Bh)

2Bh	Row Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1
2nd Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
3rd Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	

Description

This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.



X = Don't care

Restriction

SP [15:0] always must be equal to or less than EP [15:0]

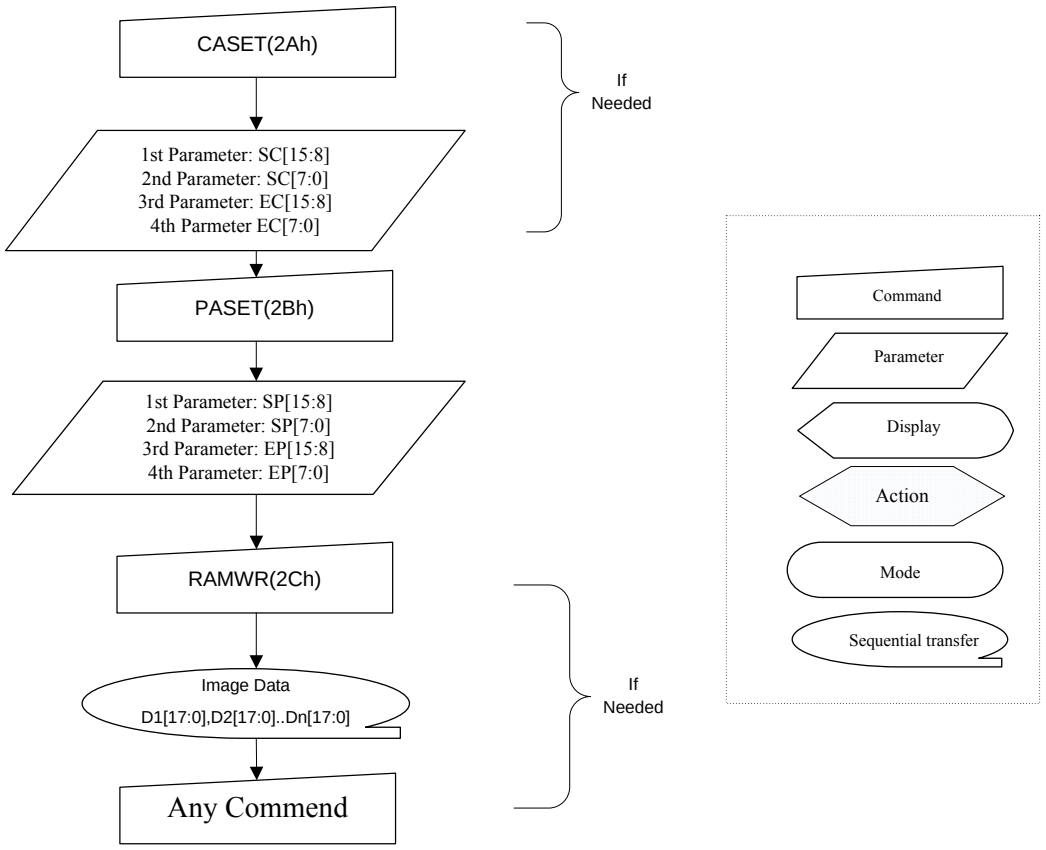
Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
Power On Sequence	SP [15:0]=0000h	EP [15:0]=013Fh
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=013Fh
		If MADCTL's B5 = 1: EP [15:0]=0EFh
HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh

Flow Chart	

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
If Needed
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
If Needed
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.21. Memory Write (2Ch)

2Ch	Memory Write												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX

Description

This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] isstored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.

Restriction

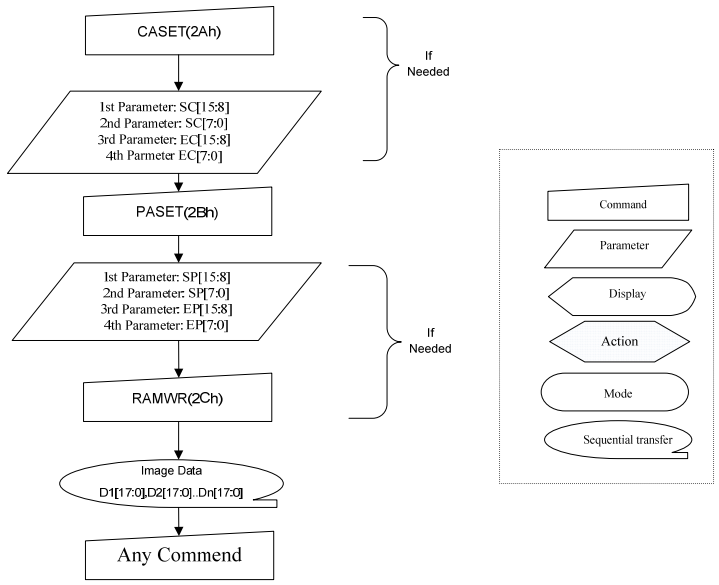
In all color modes, there is no restriction on length of parameters.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart	 CASET(2Ah) 1st Parameter: SC[15:8] 2nd Parameter: SC[7:0] 3rd Parameter: EC[15:8] 4th Parmeter EC[7:0] If Needed PASET(2Bh) 1st Parameter: SP[15:8] 2nd Parameter: SP[7:0] 3rd Parameter: EP[15:8] 4th Parameter: EP[7:0] If Needed RAMWR(2Ch) Image Data D1[17:0],D2[17:0]..Dn[17:0] Any Commend Command Parameter Display Action Mode Sequential transfer

6.2.22. Memory Read (2Eh)

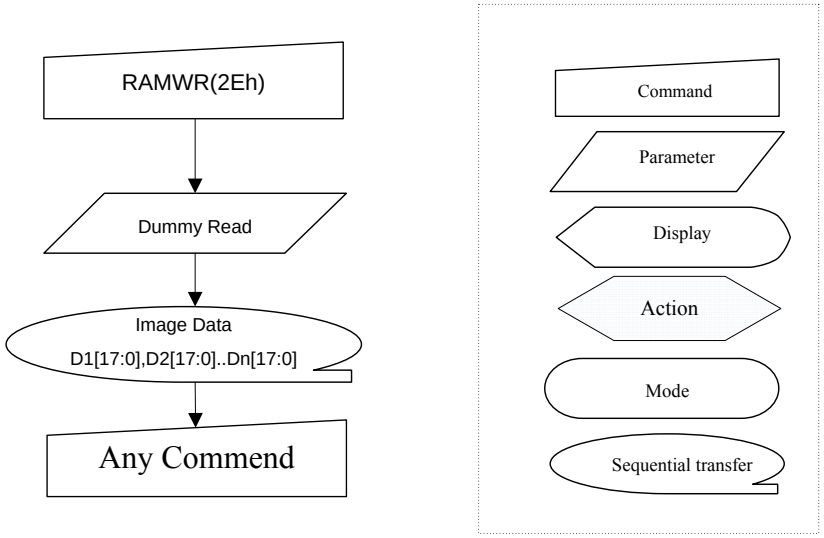
2Eh	Memory Read												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	D1 [17:0]									XX
:	1	↑	1	Dx [17:0]									XX
(N+1)th Parameter	1	↑	1	Dn [17:0]									XX
Description	This command transfers image data from GC9301's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands. If Memory Access control B5 = 0: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command. If Memory Access Control B5 = 1: The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.												
Restriction	There is no restriction on length of parameters.												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

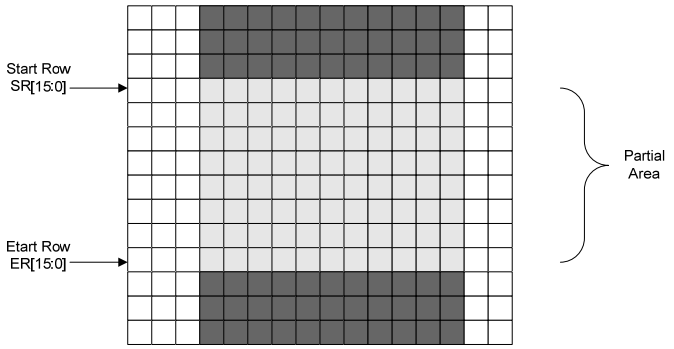
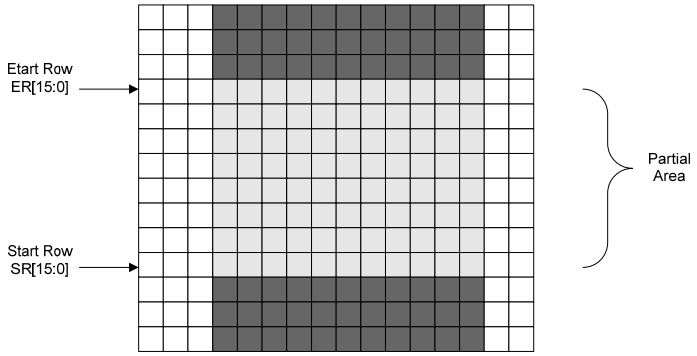
Default

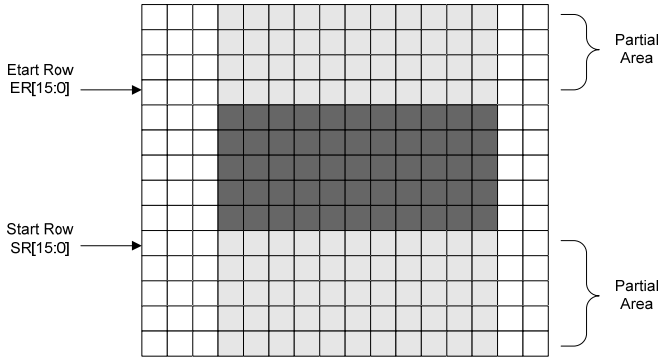
Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is set randomly
HW Reset	Contents of memory is set randomly

Flow Chart	

RAMWR(2Eh)
Dummy Read
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.23. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-												



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction

SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

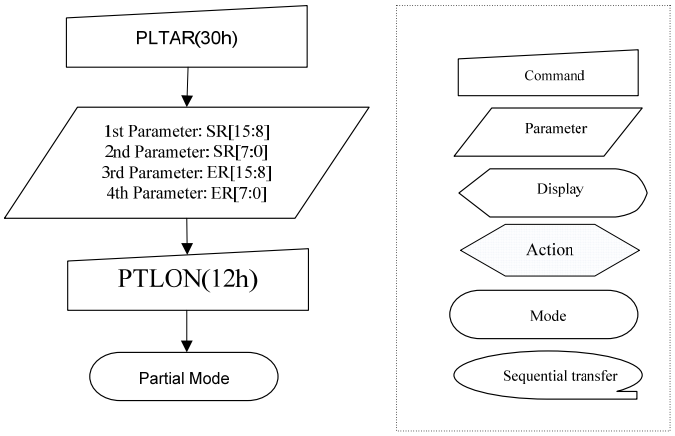
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

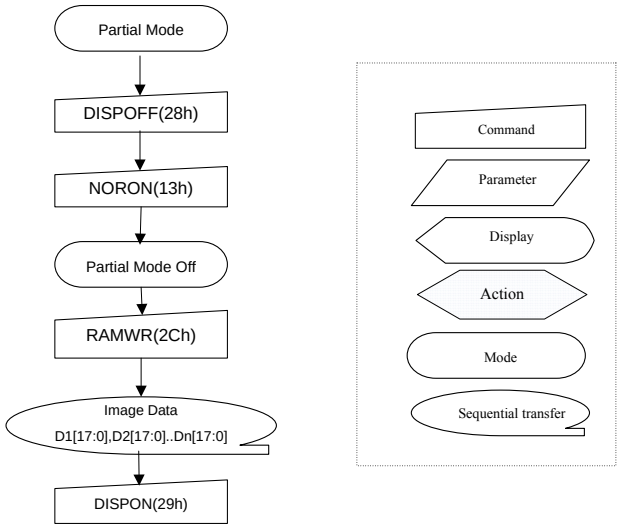
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h013Fh
SW Reset	16'h0000h	16'h013Fh
HW Reset	16'h0000h	16'h013Fh

Flow Chart

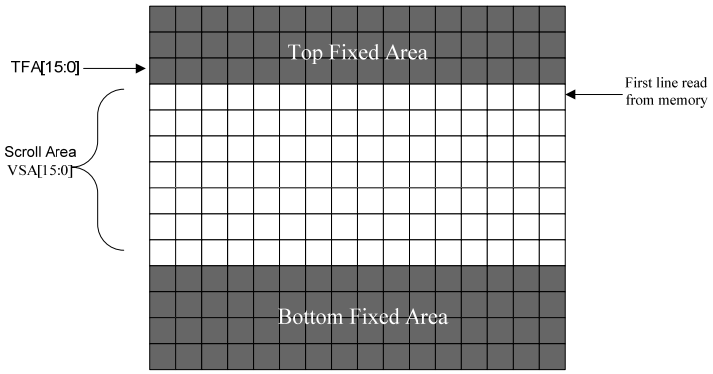
1. To Enter Partial Mode

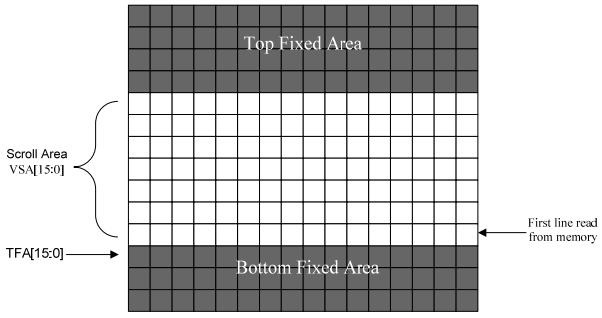


2. To Leave Partial Mode



6.2.24. Vertical Scrolling Definition (33h)

<table>
<tr><td>33h</td><td colspan="13">Vertical Scrolling Definition</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>33h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">TFA [15:8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">TFA [7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VSA [15:8]</td><td>01</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">VSA [7:0]</td><td>40</td></tr>
<tr><td>Description</td><td colspan="13">This command defines the Vertical Scrolling Area of the display.
When MADCTL B4=0
The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.
 

When MADCTL B4=1
The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.
 

X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
</table>

Register Availability

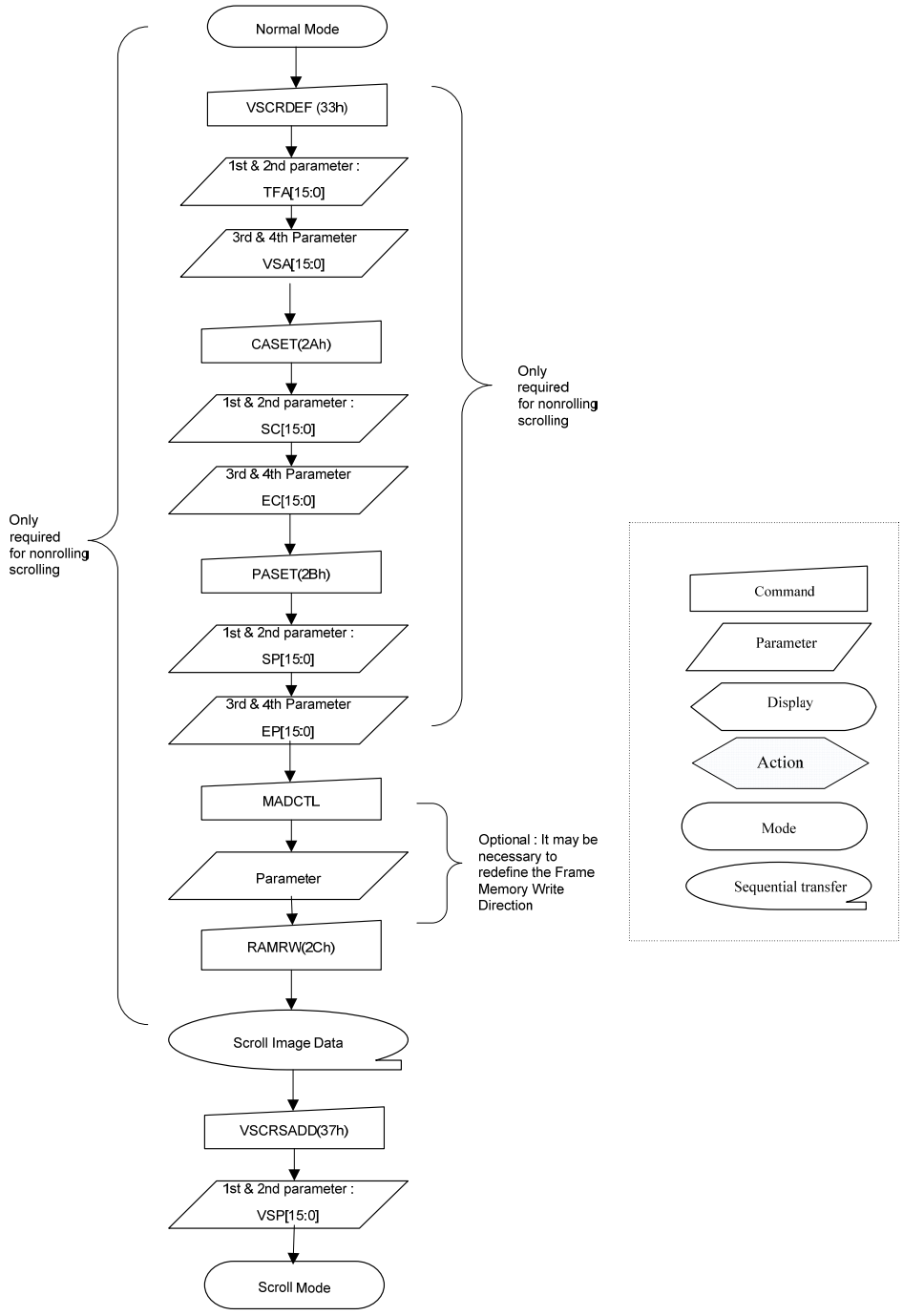
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16'h0000h	16'h0140h
SW Reset	16'h0000h	16'h0140h
HW Reset	16'h0000h	16'h0140h

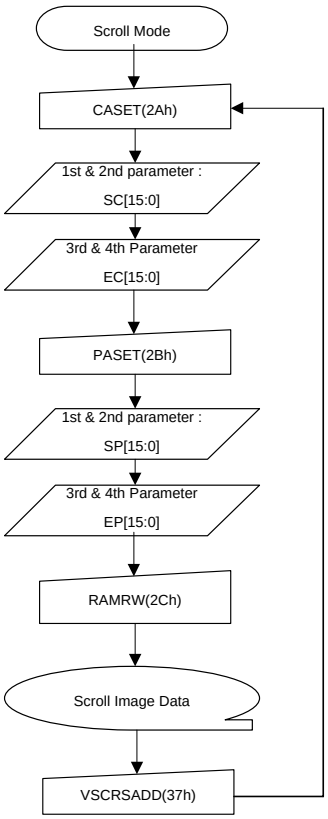
Flow Chart

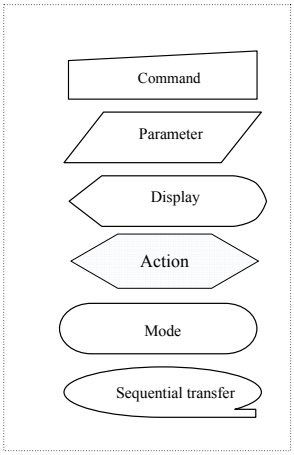
1. To enter Vertical Scroll Mode :



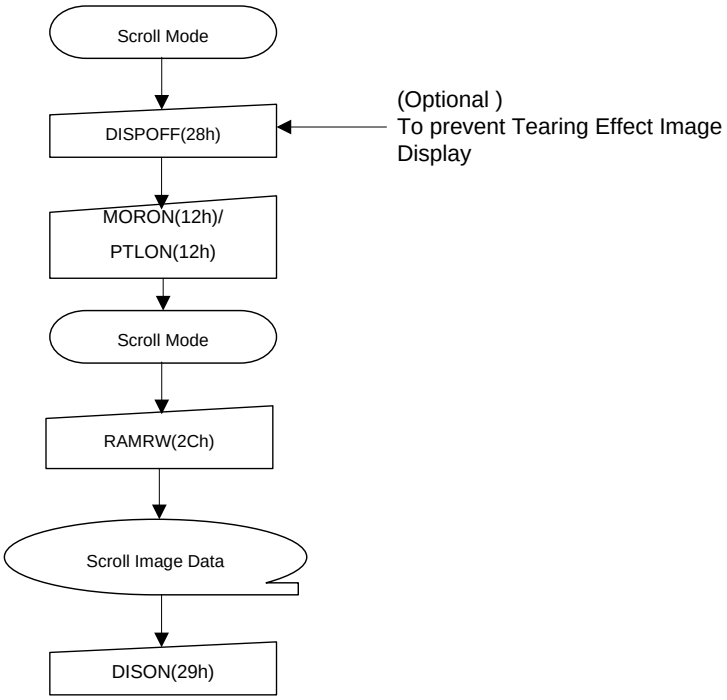
Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



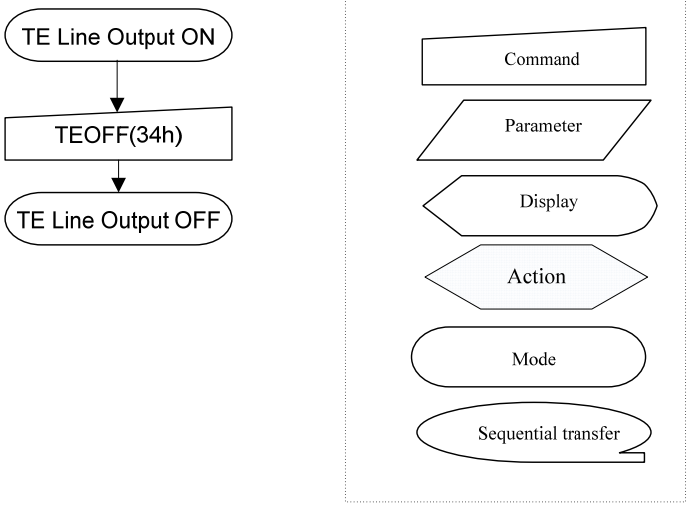


3.To Leave Vertical Scroll Mode:



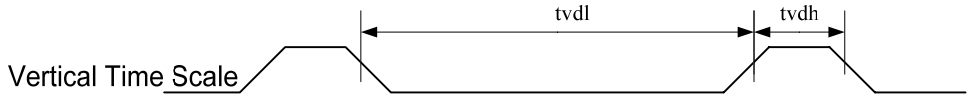
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

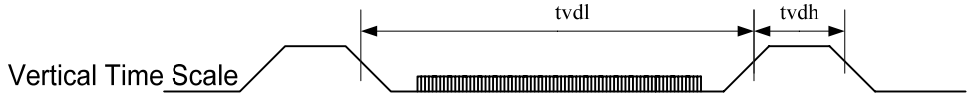
6.2.25. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

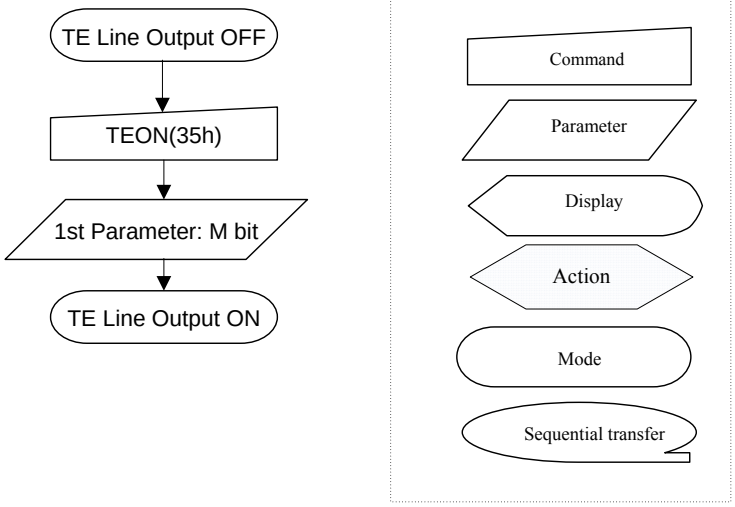
6.2.26. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

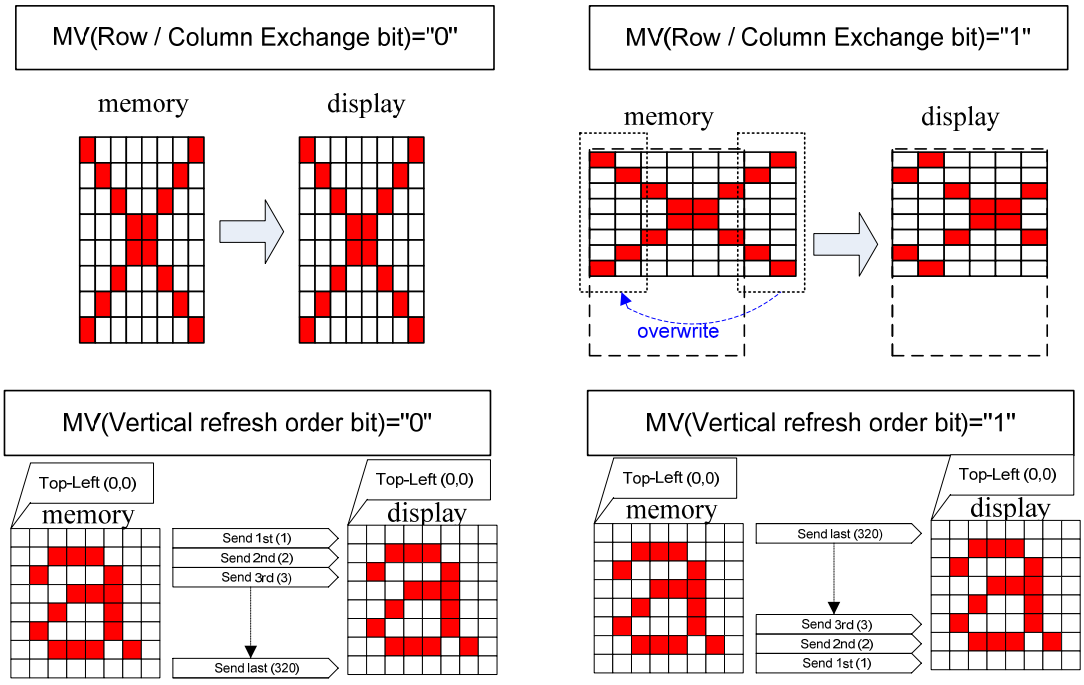
When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

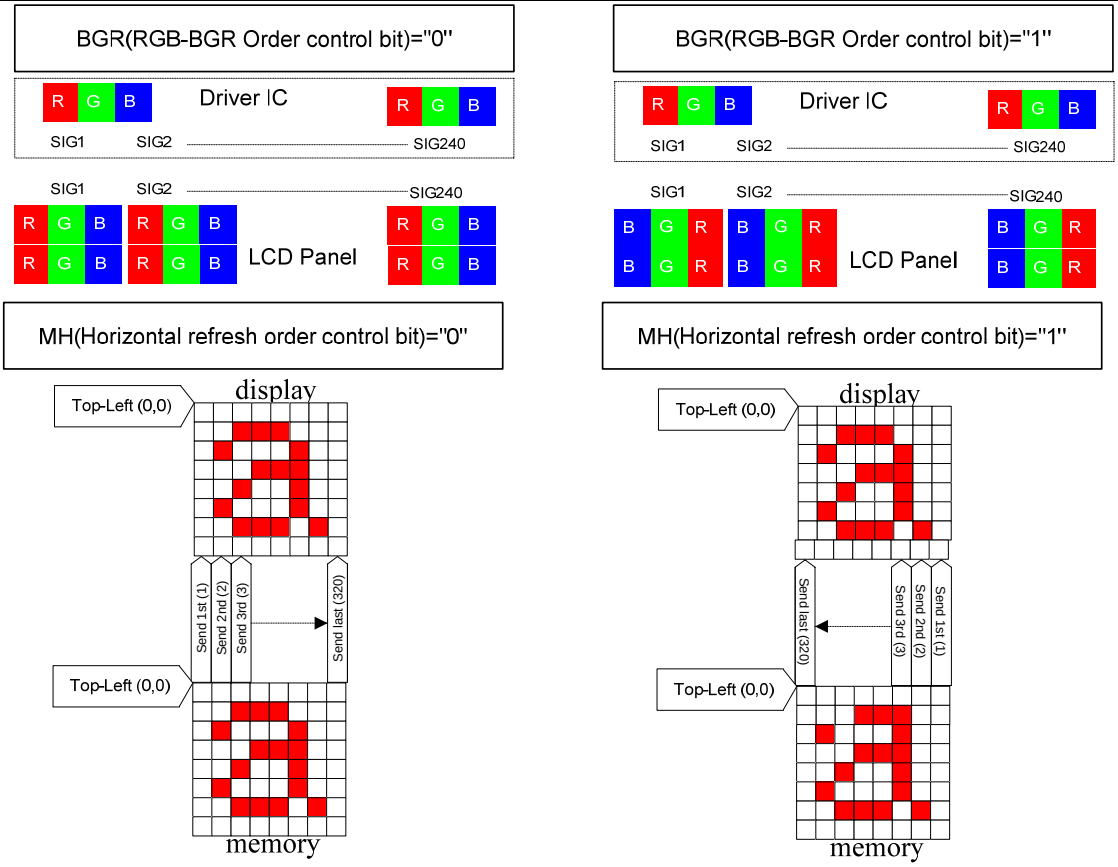
Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.27. Tearing Effect Line ON (36h)

<table>
<tr><td>36h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>BGR</td><td>MH</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits control MCU to memory write/read direction.</td></tr>
<tr><td>MX</td><td>Column Address Order</td></tr>
<tr><td>MV</td><td>Row / Column Exchange</td></tr>
<tr><td>ML</td><td>Vertical Refresh Order</td><td>LCD vertical refresh direction control.</td></tr>
<tr><td>BGR</td><td>RGB-BGR Order</td><td>Color selector switch control
(0=RGB color filter panel, 1=BGR color filter panel)</td></tr>
<tr><td>MH</td><td>Horizontal Refresh ORDER</td><td>LCD horizontal refreshing direction control.</td></tr>
</table>
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.
X = Don’t care.

</td></tr>
</table>



Note: Top-Left (0,0) means a physical memory location.

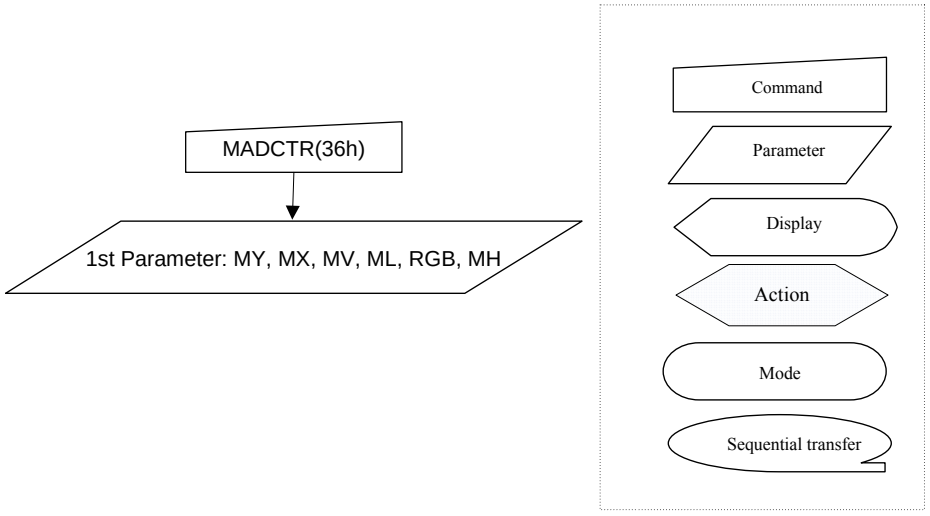
Restriction	This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

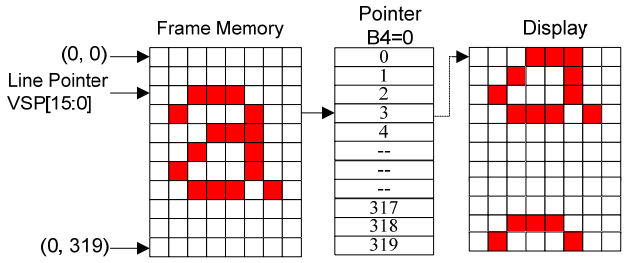
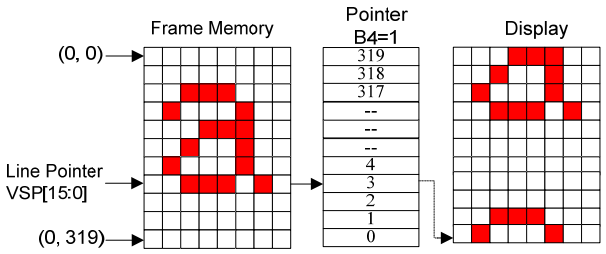
Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart	

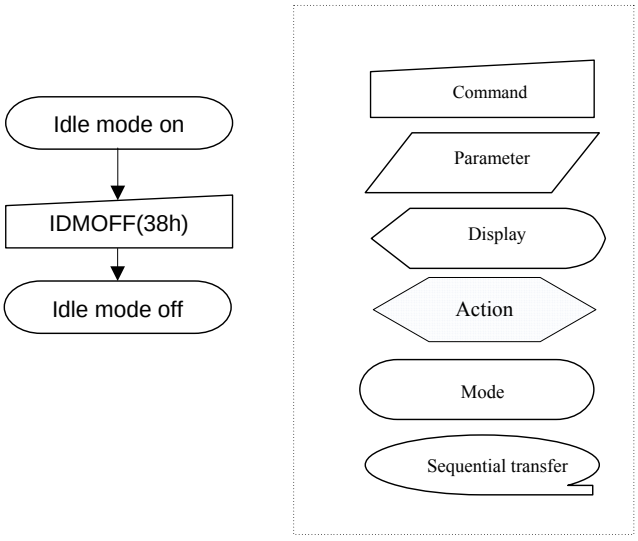
MADCTR(36h)
1st Parameter: MY, MX, MV, ML, RGB, MH
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.28. Vertical Scrolling Start Address (37h)

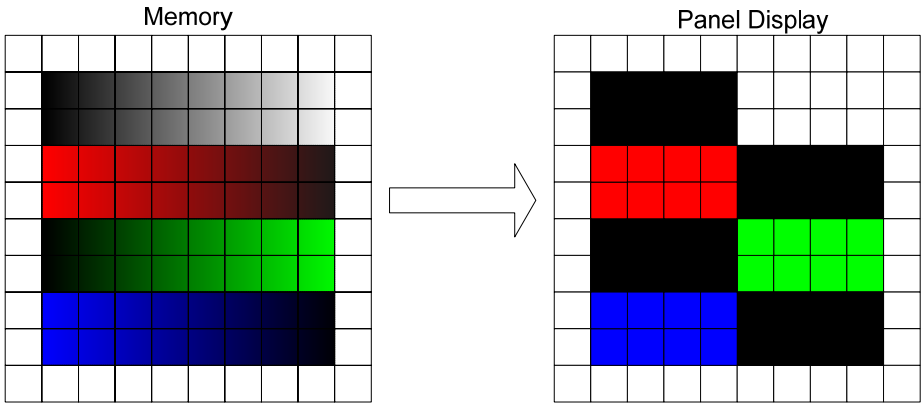
37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								00
2nd Parameter	1	1	↑	XX	VSP [7:0]								00
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:- When MADCTL B4=0 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.  When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.  *Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.* *(2) This command is ignored when the GC9301 enters Partial mode.* X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already ON												

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.29. Idle Mode OFF (38h)

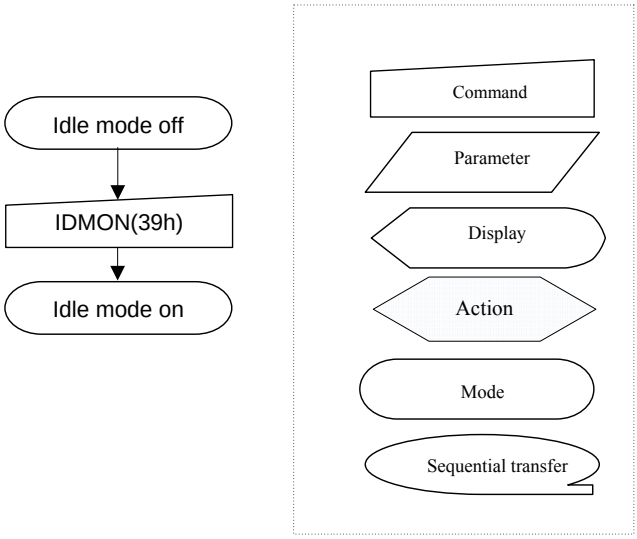
<table>
<tr><td>38h</td><td colspan="13">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.30. Idle Mode ON (39h)

<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
 
<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1 R0</td><td>G5 G4 G3 G2 G1 G0</td><td>B5 B4 B3 B2 B1 B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

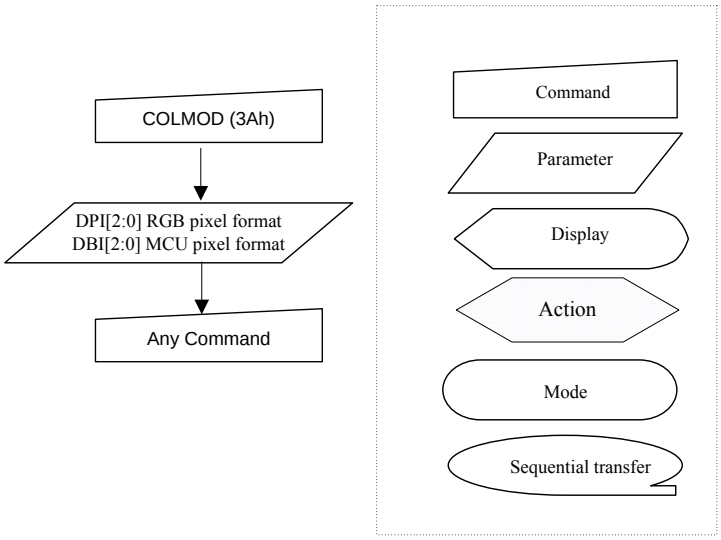
<table>
<tr><td>Default</td><td>

Status	Default Value
Power On Sequence	Idle mode OFF
SW Reset	Idle mode OFF
HW Reset	Idle mode OFF

</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

6.2.31. COLMOD: Pixel Format Set (3Ah)

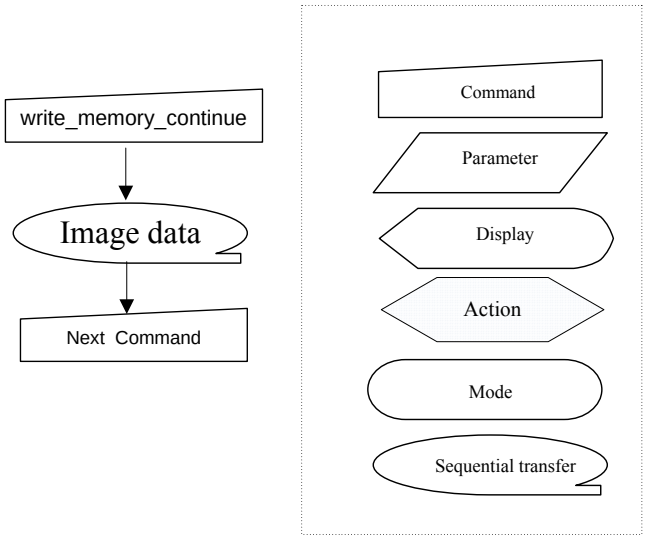
<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">DPI [2:0]</td><td>0</td><td colspan="3">DBI [2:0]</td><td>0</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
If using RGB Interface must selection serial interface.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

COLMOD (3Ah)
DPI[2:0] RGB pixel format
DBI[2:0] MCU pixel format
Any Command
Command
Parameter
Display
Action
Mode
Sequential transfer

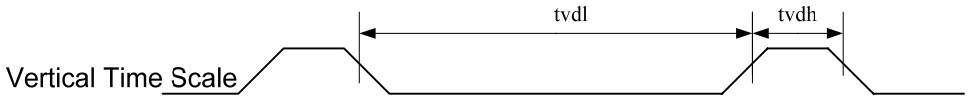
6.2.32. write_memory_continue (3Ch)

3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1 [17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
Xth Parameter	1	1	↑	D1 [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
Nth Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.												

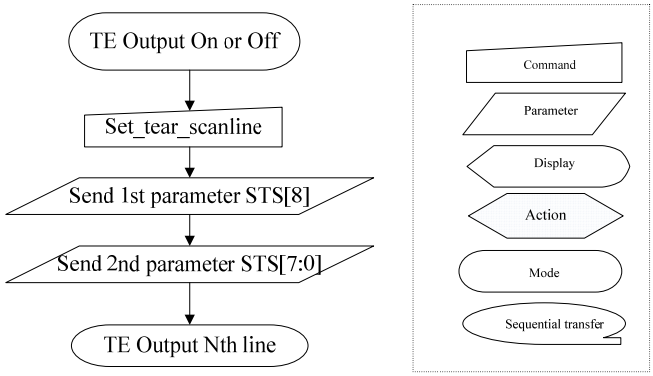
<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Random value</td></tr>
<tr><td>SW Reset</td><td>No change</td></tr>
<tr><td>HW Reset</td><td>No change</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

6.2.33. Set_Tear_Scanline (44h)

<table>
<tr><td>44h</td><td colspan="13">Set_Tear_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>STS [7]</td><td>STS [6]</td><td>STS [5]</td><td>STS [4]</td><td>STS [3]</td><td>STS [2]</td><td>STS [1]</td><td>STS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS. The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.
 

Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr><tr><td>SW Reset</td><td>STS [8:0]=0000h</td></tr><tr><td>HW Reset</td><td>STS [8:0]=0000h</td></tr></table></td></tr>
</table>

Flow Chart	

TE Output On or Off
Set_tear_scanline
Send 1st parameter STS[8]
Send 2nd parameter STS[7:0]
TE Output Nth line
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.34. Get_Scanline (45h)

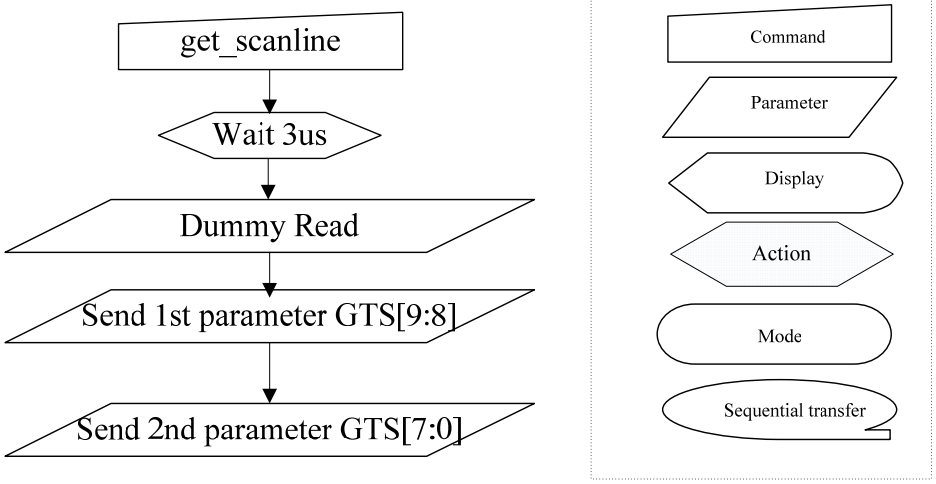
45h	Get_Scanline												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
1st Parameter	1	↑	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00
2nd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00
Description	The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

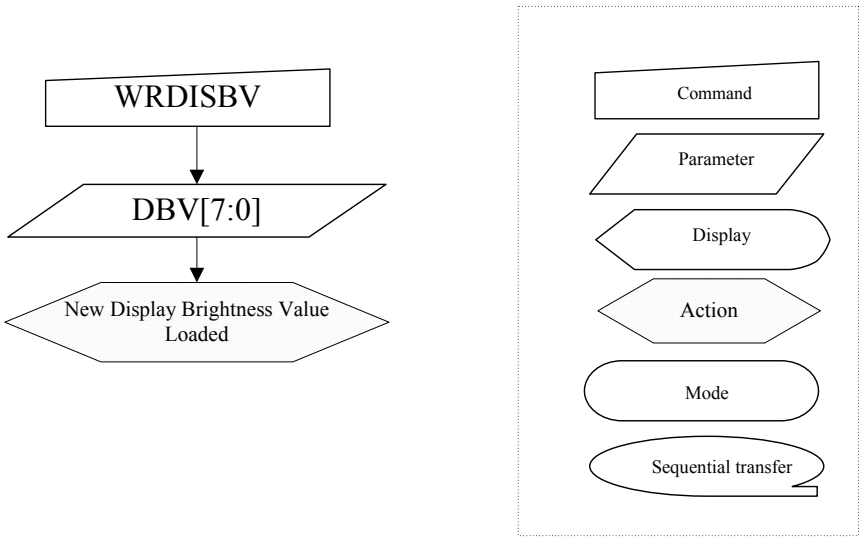
Default

Status	Default Value
Power On Sequence	GTS [9:0]=0000h
SW Reset	GTS [9:0]=0000h
HW Reset	GTS [9:0]=0000h

Flow Chart	

get_scanline
Wait 3us
Dummy Read
Send 1st parameter GTS[9:8]
Send 2nd parameter GTS[7:0]
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.35. Write Display Brightness (51h)

<table>
<tr><td>51h</td><td colspan="13">Write Display Brightness</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>DBV[7]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>DBV[3]</td><td>DBV[6]</td><td>DBV[5]</td><td>DBV[4]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to adjust the brightness value of the display.
It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.
In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>SW Reset</td><td>DBV [7:0]= 8’h00</td></tr><tr><td>HW Reset</td><td>DBV [7:0]= 8’h00</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.36. Read Display Brightness (52h)

52h	Read Display Brightness												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[6]	DBV[5]	DBV[4]	00
Description	This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

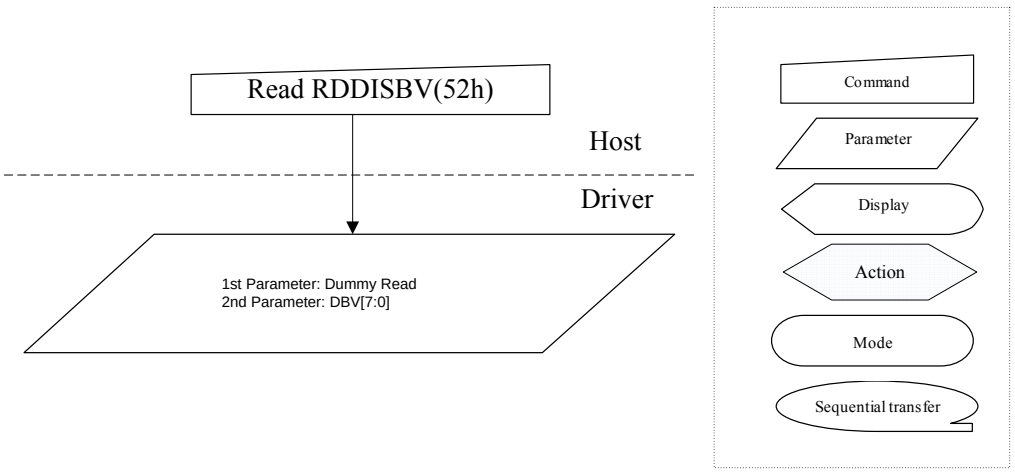
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DBV [7:0]= 8'h00
SW Reset	DBV [7:0]= 8'h00
HW Reset	DBV [7:0]= 8'h00

Flow Chart



6.2.37. Write CTRL Display (53h)

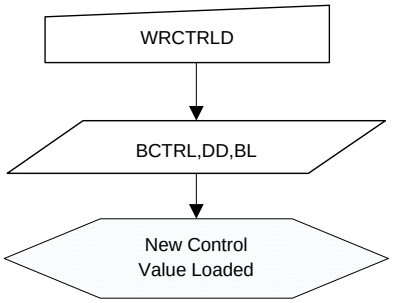
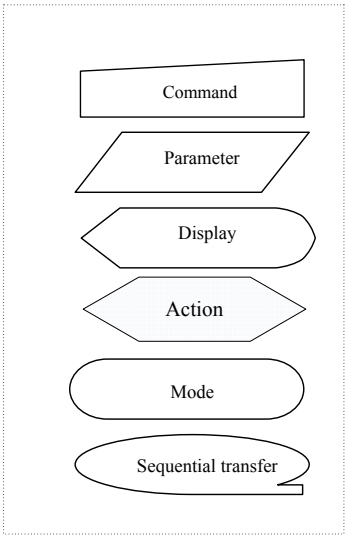
53h	Write CTRL Display												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
1st Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command is used to return brightness setting. **BCTRL**: Brightness Control Block On/Off, '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the DBV[7..0] parameters.) **DD**: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on **BL**: Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On												
Restriction	The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI. Only 2nd parameter is sent on DSI (The 1st parameter is not sent).												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1'b0	1'b0	1'b0
SW Reset	1'b0	1'b0	1'b0
HW Reset	1'b0	1'b0	1'b0

Flow Chart	 

6.2.38. Read CTRL Display (54h)

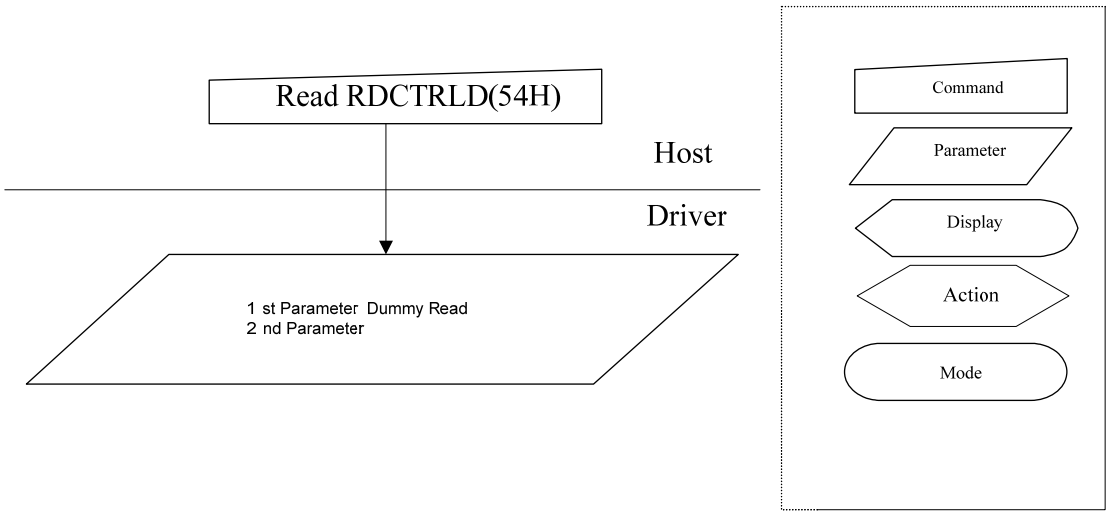
54h	Read CTRL Display												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00
Description	This command is used to control display brightness. **BCTRL**: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) **DD**: Display Dimming, only for manual brightness setting DD = 0: Display Dimming is off DD = 1: Display Dimming is on **BL**: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 →1 or 1→ 0. When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.												
Restriction	None												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	BCTRL	DD	BL
Power On Sequence	1’b0	1’b0	1’b0
SW Reset	1’b0	1’b0	1’b0
HW Reset	1’b0	1’b0	1’b0

Flow Chart	

Read RDCTRLD(54H)
Host
Driver
1 st Parameter Dummy Read
2 nd Parameter
Command
Parameter
Display
Action
Mode

6.2.39. Read ID1 (DAh)

DAh	Read ID1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID1 [7:0]								XX
Description	This read byte identifies the LCD module's manufacturer ID and it is specified by User The 1st parameter is dummy data. The 2nd parameter is LCD module's manufacturer ID. X = Don't care												
Restriction	None												

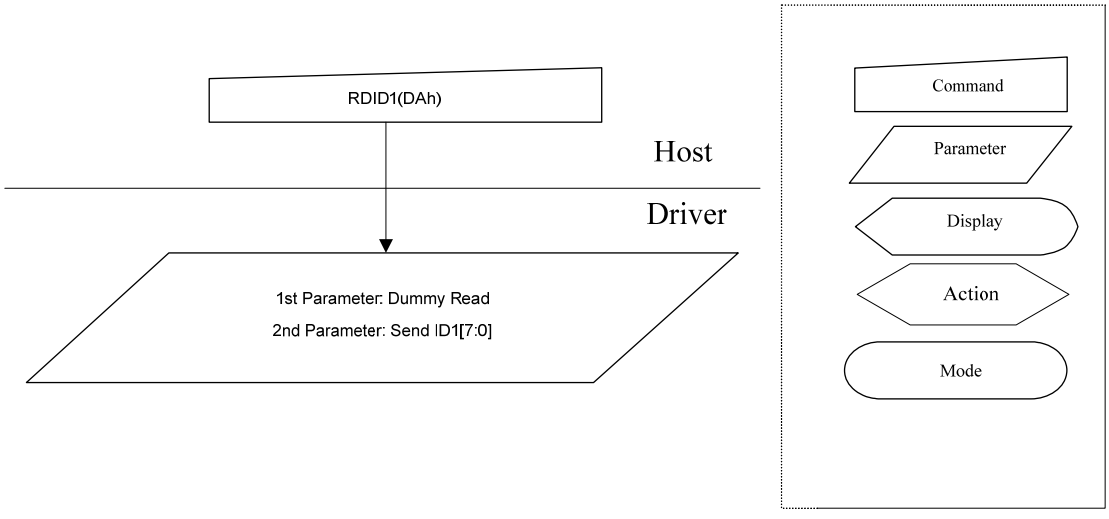
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



6.2.40. Read ID2 (DBh)

DBh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID2 [7:0]								XX
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID2 can be programmed by MTP function. X = Don't care												
Restriction	None												

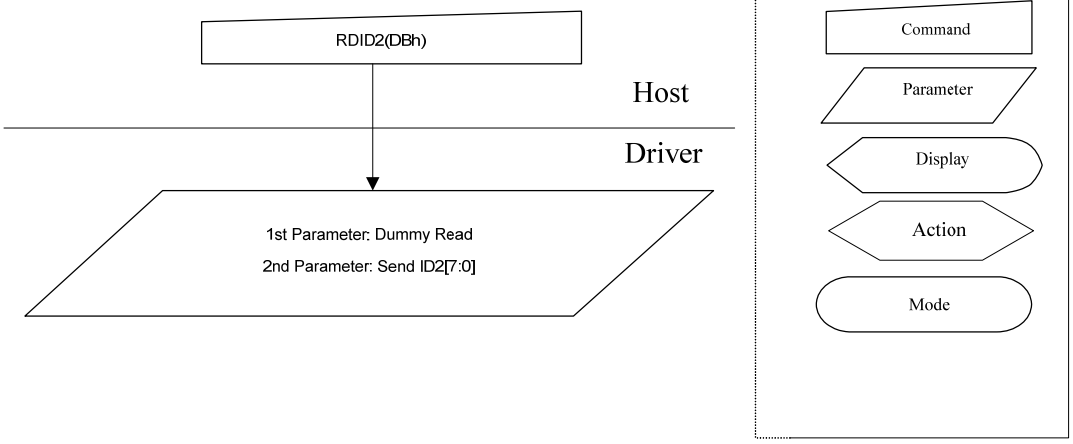
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



6.2.41. Read ID3 (DCh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								XX
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

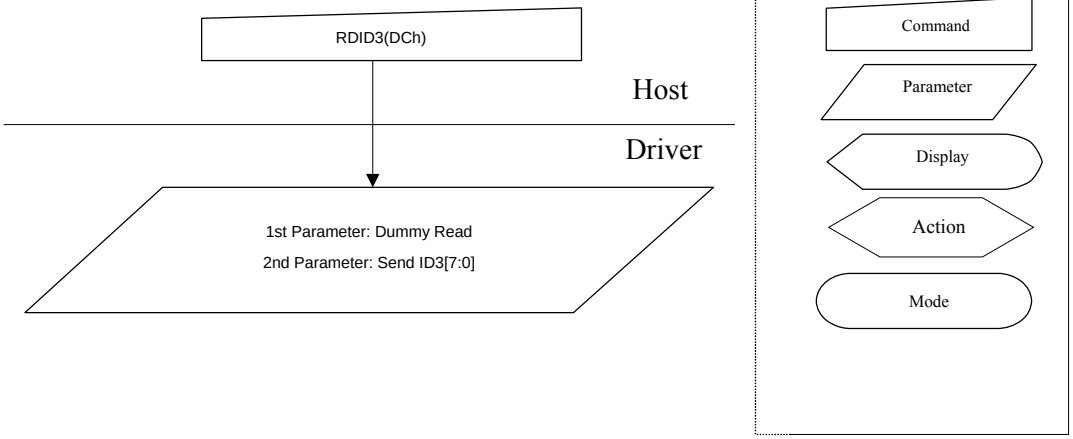
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h00h	MTP value
SW Reset	8'h00h	MTP value
HW Reset	8'h00h	MTP value

Flow Chart



6.3. Description of Level 2 Command

6.3.1. RGB Interface Signal Control (B0h)

B0h	RGB Interface Signal Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
1st Parameter	1	1	↑	XX	0	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40
Description	Sets the operation status of the display interface. The setting becomes effective as soon as the command is received. **EPL**: DE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface) **DPL**: DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time) **HSPL**: HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) **VSPL**: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) **RCM [1:0]:** RGB interface selection (refer to the RGB interface section).												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value				
	RCM[1:0]	VSPL	HSPL	DPL	EPL
Power On Sequence	2'b10	1'b0	1'b0	1'b0	1'b0
SW Reset	2'b10	1'b0	1'b0	1'b0	1'b0
HW Reset	2'b10	1'b0	1'b0	1'b0	1'b0

6.3.2. Display Inversion Control (B4h)

B4h	Display Inversion Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h
1st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	0	0	00
Description	Display inversion mode set NLA: 0 = Line inversion; 1 = Frame inversion The register inv_ctl in Level 3 Command can also control display inversion mode set .The display inversion mode is set by the latest value setting of NLA or inv_ctl												
Restriction	EXTC should be high to enable this command												
Register Availability	Normal Mode On, Idle Mode Off, Sleep Out: Yes Normal Mode On, Idle Mode On, Sleep Out: Yes Partial Mode On, Idle Mode Off, Sleep Out: Yes Partial Mode On, Idle Mode On, Sleep Out: Yes Sleep In: Yes												
Default	Power On Sequence: 1'b0 SW Reset: 1'b0 HW Reset: 1'b0												

6.3.3.Blanking Porch Control (B5h)

B5h	Blanking Porch Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	VFP [6:0]							02
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							02
3rd Parameter	1	1	↑	XX	0	0	0	HFP [4:0]					0A
4th Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	126
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HFP [4:0] / HBP [4:0]: The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.

HFP [4:0] HBP [4:0]	Number of HSYNC of front/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="4">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HFP [4:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>SW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
<tr><td>HW Reset</td><td>7’h02h</td><td>7’h02h</td><td>5’h0Ah</td><td>5’h14h</td></tr>
</table>
</td></tr>
</table>

6.3.4. Display Function Control (B6h)

B6h	Display Function Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	1	↑	XX	REV	GS	SS	SM	ISC [3:0]				82
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						27

Description

SS: Select the shift direction of outputs from the source driver.

SS	Source Output Scan Direction
0	S1 → S720
1	S7201 → S

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

REV: Select whether the liquid crystal type is normally white type or normally black type.

REV	Liquid crystal type
0	Normally black
1	Normally white

ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] ="10" to select interval scan. Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.

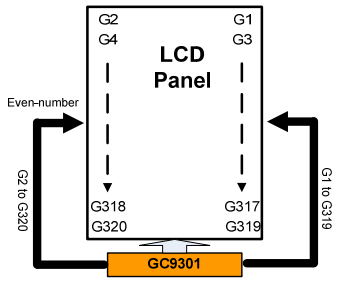
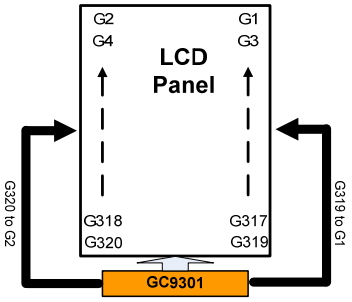
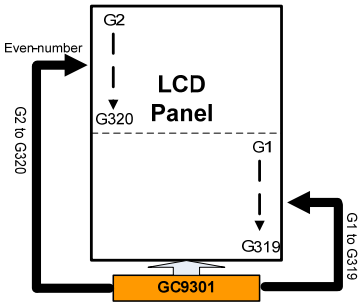
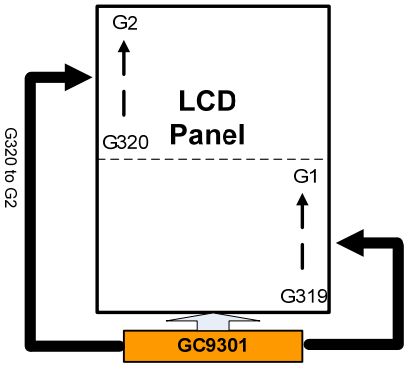
ISC [3:0]	Scan Cycle	f_{FLM} = 60Hz
0000	1 frame	17ms
0001	3 frames	51ms
0010	5 frames	85ms
0011	7 frames	119ms
0100	9 frames	153ms
0101	11 frames	187ms
0110	13 frames	221ms
0111	15 frames	255ms
1000	17 frames	289ms
1001	19 frames	323ms
1010	21 frames	357ms
1011	23 frames	391ms
1100	25 frames	425ms
1101	27 frames	459ms
1110	29 frames	493ms
1111	31 frames	527ms

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1→G320
1	G320→G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module

.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1 G2 G3 G4 → G317 G318 G319 G320
0	1		G320 G319 G 318 G317 → G4 G3 G2 G1
1	0		G1 G3 →G317 G319 →G2 G4 → G318 G320
1	1		G320 G318 → G4 G2 → G319 G317 → G3 G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

NL [5:0]						LCD Drive Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
Others						Setting prohibited

Restriction

EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value			
	VFP [6:0]	VBP [6:0]	HFP [4:0]	HBP [4:0]
Power On Sequence	7'h02h	7'h02h	5'h0Ah	5'h14h
SW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h
HW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h

6.3.5. Read ID4 (D3h)

D3h	Read ID4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00
3rd Parameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93
4th Parameter	1	↑	1	XX	0	1	0	0	0	0	0	0	41
Description	Read IC device code. The 1st parameter is dummy read period. The 2nd parameter means the IC version. The 3rd and 4th parameter mean the IC model name.												
Restriction	EXTC should be high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	24'h009341h
SW Reset	24'h009341h
HW Reset	24'h009341h

6.3.6. Interface Control (F6h)

<table>
<tr><td>F6h</td><td colspan="13">Interface Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>F6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>BGR_ EOR</td><td>X</td><td>X</td><td>WE MODE</td><td>01</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">MDT[1:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">DM [1:0]</td><td>RM</td><td>RIM</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
MDT [1:0]: Select the method of display data transferring.
WEMODE: Memory write control
WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.
WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
DM [1:0]: Select the display operation mode.
<table>
<tr><th>DM[1]</th><th>DM[0]</th><th>Display Operation Mode</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock operation</td></tr>
<tr><td>0</td><td>1</td><td>RGB Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>VSYNC interface Mode</td></tr>
<tr><td>1</td><td>1</td><td>Setting disabled</td></tr>
</table>
RM: Select the interface to access the GRAM.
Set RM to “1” when writing display data by the RGB interface.
<table>
<tr><th>RM</th><th>Interface for RAM Access</th></tr>
<tr><td>0</td><td>System interface/VSYNC interface</td></tr>
<tr><td>1</td><td>RGB interface</td></tr>
</table>
RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.
<table>
<tr><th>RIM</th><th>COLMOD [6:4]</th><th>RGB Interface Mode</th></tr>
<tr><td rowspan="2">0</td><td>110 (262K color)</td><td>18- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>101 (65K color)</td><td>16- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>1</td><td>(262K color)</td><td>6- bit RGB interface (3 transfer/pixel)</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default

Status	Default Value					
	BGR_ EOR	WE MODE	MDT[1:0]	DM [1:0]	RM	RIM
Power On Sequence	1'b0	1'b1	2'b00	2'b00	1'b0	1'b0
SW Reset	1'b0	1'b1	2'b00	2'b00	1'b0	1'b0
HW Reset	1'b0	1'b1	2'b00	2'b00	1'b0	1'b0

6.4. Description of Level 3 Command

6.4.1. Frame Rate and Display Inversion Control (A3h)

<table>
<tr><td>A3h</td><td colspan="13">Frame Rate and Display Inversion Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>A3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>Inv_ctl</td><td>X</td><td>X</td><td>X</td><td colspan="4">frs[3:0]</td><td>84</td></tr>
<tr><td>Description</td><td colspan="13">Display inversion mode set
<table><tr><th>Inv_ctl</th><th>Inversion</th></tr><tr><td>1</td><td>Line inversion</td></tr><tr><td>0</td><td>Frame inversion</td></tr></table>The register NAL in Level 2 Command can also control display inversion mode set .The display inversion mode is set by the latest value setting of NLA or inv_ctl .
fRS[3:0] Set the frame rate when the internal resistor is used for oscillator circuit.
<table><tr><th>frs<3:0></th><th>Frame Rate</th></tr><tr><td>0</td><td>50</td></tr><tr><td>1</td><td>60</td></tr><tr><td>10</td><td>70</td></tr><tr><td>11</td><td>80</td></tr><tr><td>100</td><td>90</td></tr><tr><td>101</td><td>100</td></tr><tr><td>110</td><td>110</td></tr><tr><td>111</td><td>120</td></tr><tr><td>1000</td><td>130</td></tr><tr><td>1001</td><td>140</td></tr><tr><td>1010</td><td>150</td></tr><tr><td>1011</td><td>160</td></tr><tr><td>1100</td><td>170</td></tr><tr><td>1101</td><td>180</td></tr><tr><td>1110</td><td>190</td></tr><tr><td>1111</td><td>200</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
</table>

Default

Status	Default Value	
	Inv_ctl	frs[3:0]
Power On Sequence	1'b1	4'h4
SW Reset	1'b1	4'h4
HW Reset	1'b1	4'h4

6.4.2. Power control 1 (A4h)

A4h	Power control 1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	0	0	1	0	0	A4h
1st Parameter	1	1	1	XX	VCIRE	X	X	X	VRH[3:0]				8C

Description

VRH[3:0] Set the amplifying rate (1.6 ~ 1.9) of Vci applied to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.

VCIRE=0	External reference voltage Vci (default)
VCIRE =1	Internal reference voltage 2.5V

VCIRE=0		VCIRE=1	
VRH[3:0]	**VREG1OUT**	**VRH[3:0]**	**VREG1OUT**
4'h0	Halt	4'h0	Halt
4'h1	vci*1.90	4'h1	2.5*1.90=4.750v
4'h2	vci*1.90	4'h2	2.5*1.90=4.750v
4'h3	vci*1.90	4'h3	2.5*1.90=4.750v
4'h4	vci*1.90	4'h4	2.5*1.90=4.750v
4'h5	vci*1.90	4'h5	2.5*1.90=4.750v
4'h6	vci*1.90	4'h6	2.5*1.90=4.750v
4'h7	vci*1.90	4'h7	2.5*1.90=4.750v
4'h8	vci*1.60	4'h8	2.5*1.60=4.000v
4'h9	vci*1.65	4'h9	2.5*1.65=4.125v
4'h10	vci*1.70	4'h10	2.5*1.70=4.250v
4'h11	vci*1.75	4'h11	2.5*1.75=4.375v
4'h12	vci*1.80	4'h12	2.5*1.80=4.500v
4'h13	vci*1.85	4'h13	2.5*1.85=4.625v
4'h14	vci*1.90	4'h14	2.5*1.90=4.750v
4'h15	vci*1.90	4'h15	2.5*1.90=4.750v

Restriction: Inter_command should be set high to enable this command

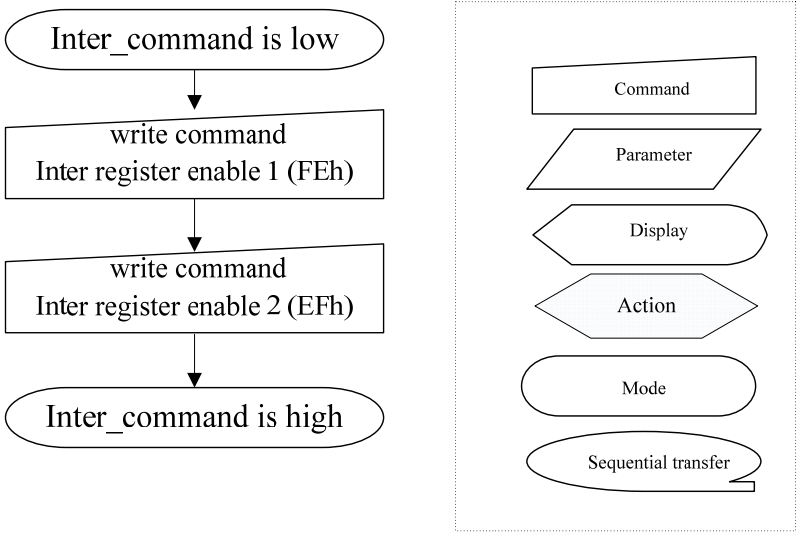
Default

Status	Default Value	
	VCIRE	VRH[3:0]
Power On Sequence	1'b0	4'hc
SW Reset	1'b0	4'hc
HW Reset	1'b0	4'hc

6.4.3. Power control 2 (EDh)

<table>
<tr><td>EDh</td><td colspan="13">Power control 2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>EDh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td colspan="3">dc1[2:0]</td><td colspan="3">dc0[2:0]</td><td>0A</td></tr>
<tr><td>Description</td><td colspan="13">DC0[2:0]: Selects the operating frequency of the step-up circuit 1. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.
DC1[2:0]: Selects the operating frequency of the step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.
<table>
<tr><th>DC 02</th><th>DC 01</th><th>DC 00</th><th>Step-up circuit1 step-up frequency (fDCDC1)</th><th></th><th>DC 12</th><th>DC 11</th><th>DC 10</th><th>Step-up circuit1 step-up frequency (fDCDC1)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Fosc</td><td></td><td>0</td><td>0</td><td>0</td><td>Fosc/4</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Fosc/2</td><td></td><td>0</td><td>0</td><td>1</td><td>Fosc/8</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Fosc/4</td><td></td><td>0</td><td>1</td><td>0</td><td>Fosc/16</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Fosc/8</td><td></td><td>0</td><td>1</td><td>1</td><td>Fosc/32</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Fosc/16</td><td></td><td>1</td><td>0</td><td>0</td><td>Fosc/64</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Fosc/32</td><td></td><td>1</td><td>0</td><td>1</td><td>Fosc/128</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Fosc/64</td><td></td><td>1</td><td>1</td><td>0</td><td>Fosc/256</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Halt step-up circuit 1</td><td></td><td>1</td><td>1</td><td>1</td><td>Halt step-up circuit 2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

6.4.4. Inter register enable 2 (EFh)

EFh	Inter register enable 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.5. SET_GAMMA1 (F0h)

<table>
<tr><td>F0h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KP1[2:0]</td><td>X</td><td colspan="3">KP0[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">KP1-0[2:0] : γgradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KP1[2:0]</th><th>KP0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h0</td><td>3’h0</td></tr><tr><td>SW Reset</td><td>3’h0</td><td>3’h0</td></tr><tr><td>HW Reset</td><td>3’h0</td><td>3’h0</td></tr></table></td></tr>
</table>

6.4.6. SET_GAMMA2 (F1h)

<table>
<tr><td>F1h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>F1h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KP3[2:0]</td><td>X</td><td colspan="3">KP2[2:0]</td><td>55</td></tr>
<tr><td>Description</td><td colspan="13">kP3-2[2:0] : γgradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KP3[2:0]</th><th>KP2[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h5</td><td>3’h5</td></tr><tr><td>SW Reset</td><td>3’h5</td><td>3’h5</td></tr><tr><td>HW Reset</td><td>3’h5</td><td>3’h5</td></tr></table></td></tr>
</table>

8.4.7. SET_GAMMA3 (F2h)

<table>
<tr><td>F2h</td><td colspan="13">SET_GAMMA3</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>F2h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KP5[2:0]</td><td>X</td><td colspan="3">KP4[2:0]</td><td>07</td></tr>
<tr><td>Description</td><td colspan="13">kP5-4[2:0] : γgradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KP5[2:0]</th><th>KP4[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h0</td><td>3’h7</td></tr><tr><td>SW Reset</td><td>3’h0</td><td>3’h7</td></tr><tr><td>HW Reset</td><td>3’h0</td><td>3’h7</td></tr></table></td></tr>
</table>

6.4.8. SET_GAMMA4 (F3h)

<table>
<tr><td>F3h</td><td colspan="13">SET_GAMMA4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>F3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">RP1[2:0]</td><td>X</td><td colspan="3">RP0[2:0]</td><td>52</td></tr>
<tr><td>Description</td><td colspan="13">RP1-0[2:0] : γgradient adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>RP1[2:0]</th><th>RP0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h5</td><td>3’h2</td></tr><tr><td>SW Reset</td><td>3’h5</td><td>3’h2</td></tr><tr><td>HW Reset</td><td>3’h5</td><td>3’h2</td></tr></table></td></tr>
</table>

6.4.9. SET_GAMMA5 (F4h)

<table>
<tr><td>F4h</td><td colspan="13">SET_GAMMA5</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>F4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="4">VRP0[3:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VRP0[4:0] : γ amplitude adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VRP0[3:0]</th></tr><tr><td>Power On Sequence</td><td>4’h00</td></tr><tr><td>SW Reset</td><td>4’h00</td></tr><tr><td>HW Reset</td><td>4’h00</td></tr></table></td></tr>
</table>

6.4.10. SET_GAMMA6 (F5h)

<table>
<tr><td>F5h</td><td colspan="13">SET_GAMMA6</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>F5h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">VRP1[3:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VRP1[4:0] : γ amplitude adjustment register for positive polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VRP1[3:0]</th></tr><tr><td>Power On Sequence</td><td>4’h00</td></tr><tr><td>SW Reset</td><td>4’h00</td></tr><tr><td>HW Reset</td><td>4’h00</td></tr></table></td></tr>
</table>

6.4.11. SET_GAMMA7(F7h)

<table>
<tr><td>F7h</td><td colspan="13">SET_GAMMA7</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>F7h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KN1[2:0]</td><td>X</td><td colspan="3">KN0[2:0]</td><td>22</td></tr>
<tr><td>Description</td><td colspan="13">KN1-0[2:0] : γfine adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KN1[2:0]</th><th>KN0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’b0</td><td>3’h7</td></tr><tr><td>SW Reset</td><td>3’b0</td><td>3’h7</td></tr><tr><td>HW Reset</td><td>3’b0</td><td>3’h7</td></tr></table></td></tr>
</table>

6.4.12. SET_GAMMA8(F8h)

<table>
<tr><td>F8h</td><td colspan="13">SET_GAMMA8</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>F8h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KN3[2:0]</td><td>X</td><td colspan="3">KN2[2:0]</td><td>22</td></tr>
<tr><td>Description</td><td colspan="13">KN3-2[2:0] : γfine adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KN1[2:0]</th><th>KN0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h2</td><td>3’h2</td></tr><tr><td>SW Reset</td><td>3’h2</td><td>3’h2</td></tr><tr><td>HW Reset</td><td>3’h2</td><td>3’h2</td></tr></table></td></tr>
</table>

6.4.13. SET_GAMMA9(F9h)

<table>
<tr><td>F9h</td><td colspan="13">SET_GAMMA9</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>F9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">KN5[2:0]</td><td>X</td><td colspan="3">KN4[2:0]</td><td>77</td></tr>
<tr><td>Description</td><td colspan="13">KN5-4[2:0] : γfine adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>KN1[2:0]</th><th>KN0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h7</td><td>3’h7</td></tr><tr><td>SW Reset</td><td>3’h7</td><td>3’h7</td></tr><tr><td>HW Reset</td><td>3’h7</td><td>3’h7</td></tr></table></td></tr>
</table>

6.4.14. SET_GAMMA10(FAh)

<table>
<tr><td>FAh</td><td colspan="13">SET_GAMMA10</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>FAh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td colspan="3">RN1[2:0]</td><td>X</td><td colspan="3">RN0[2:0]</td><td>25</td></tr>
<tr><td>Description</td><td colspan="13">RN1-0[2:0] : γgradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>RN1[2:0]</th><th>RN0[2:0]</th></tr><tr><td>Power On Sequence</td><td>3’h2</td><td>3’h5</td></tr><tr><td>SW Reset</td><td>3’h2</td><td>3’h5</td></tr><tr><td>HW Reset</td><td>3’h2</td><td>3’h5</td></tr></table></td></tr>
</table>

6.4.15. SET_GAMMA11(FBh)

FBh	SET_GAMMA11												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	0	1	1	FBh
1st Parameter	1	1	↑	XX	X	X	X	X	VRN0[3:0]				00
Description	VRN0[3:0] : γamplitude adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VRN0[3:0]
Power On Sequence	4'h0
SW Reset	4'h0
HW Reset	4'h0

6.4.16. SET_GAMMA12(FCh)

<table>
<tr><td>FCh</td><td colspan="13">SET_GAMMA12</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>FCh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td colspan="5">VRN1[4:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">VRN1[4:0] : γamplitude adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th>Default Value</th></tr><tr><th>VRN1[4:0]</th></tr><tr><td>Power On Sequence</td><td>4’h00</td></tr><tr><td>SW Reset</td><td>4’h00</td></tr><tr><td>HW Reset</td><td>4’h00</td></tr></table></td></tr>
</table>

6.4.17. Power control 3 (FDh)

FDh	Power control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	0	1	FDh
1st Parameter	1	1	↑	XX	X	X	VCM[5:0]						1C

Description

VCM[5:0] Set the internal VcomH voltage.

VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH (*VREG1OUT)	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	VCOMH (*VREG1OUT)
0	0	0	0	0	0	0.685	1	0	0	0	0	0	0.845
0	0	0	0	0	1	0.690	1	0	0	0	0	1	0.850
0	0	0	0	1	0	0.695	1	0	0	0	1	0	0.855
0	0	0	0	1	1	0.700	1	0	0	0	1	1	0.860
0	0	0	1	0	0	0.705	1	0	0	1	0	0	0.865
0	0	0	1	0	1	0.710	1	0	0	1	0	1	0.870
0	0	0	1	1	0	0.715	1	0	0	1	1	0	0.875
0	0	0	1	1	1	0.720	1	0	0	1	1	1	0.880
0	0	1	0	0	0	0.725	1	0	1	0	0	0	0.885
0	0	1	0	0	1	0.730	1	0	1	0	0	1	0.890
0	0	1	0	1	0	0.735	1	0	1	0	1	0	0.895
0	0	1	0	1	1	0.740	1	0	1	0	1	1	0.900
0	0	1	1	0	0	0.745	1	0	1	1	0	0	0.905
0	0	1	1	0	1	0.750	1	0	1	1	0	1	0.910
0	0	1	1	1	0	0.755	1	0	1	1	1	0	0.915
0	0	1	1	1	1	0.760	1	0	1	1	1	1	0.920
0	1	0	0	0	0	0.765	1	1	0	0	0	0	0.925
0	1	0	0	0	1	0.770	1	1	0	0	0	1	0.930
0	1	0	0	1	0	0.775	1	1	0	0	1	0	0.935
0	1	0	0	1	1	0.780	1	1	0	0	1	1	0.940
0	1	0	1	0	0	0.785	1	1	0	1	0	0	0.945
0	1	0	1	0	1	0.790	1	1	0	1	0	1	0.950
0	1	0	1	1	0	0.795	1	1	0	1	1	0	0.955
0	1	0	1	1	1	0.800	1	1	0	1	1	1	0.960
0	1	1	0	0	0	0.805	1	1	1	0	0	0	0.965
0	1	1	0	0	1	0.810	1	1	1	0	0	1	0.970
0	1	1	0	1	0	0.815	1	1	1	0	1	0	0.975
0	1	1	0	1	1	0.820	1	1	1	0	1	1	0.980
0	1	1	1	0	0	0.825	1	1	1	1	0	0	0.985
0	1	1	1	0	1	0.830	1	1	1	1	0	1	0.990
0	1	1	1	1	0	0.835	1	1	1	1	1	0	0.995
0	1	1	1	1	1	0.840	1	1	1	1	1	1	1.000

Restriction	Inter_command should be set high to enable this command

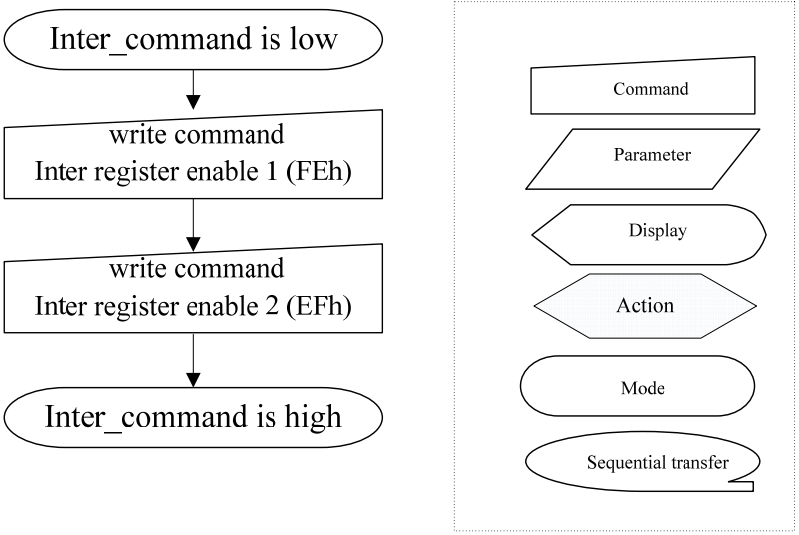
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VCM[5:0]
Power On Sequence	5'h1c
SW Reset	5'h1c
HW Reset	5'h1c

6.4.18. Inter register enable 1 (FEh)

<table>
<tr><td>FEh</td><td colspan="13">Inter register enable 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FEh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.19. Power control 4 (FFh)

FFh	Power control 4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	1	1	1	1	FFh
1st Parameter	1	1	↑	XX	X	X	X	VDV[4:0]					16

Description

VDV[4:0] Select the factor of VREG1OUT to set the amplitude of Vcom alternating voltage from 0.70 to 1.24 xVREG1OUT .

VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude (*VREG1OUT)	VDV4	VDV3	VDV2	VDV1	VDV0	VCOM Amplitude (*VREG1OUT)
0	0	0	0	0	0.70	1	0	0	0	0	0.94
0	0	0	0	1	0.72	1	0	0	0	1	0.96
0	0	0	1	0	0.74	1	0	0	1	0	0.98
0	0	0	1	1	0.76	1	0	0	1	1	1.00
0	0	1	0	0	0.78	1	0	1	0	0	1.02
0	0	1	0	1	0.80	1	0	1	0	1	1.04
0	0	1	1	0	0.82	1	0	1	1	0	1.06
0	0	1	1	1	0.84	1	0	1	1	1	1.08
0	1	0	0	0	0.86	1	1	0	0	0	1.10
0	1	0	0	1	0.88	1	1	0	0	1	1.12
0	1	0	1	0	0.90	1	1	0	1	0	1.14
0	1	0	1	1	0.92	1	1	0	1	1	1.16
0	1	1	0	0	0.94	1	1	1	0	0	1.18
0	1	1	0	1	0.96	1	1	1	0	1	1.20
0	1	1	1	0	0.98	1	1	1	1	0	1.22
0	1	1	1	1	1.00	1	1	1	1	1	1.24

Restriction: Inter_command should be set high to enable this command

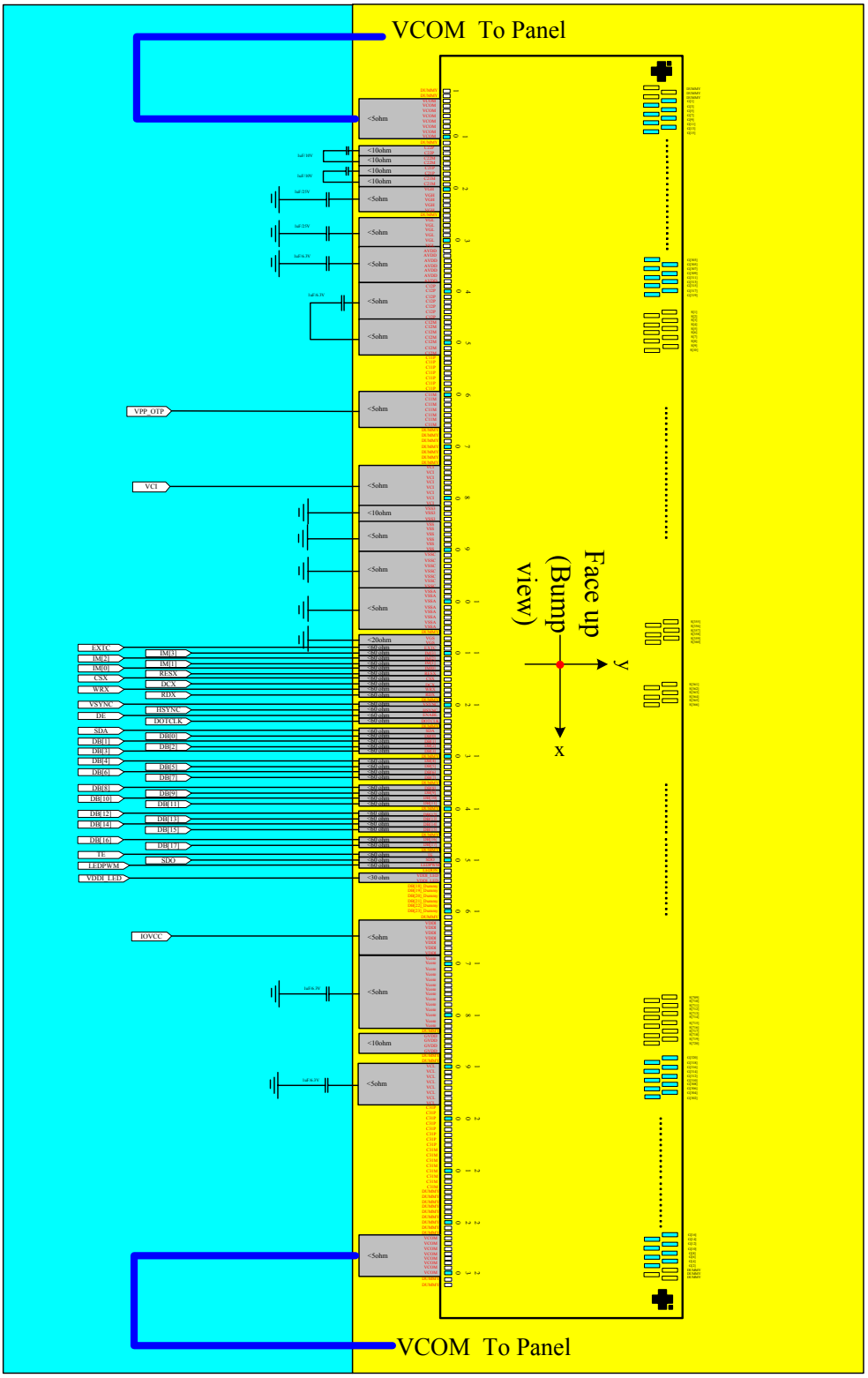
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	VDV[4:0]
Power On Sequence	5'h16
SW Reset	5'h16
HW Reset	5'h16

7. Application



Items	Recommended Specification	Pin connection
Capacity 1uF (B characteristics)	6.3V	AVDD,VCORE,VCL,C12P/M
	10V	C21P/M,C22P/M
	25V	VGH,VGL

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9301 is used out of the absolute maximum ratings, GC9301 may be permanently damaged. To use GC9301 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9301 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	VDDI	V	-0.3~+4.6
Supply voltage(Digital)	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+85
Storage temperature	Tstg	℃	-55~+110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2 DC Characteristics

General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-16.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	32	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	|VCOMH-VCOML|	4.0	-	5.5	Note3
Source Driver							

Source Output Range	Vsout	V	-	0.1	-	AVDD -0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage(Source Output channel)	Vdev	mV	Sout>=4.2V Sout<=0.8V	-	-	20	Note4
			4.2V>Sout>0.8V	-	-	15	-
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation							
1st Boost（VCI*2) Voltage	AVDD	V	-	4.95 (Note5)	-	5.5 (Note6)	Note3
1st Booster（VCI*2) Drop Voltage	VCI*2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	AVDD -0.2	

Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

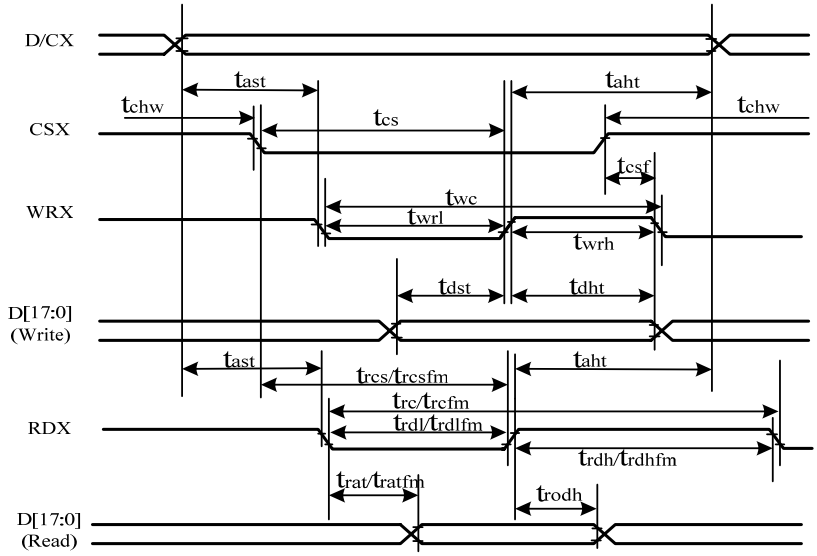
Note5: VCI=2.6V

Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

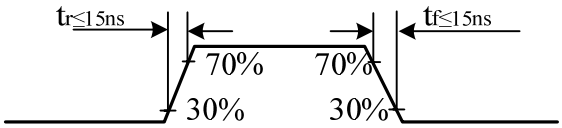
8.3 AC Characteristics

8.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ)

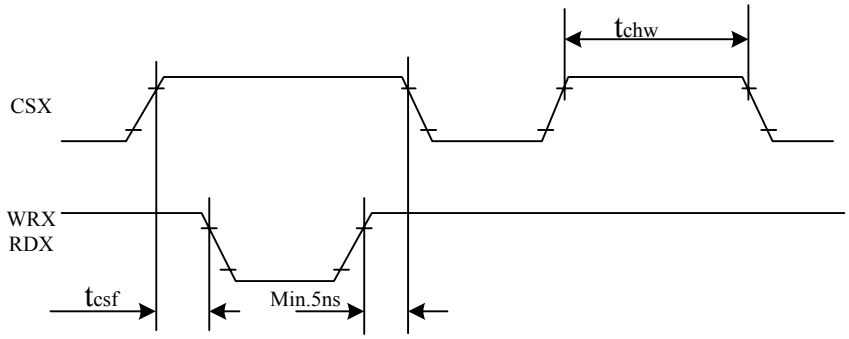


Signal	Symbol	Parameter	max	min	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	45	-	ns	
D[17:0],D[15:0],D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

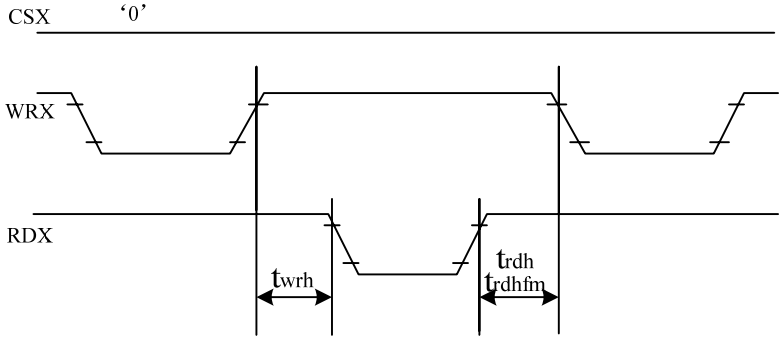


CSX timings :



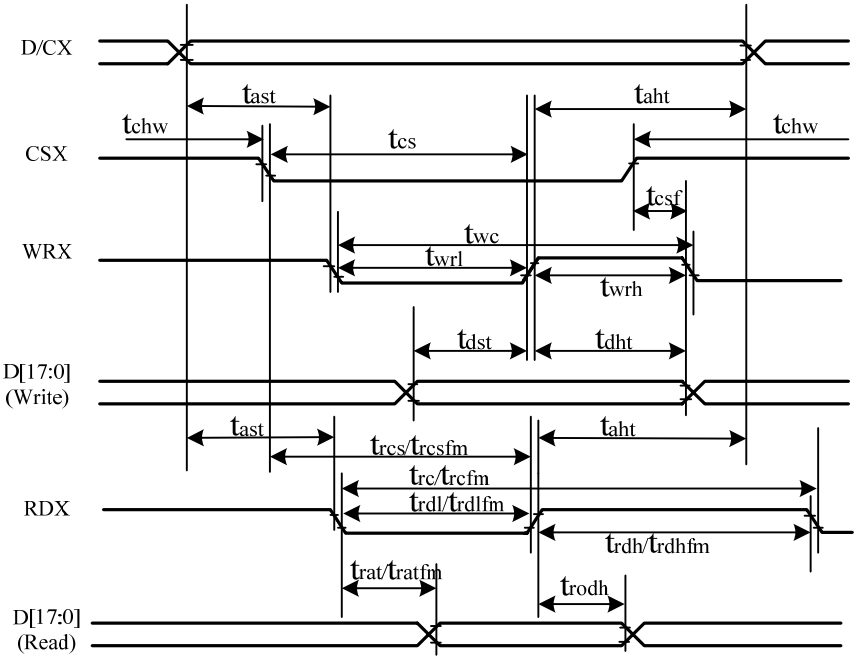
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



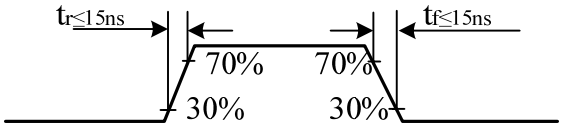
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ)

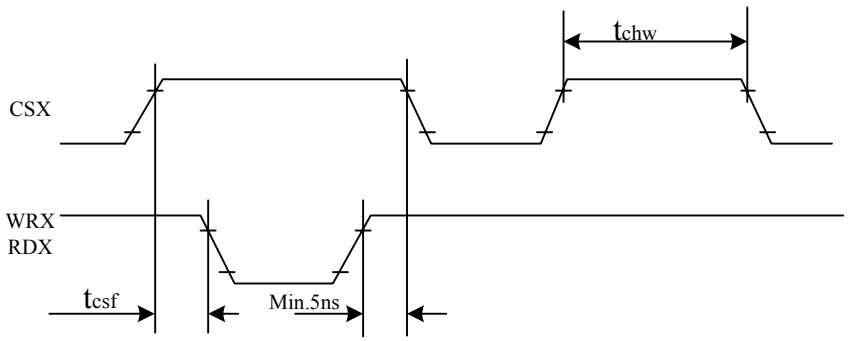


Signal	Symbol	Parameter	max	min	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0],D[17:10]& D[8:1],D[17:10],D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

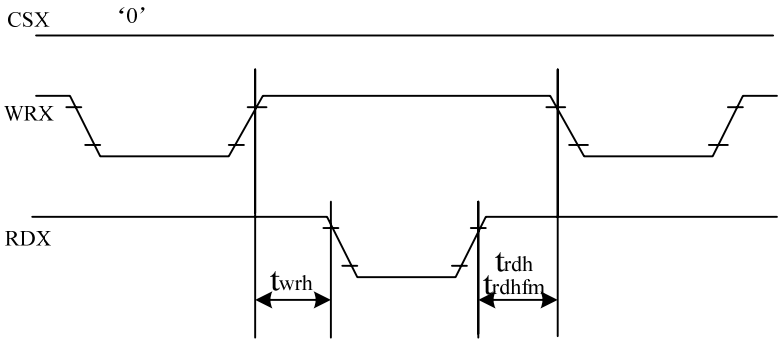


CSX timings :



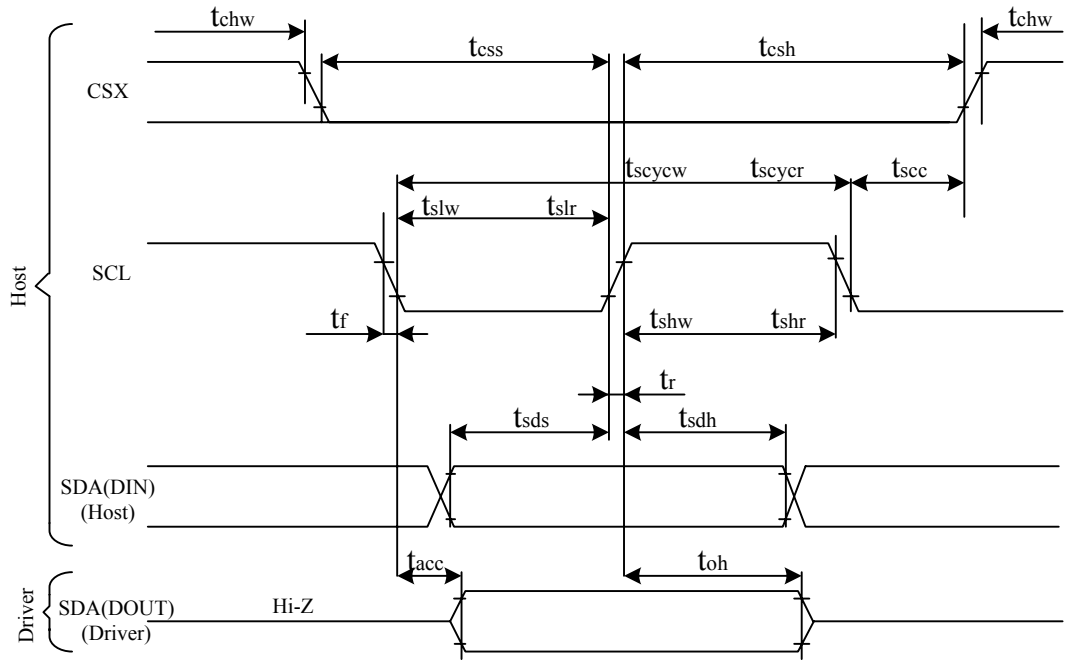
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



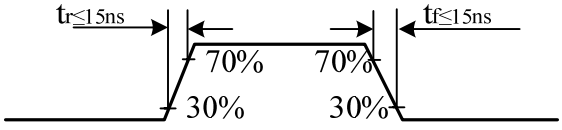
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)

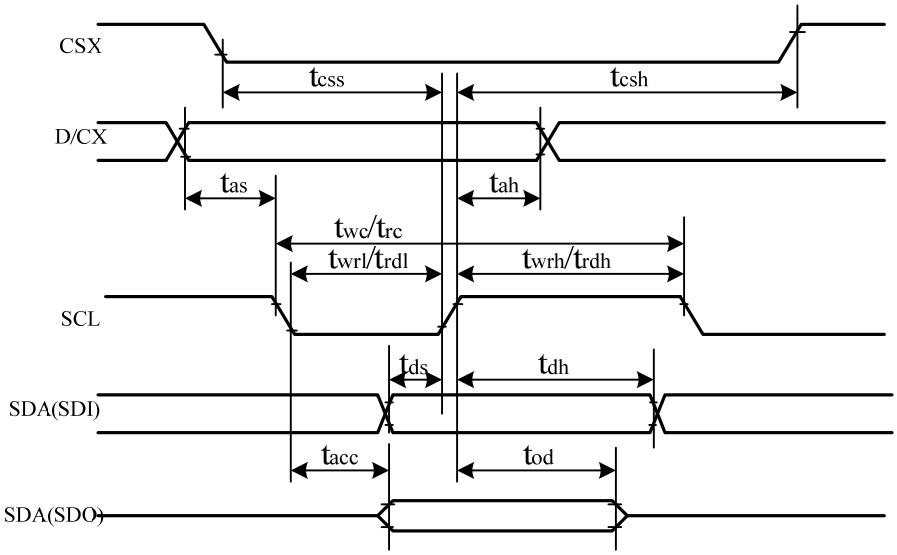


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

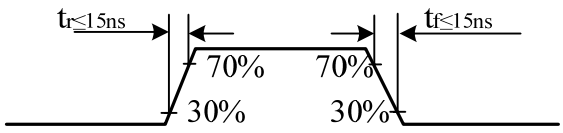


8.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)

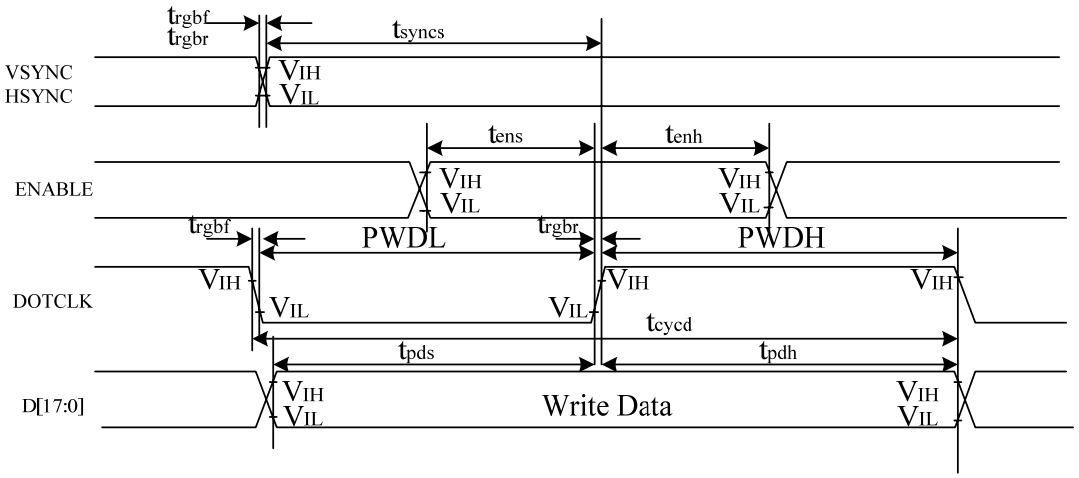


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	100	-	ns	
	twrh	SCL "H" Pulse Width (Write)	40	-	ns	
	twrl	SCL "L" Pulse Width (Write)	40	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	toh	Output disable time (Read)	10	50	ns	For minmum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

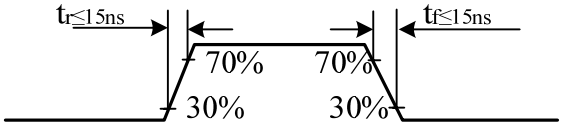


8.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



9. Revision History

Version No.	Date	Page	Description
V1.00	2011-12-09	All	New Created
V1.01	2012-01-18	1.P179 2.P188 3.P209	1.Add display inversion control instruction B4H 2.Add frame rate control instruction A3H 3.Delete C31P/M capacitance of application circuit
V1.02	2012-05-15	P185	The POR value of Register is modified to 009341h