an Intel company

2.5 Gbit/s 16:1 Multiplexer GD16523

General Information

The GD16523 is a multirate (STM 1/4/16 plus 1.25 Gbit/s bit-rates) 16:1 re-timing multiplexer with jitter clean-up capability.

The data inputs are forward clocked into a 2 bit elastic buffer enabling a very low jitter transfer by using a double PLL system.

The GD16523 tolerates up to 1.7 UI_{PP} (155 MHz) jitter on the input data and forward clock relative to the jitter output clock.

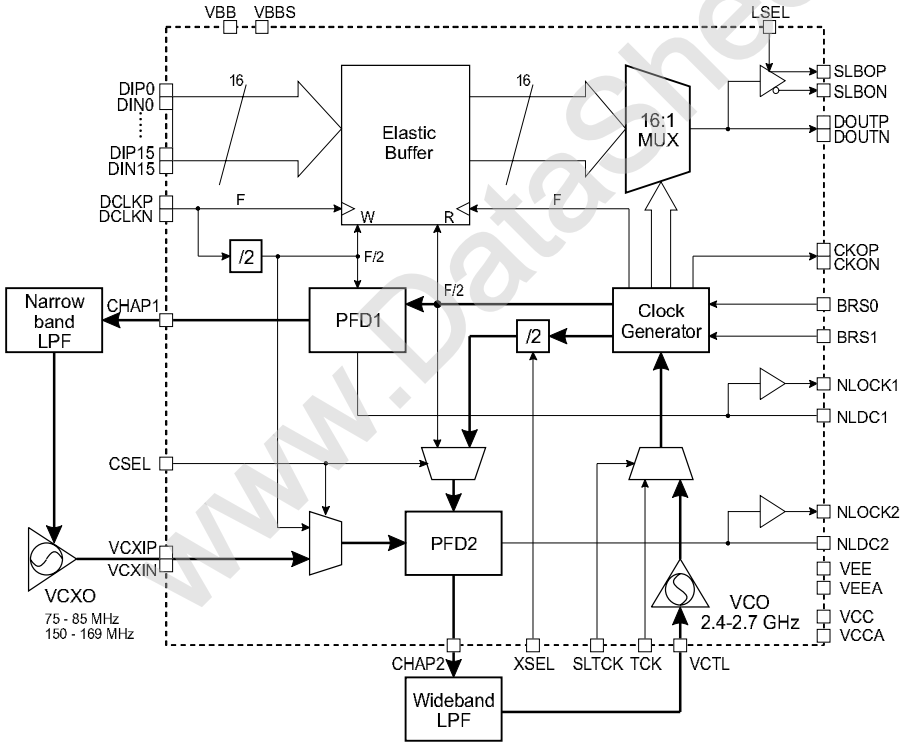
Each of the PLLs has a separate PCMOS lock- detect output.

The VCXO reference clock input is differential and the frequency is selectable 78 MHz or 155 MHz.

Data inputs are differential LVPECL inputs. 2.5 GHz clock and data outputs are differential CML with internal 50 Ω terminations.

The GD16523 operates from a single +3.3 V supply voltage using 800 mW (typical).

The GD16523 is available in a 100 pin TQFP package (14 × 14 mm) with a heat slug on bottom surface.



Features

- Multirate Multiplexer:
  - 2.4 - 2.7 Gbit/s
  - 1.25 Gbit/s
  - 622 Mbit/s
  - 155 Mbit/s
- Forward clocked input data.
- Jitter clean-up PLL.
- 2 bit elastic buffer.
- Differential reference clock input.
- High-speed clock output.
- LVTTL lock detect outputs.
- Near-end loop-back output with power down capability.
- Single power supply: +3.3 V.
- Power dissipation: 800 mW (typ.).
- Available in a 100 pin TQFP package (14 × 14 mm) with exposed heat slug on bottom surface.

Functional Details

The GD16523 multiplexes the 16 data inputs (DIP/N0-15) into a single data output (DOUT) with DIP/N0 as the first bit to be output and DIP/N15 as the last. The data inputs are forward clocked by the DCLK input. The data inputs are differential LVPECL type and the output is differential CML, driving 10 mA in a 50 Ω load connected to VCC.

In order to reduce jitter on the data output a 2 bit elastic buffer combined with a double PLL system has been implemented. The first PLL consists of an external passive loop filter and an external crystal VCO (VCXO). The centre frequency of the external VCXO can be selected to be in either range 150 - 169 MHz or 75 - 85 MHz by the XSEL pin. The second PLL requires only a passive external loop filter consisting of a resistor and a capacitor.

The jitter performance on the output of the chip depends on three phase noise contributing sources: the forward clock (DCLK), the external VCO (VCXO) and the internal VCO, see Figure 1. The output noise is a combination of these three curves. First the noise follows the DCLK curve until the loop-bandwidth of LPF1 then the noise follows the curve of the VCXO until the loop-bandwidth of LPF2, and finally it follows the noise of the internal VCO, see Figure 2.

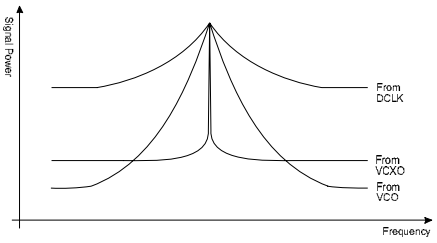


Figure 1. *Noise sources contributing to the output noise. Normalized to same signal power and carrier frequency.*

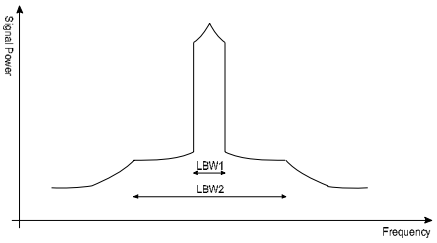


Figure 2. *Spectrum of output clock, with optimized LBW2.*

Above the PLL1 loop-filter frequency the noise performance is determined by the VCXO therefore the PLL1 loop-filter frequency should be set as low as possible. At the same time the jitter difference between the forward clock and output clock may not exceed 1.7 UI_{PP} (155 MHz). The optimum bandwidth of PLL1 is therefore the bandwidth where just below 1.7 UI_{PP} of jitter is filtered away from the forward clock.

The optimum loop bandwidth of PLL2 is the frequency where the VCO curve crosses the VCXO curve, see Figure 1.

A no-lock detect output pin is available for each PLL, indicating if the corresponding PLL is out of lock. To enable this function a 5 - 10 nF capacitor should be connected to each of the NLDC pins. This capacitor filters the NLDET signal generated internally by XORing the two signals going to the PFD and putting this through a charge pump to the NLDC pin. This filtering enables the NLOCK pin to go low when the corresponding PLL is in lock and high when out of lock.

A high level on the CSEL input bypasses the PLL1 so that the write signal to the elastic buffer goes directly to the PFD2. It also bypasses the divider between the Clock Generator and the PFD2. Note that changing the bit rate in this mode changes the loop-bandwidth of PLL2.

The auxillary output SLBOP/SLBON is a second data output to accommodate near-end loop back. To save power in normal operation and reduce noise in the receiver the output can be turned off by setting LSEL low.

The two bit rate select signals BRS1 and BRS0 select the bit rate of the chip.

BRS1	BRS0	DIP/N0..15	DOUTP/N
1	1	155 Mbit/s	2.5 Gbit/s
1	0	77 Mbit/s	1.25 Gbit/s
0	1	38 Mbit/s	622 Mbit/s
0	0	9.7 Mbit/s	155 Mbit/s

Application Details

PLL Loop Filters

The loop filters can be made as shown in Figure 3. For optimal jitter performance the values of LPF1 should be adjusted according to the jitter on the input data and the values for LPF2 should be adjusted according to the jitter on the VCXO.

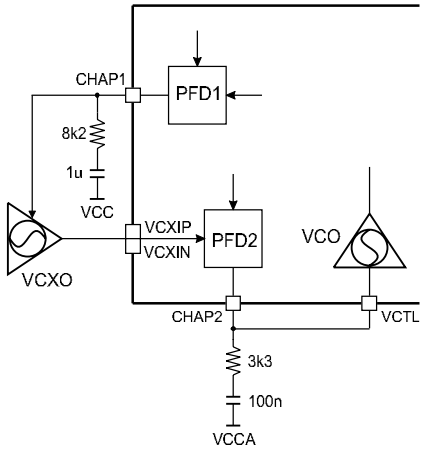


Figure 3. *Loop Filters*

For noise and jitter reasons it is important that the capacitor (C2) is connected to VCCA close to the VCTL pin.

Biasing the Data Inputs

All the data inputs are biased internally on the chip with the 5 kΩ resistive network to VBB as shown in Figure 4 .

The data inputs can be used both differential and single-ended without any external pull-ups/downs and can be AC-coupled as well.

The VBB input may be shorted to the VBBS output and de-copled with at least one external capacitor on either pin 23 or 61.

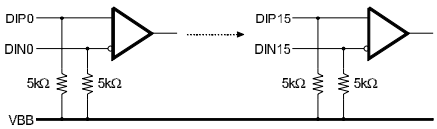


Figure 4. *Data Inputs*

Pin List

Mnemonic:	Pin numbers:	Pin Type:	Description:
DIP0 DIN0 DIP1 DIN1 DIP2 DIN2 DIP3 DIN3 DIP4 DIN4 DIP5 DIN5 DIP6 DIN6 DIP7 DIN7 DIP8 DIN8 DIP9 DIN9 DIP10 DIN10 DIP11 DIN11 DIP12 DIN12 DIP13 DIN13 DIP14 DIN14 DIP15 DIN15	26, 27 28, 29 30, 31 32, 33 34, 35 36, 37 39, 40 41, 42 43, 44 45, 46 47, 48 49, 50 53, 54 55, 56 57, 58 59, 60	LVPECL IN	Differential data inputs multiplexed to the serial output starting with DIP0, followed by DIP1, DIP2....DIP15. Pre-biased to VBB.
DCLKP, DCLKN	63, 64	LVPECL IN	Differential clock input. These pins are used to forward clock the data inputs.
VCXIP, VCXIN	88, 89	LVPECL IN	Differential VCXO clock input for PLL1.
VCTL	96	ANL IN	Internal VCO frequency control input.
CSEL	71	LVTTL IN	PLL1 bypass select signal. 0 (or NC) PLL1 VCXO is active. 1 PLL1 is bypassed.
LSEL	72	LVTTL IN	Loop select. 0 (or NC) SLBOP/N output buffer is powered down. 1 SLBOP/N output buffer is powered up
XSEL	73	LVTTL IN	Select input for reference clock frequency. 0 Selects 77.76 MHz VCXO 1 (or NC) Selects 155 MHz VCXO.
BRS0, BRS1	68, 69	LVTTL IN	Bit rate select. BRS1 BRS0 DIP0..DIP15 DOUTP/N 1 (or NC) 1 (or NC) 155.52 Mbit/s 2.488 Gbit/s 1 (or NC) 0 77.76 Mbit/s 1.244 Gbit/s 0 1 (or NC) 38.88 Mbit/s 622 Mbit/s 0 0 9.72 Mbit/s 155 Mbit/s
DOUTP, DOUTN	9, 10	CML OUT	Multiplexed data output. On-chip terminated, refer to Figure 6.
SLBOP, SLBON	3, 4	CML OUT	Near-end loop back output. On-chip terminated, refer to Figure 6.
SLTCK	91	LVTTL IN	Clock source select input. 0 (or NC) Selects internal VCO 1 Selects TCK input
TCK	92	LVTTL IN	Test clock input. This pin is used as clock source instead of the internal VCO when the SLTCK input pin is high.
CKOP, CKON	18, 19	CML OUT	Clock output in phase with the multiplexed data output. On-chip terminated, refer to Figure 6.
CHAP1	84	ANL OUT	Charge-pump 1 output. Sinks current when VCXO is leading. Sources current when VCXO is lagging, use positive transfer VCXO.
CHAP2	93	ANL OUT	Charge-pump 2 output. Sources current when internal VCO is leading. Sinks current when internal VCO is lagging. Internal VCO is negative transfer.
VBB	23, 61	ANL IN	Reference voltage input for differential data inputs.
VBBS	22	ANL OUT	Reference voltage output.
NLOCK1	77	PCMOS OUT	PLL1 lock detect output. 0 PLL1 is in lock. 1 PLL1 is out of lock.

Mnemonic:	Pin numbers:	Pin Type:	Description:
NLOCK2	78	PCMOS OUT	PLL2 lock detect output. 0 PLL2 is in lock. 1 PLL2 is out of lock.
NLDC1	80	ANL IN/OUT	A capacitor should be connected to this pin to set the time constant for the NLOCK1 output.
NLDC2	82	ANL IN/OUT	A capacitor should be connected to this pin to set the time constant for the NLOCK2 output.
VEE	12, 25, 38, 51, 62, 65, 67, 74, 75, 81, 87, 90	PWR	0 V Power for core and PECL I/O.
VEEA	95, 97, 98	PWR	0 V Power for VCO.
VEEO	13, 14	PWR	0 V Power for high-speed outputs.
VCC	1, 24, 52, 66, 70, 76, 79, 83, 85, 86	PWR	+3.3 V Power for core and PECL I/O.
VCCA	94, 99, 100	PWR	+3.3 V Power for VCO.
VCCO	6, 7, 15, 16, 21	PWR	+3.3 V Power for high-speed outputs.
NC	2, 5, 8, 11, 17, 20		
Heat sink	Package bottom		Internally connected to VEE.

Package Pinout

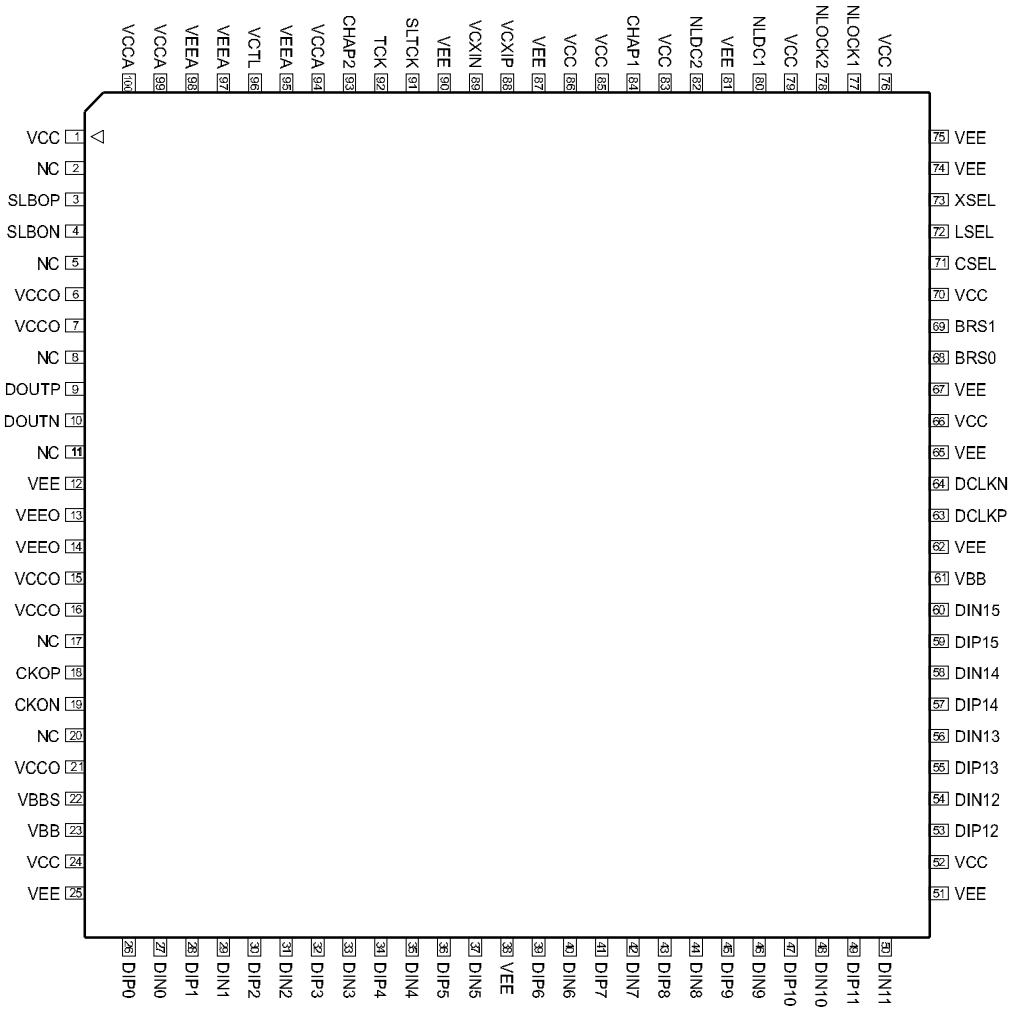


Figure 5. *Package Pinout. Top View.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to V_{EE} .
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}	Power supply		-0.5		6	V
$I_{O\,CML}$	CML output current		-15		15	mA
V_I	Applied voltage (all inputs)		-0.5		V_{CC}+0.5	V
V_O	Applied voltage (all outputs)		-0.5		6.0	V
$V_{IO\,ESD,CML}$	Static Discharge Voltage	Note 1	500			V
$I_{I\,LVPECL}$	LVPECL input current		-1		1	mA
$I_{O\,PCMOS}$	PCMOS output source current		-250		250	µA
$I_{O\,PCMOS}$	PCMOS output sink current		-250		250	µA
$I_{O\,CHAP,\,NLDC}$	Charge pump output current		-250		250	µA
T_O	Operating temperature	Case	-40		+110	°C
T_S	Storage temperature		-65		+125	°C

Note 1: Human body model (100 pF, 1500 Ω) MIL 883 std.

DC Characteristics

T_{CASE} = -40 °C to +85 °C. Appropriate heat sink may be required. Device is DC tested in the temperature range 0 °C to 85 °C. Specifications from -40 °C to 0 °C are guaranteed by design and evaluated during the engineering test.
V_{CC} = 2.97 V to 3.6 V.

All voltages in the table are referred to V_{EE}.
All input signal and power currents in the table are defined positive into the pin.
All output signal currents are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}	Supply voltage		+2.97	+3.3	+3.6	V
I_{CC}	Supply current			242	277	mA
I_{CCA}	Supply current for internal VCO			25		mA
I_{CCO}	Supply current for high-speed outputs			92		mA
P_{DISS}	Power dissipation	Note 1		800	1000	mW
P_{LSEL}	Loop-back output power dissipation			73		mW
V_{IH} LVPECL	LVPECL-input HI voltage		V_{CC} -1.17		V_{CC} -0.87	V
V_{IL} LVPECL	LVPECL-input LO voltage		V_{CC} -2.01		V_{CC} -1.47	V
I_{IH} LVPECL	LVPECL-input current	$V_{IH\ MAX}$ to $V_{IL\ MIN}$	-200		+100	µA
V_I LVTTL	LVTTL-input HI voltage		2.0		V_{CC}	V
V_{IL} LVTTL	LVTTL-input LO voltage		0.0		0.8	V
I_{IH} LVTTL	LVTTL-input HI current				1000	µA
I_{IL} LVTTL	LVTTL-input LO current		-1200			µA
IVCTL	VCTL leakage current	$V_{EE}<V_{VCTL}<V_{CC}$-0.25	-30			µA
V_{OH} CML	CML-output voltage swing	Note 2	400	500	800	mV
Z_{OUT} CML	CML-output impedance to V_{CC}		35	50	65	Ω
V_{OH} PCMOS	PCMOS-output HI voltage	Note 3		V_{CC} -300		mV
V_{OL} PCMOS	PCMOS-output LO voltage	Note 3		V_{EE} +300		mV
I_{OH} CHAP,NLDC	Charge pump output source current			100		µA
I_{OL} CHAP,NLDC	Charge pump output sink current			-100		µA
V_{VBBS}	Reference output voltage		V_{CC} -1.4	V_{CC} -1.3	V_{CC} -1.2	V
I_{VBBS}	Reference output current		0.1		3.0	mA
V_{VBB}	Input data reference voltage		V_{CC} -1.50		V_{CC} -1.1	V

Note 1: This includes externally dissipated heat in 50 Ω termination loads connected to the DOUTP/N and CKOP/N. The SLBOP/N loop-back output is powered down.
Note 2: With 50 Ω load impedance connected.
Note 3: The PCMOS output is based on GIGA's Charge Pump output cell.

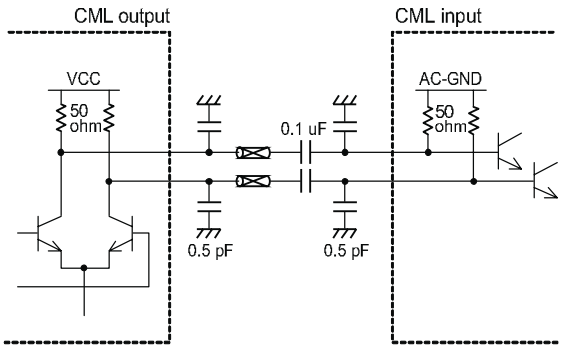
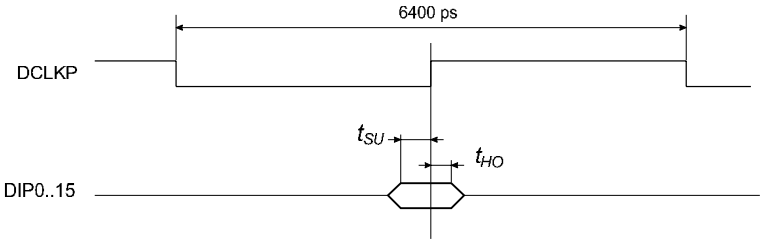
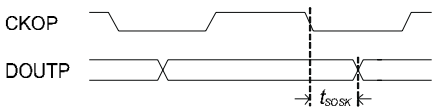


Figure 6. *CML Output Circuit. All capacitances (except 0.1 µF) are parasitic capacitances.*

AC Characteristics

T_{CASE} = -40 °C to +85 °C. Appropriate heat sink may be required. Device is AC tested in the temperature range 0 °C to 85 °C. Specifications from –40 °C to 0 °C are guaranteed by design and evaluated during the engineering test.
V_{CC} = 2.97 V to 3.6 V.





Symbol:	**Characteristic:**	**Conditions:**	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
J_{Gen}	Jitter generation	12 kHz to 20 MHz, Note 1		3.0	5.0	mUI_{RMS}
J_{Gen}	Jitter generation	5 kHz to 20 MHz, Note 1		40	60	mUI_{PP}
J_{Tol}	Input data jitter tolerance	See Figure 8 , Note 2	1.7			UI_{PP}
$t_{LH\ CML}$	CML output rise time	Note 3	50	90	110	ps
$t_{HL\ CML}$	CML output fall time	Note 3	40	80	100	ps
t_{SU}	Input data set-up time before DCLK	See Figure above	600			ps
t_{HO}	Input data hold time from DCLK	See Figure above	300			ps
$t_{R\ DI0..15,\ DCLK}$	Maximum allowed rise time				1.6	ns
F_{VCXI}	VCXI input frequency	XSEL is High XSEL is Low	144 72	155.52 77.76	162 81	MHz MHz
F_{DOUT}	Output data bit rate	See Table below				
K_{VCO}	VCO gain constant	@ 2.488 GHz		-180		MHz/V
t_{LOCK}	Lock response time	Note 4		300	500	µs
t_{PD}	Time from DCLK to first bit is out	Note 5		38		ns
t_{SOSK}	Serial output skew	See Figure above	-10	20	50	ps
$F_{VCO\ MIN}$	VCO frequency range	VCTL = V_{CC}-0.3 V			2.4	GHz
$F_{VCO\ MAX}$	VCO frequency range	VCTL = 0.3 V	2.7			GHz
F_{VCXI}	VCXI duty cycle		40		60	%
F_{DCLK}	DCLK duty cycle		40		60	%

Note 1: PPL1: Low noise VCXO (LBW = 3 kHz); PLL2: LBW = 1 MHz
Measured on GD90523/524 evaluation board with test set directly coupled to chip and both PLLs in lock.
Note 2: 1 UI = 6430 ps. The tolerance is reduced 0.2 UI_{PP} per 10 µA leakage current to/from the CHAP1 output.
Note 3: 20% - 80%, loaded with 50 Ω and 0.5 pF in parallel to VCC. See Figure 6.
Note 4: With 10 nF on NLDC.
Note 5: Value when in 2.5 Gbit/s mode. Value scales inversely with bit rate.

BRS1	BRS0	Input Bit Rate (IBR)	Output Bit Rate (OBR)
0	0	9.4 - 10.1 Mbit/s	150 - 169 Mbit/s
0	1	38 - 40 Mbit/s	600 - 675 Mbit/s
1	0	75 - 81 Mbit/s	1200 - 1350 Mbit/s
1	1	150 - 163 Mbit/s	2400 - 2700 Mbit/s

	f0 [Hz]	f1 [Hz]	f2 [Hz]	f3 [Hz]	f4 [Hz]	A1 [UI_{p-p}]	A2 [UI_{p-p}]	A3 [UI_{p-p}]
OC-3/STS-3	10	30	300	6.5k	65k	0.15	1.5	15
STM-1	0.125	19.3	500	6.5k	65k	0.15	1.5	15

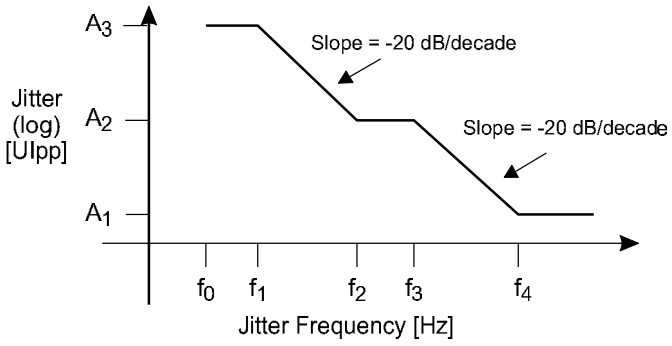


Figure 7. *Minimum required jitter tolerance on a SONET or SDH Line.*

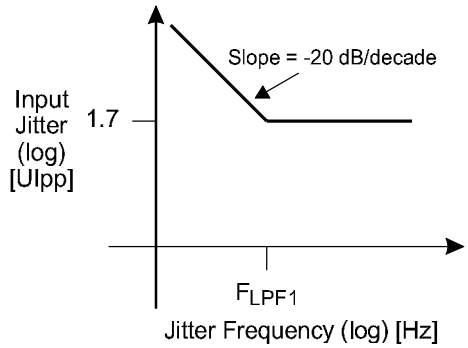
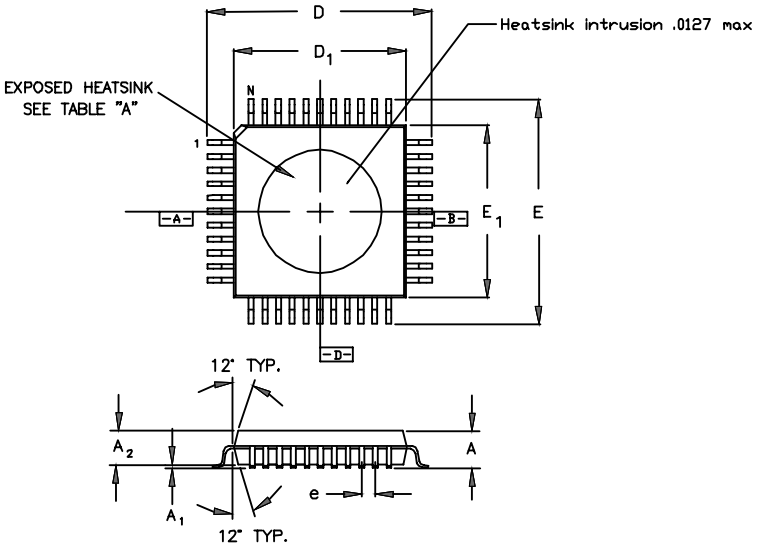


Figure 8. *Minimum jitter tolerance of GD16523 (1 UI = 6400 ps).*

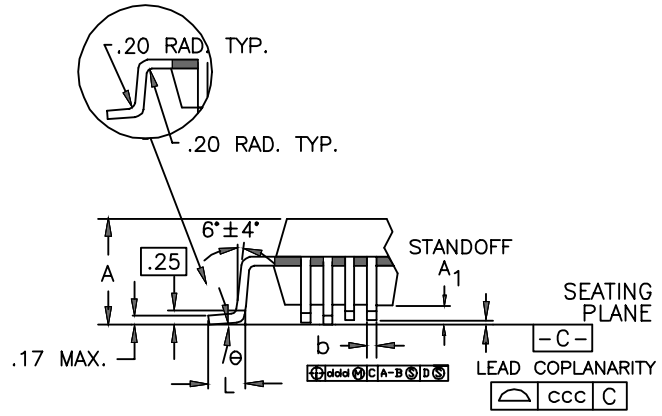
Package Outline



BODY + 2.00 mm FOOTPRINT		
	LEADS	100L–1.4 THK.
DIMS. / TOL.		
A	MAX.	1.60
A_1		.05 MIN./.15 MAX.
A_2	±.05	1.40
D	±.20	16.00
D_1	±.05	14.00
E	±.20	16.00
E_1	±.05	14.00
L	+.15/−.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

TABLE "A"

INTERPOSER RING SIZE	EXPOSED HEATSINK DIA.
6.10x6.10 / 7.11x7.11	6.60 ±.50



NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED.
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") OR 0.15 MM (.006") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.

Figure 9. *100 pin TQFP. All dimensions are in mm. Exposed heat slug is mounted on bottom of the package.*

Device Marking

Figure 10.*Device Marking. Top View.*

Ordering Information

To order, please specify as shown below:

Product Name:	Intel Order Number:	Package Type:	Case Temperature Range:
GD16523-100BA	**FAGD16523100BA** MM#: 836091	100 pin EDQUAD TQFP	-40...+85 °C

an Intel company
Mileparken 22, DK-2740 Skovlunde
Denmark
Phone : +45 7010 1062
Fax : +45 7010 1063
E-mail : sales@giga.dk
Web site : http://www.intel.com/ixa

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