10 Gbit/s Transmitter MUX with Re-timing GD16585

Preliminary

General Description

GD16585 is a 9.95328 Gbit/s transmitter chip for use in SDH STM-64 and SONET OC-192 optical communication systems.

GD16585 integrates all the main functions of the transmitter, which is clock generation, PLL circuits and multiplexer in a single monolithic IC. Hence only an external loop filter and a VCXO are required.

The main functions of GD16585 are shown in the figure below. The clock generation is made on-chip by a low noise and tuneable 10 GHz VCO. The VCO frequency is controlled by the PLL with an external loop filter, allowing the user to control the loop characteristic.

The clock synchronisation is controlled by the Phase and Frequency Detector with a 155 MHz or 622 MHz reference clock input.

GD16585 multiplexes a 16 bit parallel 622 Mbit/s interface into a serial 9.9553 Gbit/s data stream.

The timing between the input data and the on-chip clock system are controlled by a second Phase and Frequency Detector (PFCX). It compares the input data clock with the on-chip load clock. The output of the PFCX is the phase and frequency control of the external VCXO reference clock.

The output of the MUX stage is retimed by the 10 GHz clock and the output driver is a *Current Mode Logic* (CML) output with internal 50 Ω termination resistors.

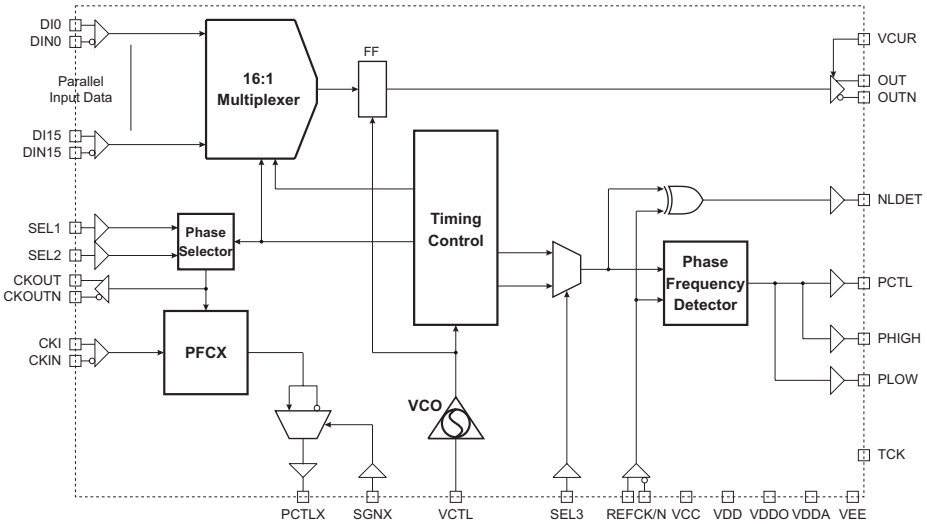
The 16 bit wide parallel input interface is LVDS compatible with a 2 × 50 Ω internal load termination.

GD16585 is manufactured in a Silicon Bipolar process.

GD16585 uses a -5.2 V supply voltage and +3.3 V supply for interfacing LVDS.

The power dissipation is 2.2 W, typical.

GD16585 is delivered in an 132 leads ceramic Ball Grid Array (BGA). The size of the package is 13 × 13 mm.



Features

- On-chip low noise VCO with a wide tuning range.
- Automated capture of the VCO frequency by a true phase and frequency detector.
- Retiming of MUX stage output with 10 GHz clock.
- Clock failure detection NLDET.
- Phase nulling circuit for easy interfacing with the system ASIC.
- 16:1 MUX with differential 622 Mbit/s LVDS data inputs.
- CML data input with 50 Ω internal load termination.
- LVDS compatible data and clock inputs with 100 Ω internal load termination.
- 622 MHz clock output for counter clocking.
- 155 MHz or 622 MHz reference clock input (selectable).
- Dual supply operation: -5.2 V and +3.3 V
- Low power dissipation: 2.2 W (typ.).
- Silicon Bipolar process.
- 132 leads ceramic BGA 13 × 13 mm package.
- Available in two versions:
  - GD16585 for 10 Gbit/s
  - GD16589 for 10.66 Gbit/s

Applications

- Telecommunication systems:
  - SDH STM-64
  - SONET OC-192.
- Fibre optic test equipment.

Functional Details

The main function of GD16585 is as transmitter in STM-64 and SONET OC-192 optical communication systems.

It integrates:

- *Voltage Controlled Oscillator* (VCO)
- *Phase and Frequency Detector* (PFD)
- 16:1 Multiplexer
- Re-timing of output data.
- Phase nulling circuit for interfacing input data and clock.

VCO

The VCO is an LC-type differential 10 GHz oscillator controlled by pin VCTL and with a tuning range of ±5 %. The VCO and the clock divider circuit generates the clock signal and load pulses needed for multiplexing and timing control.

With the VCTL voltage at -3 V the VCO frequency is fixed at 9.953 GHz and by changing the voltage from 0 to –5.2 V the frequency is controlled from 9 GHz to 10.2 GHz. The modulation bandwidth of VCTL is 90 MHz.

PFD

The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock (REFCK/REFCKN) to the PFD is 155 or 622 MHz selectable by SEL3.

A No Lock DETection signal (NLDET) is provided as a status signal of the PLL. It compares the VCO clock with the reference clock and is high whenever they differ. Using NLDET the situation of clock failure, i.e. loss of lock can be detected.

The reference clock input is a CML input with 2 × 50 Ω internal termination resistors and should be used differential for obtaining lowest clock jitter.

The PLL synchronizes the 10 GHz VCO to the external reference clock (VCXO). Spectral noise from the reference clock, within the PLL bandwidth, will be multiplied and added to the 10 Gbit/s output by the divider ratio between VCO and reference clock i.e. N = 16 / 64 or in terms of phase noise as 20Log(16) = 24 dB or 36 dB. A low noise reference clock with high frequency stability is required in order to fulfill the ITU-T jitter requirements.

Inputs

The parallel input interface is 622 Mbit/s LVDS with 100 Ω internal resistors. The 16 bits are multiplexed starting with DI0, DI1...DI15.

The input data clock (CKI, CKIN), which is synchronized with the data signals, is LVDS compatible.

The select inputs (SEL1-3 and SGNX) are low- speed inputs, which can be connected directly to the negative supply rails (0 / -5.2 V).

Loop Filter for the On-chip VCO.

The external loop filter is made using an operational amplifier connected to output pins (PHIGH and PLOW). The characteristics of the phase lock loop are controlled by the loop filter components hence the op-amp is designed as an integrator by a feedback capacitor and a resistor. The gain-bandwidth of the op-amp need to be larger than the required PLL bandwidth in order not to limit it. The recommended op-amp is Analog Devices (AD8042) with a gain-bandwidth of 160 MHz sufficient for PLL bandwidths up to 50 MHz. The op-amp uses single supplied by -5.2 V. See Figure 1 for application information.

The phase information from the PFD is high frequency pulses at output pins (PHIGH and PLOW). They are open collector outputs with an 8 mA current drive and are terminated externally by 220 Ω to 0 V. A pre-filtering of the phase pulses are applied by a parallel 10 pF capacitor.

The PCB layout of the external loop filter and the connecting lines to PHIGH, PLOW and VCTL are critical for the jitter performance of the component. The artwork for the op-amp and the passive components should be placed very close to the pins of GD16585 in order to have connecting lines as short as possible. Ideally the loop filter components are placed on the opposite side of the PCB directly underneath GD16585.

The PCTL pin is available for future use with a passive loop filter.

The jitter performance using a passive loop filter will be characterized by GIGA upon release of prototypes. Please contact GIGA for further information.

The Outputs

The 10 Gbit/s output driver is internal terminated with 50 Ω resistors to 0 V. The output should be terminated externally with 50 Ω at the receive end and should be used differential. Both OUT and OUTN are best terminated with the same load resistor e.g. 50 Ω, an asymmetrically loading will decrease the performance of the output due to reflections.

Both outputs **OUT/OUTN are not ESD protected** and extra precautions should be taken when handling the outputs (the internal 50 Ω resistor provides some ESD hardness making the ouput low impedance).

The clock outputs (CKOUT/N) are differential open collector outputs with a 8 mA output current. They are terminated externally with resistors and can be terminated to the positive 3.3 V supply. The clock output should be terminated even though it is not used.

The Output Voltage Control

By controlling the voltage at VCUR the output voltage swing at OUT/OUTN is adjusted in the range from 0.1 V to 0.8 V. The VCUR can be operated from 0 V to VEE, but the control range is from 0 V to VEE +2 V. The maximum output voltage is with VCUR = 0 V and the minimum voltage is with VCUR = VEE +2 V.

Package

GD16585 is packaged in an 132 leads ceramic BGA (13 × 13 mm).

External Circuits

The main external circuits needed to make GD16585 work as a 10 Gbit/s transmitter IC with re-timing and multiplexer are:

- An active loop filter with op-amp
- A reference clock at 155 MHz or 622 MHz with high frequency stability
- Termination resistors and de-coupling capacitors
- VCXO (622 or 155 MHz).

Timing Control to the System ASIC

The timing to the System ASIC is controlled by a Phase Nulling Circuit between the input data clock and data load clock. It is implemented as a PLL with an on-chip Phase and Frequency Detector (PFCX) and an external VCXO. The PFCX compares the load clock and the input data clock and detects the phase difference. The phase information (at PCTLX) is feed to an external VCXO which generates a low jitter reference clock (REFCK, REFCKN) to the transmitter.

The loop filter for the Phase Nulling Circuit should be low (<5 kHz) in order to clean-up the clock applied as a reference clock and still phase nulling any low frequency (<5 kHz) phase differences between the load clock and the input data clock.

The sign of the VCXO constant (frequency versus voltage [MHz/V] is set by pin SGNX to positive or negative.

A static phase difference between the load clock and the input data clock can be selected by SEL1 and SEL2. Four static settings are available (0°, 90°, 180° and 270°).

Counter Clocking Timing Control

A 622 MHz output clock is available at pin CKOUT, CKOUTN. This clock can be used in application where the phase nulling circuit (as described above) can not be used.

It contols the timing to the System ASIC by clocking out the data from System ASIC making the data available before the next load clock.

It is very important that the round trip delay (from the clock out to valid input data) is significant lower than the bit period.

The static phase of the output clock can be selected in four static settings as described above.

Thermal Condition

The component dissipates 2.2 W with a –5.2 V and +3.3 V voltage supply.

The component conducts most af the power through the center leads of the package (all VDD connected leads).

It is important to have a good thermal connection from the center leads of the package to the ambient environment to ensure the case temperature in the range from 0 to 70 °C.

Power Noise Rejection

In a noisy environment special attention must be taken as described above to optimize the jitter performance. The *Power Supply Rejection Ratio* (PSRR) is improved by adding a serial resistor (3.3 kΩ) and capacitor (33 nF) from the positive input of the op-amp to the power pin (VEE) as shown in Figure 1.

10.66 Gbit/s Application

A version of the transmitter with a bit rate of 10.66 Gbit/s for forward error correction application is available. The part number is GD16589.

The functionality and the pin-out are identically to GD16585.

The center frequency of the VCO (10.66 GHz) is the only difference to GD16585.

Application

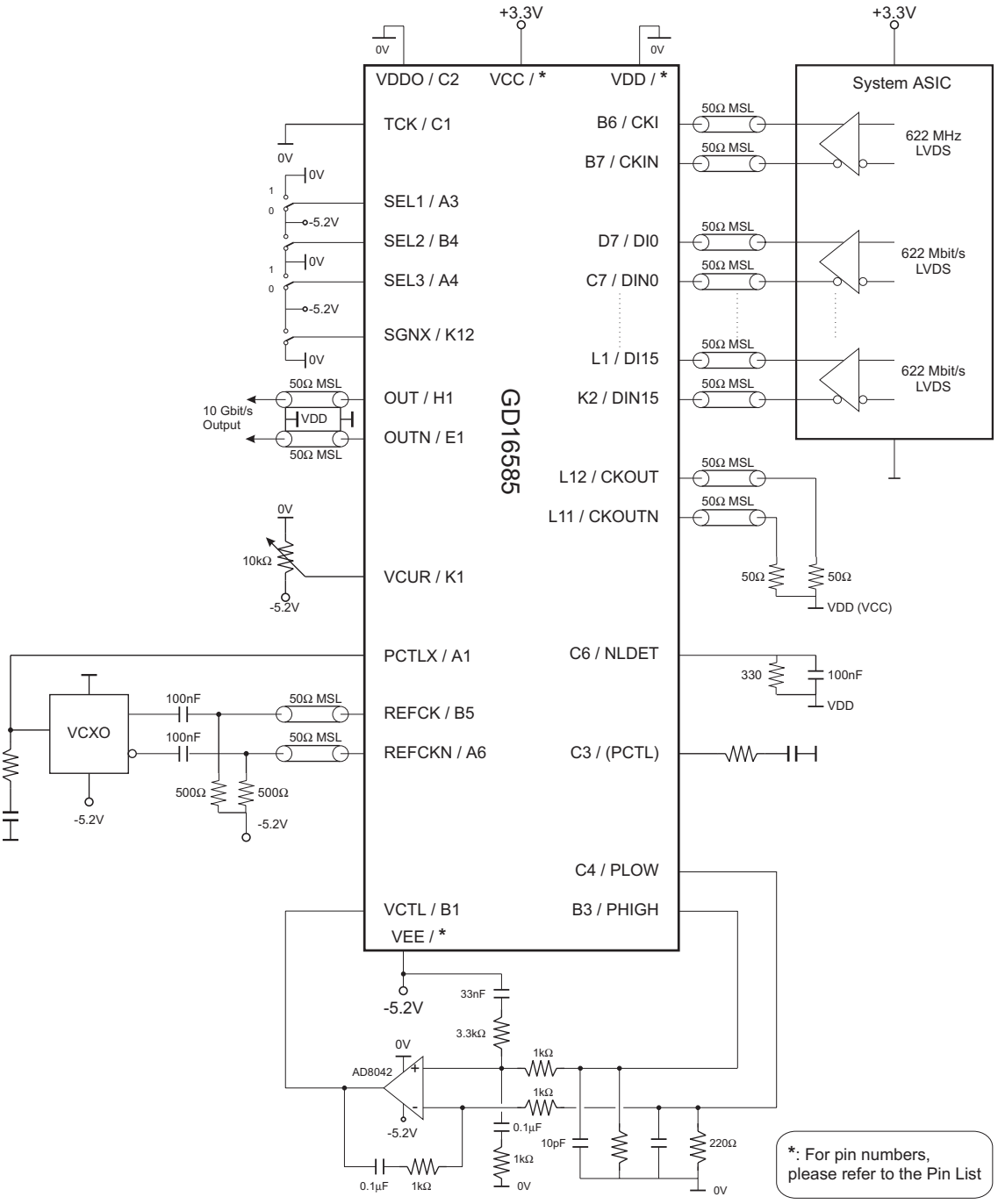


Figure 1. *Application Information*

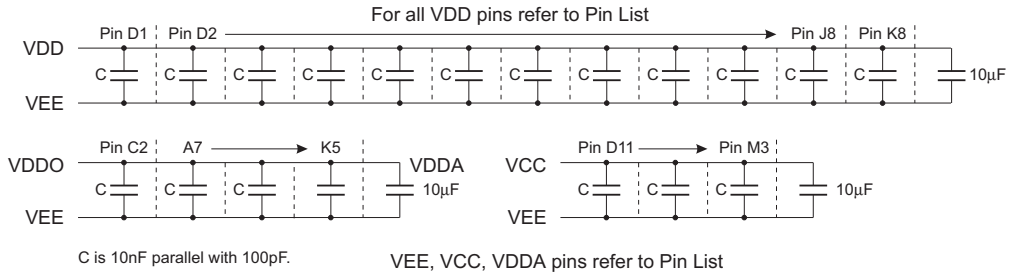


Figure 2. *De-coupling of the Power Supply*

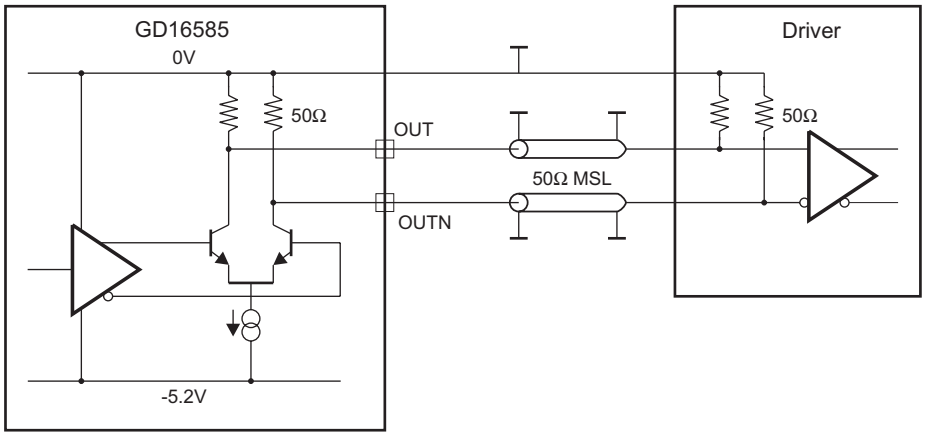


Figure 3. *10 Gbit/s Outputs (OUT/OUTN), DC Coupled.*

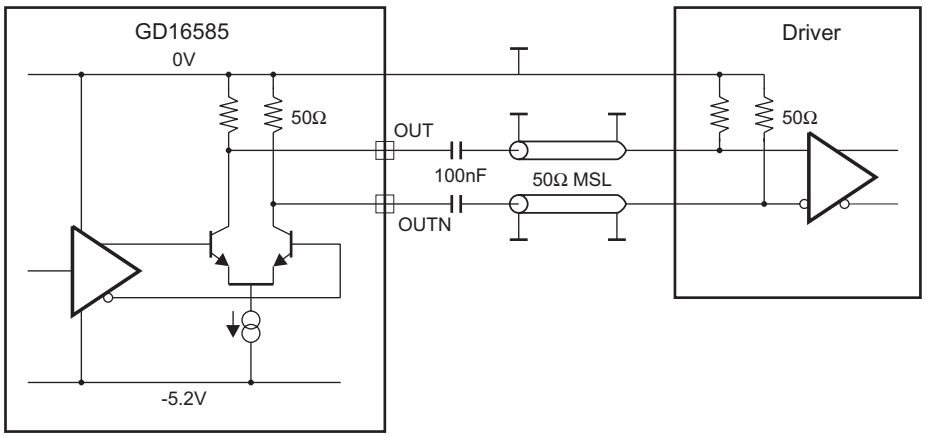


Figure 4. *10 Gbit/s Outputs (OUT/OUTN), AC Coupled.*

622 Mbit/s Output Interface

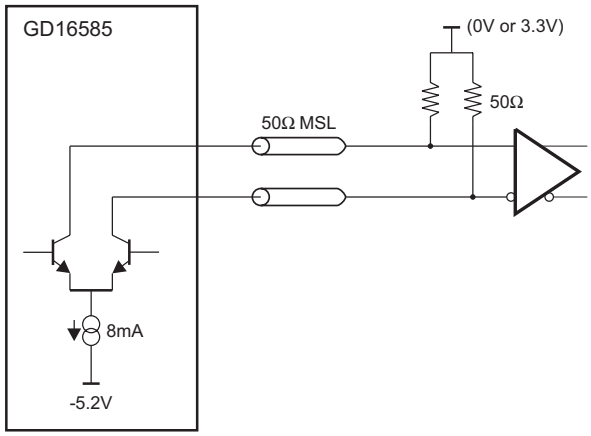


Figure 5. *Open Collector Output.*

Open collector outputs should always be terminated at the receiver end, by preferably 50 Ω.

622 Mbit/s Input Interface

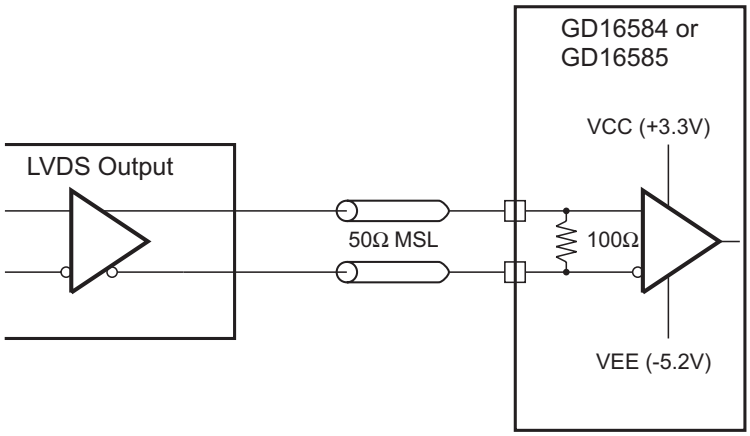


Figure 6. *LVDS Compatible Input.*

Reference Clock Input

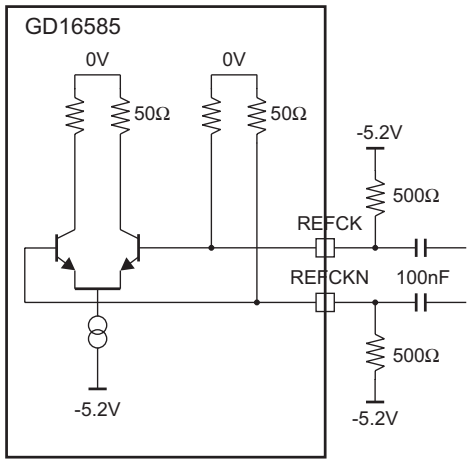


Figure 7. *Reference Clock Input (REFCK/REFCKN), Differential AC Coupled.*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DI0, DIN0 DI1, DIN1 DI2, DIN2 DI3, DIN3 DI4, DIN4 DI5, DIN5 DI6, DIN6 DI7, DIN7 DI8, DIN8 DI9, DIN9 DI10, DIN10 DI11, DIN11 DI12, DIN12 DI13, DIN13 DI14, DIN14 DI15, DIN15	C7, D7 A8, B8 A9, B9 B10, A11 C11, C12 D12, E12 G11, H12 J12, J11 L9, M9 L8, M8 L6, K6 M5, L5 M4, L4 L3, M2 K3, L2 L1, K2	LVDS In	Data input, differential 622 Mbit/s. Multiplexed to serial output starting with DI0, DI1...DI15.
REFCK, REFCKN	B5, A6	CML In	Reference clock input, differential 155 MHz or 622 MHz.
SEL1, SEL2	A3, B4	ECL In	Select the phase of CKOUT. SEL1 SEL2 0 0 T_D=0° 1 0 T_D=90° 0 1 T_D=180° 1 1 T_D=270° When left open, the inputs are pulled to “1” (VDD).
SEL3	A4	ECL In	Select the reference clock. 0 155 MHz 1 622 MHz When left open, the input is pulled to “1” (VDD).
CKI, CKIN	B6, B7	LVDS In	Data clock input.
OUT, OUTN	H1, E1	CML Out	Data output, differential 10 Gbit/s. **No internal ESD output protection**.
CKOUT, CKOUTN	L12, L11	Open Collector	Clock output, differential 622 MHz. Should always be terminated with a resistor.
(PCTL)	C3	Analogue Out	For future use with a passive loop filter.
PCTLX	A1	Analogue Out	Charge pump output from PFCX to external VCXO
PHIGH, PLOW	B3, C4	Open Collector	Phase-Frequency detector outputs. Should always be terminated with a resistor to VDD.
VCTL	B1	Analogue In	VCO input voltage control.
VCUR	K1	Analogue In	Output voltage control.
NLDET	C6	Open Collector	No Lock DETect output. Should always be terminated with a resistor.
SGNX	K12	ECL In	Selects between positive and negative VCXO constant. When left open, the input is pulled to VDD.
TCK	C1	ECL In	Used for test purpose. Connect to VDD.
VDD	A2, A5, D1-2, D6, E4-9, F1-2, F4-9, F11, G1-2, G4-9, H4-9, J1-2, J6, J8, K8	PWR	Digital Ground 0 V.
VDDA	A7, C5 (D5), J5 (K5)	PWR	PLL Ground 0 V.

Mnemonic:	Pin No.:	Pin Type:	Description:
VDDO	C2	PWR	VCO Ground 0 V. For test purpose connect to VEE.
VEE	B2, C8, C10, D8, D10, J4, J9, K4, J9	PWR	-5.2 V Digital supply voltage.
VCC	D11, J7, J10 (K10), M3	PWR	+3.3 V supply voltage for LVDS I/O.
NC	A10, A12, B11-12, C9, D9, F12, G12, K7, K11, L7, L10, M1, M6, M7, M10-12		Not Connected. Reserved for future use.
NC	D3-4, J3		DO NOT CONNECT.

Package Pinout

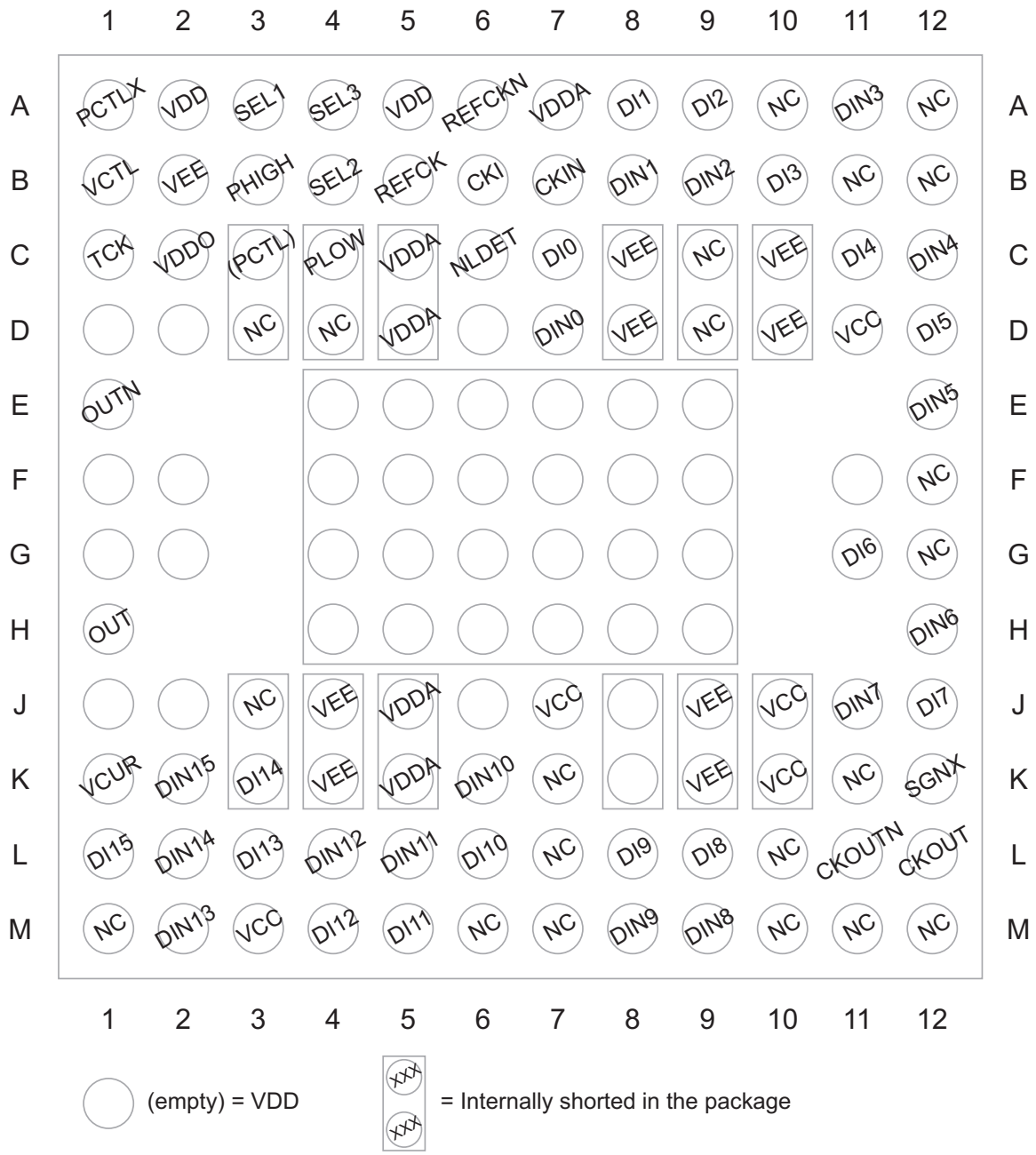


Figure 8. *Package Pinout. Top View Seen Through the Package.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD/VDDA.
All currents are defined positive out of the pin.
VDD is 0 V or GND

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply		0		-6	V
V_{CC}	Positive Supply				+4	V
$V_{O\ CML}$	CML Output Voltage		0		V_{EE}	V
$I_{O\ CML}$	CML Output Current	Note 1	0		-12	mA
$I_{I\ CML}$	CML Input Current	Note 1	-25		25	mA
T_J	Junction Temperature		-55		+125	°C
T_S	Storage Temperature		-65		+150	°C

Note 1: Nominal supply voltages.

DC Characteristics

T_{CASE} = 0 °C to 70 °C. VEE = -5.2 V. VCC = +3.3 V.
All voltages in table are referred to VDD.
All currents are defined positive out of pin.
VDD is 0 V or GND

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply Voltage		-5.0	-5.2	-5.4	V
V_{CC}	Positive Supply for LVDS I/O		+3.2	+3.3	3.4	V
I_{EE}	Negative Supply Current			400	500	mA
I_{CC}	Positive Supply Current			17		mA
$V_{IH\ LVDS}$	LVDS Input Voltage High, (differential)			100		mV
$V_{IL\ LVDS}$	LVDS Input Voltage Low, (differential)			-100		mV
$V_{IVR\ LVDS}$	LVDS Input Voltage Range		0		2	V
$R_{IN\ LVDS}$	LVDS Input Resistor Termination	DC	80	100	120	Ω
$V_{OH\ OC}$	Open Collector Output Voltage High	Note 1	-0.05	0	+0.05	V
$V_{OL\ OC}$	Open Collector Output Voltage Low	Note 1	-0.3	-0.4	-0.5	V
$I_{OH\ OC}$	Open Output Current High	Note 1	-0.1	0	+0.1	mA
$I_{OL\ OC}$	Open Output Current Low	Note 1	-7	-8	-9	mA
$V_{OH\ OUT}$	OUT/OUTN Voltage High	Note 1, 10 MHz	-0.1	-0.05	+0.05	V
$V_{OL\ OUT}$	OUT/OUTN Voltage Low	Note 1, 10 MHz	-0.5	-0.7	-0.8	V
$I_{OH\ OUT}$	OUT/OUTN Current High	Note 1		0		mA
$I_{OL\ OUT}$	OUT/OUTN Current Low	Note 1		-14		mA
$V_{IH\ SEL1\text{-}3,SGNX}$	SEL1-3, SGNX Input Voltage High	Note 2	0	V_{EE} + 2		V
$V_{IL\ SEL1\text{-}3,\ SGNX}$	SEL1-3, SGNX Input Voltage Low	Note 2		V_{EE} + 0.8	V_{EE}	V

Note 1: Output externally terminated by 50 Ω to 0 V.
Note 2: SEL1-3 and SGNX can be connected directly to VDD or VEE.

AC Characteristics, General

T_{CASE} = 0 °C to 70 °C, VEE = -5.2 V. VCC = +3.3 V.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{TRF}	Jitter transfer	12 kHz < F < 2 MHz Note 1		0.0	0.1	dB
J_{GEN}	Jitter generation	12 kHz < F < 80 MHz Note 1			0.1	UI_{PP}
V_{OUT}	10 Gbit/s output voltage	Note 3, VCUR open	550	650		mV_{PP}
$V_{I,CML}$	CML input voltage sensitivity			100	200	mV_{PP}
Γ_{OUT}	OUT/OUTN output reflection coefficient	Note 2		-10		dB
F_{REFCK}	REFCK/REFCKN frequency, stability		-10		+10	ppm
$D_{CYCLE, CKOUT/N}$	CKOUT/CKOUTN duty cycle	Differential	45		55	%
$D_{CYCLE, REFCK}$	REFCK duty cycle		45		55	%
$F_{MAX, REFCK}$	Maximum REFCK frequency				635	MHz

Note 1: With the recommended loop filter.
Note 2: From DC to 6 GHz
Note 3: The output voltage is adjustable by pin VCUR.

AC Characteristics, Timing Control to System ASIC.

T_{CASE} = 0 °C to 70 °C, VEE = -5.2 V.

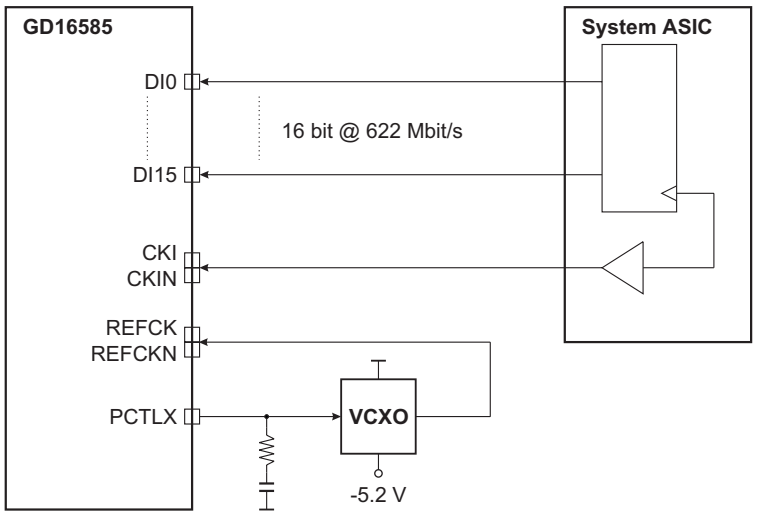


Figure 9. *Phase Nulling Circuit.*

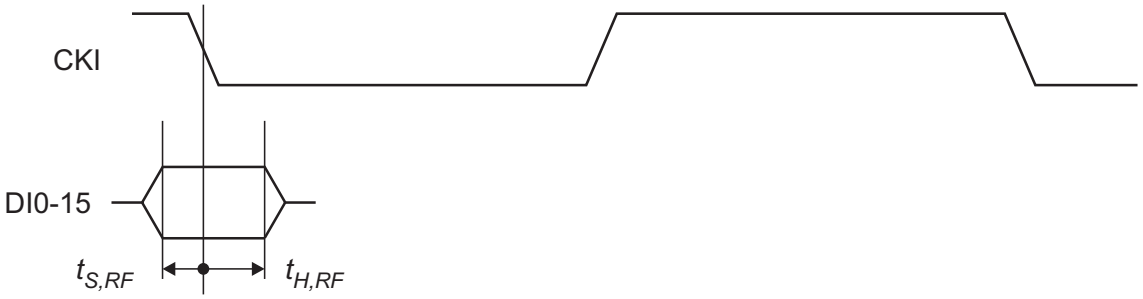


Figure 10. *Timing relation between input data and clock.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$t_{S,RF}$	DI0-15 setup before CKI	VEE = -5.2V, T_C=70°, SEL3 = 1		TBD		ps
$t_{H,RF}$	DI0-15 hold from CKI	VEE = -5.2V, T_C=70°, SEL3 = 1		TBD		ps

Package Outline

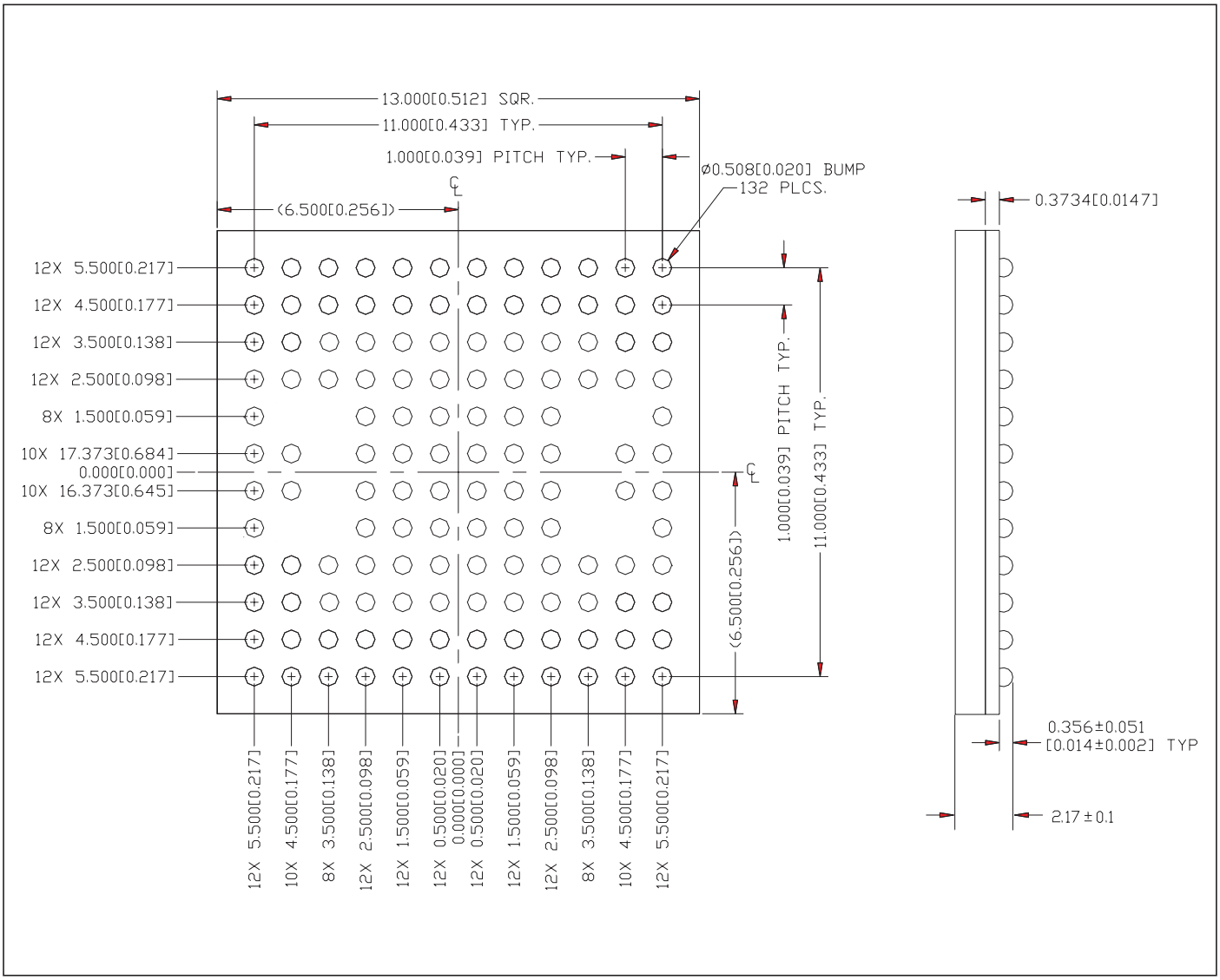


Figure 11. *Package 132 pin ceramic BGA.*

Device Marking

TBD

Ordering Information

To order, please specify as shown below:

Product Name:	Options:	Package Type:	Case Temperature Range:
GD16585-132EA	10 Gbit/s	132 pin ceramic BGA	0...70°C
GD16589-132EA	10.66 Gbit/s	132 pin ceramic BGA	0...70°C

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