an Intel company

10 Gbit/s Transmitter MUX with Re-timing GD16585/GD16589 (FEC)

Preliminary

General Description

GD16585 and GD16589 are transmitter chips used in SDH STM-64 and SONET OC-192 optical communication systems.

The device is available in two versions:
- GD16585 for 9.5328 Gbit/s.
- GD16589 for 10.66 Gbit/s with Forward Error Correction (FEC).

Except the different operating bit rate the two versions are functional identical.

The transmitter integrates the main functions of the serializer which are:
- Clock Multiply Unit (CMU)
- 16:1 Multiplexer in a single monolithic IC.

The CMU consists of Phase Locked Loop (PLL) controlled from an external reference clock. The PLL characteristics are controlled by an external loop filter allowing the user to optimize the jitter perfomance of the device.

The 16:1 Multiplexer accepts 16 parallel input bits at 622.88 Mbit/s (or 666 Mbit/s) that are serialized into a 9.9538 Gbit/s (or 10.66 Gbit/s) data stream. The serialized data stream is re-timed by the high-speed clock from the VCO.

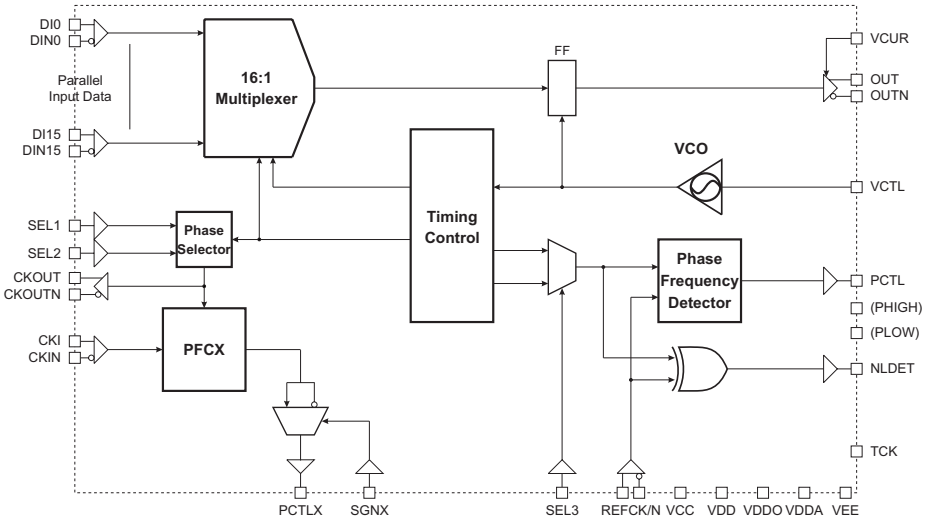
The parallel input interface features GIGA's unique self-synchronizing dynamic phase alignment scheme that allows both:
- Source synchronous counter clocking for OIF99.102.5 interfaces.
- Forward clocking with phase nulling and jitter clean-up of the clock.

These schemes enable the serializer to absorb output delay variations from the upstream System ASIC without use of initialization or reset.

The data and clock inputs to the MUX are LVDS and the output data is CML compatible.

The device operates from a dual -5.2 V and +3.3 V power supply. The power dissipation is 2.2 W, typical.

The device is manufactured in a Silicon Bipolar process and packaged in an 132 balls 13 × 13 mm Ceramic/Plastic Ball Grid Array (CBGA).



Features

- PLL based CMU with on-chip 10 GHz or 10.66 GHz VCO.
- 16:1 Multiplexer with a last stage re-timing.
- OIF99.102.5 compliant timing .
- LVDS compatible parallel data and clock inputs
- CML compatible serial data output.
- 155 MHz or 622 MHz reference clock input (selectable).
- Divide by 16 clock output.
- PLL out of lock detector.
- Dual supply operation: -5.2 V and +3.3 V
- Low power dissipation: 2.2 W (typ.).
- Available in three package versions:
  - EB: 132 ball (16 mill) Ceramic BGA 13 × 13 mm
  - EF: 132 ball (20 mill) Ceramic BGA 13 × 13 mm
  - FB: 132 ball (20 mill) Plastic BGA 13 × 13 mm
-
- Available in two versions:
  - GD16585 for 10 Gbit/s
  - GD16589 for 10.66 Gbit/s

Applications

- Telecommunication systems:
  - SDH STM-64
  - SONET OC-192
  - Optical Transport Networking (OTN)
  - FEC applications
- Fibre optic test equipment.

Functional Details

The main function of GD16585/GD16589 is as transmitter in STM-64 /OC-192 and OTN optical communication systems.

It integrates:

- Voltage Controlled Oscillator (VCO)
- Phase and Frequency Detector (PFD)
- 16:1 Multiplexer
- Re-timing of output data.
- Phase nulling circuit for interfacing input data and clock.

VCO

The VCO is an LC-type differential oscillator controlled by pin VCTL and with a tuning range of ±5 %. The VCO and the clock divider circuit generate the clock signals and load pulses needed for multiplexing and timing control.

With the VCTL voltage at -3 V the VCO frequency is fixed at 9.953 GHz (for GD16585) and by changing the voltage from 0 to –5.2 V the frequency is controlled from 9 GHz to 10.2 GHz. The modulation bandwidth of VCTL is 90 MHz.

The Reference Clock

The PFD is made with digital set/reset cells giving it a true phase and frequency characteristic. The reference clock (REFCK/REFCKN) to the PFD is 155 or 622 MHz selectable by SEL3.

The reference clock input is a CML input with 50 Ω internal termination resistors. The reference clock should be used differential for obtaining lowest clock jitter.

The PLL synchronizes the VCO to the external reference clock. Spectral noise from the reference clock, within the PLL bandwidth, will be multiplied and added to the serial output by the divider ratio between the VCO and reference clock i.e. N = 16 or in terms of phase noise as 20Log(16) = 24 dB (or 36 dB at N = 64). A low noise reference clock with low clock jitter is required in order to fulfill the ITU-T jitter requirements.

Inputs

The parallel data (DIx/DINx) and clock (CKI/CKIN) inputs are LVDS compatible with internal differential 100 Ω resistors.

The set-up and hold time between input clock and data is selectable in four settings by SEL1-2.

The timing relation is OIF99.102.5 complaint with SEL1,2 = 1,1 (0 V).

The select inputs (SEL1-3 and SGNX) are low-speed ECL compatible inputs, which can be connected directly to the negative supply rails (0 / -5.2 V).

Bit Order

The parallel data input is multiplexed with DI0 as the first sent bit, DI1 as the second sent bit and with DI15 as the last sent bit in a 16 bit frame.

Note: This bit naming covention is opposite to OIF99.102.5

For OIF interfaces the data pins should be connected as shown in the following table.

Input Pin:	OIF:
DI0/DIN0	TXDATA15_P/N (MSB)
DI1/DIN1	TXDATA14_P/N
DI2/DIN2	TXDATA13_P/N
DI3/DIN3	TXDATA12_P/N
DI4/DIN4	TXDATA11_P/N
DI5/DIN5	TXDATA10_P/N
DI6/DIN6	TXDATA9_P/N
DI7/DIN7	TXDATA8_P/N
DI8/DIN8	TXDATA7_P/N
DI9/DIN9	TXDATA6_P/N
DI10/DIN10	TXDATA5_P/N
DI11/DIN11	TXDATA4_P/N
DI12/DIN12	TXDATA3_P/N
DI13/DIN13	TXDATA2_P/N
DI14/DIN14	TXDATA1_P/N
DI15/DIN15	TXDATA0_P/N (LSB
CKI	TXCLK_P
CKIN	TXCLK_N

Loop Filter for the CMU

An external passive loop filter is used, consisting of a resistor and a capacitor driven from the PCTL pin, which outputs the phase and frequency information from the PFD. The values of the external components determines the characterisitcs of the PLL e.g. bandwidth and transfer function. For recommended loop filter values see Figure 1.

The PCB layout of the loop filter and the connecting lines between PCTL and VCTL are critical for the jitter performance of the device. The external components and the artwork should be placed very close to the pins at GD16585.

If the PHIGH and PLOW outputs are not used they must be shorted to VDD (0 V), please refer to Figure 1.

The Outputs

The output of the MUX stage is retimed by the 10 GHz (or 10.66 GHz) clock and the output driver is a Current Mode Logic (CML) output with internal 50 Ω termination resistors.

The serial output driver is internally terminated with 50 Ω resistors to 0 V. The output should be terminated externally with 50 Ω at the receive end and should be used differential. Both OUT and OUTN are best terminated with the same load resistor e.g. 50 Ω, an asymmetric loading will decrease the performance of the output due to reflections.

Both outputs **OUT/OUTN are not ESD protected** and extra precautions should be taken when handling the outputs (the internal 50 Ω resistor provides some ESD hardness making the ouput low impedance).

A divide by 16 clock output from the CMU is available at CKOUT/N for jitter measurement and test purpose. These outputs are differential open collector with a 8 mA output current. They are terminated externally with resistors and can be terminated to the positive 3.3 V supply. The clock outputs should be terminated even though they are not used.

PLL out of lock detect signal (NLDET) is provided as a status signal of the PLL. It compares the VCO clock with the reference clock and is low whenever the VCO is locked to the reference clock. The NLDET is an open collector output and must be terminated by an external resistor.

The Output Voltage Control

The serial output voltage swing at OUT/OUTN is controlled by VCUR in the range from 0.1 V to 0.8 V. The voltage swing is increased by increasing the VCUR voltage and the output is off at voltages below VEE +2 V.

If no adjustement is needed the VCUR can be lefted open.

With AC coupled outputs the VCUR pin must not be directly connected to 0 V which may cause the output stage to saturate deteriorating the eye-diagram.

Refer to Figure 1 for the recommended set-up of VCUR.

Timing to the System ASIC

The component supports source synchronouse clocking for OIF99.102.5 interface (311 MHz clock mode is not supported) and forward clocking with phase nulling and jitter clean-up of the reference clock. With a OIF interface a phase adjusted source clock is feed back to the System ASIC and data and clock are feed forward to the high-speed MUX.

The phase difference between the forward clock (CKI/CKIN) and the internal load pulse is detected by the Phase and Frequency Detector (PFCX) and the Phase Information (PCTLX) are use to control the phase and frequency of the external VCXO (622 MHz). The phase adjusted output clock of the VCXO can be used either as a source (counter) clock to the System ASIC (OIF99.102.5 in 622 MHz clock mode) or as a jitter clean reference clock (REFCK/N) to the on-chip CMU.

The phase information at PCTLX is filtered in an external low pass filter consisting of a capacitor and a resistor. For recommended component values, please refer to Figure 1.

Package

GD16585 and GD16589 are packaged in an 132 ball Ceramic/Plastic BGA (13×13 mm). For the package outline, please refer to Figure 14 and 15.

In ceramic packages following pin pairs are individually shorted inside the package and mainly used as power pins: C3/D3, C4/D4, C5/D5, C8/D8, C9/D9, C10/D10, J3/K3, J4/K4, J5/K5, J8/K8, J9/K9, and J10/K10, please refer to “Package Pinout” Figure 8 on page 8.

Thermal Condition

The component dissipates 2.2 W with a –5.2 V and +3.3 V voltage supply.

The die is mounted in a cavity on a metal pad directly connected to the center balls (E4-9, F4-9, G4-9, and H4-9).

It is important to have a good thermal connection from the center balls of the package to the ambient environment to ensure the best thermal conditions.

Note: To obtain $T_{CASE} < 70°C$, the PGBA (compared to the CBGA) requires additional cooling on the case, For details, please refer to Application Note “ PBGA - Thermal data....”.

10.66 Gbit/s Application

A version of the transmitter with a bit rate of 10.66 Gbit/s for Optical Transport Networking (OTN) and Forward Error Correction (FEC) application is available. The part number is GD16589.

The functionality and the pin-out are identically to the GD16585.

The center frequency of the VCO (10.66 GHz) is the only difference to the GD16585.

Application

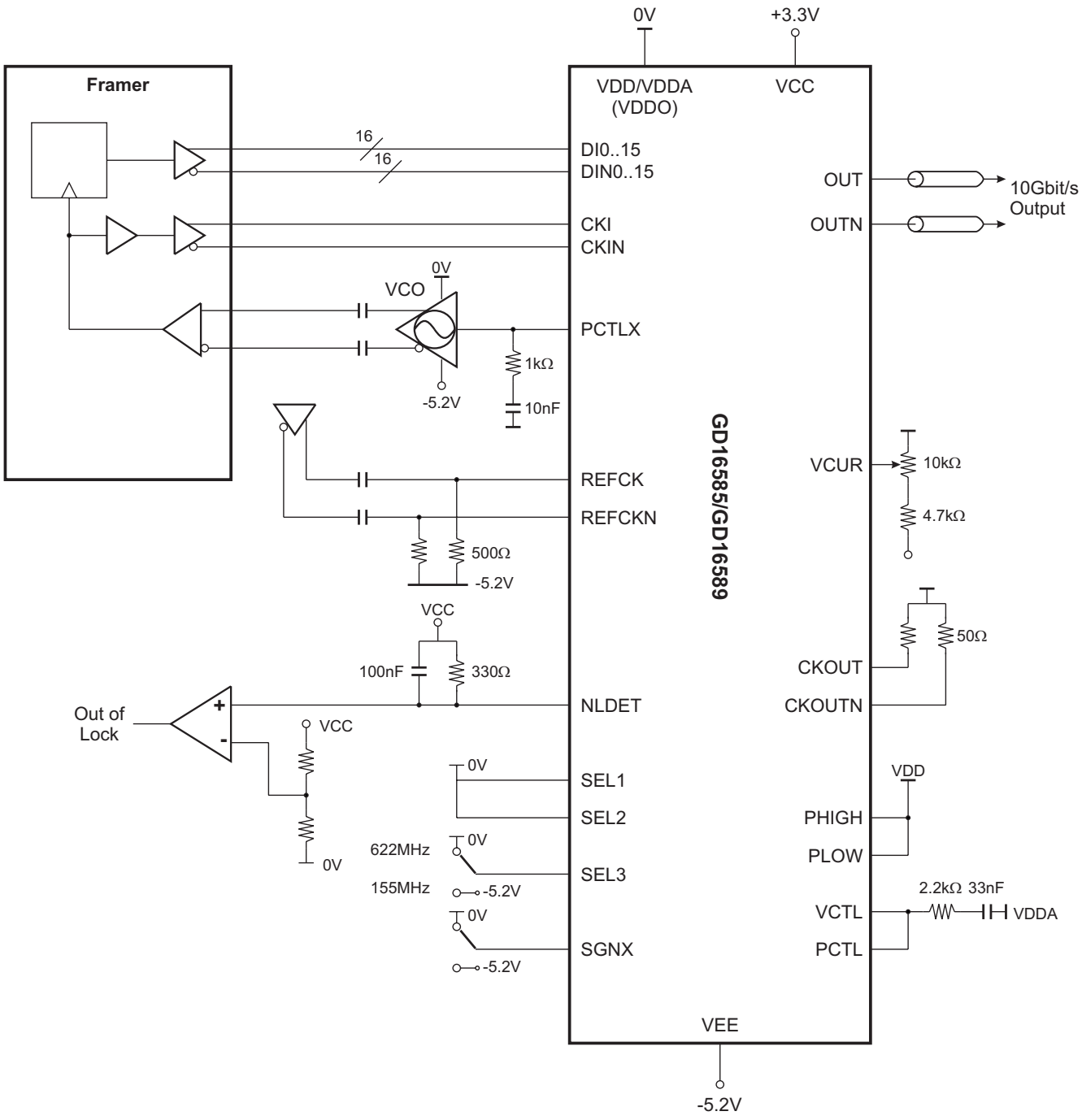


Figure 1. *Application Information, OIF interface to the Framer.*

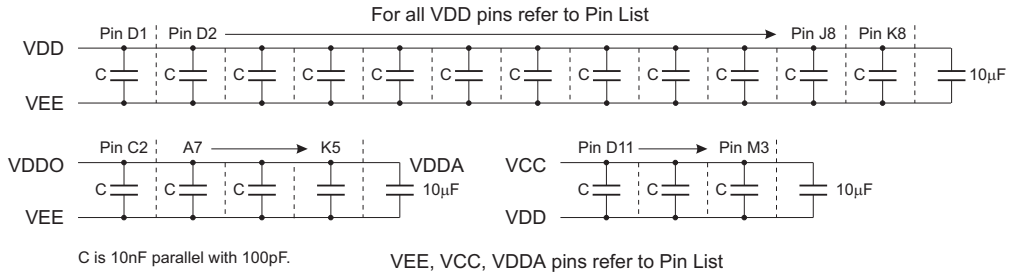


Figure 2. *De-coupling of the Power Supply*

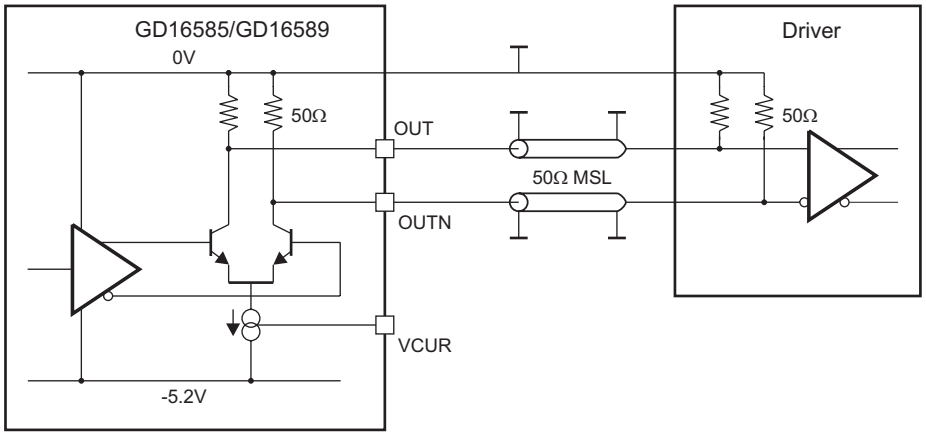


Figure 3. *10 Gbit/s outputs (OUT/OUTN), DC coupled.*

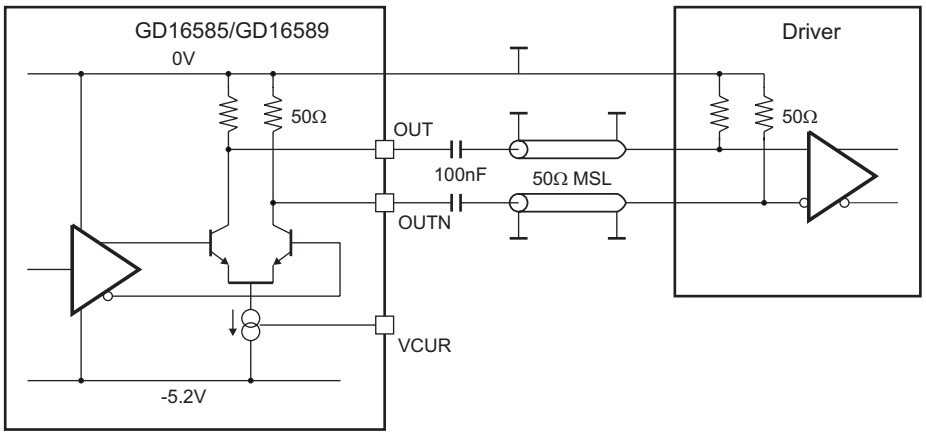


Figure 4. *10 Gbit/s outputs (OUT/OUTN), AC coupled.*

Note: With AC coupled outputs VCUR **must not** be connected directly to 0 V.

622 Mbit/s Output Interface

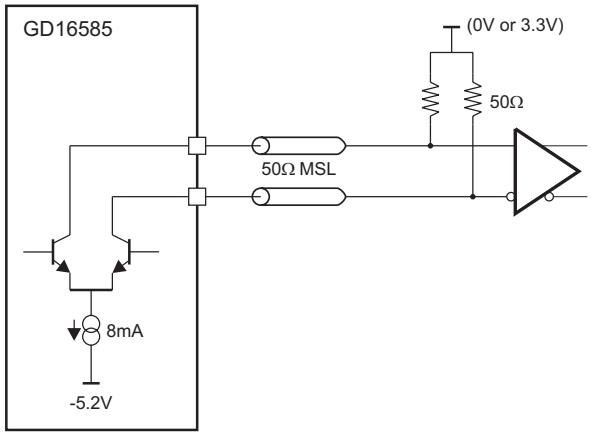


Figure 5. *Open collector output.*

Open collector outputs should always be terminated at the receiver end, by preferably 50 Ω.

622 Mbit/s Input Interface

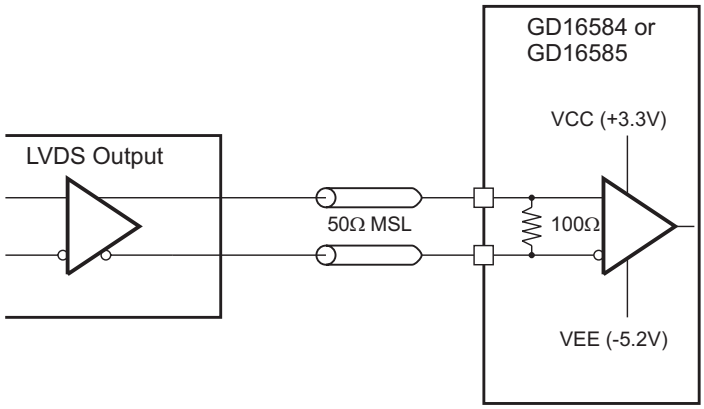


Figure 6. *LVDS compatible input.*

Reference Clock Input

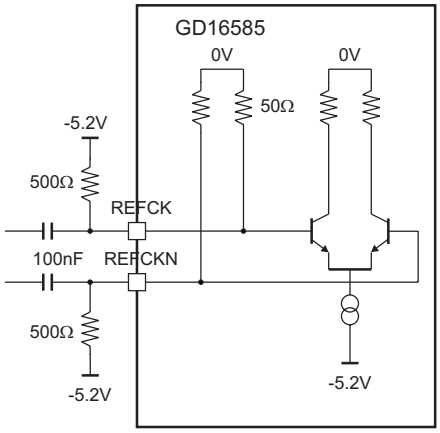


Figure 7. *Reference Clock Input (REFCK/REFCKN), Differential AC Coupled.*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
DI0, DIN0 DI1, DIN1 DI2, DIN2 DI3, DIN3 DI4, DIN4 DI5, DIN5 DI6, DIN6 DI7, DIN7 DI8, DIN8 DI9, DIN9 DI10, DIN10 DI11, DIN11 DI12, DIN12 DI13, DIN13 DI14, DIN14 DI15, DIN15	C7, D7 A8, B8 A9, B9 B10, A11 C11, C12 D12, E12 G11, H12 J12, J11 L9, M9 L8, M8 L6, K6 M5, L5 M4, L4 L3, M2 K3, L2 L1, K2	LVDS In	Data input, differential 622 Mbit/s. Multiplexed to serial output starting with DI0, DI1...DI15. **Note:** The bit naming convention is opposite to OIF99.102.5: DI0 is MSB. Please refer to item “Bit Order” on page 2.
REFCK, REFCKN	B5, A6	CML In	Reference clock input, differential 155 MHz or 622 MHz.
SEL1, SEL2	A3, B4	ECL In	Select the set-up and hold time beetwen the data and clock inputs in four settings. For setting, please refer to Figure 13 and table on page 14. When left open, the inputs are pulled to “1” (VDD).
SEL3	A4	ECL In	Select the reference clock frequency. 0 155 MHz 1 622 MHz When left open, the input is pulled to “1” (VDD).
CKI, CKIN	B6, B7	LVDS In	Data clock input.
OUT, OUTN	H1, E1	CML Out	Data output, differential 10 Gbit/s. **No internal ESD output protection**.
CKOUT, CKOUTN	L12, L11	Open Collector	Clock output, differential 622 MHz. Always terminate by 50 Ω to VDD.
PCTL	C3	Analogue Out	Charge pump output for CMU PLL.
PCTLX	A1	Analogue Out	Charge pump output from PFCX to external VCXO.
(PHIGH, PLOW)	B3, C4	Open Collector	Not used. Always terminate to VDD.
VCTL	B1	Analogue In	VCO input voltage control.
VCUR	K1	Analogue In	Output voltage control.
NLDET	C6	Open Collector	No Lock DETect output. Always terminate with a resistor to VDD.
SGNX	K12	ECL In	Selects between positive and negative VCXO constant. 0 Positive VCXO constant 1 Negative VCXO constant When left open, the input is pulled to “1” (VDD).
TCK	C1	ECL In	Used for test purpose. Connect to VDD.
VDD	A2, A5, D1-2, D6, E4-9, F1-2, F4-9, F11, G1-2, G4-9, H4-9, J1-2, J6, J8, K8	PWR	Digital Ground 0 V.
VDDA	A7, C5 (D5), J5 (K5)	PWR	PLL Ground 0 V.
VDDO	C2	PWR	VCO Ground 0 V. For test purpose connect to VEE.

Mnemonic:	Pin No.:	Pin Type:	Description:
VEE	B2, C8, C10, D8, D10, J4, J9, K4, K9	PWR	-5.2 V Digital supply voltage.
VCC	D11, J7, J10 (K10), M3	PWR	+3.3 V supply voltage for LVDS I/O.
NC	A10, A12, B11-12, C9, D9, F12, G12, K7, K11, L7, L10, M1, M6, M7, M10-12		Not Connected. Reserved for future use.
NC	D3-4, J3		DO NOT CONNECT.

Package Pinout

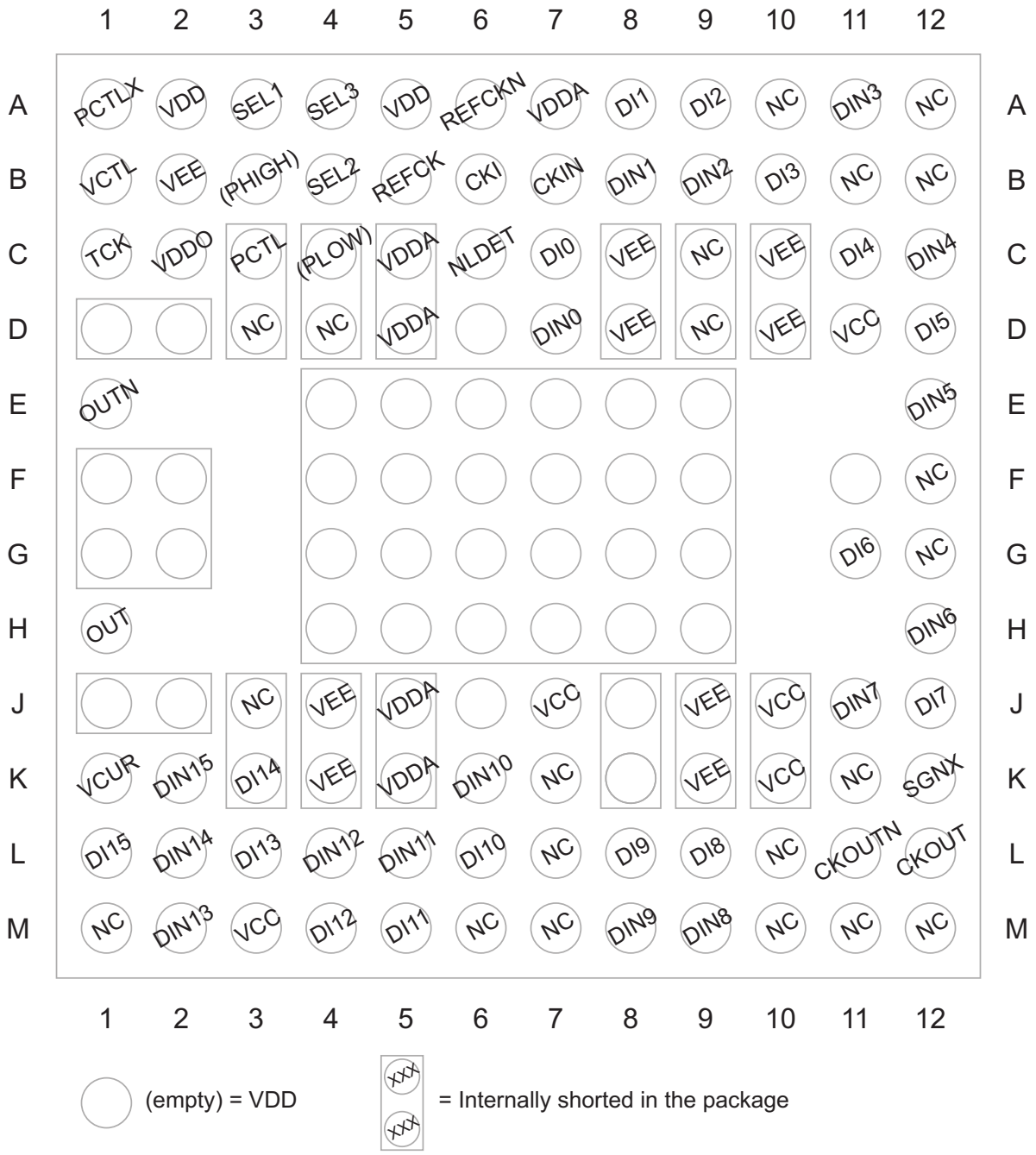


Figure 8. *Packages EB and EF Pinout. Top view seen through the package.*

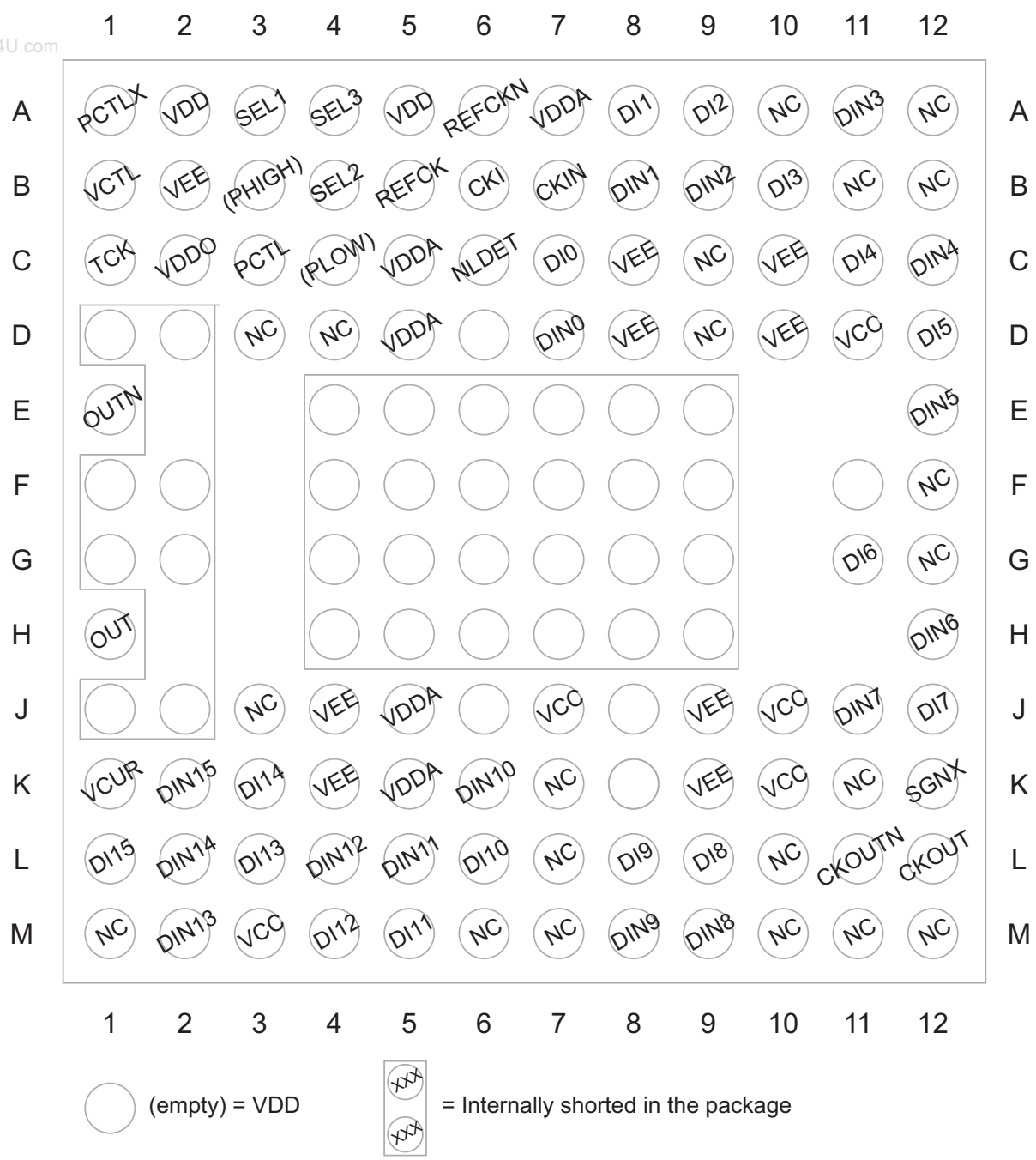


Figure 9. *Package FB Pinout. Top view seen through the package.*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in table are referred to VDD/VDDA.
All currents are defined positive out of the pin.
VDD is 0 V or GND

Symbol:	**Characteristic:**	**Conditions:**	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
V_{EE}	Negative Supply		-6			V
V_{CC}	Positive Supply				+4	V
$V_{I\ LVDS}$	LVDS Input Voltage		0		V_{CC}+0.5	V
$I_{I\ LVDS,\ CML}$	LVDS and CML Output Current	Note 1	-24		24	mA
$V_{I\ CML}$	CML Input Voltage		V_{EE} +3		0.5	V
$V_{O\ CML}$	CML Output Voltage		V_{EE} +3		0.5	V
V_{ESD}	Static Discharge Voltage	HBM, Note 3			500	V
		CDM, Note 4			50	V
T_J	Junction Temperature	Note 2	-55		+125	°C
T_S	Storage Temperature		-65		+125	°C

Note 1: Nominal supply voltages.
Note 2: The maximum temperature equals a maximum case temperature of 105 °C (top side) with the device mounted on the GD90584/585 Evaluation Board.
Note 3: Human Body Model: MIL 883D 3015.7 standard.
Note 4: Charge Device Model.: JESD2-C101 standard.

DC Characteristics

T_{CASE}* = 0 °C to 70 °C. VEE = -5.2 V. VCC = +3.3 V. VDD is 0 V or GND.
All voltages in table are referred to VDD.
All currents are defined positive out of pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}	Negative Supply Voltage		-5.46	-5.2	-4.94	V
V_{CC}	Positive Supply for LVDS I/O		+3.135	+3.3	3.465	V
I_{EE}	Negative Supply Current			400	500	mA
I_{CC}	Positive Supply Current		-21	-17		mA
$V_{IH\ LVDS}$	LVDS Input Voltage High, (differential)		100			mV
$V_{IL\ LVDS}$	LVDS Input Voltage Low, (differential)				-100	mV
$V_{IVR\ LVDS}$	LVDS Input Voltage Range		0.8		2.4	V
$R_{IN\ LVDS}$	LVDS Input Resistor Termination	DC	80	100	120	Ω
$V_{OH\ OC}$	Open Collector Output Voltage High	Note 1	-0.05	0	+0.05	V
$V_{OL\ OC}$	Open Collector Output Voltage Low	Note 1	-0.5	-0.4	-0.3	V
$I_{OH\ OC}$	Open Output Current High	Note 1	-0.1	0	+0.1	mA
$I_{OL\ OC}$	Open Output Current Low	Note 1	-9	-8	-7	mA
$V_{OH\ OUT}$	OUT/OUTN Voltage High	Note 1, 10 MHz	-0.1	-0.05	+0.05	V
$V_{OL\ OUT}$	OUT/OUTN Voltage Low	Note 1, 10 MHz	-0.8 Note 3	-0.7	-0.5	V
$I_{OH\ OUT}$	OUT/OUTN Current High	Note 1		0		mA
$I_{OL\ OUT}$	OUT/OUTN Current Low	Note 1		-14		mA
$V_{IH\ SEL1\text{-}3,SGNX}$	SEL1-3, SGNX Input Voltage High	Note 2	0	V_{EE} + 2		V
$V_{IL\ SEL1\text{-}3,\ SGNX}$	SEL1-3, SGNX Input Voltage Low	Note 2	V_{EE}	V_{EE} + 0.8		V

Note 1: Output externally terminated by 50 Ω to 0 V.
Note 2: SEL1-3 and SGNX can be connected directly to VDD or VEE.
Note 3: $V_{OL\ OUT}$ MIN. may require VCUR adjustment, VCUR > -1 V.
***:** T_{CASE} measured at the center of the top.

AC Characteristics, General

T_{CASE} *= 0 °C to 70 °C, VEE = -5.2 V. VCC = +3.3 V.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
J_{TRF}	Jitter transfer	f < 8 MHz Note 1		0.0	0.1	dB
J_{GEN}	Jitter generation	12 kHz < f < 80 MHz Note 1			0.1	UI_{PP}
V_{OUT}	10 Gbit/s output voltage	Note 3, VCUR open -0.5 V < VCUR < 0 V	550 800	650		mV_{PP} mV_{PP}
Γ_{OUT}	OUT/OUTN output reflection coefficient	Note 2		-10		dB
F_{REFCK}	Reference clock jitter	REFCK/REFCKN, f < 10 MHz			+5	ps_{PP}
$D_{CYCLE, CKOUT/N}$	CKOUT/CKOUTN duty cycle	Differential	45		55	%
$D_{CYCLE, REFCK}$	REFCK duty cycle		40		60	%
$F_{MAX, REFCK}$	Maximum REFCK/N frequency	GD16585 GD16589			635 680	MHz MHz

Note 1: With the recommended loop filter.
Note 2: From DC to 6 GHz, measured on the GD90584/585 Evaluation Board.
Note 3: The output voltage is adjustable by pin VCUR.

***:** T_{CASE} measured at the center of the top.

AC Characterisitcs, Source Synchronous Clocking - OIF99.102.5

T_{CASE}* = 0 °C to 70 °C, VEE = -5.2 V.

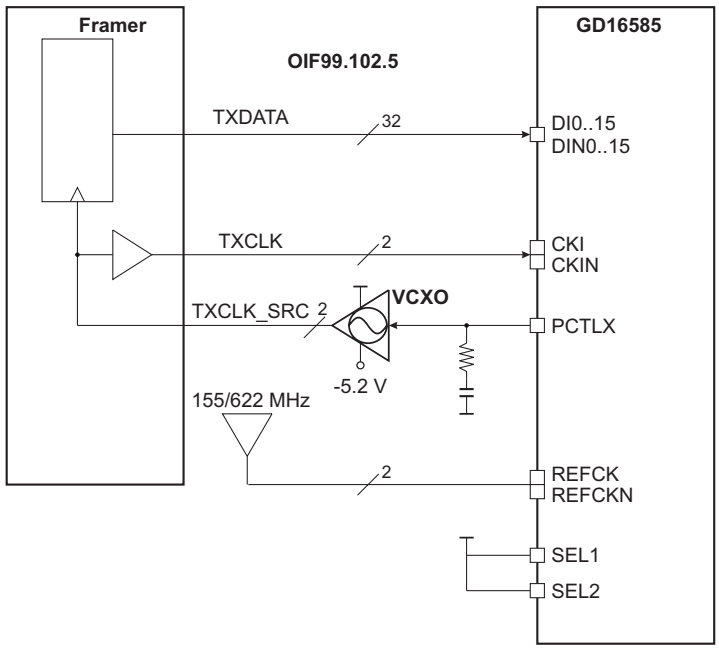


Figure 10. *OIF interface.*

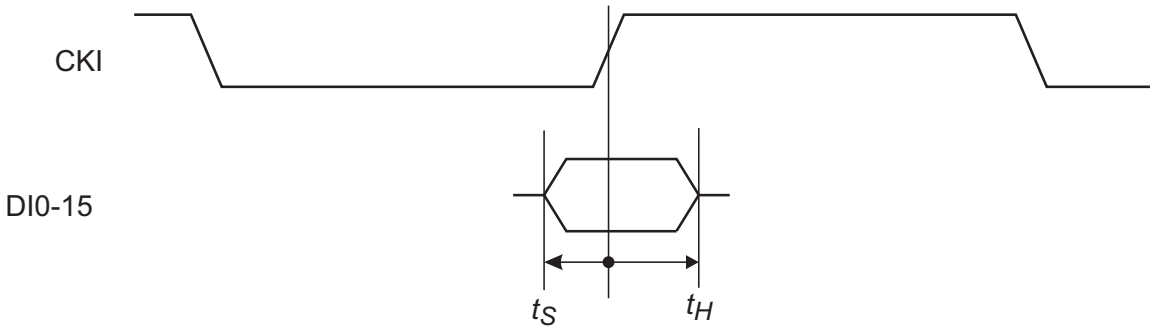


Figure 11. *Timing relation between input data and clock.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
t_S	DI0-15 setup	SEL1 = SEL2 = “1”			125	ps
t_H	DI0-15 hold	SEL1 = SEL2 = “1”			175	ps

Note: The setup and hold time is defined from the rising edge of CKI. The setup time is positive before the edge and the hold time is positive after the edge.

***:** T_{CASE} measured at the center of the top.

AC Characteristics, Forward Clocking to System ASIC

T_{CASE} *= 0 °C to 70 °C, VEE = -5.2 V.

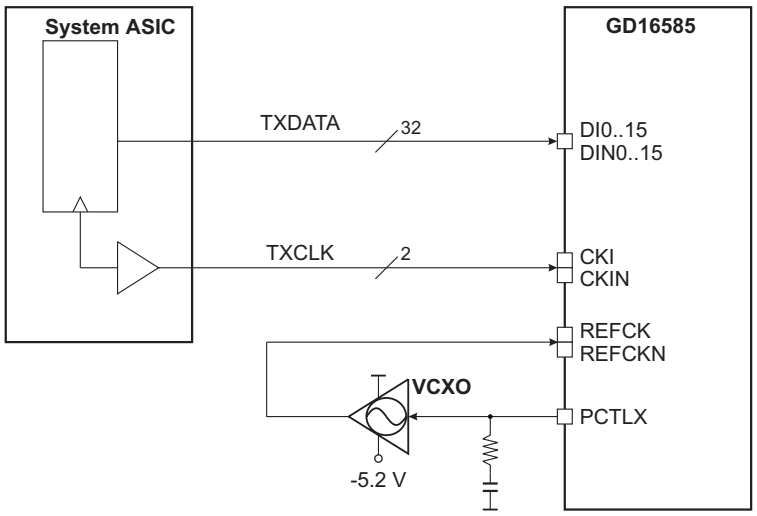


Figure 12. *Forward clocking with phase nulling circuit.*

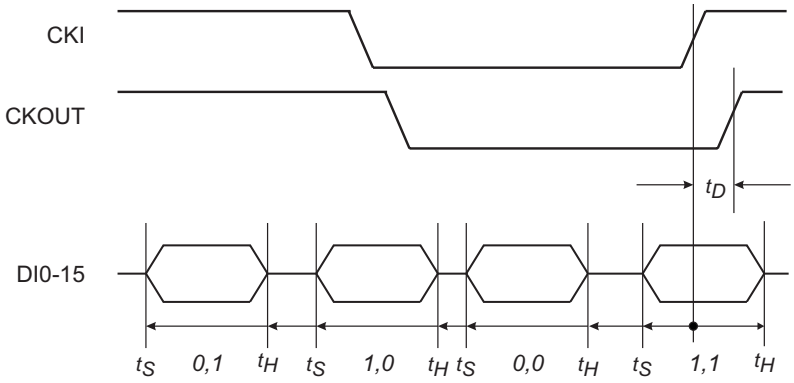


Figure 13. *Timing relation between input data and clock.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$t_{S,11}$	DI0-15 setup time	(SEL1,SEL2) = (1,1)			125	ps
$t_{H,11}$	DI0-15 hold time	(SEL1,SEL2) = (1,1)			175	ps
$t_{S,00}$	DI0-15 setup time	(SEL1,SEL2) = (0,0)			560	ps
$t_{H,00}$	DI0-15 hold time	(SEL1,SEL2) = (0,0)			-260	ps
$t_{S,10}$	DI0-15 setup time	(SEL1,SEL2) = (1,0)			930	ps
$t_{H,10}$	DI0-15 hold time	(SEL1,SEL2) = (1,0)			-630	ps
$t_{S,01}$	DI0-15 setup time	(SEL1,SEL2) = (0,1)			1350	ps
$t_{H,01}$	DI0-15 hold time	(SEL1,SEL2) = (0,1)			-1050	ps
t_D	Delay between CKI and CKOUT				TBD	ps

Note: The setup and hold time is defined from the rising edge of CKI. The setup time is positive before the edge and the hold time is positive after the edge.
SEL3 = “0”

***:** T_{CASE} measured at the center of the top.

Package Outline

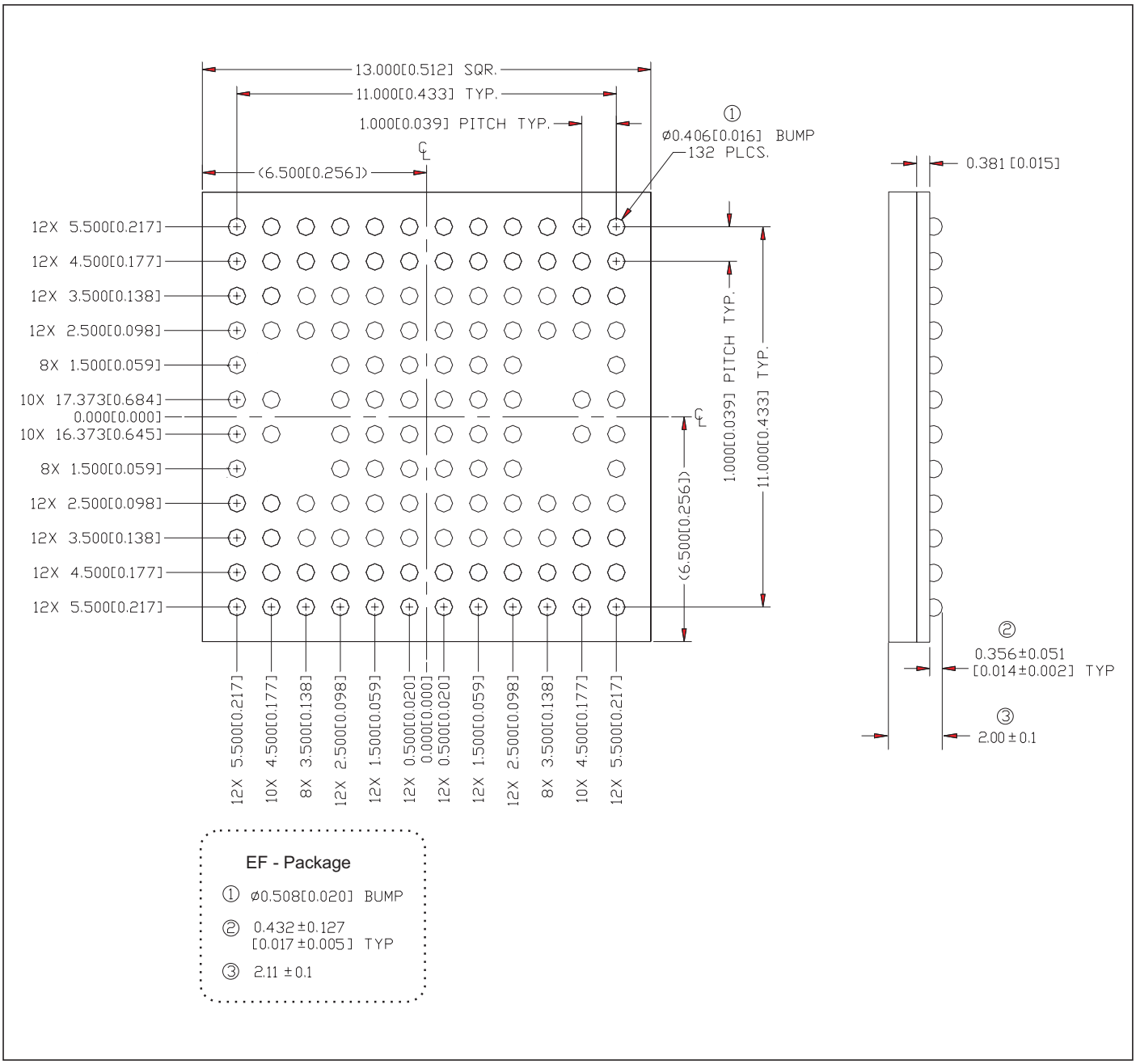


Figure 14. *Package 132 ball Ceramic BGA (EB and EF package).*

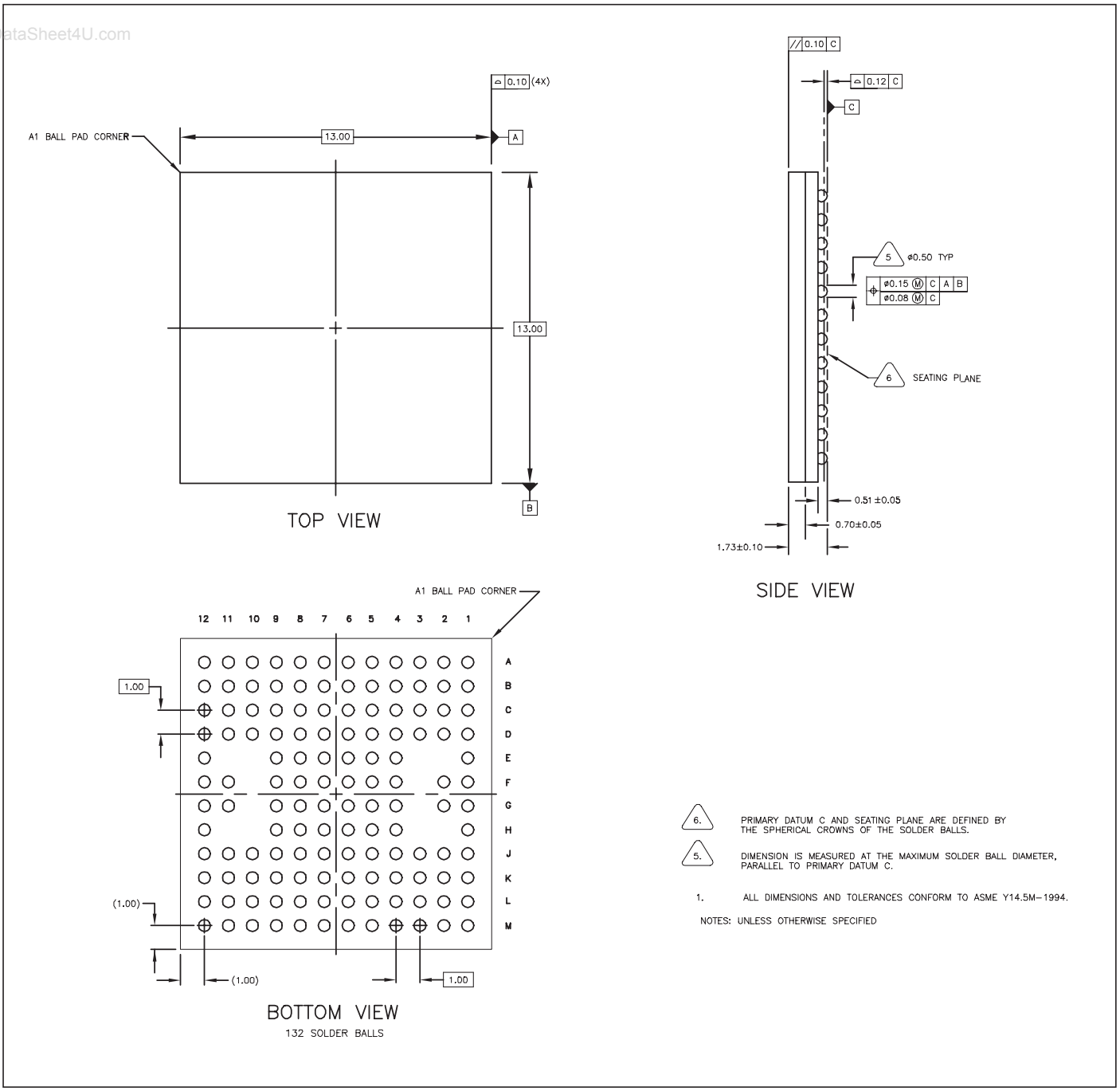


Figure 15. *Package 132 ball Plastic BGA (FB package).*

Device Marking

Figure 16. *Device marking. Top view.*

Ordering Information

To order, please specify as shown below:

Product Name:	Version:	Package Type:	Intel Order Number:	Case Temperature Range:
GD16585-EB	10 Gbit/s	132 ball (16 mil) Ceramic BGA	**HCGD16585EB** MM# 835479	0...70 °C
GD16585-EF	10 Gbit/s	132 ball (20 mil) Ceramic BGA	**HCGD16585EF** MM# 837348	0...70 °C
GD16585-FB	10 Gbit/s	132 ball (20 mil) Plastic BGA	**RCGD16585FC** MM# TBD	0...70 °C
GD16589-EB	10.66 Gbit/s	132 ball (16 mil) Ceramic BGA	**HCGD16589EB** MM# 835481	0...70 °C
GD16589-EF	10.66 Gbit/s	132 ball (20 mil) Ceramic BGA	**HCGD16589EF** MM# 837350	0...70 °C
GD16589-FB	10.66 Gbit/s	132 ball (20 mil) Plastic BGA	**RCGD16589FC** MM# TBD	0...70 °C

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