an Intel company

1.244 GHz Generic PLL Clock Synthesiser GD16590

Preliminary

General Information

The GD16590 is a generic PLL clock synthesiser. The device targets clock distribution in SDH/SONET telecommunication systems but is well suited for a wide range of applications requiring high performance high-speed clock synthesis.

The device implements a fully integrated multiplying PLL including:

- An on-chip Voltage Controlled Oscillator (VCO)
- Phase-Frequency Detector
- Programmable frequency dividers (prescalers).

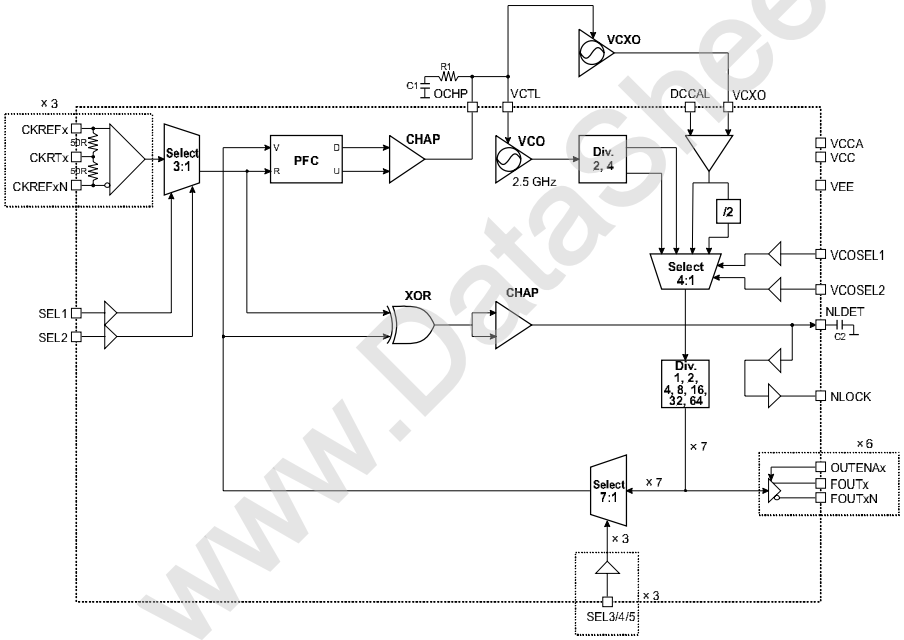
The loop-filter is external in order to optimise the PLL for different applications.

As an option the GD16590 may be operated with an external Voltage Controlled Crystal Oscillator for applications demanding a high-Q oscillator.

The reference clock may range from 19 to 622 MHz.

The GD16590 requires a single +3.3 V power supply.

The device is housed in a 48 TQFP 7 × 7 mm thermally enhanced package.



Features

- Six separate differential clock outputs from the PLL at :
  1,244.16 / 622.08 MHz
  1,244.16 / 622.08 MHz
  622.08 / 311.04 MHz
  311.04 / 155.52 MHz
  155.52 / 77.76 MHz
  77.76 / 38.88 MHz
  all with separate enable.
- Three independent selectable reference clock inputs.
- Intrinsic jitter: 0.005 UI_{PP} @ 622 MHz.
- Low phase skew between output clocks: < 200 ps.
- Optional external VCXO possible.
- Simple external loop filter.
- Lock detect output signal.
- Single power supply: +3.3 V.
- Low power operation: 0.54 W (Typ.).
- Package: 48 pin TQFP (7 × 7 mm).

Applications

- Tele Communications systems:
  – SDH
  – SONET
- Datacom
- High-speed general clock distribution.

Functional Details

The GD16590 comprises:
- a low-noise LC-type VCO
- a Phase-Frequency Detector
- frequency dividers (prescalers)
- a charge pump

into an integrated PLL frequency synthesiser. Careful design and layout matching ensures short delay and minimum skew between input reference clocks and outputs.

Jitter Performance

The frequency of the input reference clock may range between 19.44 MHz and 622.08 MHz. Since changing the reference frequency alters the loop-gain within the PLL it may be necessary to adjust the loop-filter components when switching to a different reference frequency in order to achieve ITU-T recommended performance.

PLL Propagation Delay

When the PLL is in lock the Phase Frequency Detector aligns the positive (low to high transition) flanks of the reference clock and divided VCO clock on it's inputs. These inputs are marked R and V on the Figure 1. This means the positive transition of any FOUTx output clock is aligned with the positive transition of the reference clock under the condition of equal reference clock frequency and FOUTx output frequency, please refer to Figure 7. Figure 7 defines the PLL propagation delay parameter (D_{OUT}) that is the skew between the reference clock and output clock when the loop is locked. Note that D_{OUT} will change with leakage currents drawn from the loop-filter, hence D_{OUT} is loop-filter dependant.

Figure 9 shows a measurement of D_{OUT}. The CKREF1 input signal is shown together with the FOUTA output signal, both running 622 MHz with the PLL locked using the recommended loop-filter and no excessive leakage current drawn from the charge pump output. A skew of approximately 80 ps was observed. The skew has been investigated over supply and temperature and was observed as less than 200 ps at any combination of extremes. The observations are only valid with the PLL locked when using the recommended loop-filter.

Figure 10 illustrates the phase relationship when a 155 MHz clock is input at CKREF1 and the FOUTA output is running at 622 MHz. Note the asymmetric reference clock.

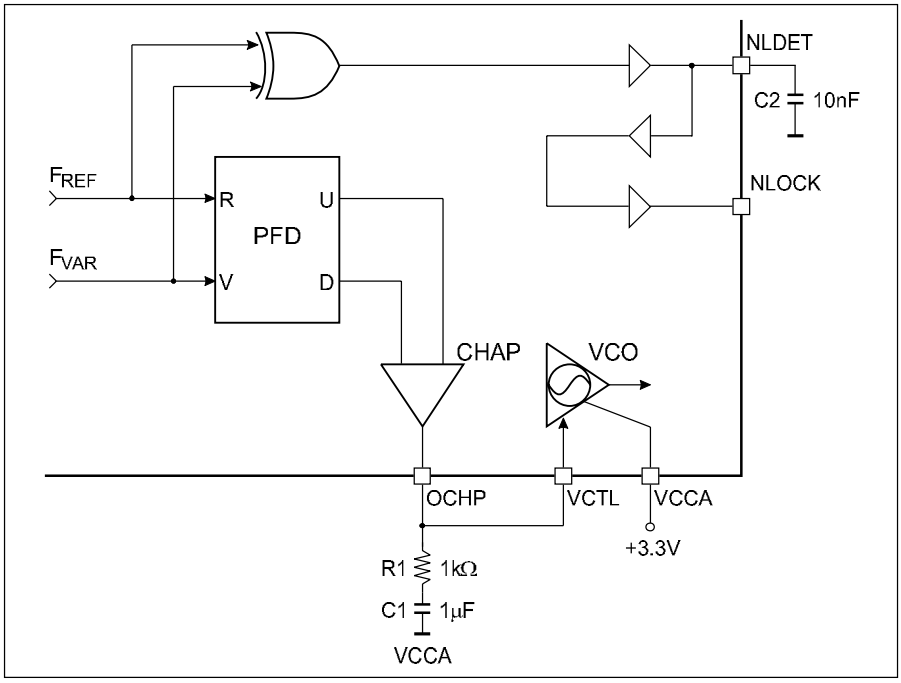


Figure 1. *Application diagram.*

Output Clocks

The GD16590 is equipped with six LVPECL compatible output buffers. Each of the output buffers is equipped with an LVTTL enable pin that may be used to disable clock signals not in use for noise reduction. The phases of the clock output signals are aligned with less than 200 ps skew peak-to-peak between any two clock signals. Available clocks signals from the PLL are divide by 1 (signal FOUTA and by FOUTB), divide by 2 (FOUT2), divide by 4 (FOUT4), divide by 8 (FOUT8) and divide by 16 (FOUT16).

Lock Detect

The device outputs a signal NLDET that may be used to signal whether or not the PLL is locked thus allowing fault diagnostics. The NLDET outputs the result of an XOR operation on the signals input to the phase-frequency detector. To be useful this signal must be filtered by a capacitor. The recommended value of this capacitor is 10 nF. The filtered lock-detect signal is output as an LVTTL compatible signal on the output NLOCK via a comparator.

PLL Loop-filter

It has been chosen to locate the passive loop-filter components externally to the device. This allows for easy optimisation of the loop-filter to different applications. The recommended loop-filter is a simple first-order RC-circuit as shown on Figure 1, resulting in a second order, type 2 loop.

The values of R and C depend on the application. With respect to ITU-T recommended jitter performance appropriate values for R and C have been determined to R = 1 kΩ and C = 1 μF.
The values ensures stable operation with reference clock ranging from 19 MHz to 622 MHz. Note that the loop-filter should be terminated to the positive VCO supply. An external VCXO might require a different termination point for lowest point.

Charge Pump Polarity

When the PLL increases the VCO frequency, the charge pump pin OCHP sinks current. That is, the voltage on the loop- filter capacitor drops to increase the oscillator frequency. So be aware, that an external VCO must have a negative VCO constant in order to achieve a stable lock.

On-chip VCO Power Down

When operated with an external VCXO the on-chip VCO should be powered down for noise reduction. This is done by leaving VCCA open.

VCO source and corresponding VCOSEL1, - 2 settings		FOUTA [MHz]	Input reference frequency (CKREFx [MHz]) and corresponding SEL3, -4, -5 settings							
			0,0,0	0,0,1	0,1,0	0,1,1	1,0,0	1,0,1	1,1,0	1,1,1
Internal VCO Ext. VCO: 1,244 MHz Ext. VCO: 622 MHz	0,1 0,0 1,1	622	622	311	155	78	39	19	N.A. (9.7)	Disable Feedback
Internal VCO Ext. VCO: 2,488 MHz Ext. VCO: 1,244 MHz	1,0 0,0 1,1	1,244	N.A. (1.244)	622	311	155	78	39	19	

Table 1. Input reference frequencies as function of SEL3/4/5 settings.

Prescaler Settings

For the PLL to achieve lock a proper relation must exist between the input reference frequency and the setting of the on-chip prescalers. The prescalers are set by signals: VCOSEL1, VCOSEL2, SEL3, SEL4, and SEL5 (refer to Table 1).

First, determine the desired master output frequency. This is the frequency of output clock FOUTA (FOUTA is mirrored by FOUTB). Next, select whether the oscillator is external or internal. The VCO source can be external (622, 1244 or 2488 MHz) or internal (2488 MHz). The Table 1 gives the value of VCOSEL1/2. Finally, the proper relation between the reference clock frequency and the setting of SEL3, SEL4, SEL5 is read from the Table 1.

Duty Cycle Calibration

When operated with an external oscillator the differential LVPECL inputs (VCXO and DCCAL) are to be used. In single-ended operation the duty cycle of the outputs FOUTA and FOUTB may be adjusted by tuning the voltage on DCCAL.

Practical Considerations

When designing the PCB it is important to consider noise issues. De-coupling capacitors should be applied to each supply pin. Output clock lines must be routed as transmission lines.

The reference clock inputs are terminated on-chip by 50 Ω to the positive supply. Refer to Figure 3. The termination pins CKRT1..3 are biased on-chip to 2 V. The input impedance seen into CKRT1..3 equals 1 kΩ.

The LVPECL clock outputs are terminated according to Figures 4 and 5.

Note: Unused clock outputs must be disabled or properly terminated.

LVTTL select pins are terminated on-chip with a 16 kΩ pull-up resistor giving a logic "1" when not connected.

When more than two clock outputs are used the heatsink must be connected to the positive power supply. In any case it is recommended to solder the heatsink onto a VCC power plane.

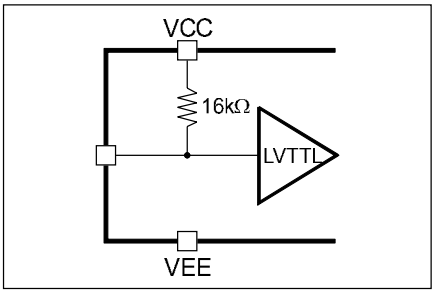


Figure 2. *LVTTL select pin.*

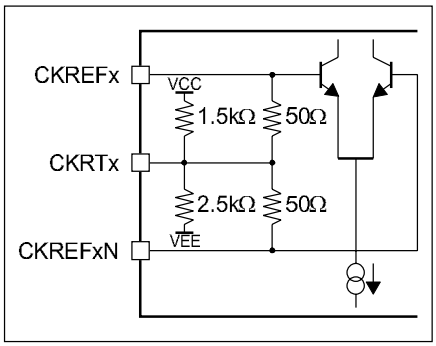


Figure 3. *Termination of CKREFx pins.*

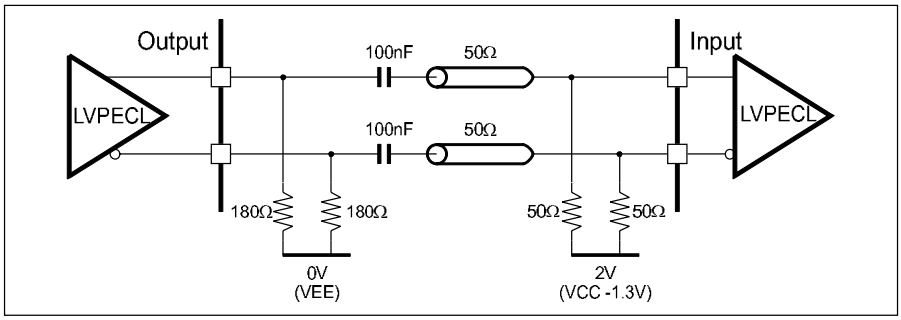


Figure 4. *LVPECL Output Termination, AC-coupled.*

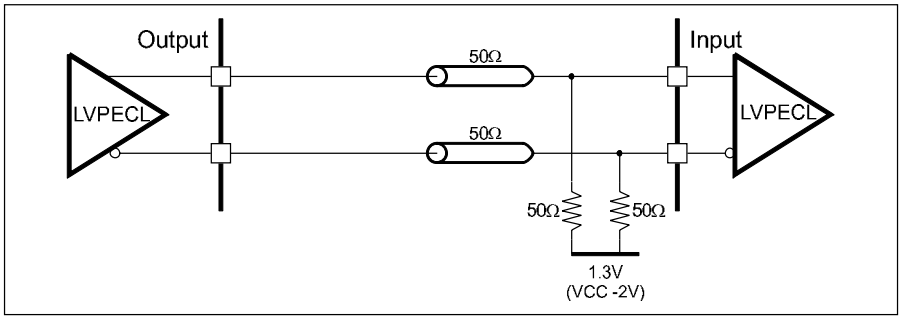


Figure 5. *LVPECL Output Termination, DC-coupled.*

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
CKREF1 CKREF1N CKRT1	2 3 4	LVPECL IN	Differential. One of three reference inputs. The input frequency is depending on the mode of operation, Maximum 670 MHz. CKRT1 is the common termination point of 2 × 50 Ω resistors, internally biased to 2 V. $Z_{IN,CKRT1}$ = 1 kΩ.
CKREF2 CKREF2N CKRT2	6 7 5	LVPECL IN	Differential. One of three reference inputs. The input frequency is depending on the mode of operation, Maximum 670 MHz. CKRT2 is the common termination point of 2 × 50 Ω resistors, internally biased to 2 V. $Z_{IN,CKRT2}$ = 1 kΩ
CKREF3 CKREF3N CKRT3	10 11 9	LVPECL IN	Differential. One of three reference inputs. The input frequency is depending on the mode of operation, Maximum 670 MHz. CKRT3 is the common termination point of 2 × 50 Ω resistors, internally biased to 2 V. $Z_{IN,CKRT3}$ = 1 kΩ .
SEL1, SEL2	8, 14	LVT IN	Select for input reference clock. The pins are equipped with 16 kΩ pull-up resistors. SEL1 SEL2 0 0 CKREF1 0 1 CKREF2 1 0 CKREF3 1 1 No input reference to PLL (default)
SEL3, SEL4, SEL5	41, 44, 45	LVT IN	Select for prescaler. The pins are equipped with 16 kΩ pull-up resistors. SEL3 SEL4 SEL5 0 0 0 Divide by 1 ($CKREF_{NOM}$ = 622 MHz) 0 0 1 Divide by 2 ($CKREF_{NOM}$ = 622 / 311 MHz) 0 1 0 Divide by 4 ($CKREF_{NOM}$ = 311 / 155 MHz) 0 1 1 Divide by 8 ($CKREF_{NOM}$ = 155 / 78 MHz) 1 0 0 Divide by 16 ($CKREF_{NOM}$ = 78 / 39 MHz) 1 0 1 Divide by 32 ($CKREF_{NOM}$ = 39 / 19 MHz) 1 1 0 Divide by 64 ($CKREF_{NOM}$ = 19 MHz) 1 1 1 No feed back to PLL from VCO (default)
VCOSEL1, VCOSEL2	35 38	LVT IN	Select for internal or external oscillator and prescale. The pins are equipped with 16 kΩ pull-up resistors. VCOSEL1 VCOSEL2 0 0 External VCXO, divide by 2, (F_{MAX} = 2.7 GHz) 0 1 Internal VCO, F_{NOM} = 622 MHz 1 0 Internal VCO, F_{NOM} = 1.244 MHz 1 1 External VCXO, divide by 1 (F_{MAX} = 1.35 GHz) (default)
VCXO, DCCAL	40, 39	LVPECL IN	Differential external clock input, F_{MAX} = 2.7 GHz / 1.35 GHz. The input can be used differentially or the DCCAL input may be used as a VCXO duty cycle control. When selecting external VCXO (divide by 1) the Duty cycle of the FOUTA/B, FOUTA/BN outputs can be controlled by DCCAL. Adjust range: 40/60 .. 60/40 assuming sinusoidal input at VCXO. DCCAL is connected to the inverted input. For detalis regarding ESD, please refer to Note 2 on page 7.
OUTENAA OUTENAB OUTENA2 OUTENA4 OUTENA8 OUTENA16	32 29 26 21 18 15	LVT IN	Output enable. The pins are equipped with 16 kΩ pull-up resistors. When set to “1” (default), the FOUTx output is enabled. When set to “0”, the FOUTx output is disabled. Disabled implies a fixed logic “0" at the output. When disabled the output will be active with respect to DC.
FOUTA, FOUTAN FOUTB, FOUTBN FOUT2, FOUT2N FOUT4, FOUT4N FOUT8, FOUT8N FOUT16, FOUT16N	34, 33 31, 30 28, 27 23, 22 20, 19 17, 16	LVPECL OUT	Differential clock outputs from PLL. $F_{FOUTA, NOM}$ = 1244 / 622 MHz $F_{FOUTB, NOM}$ = 1244 / 622 MHz $F_{FOUT2, NOM}$ = 622 / 311 MHz $F_{FOUT4, NOM}$ = 311 / 155 MHz $F_{FOUT8, NOM}$ = 155 / 78 MHz $F_{FOUT16, NOM}$ = 78 / 39 MHz
VCTL	47	Analog IN	Voltage control pin for internal VCO. To be connected to the loop-filter.

Mnemonic:	Pin No.:	Pin Type:	Description:
OCHP	46	Analog OUT	Charge Pump output to be connected to the Loop Filter (Refer to Figure 1 on page 2). The pin will sink current to increase the oscillator frequency and source current to decrease the oscillator frequency.
NLDET	43	Analog OUT	Lock-detect unfiltered. Connect this pin to a 10 nF capacitor.
NLOCK	42	LVT OUT	Lock detect buffered. When 10 nF is connected to NLDET, then NLOCK = “0” signals PLL in-lock and NLOCK = “1” signals PLL out-of-lock.
VCC	13, 24, 37	PWR	+3.3 V supply. Must be thoroughly decoupled.
VCCA	48		+3.3 V supply for VCO. Leave open when used with an external oscillator.
VEE	1, 12, 25, 36	PWR	0 V supply.
Heatsink	—	PWR	+3.3 V supply. Heatsink facing down. Must be electrically connected when more than two clock outputs are used.

Package Pinout

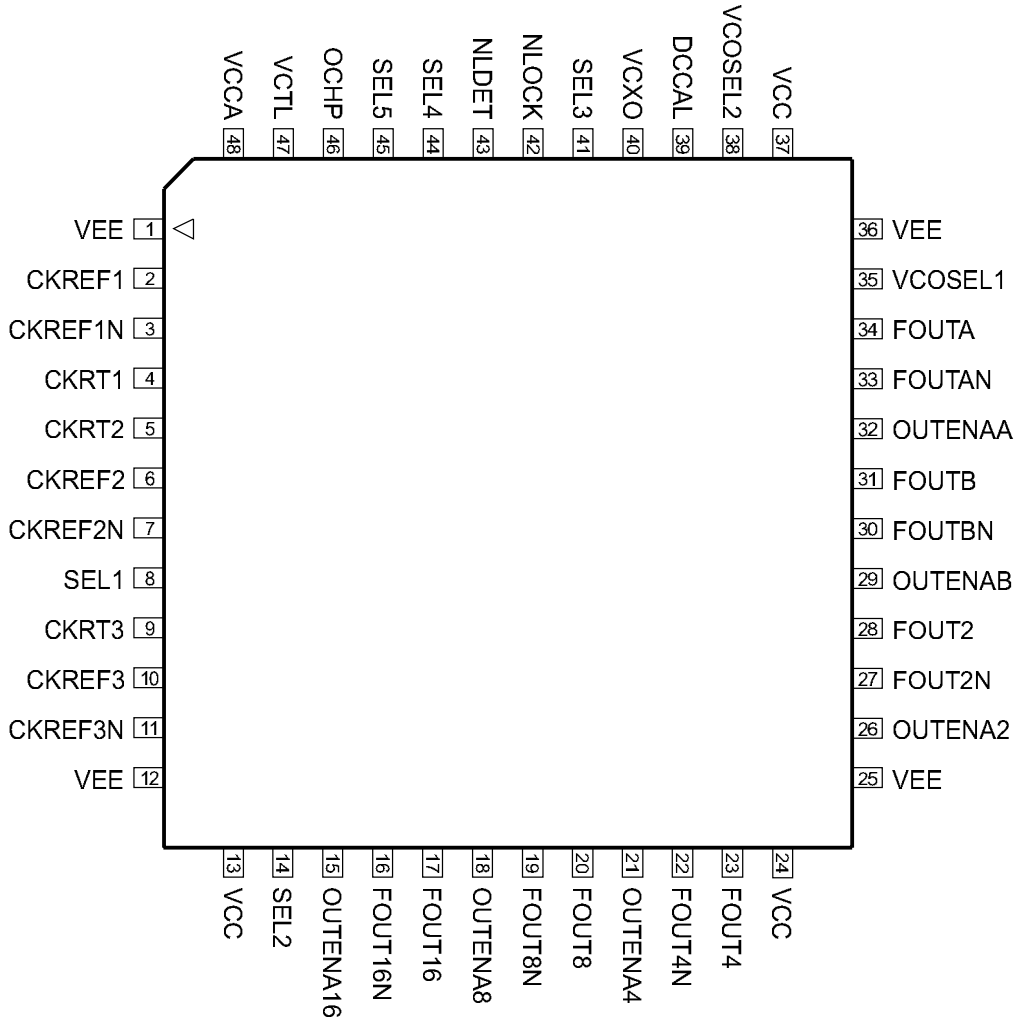


Figure 6. *Package Pinout, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to V_{EE}.
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT.:
V_{CC} , V_{CCA}	Supply Voltage		-0.5		4	V
V_0 *MAX*	Output Voltage		-0.5		V_{CC}	V
I_0 *MAX, LVPECL*	Output Current		-30		30	mA
V_I *MAX*	Input Voltage		-0.5		V_{CC} + 0.5	V
I_I *MAX*	Input Current		-1.0		1.0	mA
T_0	Operating Temperature	Junction	-40		125	°C
T_S	Storage Temperature		-65		125	°C
θ_{J-C}	Thermal Resistance	Junction – Case		5		°C/W
V_{IO}, *ESD*	Electrostatic Discharge Voltage	HBM - Note 1, 2			1000	V
		CDM - Note 3			50	V

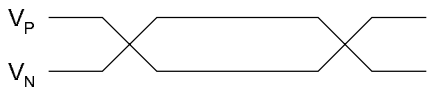
Note 1: Human Body Model: MIL std. 883D 3015.7 standard.
Note 2: Pins DCCAL (pin 39) and VCXO (pin 40) can handle ESD, HBM of maximum value: 500 V.
Note 3: Charge Device Model: JESD2-C101 standard.

DC Characteristics

$T_{AMBIENT}$ = -5 °C to 85 °C.
All voltages in table are referred to V_{EE}.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Positive Supply Current	Note 1		165		mA
V_{REF}	Internal LVPECL Reference for VCXO Input		1.8	2.0	2.2	V
$V_{REF, LVT}$	Internal LVT Reference		1.33	1.4	1.54	V
$V_{ICM, LVPECL}$	LVPECL Input Common Mode Voltage	Note 2, 3	V_{CC}-1.5		V_{CC}-1.1	V
$V_{IDIFF, LVPECL}$	LVPECL Differential Input Voltage	Note 2, 3, 7	0.250	0.500	1.400	V
V_{OH} LVPECL	LVPECL Output HI Voltage	Note 4	V_{CC} - 1.1		V_{CC} - 0.6	V
V_{OL} LVPECL	LVPECL Output LO Voltage	Note 4	V_{CC} - 2.00		V_{CC} - 1.5	V
$V_{ODIFF, LVPECL}$	LVPECL Differential Output Voltage	Note 2, 3, 4	0.600		1.300	V
$R_{TERM, CKREF}$	CKREF1..3 Internal Termination Resistor			50		Ω
$V_{IH, LVT}$	LVT Input HI Voltage		2		V_{CC}	V
$V_{IL, LVT}$	LVT Input LO Voltage		0		0.8	V
I_{IH} LVT	LVT Input HI Current	Note 5			200	µA
I_{IL} LVT	LVT Input LO Current	Note 5	-500			µA
V_{OH} LVT	LVT Output HI Voltage	I_{OH}= 3 mA	2.1		V_{CC}	V
V_{OL} LVT	LVT Output LO Voltage	I_{OL}= -1 mA	0		0.4	V
I_O OCHP	Charge Pump Output Current	Note 5, 6	-125		125	µA
V_O OCHP	Charge Pump Output Voltage	Note 5, 6	0.3		V_{CC}-0.3	V

Note 1: I_{MAX}: 1.3 × I_{TYP}; P_{MAX} = I_{MAX} × $V_{SUPPLY,MAX}$.
Note 2: Definition of common mode voltage: $V_{CM} = (V_p + V_N)/2$.
Note 3: Definition of differential voltage: $V_{DIF} = V_P - V_N$



Note 4: R_{load} = 50 Ω to V_{CC} -2.0 V.
Note 5: Under the condition of typ. supply voltage.
Note 6: Assuming a purely capacitive load.
Note 7: Regarding the reference clock inputs it has been observed that the combination of high input amplitude and an asymmetric input may cause increased jitter on the outputs. If asymmetric reference clocks are applied it is recommended that the signal amplitude does not exceed 500 mV_{PP}.

AC Characteristics

$T_{AMBIENT}$ = -5 °C to 85 °C.
All voltages in table are referred to V_{EE}.

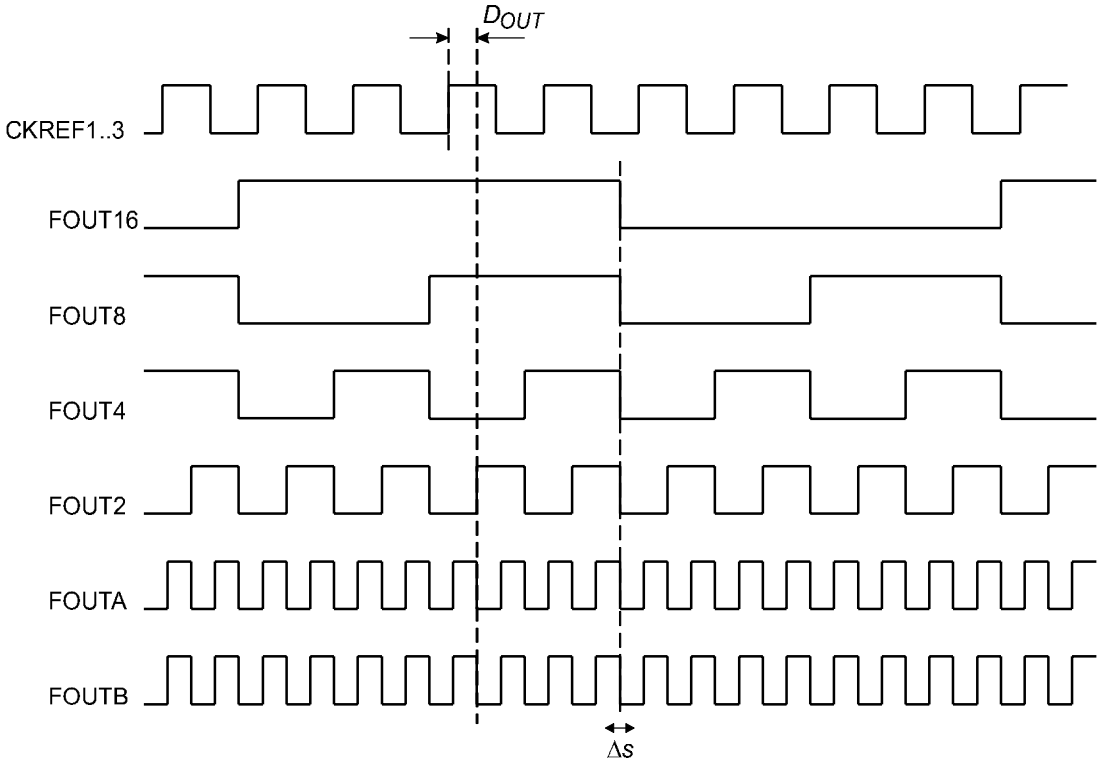


Figure 7. *Timing of output clocks with defination of output delay and peak-to-peak skew.*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
F_{VCO}	VCO tuning range	Note 1	560		662	MHz
K_{VCO}	VCO gain constant @622 MHz			-43		MHz/V
$J_{INTRINSIC}$	Intrinsic jitter	Note 2 @622 MHz Ref. Clk. Freq.		1		$mUI_{RMS,}$
$J_{TRANSFER}$	Jitter transfer function Please refer to Figure 8 on page 10.	F_{JITTER} < 2 MHz F_{JITTER} > 2 MHz Note 3			0 -20	dB dB/dec.
D_{OUT}	Output delay from reference clock (CKREFx) to clock output (FOUTx)	FOUTA,FOUTB FOUT2,4,8,16 Note 5	25 75	75 175	125 250	ps ps
Duty Cycle	Clock duty cycle, any FOUTx	Differential, Note 4	48	50	52	%
$t_{RISE/FALL, LVPECL}$	LVPECL output rise / fall time	20 / 80% differential			300	ps
Δs	Output clock skew				200	ps

Note 1: VCOSEL set to divide by 4. Maximum frequency at 670 MHz (measured at FOUTA/FOUTB) can be achieved by increasing the supply voltage to 3.5 V.
Note 2: Measurement range 12 kHz..20 MHz.
Note 3: The loop-filter is dependent on the frequency of the reference clock signal in order to exceed ITU-T jitter masks.
Note 4: When external the VCXO (divide by 1) is selected, DCCAL can be used to obtain the duty cycle requirements.
Note 5: Parameter D_{OUT} is leackage current depent and only defined when the PLL is locked using the recommended loop-filter, D_{OUT} is only defined for input and output signals of equal frequency.

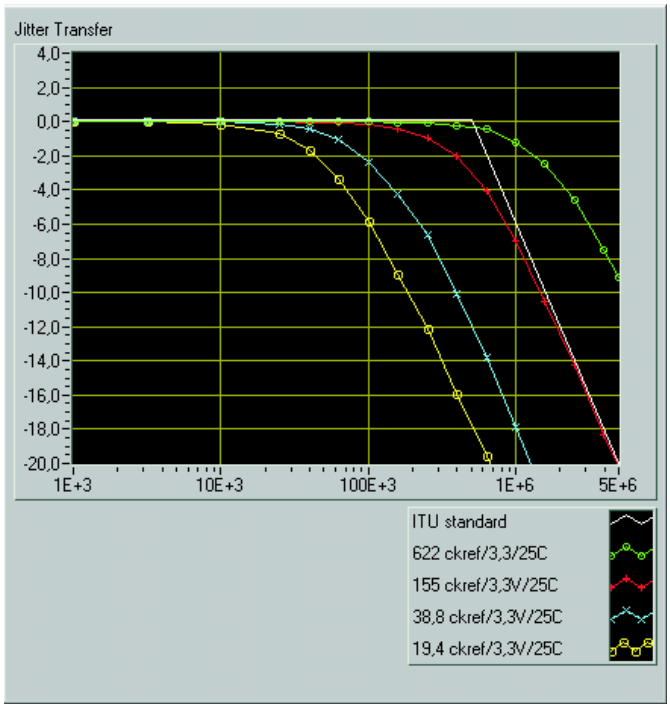


Figure 8. *Jitter transfer bandwidth vs reference clock frequency with loop filter of 1 kΩ in series with 2.2 µF.*

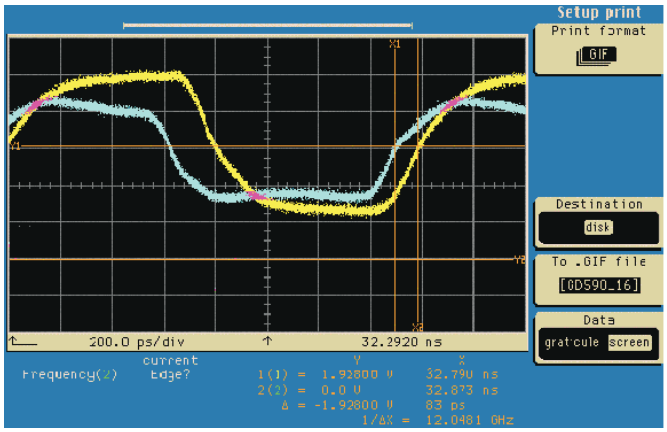


Figure 9. *Typical timing skew between CKREF1 input and FOUTA output, both recorded @622 MHz, V_{CC} = 3.3 V, Ta = 23°C.*

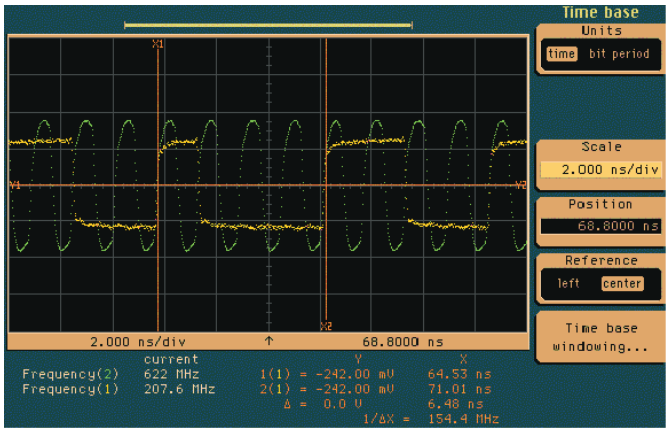
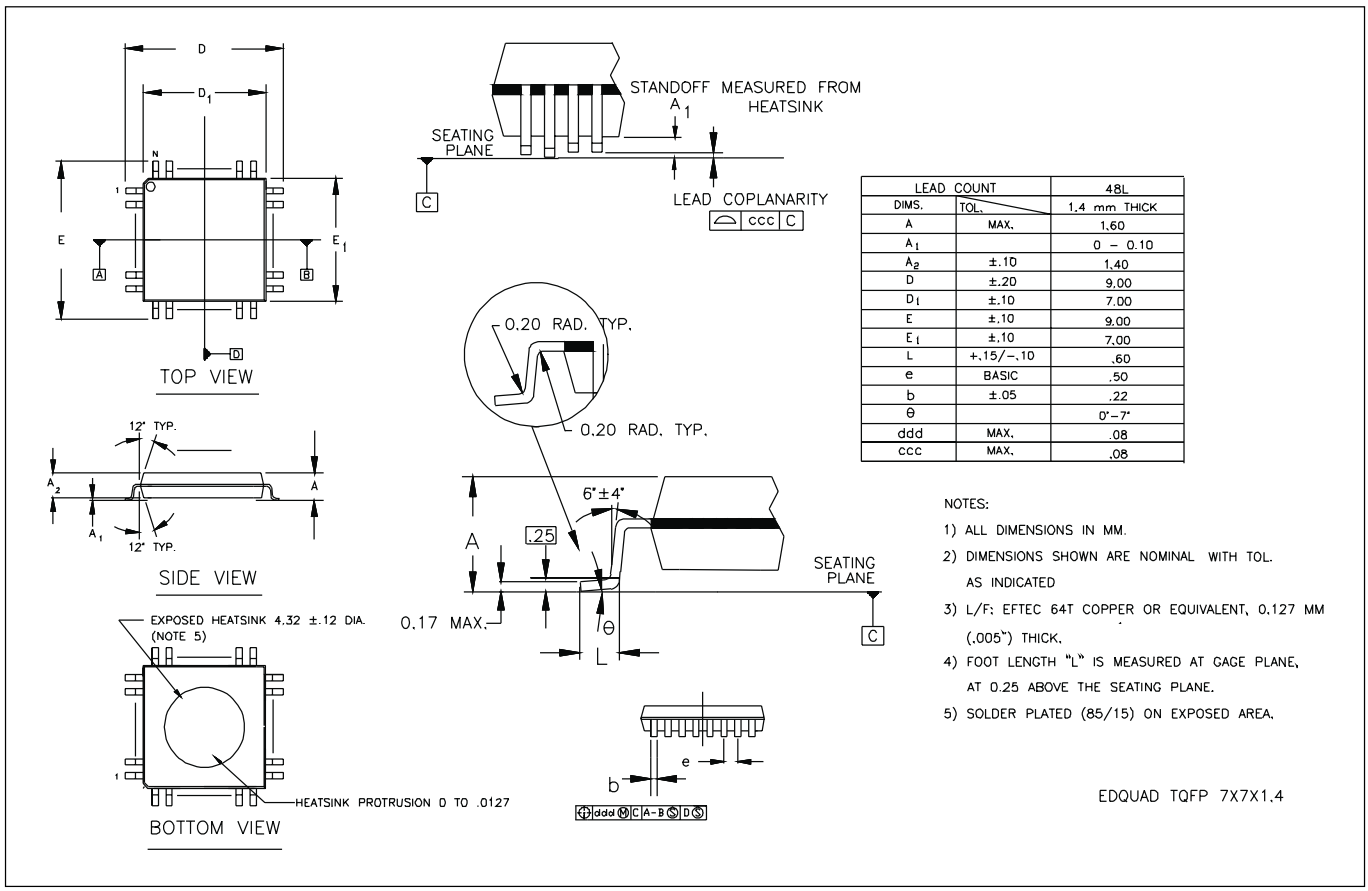


Figure 10.*Phase relation between the CKREF1 input @155MHz and the FOUTA output @622 MHz.*

Package Outline



LEAD COUNT		48L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		0 – 0.10
A_2	±.10	1.40
D	±.20	9.00
D_1	±.10	7.00
E	±.10	9.00
E_1	±.10	7.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

NOTES:
1) ALL DIMENSIONS IN MM.
2) DIMENSIONS SHOWN ARE NOMINAL WITH TOL. AS INDICATED
3) L/F: EFTEC 64T COPPER OR EQUIVALENT, 0.127 MM (.005") THICK.
4) FOOT LENGTH "L" IS MEASURED AT GAGE PLANE, AT 0.25 ABOVE THE SEATING PLANE.
5) SOLDER PLATED (85/15) ON EXPOSED AREA.

Figure 11.*Package 48 pin, TQFP. All dimensions are in mm.*

Device Marking

Figure 12.*Device marking, top view.*

Ordering Information

To order, please specify as shown below:

Product Name:	Intel Order Number:	Package Type:	Ambient Temperature Range:
GD16590-48BA	**FAGD1659048BA** MM#: 836076	48 lead TQFP, EDQUAD	-5..85 °C

an Intel company
Mileparken 22, DK-2740 Skovlunde
Denmark
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E-mail : sales@giga.dk
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