GigaDevice Semiconductor Inc.

GD30BC2416x

1.5A Switching charger with power path management

Datasheet

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- Extreme low quiescent current, <5uA in sleep mode
- Charging features
  - Switching charging up to 1.5A maximum current programmable through ISET
  - Support variety of battery chemistries, 4.1/4.2/4.3/4.35/4.4V @0.5%
  - Full charge cycle: pre-charge, constant current and constant voltage
  - Charging current and pre-charging current are all programmable through I^2C
- Boost converter
  - Support up to 1A load current
  - High efficiency synchronous boost converter @95%
  - Output current limit programmable through I^2C, 1.6A/1.8A/2.0A/2.2A
- Power path management
  - Power path management allows simultaneous battery charging and system supply, system discharge priority
  - When the system load increases, the charging current is reduced dynamically according to the input current and system voltage
  - USB current limit programmable through I^2C, 95%/100%/105%/110% @I_{CCCH} + 0.5A (Maximum current 3A)
  - Over voltage protection up to 5.6V, V_{SYS} voltage regulation limit: 4.6V
- Protection features
  - Short Circuit Protection
  - Over/Under temperature protection
  - Input Over Voltage/Current Protection
  - Boost over voltage (OV) during charge @5.5V
  - Boost under voltage (UV) when charge/discharge @4.3V
- Additional features
  - 3.3V LDO support 50mA
  - Programmable LED driver
  - Low external component count
  - Simple I^2C compatible interface

2 Applications

- Headsets and hearing aids
- Low battery applications such as smart watches and fitness accessories
- Patient monitors and portable medical equipment

3 General description

The GD30BC2416x is a highly integrated, programmable, low quiescent current power management integrated circuit (PMIC) that integrates the most common needs for wearables and low power battery applications.

The GD30BC2416x integrates a switching charger of programmable charging current (up to 1.5A) and a synchronous boost converter at Typical 5V output. The IC also includes a 12-bit ADC for battery gauge monitoring, and a low quiescent current, low noise LDO capable of delivering 50mA load current.

The device integrates advanced power path management and control that allow the device to provide power to the system while charging the battery even with poor adapters. The dynamic power path management automatically balances the currents delivered to the system and battery charging. A high voltage and over current protection circuit is implemented in the IC to protect it from high input voltage as high as 20V.

The GD30BC2416x device supports charge current up to 1.5A and termination current down to 5mA. The maximum charge current is set at a default of 1.5A and is programmable by connecting an external resistor from ISET pin to ground. The battery is charged using a standard Li-Ion charge profile with three phases: pre-charge, constant current and constant voltage regulation.

The device has several power saving modes to increase battery life whether the product is in storage or in operation. The quiescent current could be as low as 5uA when it is in sleep mode and thus most battery could sustain more than a year in shelf.

The versatile features of GD30BC2416x allow for it to best used in wearable applications such as headsets, earbuds and hearing aids, or low battery applications such as smart watches and fitness accessories, or patient monitors and portable medical equipment.

4 Device overview

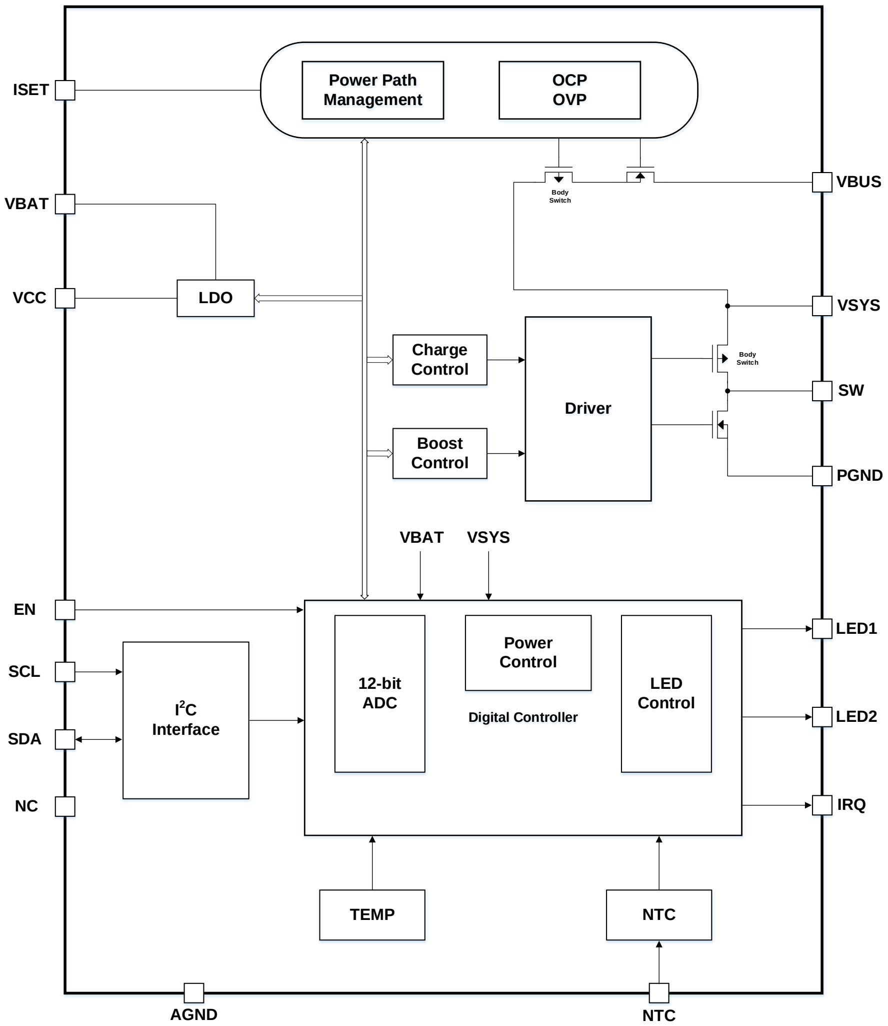
4.1 Device information

Table 4-1 Device information for GD30BC2416x

Part Order Code	Package	Description
GD30BC2416FUTR	QFN20	Cooperate with MCU solution, supports EN control

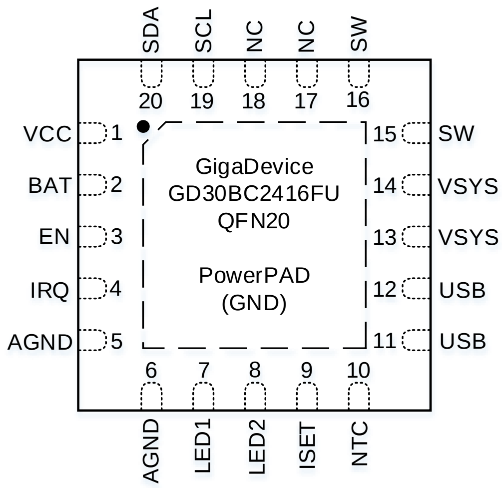
4.2 Block diagram

Figure 4-1 Block diagram for GD30BC2416x



4.3 Pinout and pin assignment

Figure 4-2 GD30BC2416x QFN20 pinouts



4.4 Pin definitions

Table 4-2. GD30BC2416x QFN20 pin definitions

Pin Name	Pins	Pin Type	Functions description
VCC	1	P	LDO output voltage, connect a capacitor to ground.
VBAT	2	P	Connect to positive node of a battery.
EN	3	I	IC enable.
IRQ	4	O	Interrupt output.
AGND	5	G	Ground.
AGND	6	G	Ground.
LED1	7	O	LED driver #1 for battery gauge monitor or other.
LED2	8	O	LED driver #2 for battery gauge monitor or other.
ISET	9	I	Set the charge current by connecting a resistor to ground.
NTC	10	I	Thermistor terminal voltage for battery, or pull high to DISABLE the IC.
VUSB	11,12	P	Power input from USB or 5-V voltage source.
VSYS	13,14	P	Output of boost converter or system voltage.
SW	15,16	P	Switching node, connecting to VBAT by an inductor.
NC	17	—	This pin is not connected to silicon.
NC	18	—	This pin is not connected to silicon.
SCL	19	I	I^2C communication to the host controller, clock.

SDA	20	I/O	I^2C communication to the host controller, data.
PGND	EPAD	G	Device power ground.

Notes:

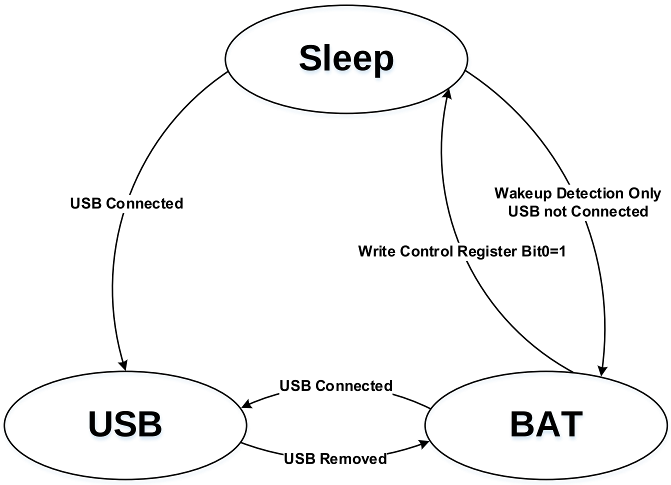
1. Type: I = input, O = output, I/O = input or output, P = power, G = Ground.

5 Functional description

5.1 Operation modes

The GD30BC2416x IC has three different operation modes: Sleep, Battery and USB operation mode, as shown in Figure 5-1.

Figure 5-1 Operation modes

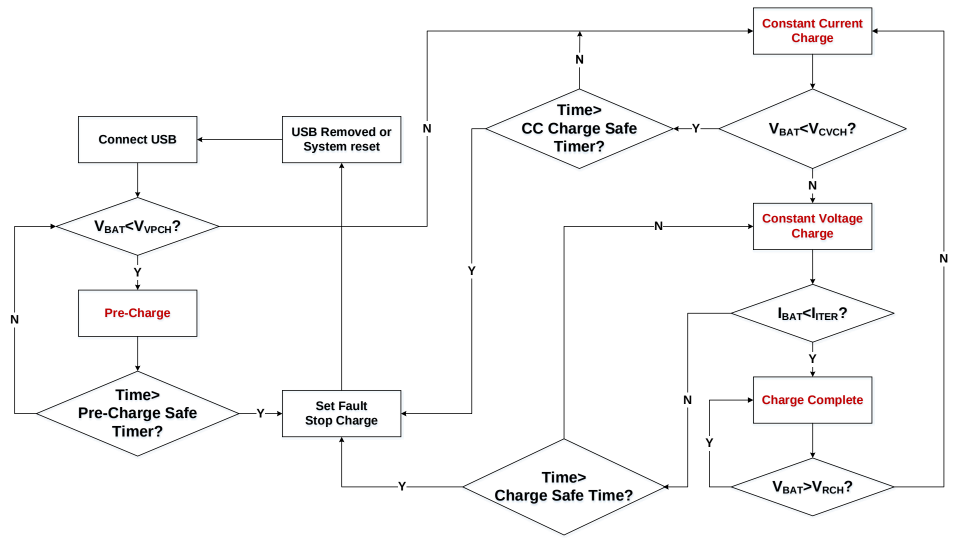


5.2 Battery charging

5.2.1 Battery charger state

The GD30BC2416x device integrates a switching charger that allows the battery to be charged with a programmable charge current up to 1.5A. In addition to the charge current, other charging parameters can be also programmed through I^2C such as the battery regulation voltage, pre-charge current. The device supports multiple battery regulation voltage regulation settings (V_{CVCH}) and charge current (I_{CCCH}) options to support multiple battery chemistries for single-cell applications**.** A full one-cell charger state diagram as shown in Figure 5-2 is implemented in the IC.

Figure 5-2 Battery charge state diagram



5.2.2 Charge parameters

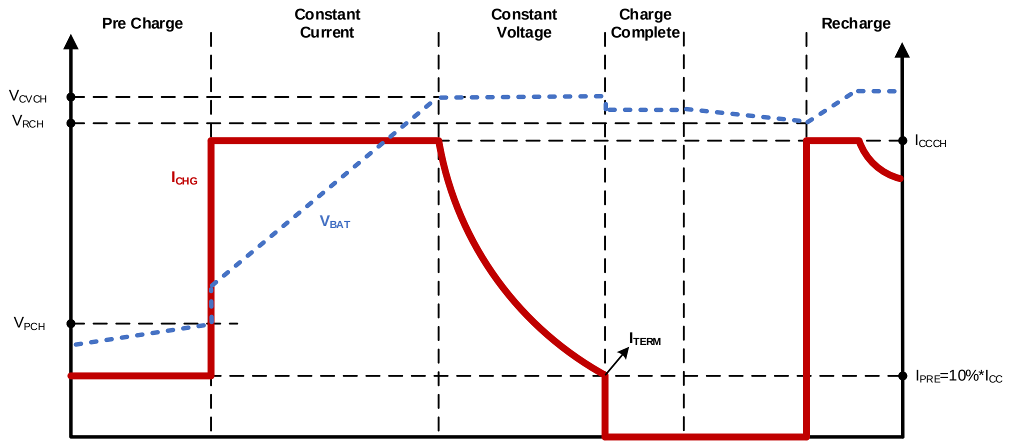
The maximum charge current is programmed by a resistor connected from the ISET pin to ground. The resistor value can be calculated as:

$$R_{CCCH} = \frac{10}{I_{CCCH}} \quad k\Omega$$

$$I_{PCH} = \frac{I_{CCCH}}{10}$$

Where the unit of I_{CCCH} is A. The charge current also varies in different charging stages constant current loop (CC), constant voltage loop (CV). During the charging process, all control loops are enabled and the one that is dominant takes control regulating the charge current as needed. The relevant charge parameters and control loops are defined as in Figure 5-3.

Figure 5-3 Battery charge cycle and charge parameters



The charger input has back to back blocking FETs to prevent reverse current flow from VBAT to VUSB. They also integrate control circuitry regulating the input current and prevents excessive currents from being drawn from the USB power supply for more reliable operation.

5.3 Synchronous boost converter

The integrated synchronous boost converter is a wide input range, high-efficiency, DC-to-DC step-up switching regulator. It is capable of delivering up to 5W of output power, integrated with a 150mΩ high side PMOS and a 150 mΩ low side NMOS. It uses a PWM current-mode control scheme. An error amplifier integrates error between the internal feedback signal proportional to VSYS and the internal reference voltage. The output of the integrator is then compared to the sum of a current-sense signal and the slope compensation ramp. This operation generates a PWM signal that modulates the duty cycle of the power MOSFETs to achieve regulation for output voltage.

Integrated VBAT to VSYS synchronous boost output function, the output voltage is 5V, which can be set to 4.8V to 5.15V by I^2C. The boost module integrates the current limiting function. When the load current is too large, the chip enters the cycle-by-cycle current limiting mode, limiting the peak inductor current to 2.0A, which can be configured to 1.6A/1.8A/2.0A/2.2A by I^2C. At the same time, the output voltage starts to drop. When the output voltage drops to 4.3V, the short-circuit protection is triggered.

The boost module also integrates an overvoltage protection function. When the output voltage is higher than 5.5V, the overvoltage protection is triggered. When the voltage of the boost module drops below 2.8V during the working process of the booster module, the boost module is automatically closed and locked in the under voltage lockout state.

The boost regulator provides excellent stability over a wide range of output current and operates in DCM at light loads for excellent efficiency. The switching frequency is fixed at 1MHz to reduce the external inductor size. The boost regulator is disabled when USB voltage is detected to save power.

5.4 Power path management

5.4.1 Power path management

The device integrates advanced power path management and control that allows the device to provide power to the system while charging the battery even with low power adapters. The dynamic power path management is able to automatically balance the currents delivered to the system and battery charging.

The charging current can be set to I_{CCCH} through the off-chip resistor connected to the ISET pin, and the chip input current is limited to I_{CCCH} +0.5A by the input current limit switch. In the charging and discharging mode, the system discharge priority. There are two situations that will cause the charging current to drop.

1) When the discharge current plus the rated charging is higher than I_{CCCH} +0.5A, the dynamic path management loop automatically reduces the charging current to meet the

discharge demand.

2) When the power supply capacity of the input adapter is lower than I_{CCCH}+0.5A, and the rated charging current plus the VSYS discharge current is greater than the power supply capacity of the adapter, the VSYS voltage will drop, as the VSYS voltage drops to 4.6V, the charging current will be reduced through the feedback loop.

The chip also integrates the charging current temperature modulation function, when the chip temperature exceeds 110 degrees Celsius, the charging current is automatically reduced.

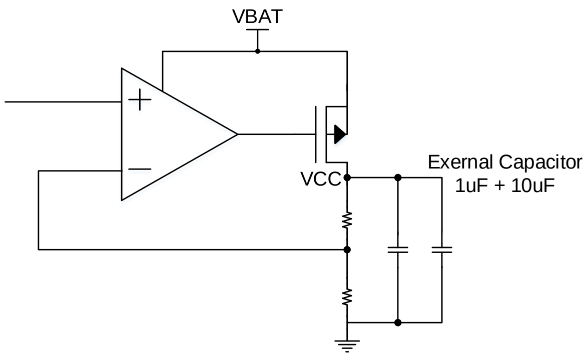
The input current limit switch also integrates short-circuit protection and over-current protection. When the current in the input switch exceeds 3A, the over-current protection is triggered. When the VSYS voltage drops below 4V, the short-circuit protection is triggered, the system stops working, and the input switch is closed. The chip enters hiccup mode and restarts every 250ms to check whether the abnormality exists. If the abnormality is removed, the chip returns to normal operation

5.4.2 LDO

A linear regulator is integrated to supply part of the chip and external circuits or MCU.

Output voltage of the LDO is 3.3V and the output driving current is 50mA. When output current exceeds 50mA, the output value will drop. When the chip works in sleep mode, LDO will enter low power mode to save power, which provides 10mA driving capability.

Figure 5-4 The principle diagram for LDO



5.5 NTC battery temperature

The GD30BC2416x chip integrates an NTC battery temperature protection circuit, which provides the over-temperature protection of high temperature 55°C and low temperature -10°C. The corresponding high and low temperature threshold voltages are respectively 30% and 60% of the input system voltage. When the battery temperature exceeds 55°C or fall below -10°C, the correlative high or low temperature output will be set high separately. If NTC pin is pulled down to GND, the NTC function is closed.

Figure 5-5 Diagram for the NTC circuit

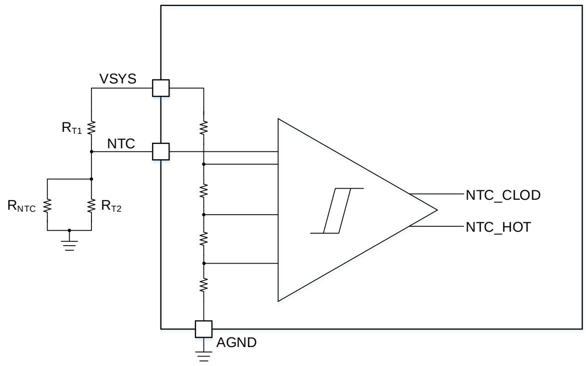


Table 5-1 Description of resistors for the NTC circuit

Symbol	Parameter	Typical value	Unit
R_{NTC}	NTC thermistor	10	KΩ
R_{T1}	Resistor for voltage division	5.23	KΩ
R_{T2}	Resistor for voltage division	9.31	KΩ

5.6 LED driver

The chip supports 1-2 LED mode (see Table 5-2 to Table 5-3). The GD30BC2416x supports LED control by I^{2}C (see Table 5-4 to Table 5-6).

5.6.1 LED connection and display mode

Figure 5-6 1-LED Mode

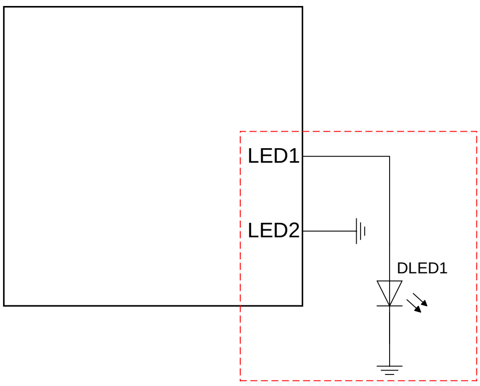


Table 5-2 1-LED Display Mode

Mode	Battery Status	DLED1
Charge	Full	Always On
	Charging	Blink at 1Hz

Figure 5-7 2-LED Mode

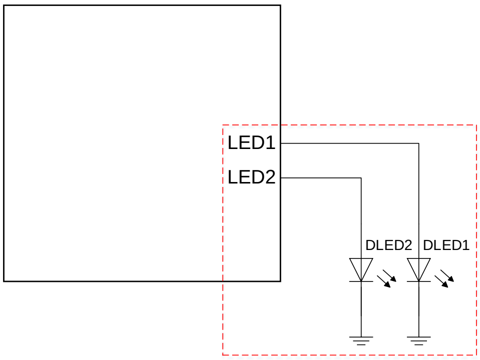


Table 5-3 2-LED Display Mode

Mode	Battery Status	DLED1	DLED2
Charge	Full	Off	Always On
	Charging	Off	Blink at 1Hz

5.6.2 LED Display Mode Configuration

Table 5-4 LED Display Mode Register

Register Address	Bits	R/W	Fields	Description
0x0d	[2:1]	RW	LED_I2C_MDST	LED mode status, default: 2'b00 00: 2 LED Mode 01: RSVD 10: 1 LED Mode 11: RSVD

5.6.3 LED Driving Capability Configuration

Table 5-5 LED Driving Register

Register Address	Bits	R/W	Fields	Description
0x04	[5:4]	RW	LED_DRV	LED current set, default: 2'b10 00: 0.5 mA 01: 1 mA 10: 2 mA 11: 4 mA

5.6.4 LED Display Control by I2C

Table 5-6 LED Control Register

Register Address	Bits	R/W	Fields	Description

Register Address	Bits	R/W	Fields	Description
0x0d	[0]	RW	LED_I2C_EN	I2C control enable, default: 1'b0 0: LED hardware control 1: LED I2C control
0x0d	[11:10]	RW	LED_I2C_ST	LED Status, default: 4'b0000 [11]: LED2 Status (0: Off, 1: On) [10]: LED1 Status (0: Off, 1: On)

5.7 EN and IRQ

The IRQ pin will generate an 8ms neg-edge pulse, when fault or work status are appeared. MCU can wake up the chip by giving a high voltage on EN pin.
IRQ sources include the following:

1) Battery charge end
2) Watch dog time out fault
3) Battery charge time out fault
4) Battery pre-charge time out fault
5) Over temperature fault (more than 150°C)
6) NTC Hot fault
7) NTC cold fault
8) VSYS under voltage fault
9) VSYS over voltage fault
10) USB plug in
11) USB pull out
12) VUSB over voltage fault
13) VBAT over voltage fault when charge the battery
14) VBAT under voltage fault when the battery discharge

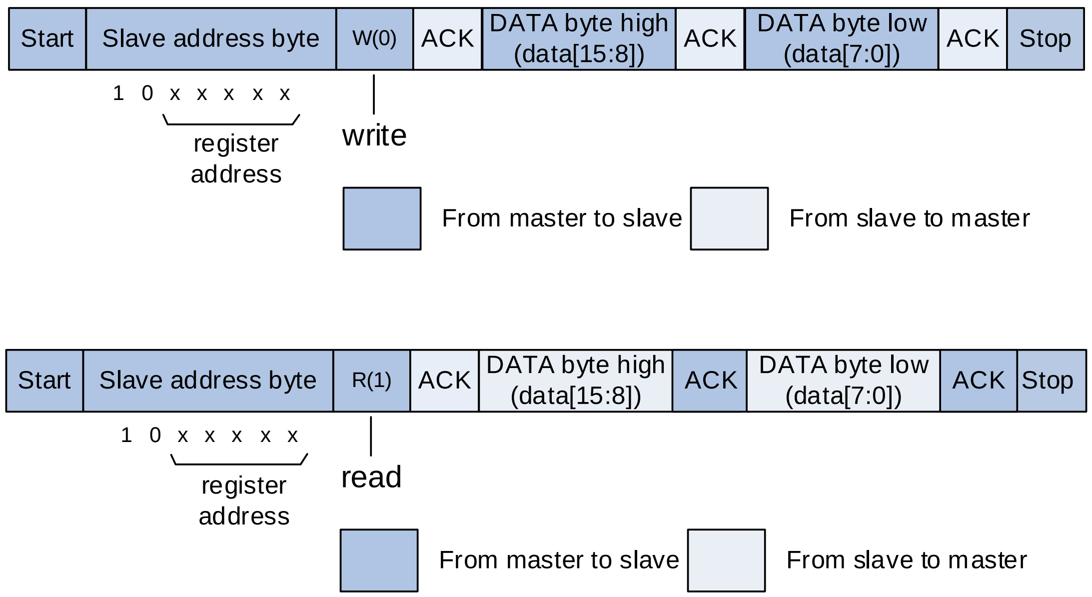
5.8 Over temperature protection

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{SD}), all the circuits are disabled, and the IRQ pin is pulled low.

5.9 I²C interface

The I²C (inter-integrated circuit) module provides an I²C interface which is an industry standard two-line serial interface for MCU to communicate with external I²C interface. I²C bus uses two serial lines: a serial data line (SDA), and a serial clock line (SCL).
The I²C interface implements standard I²C protocol with standard-mode (up to 100 kHz) and fast-mode (up to 400 kHz). The I²C interface only supports Slave-mode. The I²C interface receive data on rising SCL and transmit data on falling SCL.

Figure 5-8 I^{2}C communication flow



The data format is fixed:

8bit function (2'b10 + 5bit(register address), +1bit(1'b0-write, 1'b1-read))

+ 8bit data[15:8]

+ 8bit data[7:0].

5.10 Register Map

5.10.1 Fault Register

Address：0b 00000

Bits	R/W	fields	default	Description
15	RW	I2C_ACK_FAULT	0b0	I2C fault Software can clear it by writing 1. 0: I2C normally 1: I2C ACK fault/clear
14	R	RSVD	0b0	Must be kept at reset value.
13	R	PCH_TO_FAULT	0b0	Pre-charge timeout fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: Pre-charge normally 1: Pre-charge timeout fault
12	R	CH_TO_FAULT	0b0	Charge timeout fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: Charge normally 1: Charge timeout fault
11	R	WDG_FAULT	0b0	Watchdog timeout fault

Bits	R/W	fields	default	Description
				Software can clear it by writing Control Register bit13 WDG_CLR or writing Watchdog Register bits WDG_DATA[9:1]. 0: Watchdog normally 1: Watchdog timeout fault
10	R	VUSB_OC_FAULT	0b0	VUSB over current fault 0: VUSB current normally 1: VUSB over current fault
9	R	VUSB_OV_FAULT	0b0	VUSB over voltage fault 0: VUSB voltage normally 1: VUSB over voltage fault
8	R	RSVD	0b0	Must be kept at reset value
7	R	RSVD	0b0	Must be kept at reset value
6	R	VSYS_OV_FAULT	0b0	VSYS over voltage fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: VSYS voltage normally 1: VSYS over voltage fault
5	R	VSYS_UV_FAULT	0b0	VSYS under voltage fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: VSYS voltage normally 1: VSYS under voltage fault
4	R	NTC_HOT_FAULT	0b0	NTC_HOT fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: NTC normally 1: NTC hot fault
3	R	NTC_COLD_FAULT	0b0	NTC_COLD fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: NTC normally 1: NTC cold fault
2	R	VBAT_OV_FAULT	0b0	VBAT over voltage fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: VBAT voltage normally 1: VBAT over voltage fault
1	R	VBAT_UV_FAULT	0b0	VBAT under voltage fault Software can clear it by writing Control Register bit10 I2C_CLR_FAULT. 0: VBAT voltage normally

Bits	R/W	fields	default	Description
				1: VBAT under voltage fault
0	R	TEMP_FAULT	0b0	Over temperature fault 0: The battery temperature normally 1: The battery over temperature fault

5.10.2 Status Register 1

Address：0b 00001

Bits	R/W	fields	default	Description
15	R	PCH_ENF	0b0	Pre-charge enable flag 0: Pre-charge is disabled 1: Pre-charge is enabled
14	R	VUSB_ENF	0b0	VUSB enable flag 0: VUSB is disabled 1: VUSB is enabled
13	R	VUSBOV_ENF	0b0	VUSB over voltage detection enable flag 0: VUSB over voltage detection is disabled 1: VUSB over voltage detection is enabled
12	R	VBAT_PCH_OF	0b0	VBAT pre-charge output flag 0: VBAT is higher than pre-charge threshold voltage VPCH 1: VBAT is lower than pre-charge threshold voltage VPCH
11	R	VBAT_RCH_OF	0b0	VBAT re-charge output flag 0: VBAT is higher than re-charge threshold voltage VRCH 1: VBAT is lower than re-charge threshold voltage VRCH
10	R	RSVD	0b0	Must be kept at reset value
9	R	RSVD	0b0	Must be kept at reset value
8	R	RSVD	0b0	Must be kept at reset value.
7	R	USB_PLINF	0b0	USB plug in flag 0: USB is not plugged in 1: USB is plugged in
6	R	CH_ENDF	0b0	Charge end flag 0: Charge is not ended 1: Charge is ended
5	R	CCCH_ENDF	0b0	Constant current charge end flag 0: Constant current charge is not ended 1: Constant current charge is ended
4	R	RSVD	0b0	Must be kept at reset value
3	R	RSVD	0b0	Must be kept at reset value
2	R	RSVD	0b0	Must be kept at reset value
1	R	RSVD	0b0	Must be kept at reset value
0	R	BST_ENF	0b0	Boost enable flag

Bits	R/W	fields	default	Description
				0: Boost is disabled 1: Boost is enabled

5.10.3 Status Register 2

Address：0b 00010

Bits	R/W	fields	default	Description
15:8	R	RSVD	0b0	Must be kept at reset value.
7	R	RSVD	0b0	Must be kept at reset value
6	R	RSVD	0b0	Must be kept at reset value
5	R	RCHCMP_ENF	0b0	Re-charge comparator enable flag 0: Re-charge comparator is disabled 1: Re-charge comparator is enabled
4	R	VBAT_OV_ENF	0b0	VBAT over voltage detection enable flag 0: VBAT over voltage detection is disabled 1: VBAT over voltage detection is enabled
3:2	R	RSVD	0b0	Must be kept at reset value.
1	R	PCHCMP_ENF	0b0	Pre- charge comparator enable flag 0: Pre-charge comparator is disabled 1: Pre-charge comparator is enabled
0	R	CH_ENF	0b0	Charge enable flag 0: Charge is disabled 1: Charge is enabled

5.10.4 Control Register

Address：0b 00011

Bits	R/W	fields	default	Description
15	RW	RSVD	0b0	Must be kept at reset value.
14	RW	TEMPREG_EN	0b0	Temperature regulation enable 0: Enable temperature regulation 1: Disable temperature regulation
13	RW	WDG_CLR	0b0	Feed watchdog Software can clear it by writing 1 to this bit, or reset watchdog register bits WDG_DATA[9:1]. 0: Watchdog normally 1: Feed watchdog
12	R	RSVD	0b0	Must be kept at reset value.
11	RW	ADC_EN	0b0	ADC enable 0: Disable ADC 1: Enable ADC
10	RW	I2C_CLR_FAULT	0b0	I2C clear all faults

Bits	R/W	fields	default	Description
				0: No effect 1: Clear all faults
9	RW	RST_ALL	0b0	Reset all chip 0: No effect 1: Reset all chip
8	RW	RST_OTHS	0b0	Reset all chip but I2C itself 0: No effect 1: Reset all chip but I2C itself
7:6	RW	ADC_CLKSEL	0b0	ADC clock selection 00: ADC clock is 2MHz 01: ADC clock is 1MHz 10: ADC clock is 500kHz 11: ADC clock is 250kHz
5	R	RSVD	0b0	Must be kept at reset value.
4	RW	BST_EN	0b0	Boost enable 0: Disable boost 1: Enable boost
3	RW	CH_EN	0b0	Charge enable 0: Disable charge 1: Enable charge
2	RW	RSVD	0b0	Must be kept at reset value
1	RW	RSVD	0b0	Must be kept at reset value
0	RW	SLP_EN	0b0	Sleep mode enable 0: Disable Sleep mode 1: Enable Sleep mode

5.10.5 User configure Register 1

Address：0b 00100

Bits	R/W	fields	default	Description
15:6	R	RSVD	0b0	Must be kept at reset value.
5:4	RW	LED_DRV	0b10	LED current set 00: 0.5 mA 01: 1 mA 10: 2 mA 11: 4 mA
3:2	RW	BST_ITHSET	0b10	Boost maximum current threshold set 00: Boost maximum current threshold 1.6A 01: Boost maximum current threshold 1.8A 10: Boost maximum current threshold 2.0A 11: Boost maximum current threshold 2.2A
1:0	RW	RSVD	0b10	Must be kept at reset value

5.10.6 User configure Register 2

Address：0b 00101

Bits	R/W	fields	default	Description
15:13	R	RSVD	0b0	Must be kept at reset value.
12:10	RW	VSYS_SET	0b100	VSYS voltage set 000: Boost output voltage 4.8V 001: Boost output voltage 4.85V 010: Boost output voltage 4.9V 011: Boost output voltage 4.95V 100: Boost output voltage 5V 101: Boost output voltage 5.05V 110: Boost output voltage 5.1V 111: Boost output voltage 5.15V
9:8	RW	VUSB_CL_SET	0b01	VUSB current limit set 00: VUSB current limit is set to 95% 01: VUSB current limit is set to 100% 10: VUSB current limit is set to 105% 11: VUSB current limit is set to 110%
7:6	RW	IPCH_SET	0b01	Pre-charge current set 00: Pre-charge current is set to 50% 01: Pre-charge current is set to 100% 10: Pre-charge current is set to 150% 11: Pre-charge current is set to 150%
5:4	RW	VPCHT_SET	0b01	Pre-charge terminate voltage set 00: Pre-charge terminate voltage is 3.0V 01: Pre-charge terminate voltage is 3.1V 10: Pre-charge terminate voltage is 3.2V 11: Pre-charge terminate voltage is 3.3V
3:2	RW	ICCCH_SET	0b0	Constant current charge current set 00: Constant current charge current is set to 100% 01: Constant current charge current is set to 75% 10: Constant current charge current is set to 50% 11: Constant current charge current is set to 25%
1:0	RW	VRCHT_SET	0b01	Re-charge threshold voltage set 00: Re-charge threshold voltage is 3.9V 01: Re-charge threshold voltage is 4.0V 10: Re-charge threshold voltage is 4.1V 11: Re-charge threshold voltage is 4.2V

5.10.7 User configure Register 3

Address：0b 00110

Bits	R/W	fields	default	Description
15:7	R	RSVD	0b0	Must be kept at reset value.
6:5	RW	RSVD	0b01	Must be kept at reset value
4:2	RW	VCCCHT_SET	0b0	Constant current charge terminate voltage set 000: Constant current charge terminate voltage is 4.2V 001: Constant current charge terminate voltage is 4.1V 010: Constant current charge terminate voltage is 4.3V 011: Constant current charge terminate voltage is 4.35V 100: Constant current charge terminate voltage is 4.4V 101: Constant current charge terminate voltage is 4.2V 110: Constant current charge terminate voltage is 4.2V 111: Constant current charge terminate voltage is 4.2V
1:0	RW	ICHT_SET	0b10	Charge terminate current set 00: Charge terminate current minus 10mA 01: Charge terminate current minus 5mA 10: Charge terminate current no change 11: Charge terminate current plus 5mA

5.10.8 Watchdog Register

Address：0b 01011

Bits	R/W	Fields	default	Description
15:10	R	Reserved	0b0	Must be kept at reset value.
9:1	RW	WDG_DATA	0x1ff	Watchdog counter set Only set watchdog counter when WDG_EN is 0
0	RW	WDG_EN	0b0	Watchdog enable 0: Disable watchdog 1: Enable watchdog

5.10.9 LED Register

Address：0b 01101

Bits	R/W	fields	default	Description
15:14	R	Reserved	0b0	Must be kept at reset value.
13	RW	RSVD	0b0	Must be kept at reset value
12	RW	RSVD	0b0	Must be kept at reset value
11	RW	LED2_I2C_ST	0b0	LED2 Status 0: Off 1: On
10	RW	LED1_I2C_ST	0b0	LED1 Status 0: Off 1: On
9:3	R	RSVD	0b0	Must be kept at reset value.

Bits	R/W	fields	default	Description
2:1	RW	RSVD	0b0	LED mode status 00: 2 LED mode 10: 1 LED mode
0	RW	LED_I2C_EN	0b0	LED I2C control enable 0: LED Hardware control 1: LED I2C control

5.10.10 ADC Register

Address：0b 01110

Bits	R/W	fields	default	Description
15:4	R	ADC_DATA	0b0	ADC measure 12 bit data.
3:1	RW	ADC_CHSEL	0b0	ADC channel select 000: Channel VBAT 001: Channel VRCH 101: Channel VIC 110: Channel VIR 111: Channel AVSS
0	R	RSVD	0b0	Must be kept at reset value.

5.10.11 DEBUG Register

Address：0b 01111

Bits	R/W	fields	default	Description
15	RW	RSVD	0b1	Must be kept at reset value
14:12	R	RSVD	0b0	Must be kept at reset value.
11:10	R/W	CH_TO_SEL	0b0	Charge status timeout time select 00: 120 minute 01: 180 minute 10: 240 minute 11: 60 minute
9	R/W	VBAT_FULL	0b0	Battery is charged fully, set by software. It will affect the LED display 0: Battery is not charged fully. LED displays normally according to battery power 1: Battery is charged fully. LED displays according to battery full charge
8:0	R	RSVD	0b0	Must be kept at reset value.

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{USB}	Power supply pin from USB other 5V input	-0.3	7	V
	Power supply pin from USB other 5V input, pulsed less than 20us	-0.3	20	V
V_{BAT}	Battery voltage	-0.3	7	V
V_{SYS}	Output Voltage	-0.3	7	V
V_{CC}	LDO output voltage and Internal logic voltage	-0.3	7	V
V_{IO}	I/O pin voltage (LEDx, ISET, EN, NTC, SCL, SDA)	-0.3	7	V
V_{SW}	Switching node voltage (SW)	-0.3	7	V
Thermal characteristics				
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

6.2 Recommended operation conditions

Table 6-2 Recommended operation conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{USB}	Power supply pin from USB other 5V input	4.4	5.0	5.5	V
V_{BAT}	Battery voltage	2.2	4.0	4.4	V
V_{SYS}	BOOST output Voltage	4.8	5.0	5.15	V
V_{CC}	LDO output voltage and Internal logic voltage	2.0	3.3	3.6	V
Thermal characteristics					
T_A	Operating ambient temperature	–20	—	85	°C

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample.

Table 6-3 Electrostatic Discharge characteristics

Symbol	Parameter	Conditions	Value	Unit

$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C; JS-001-2017	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C; JS-002-2018	±1000	V

6.4 Power supplies voltages and currents

Table 6-4 Power supplies voltages and currents

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	Sleep mode quiescent current	V_{BAT} = 5 V, T_A = 25 °C	—	—	5.0	µA
		V_{BAT} = 5 V, T_A = 85 °C	—	—	TBD	µA
t_{ON}	Turn-on time	V_{USB} > V_{UVLO} to outputs ready	5.0	—	—	ms
V_{CC}	VCC regulator voltage	I_{VCC} = 0 to 50 mA (V_{BAT} > 3.4 V)	3.1	3.3	3.5	V

6.5 Logic input characteristics

Table 6-5 Logic input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input logic low voltage	—	0	—	0.35 * V_{CC}	V
V_{IH}	Input logic high voltage	—	0.65 * V_{CC}	—	5.5	V
V_{HYS}	Input logic hysteresis	—	100	—	—	mV

6.6 Open drain outputs characteristics

Open drain output pins include **SCL, SDA, IRQ.**

Table 6-6 Open drain output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output logic low voltage	I_O = 5 mA	—	—	0.1	V
I_{OZ}	Output high impedance leakage	V_O = V_{BAT}	–2	—	2	µA

6.7 NTC characteristics

Table 6-7 NTC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TL}	Low Temperature threshold voltage	—	—	0.6 * V_{SYS}	—	V
V_{TH}	High Temperature threshold voltage	—	—	0.3 * V_{SYS}	—	V
V_{offset}	Offset Volatage	—	—	—	5	mV

6.8 Switching charger characteristics

Table 6-8 Charger characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CVCH}	CV Charge voltage	Programmable	4.1	4.2	4.4	V
	CV Charge voltage precision	—	—	0.5	—	%
I_{CCCH}	CC Charge current	R_{CCCH} = 20 KΩ	—	0.5	—	A
I_{PCH}	Pre-Charge current	R_{CCCH} = 20 KΩ	40	50	60	mA
I_{TER}	Charge terminate current	—	I_{PCH} + 10			mA
V_{PCH}	Pre-Charge to CC charge transition	Programmable	—	3.0	—	V
V_{PCHHYS}	Pre-Charge hysteresis voltage	—	—	200	—	mV
V_{RCH}	Re-Charge threshold	—	—	4	—	V
V_{RCHHYS}	Re-Charge hysteresis voltage	—	—	200	—	mV

Figure 6-1. Constant current charging efficiency

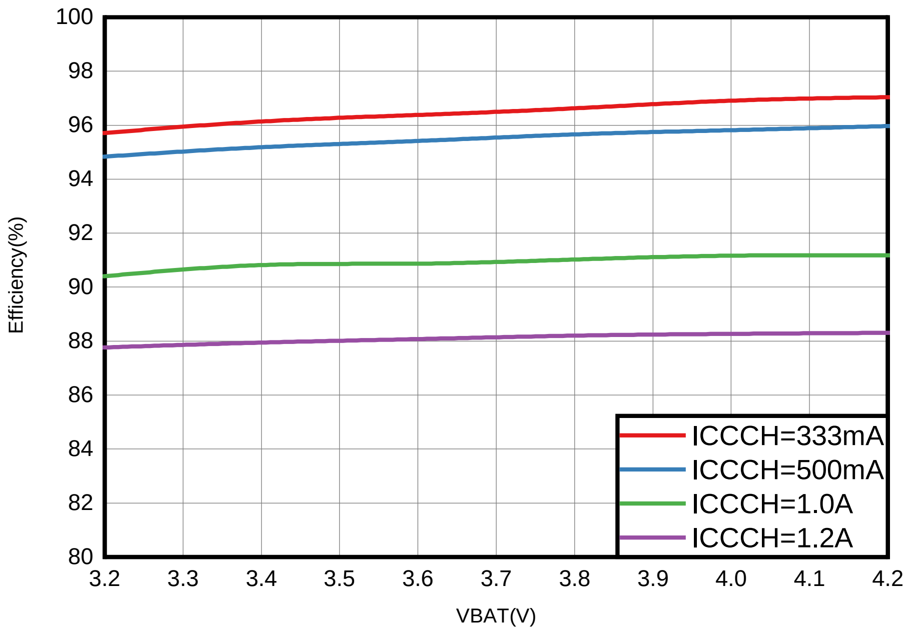
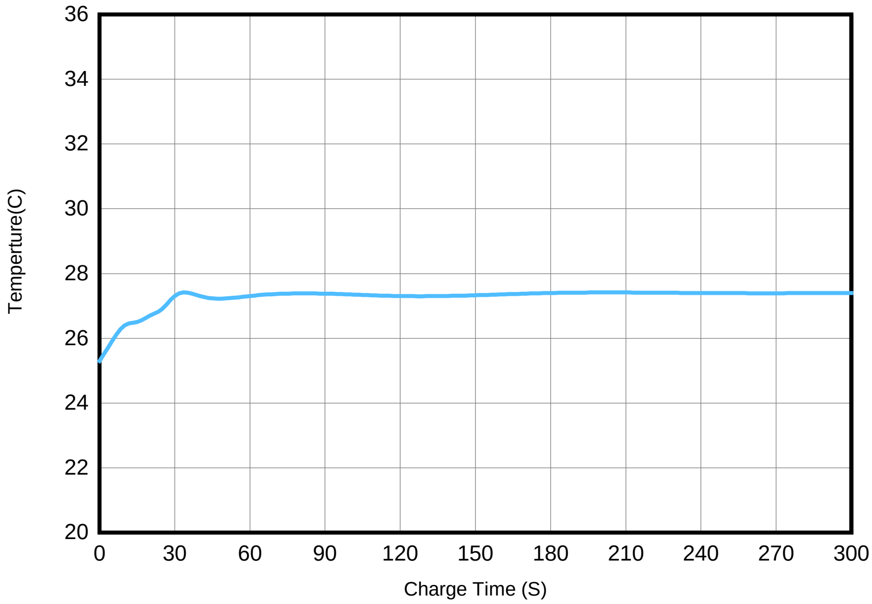


Figure 6-2. Constant current charging chip case temperature

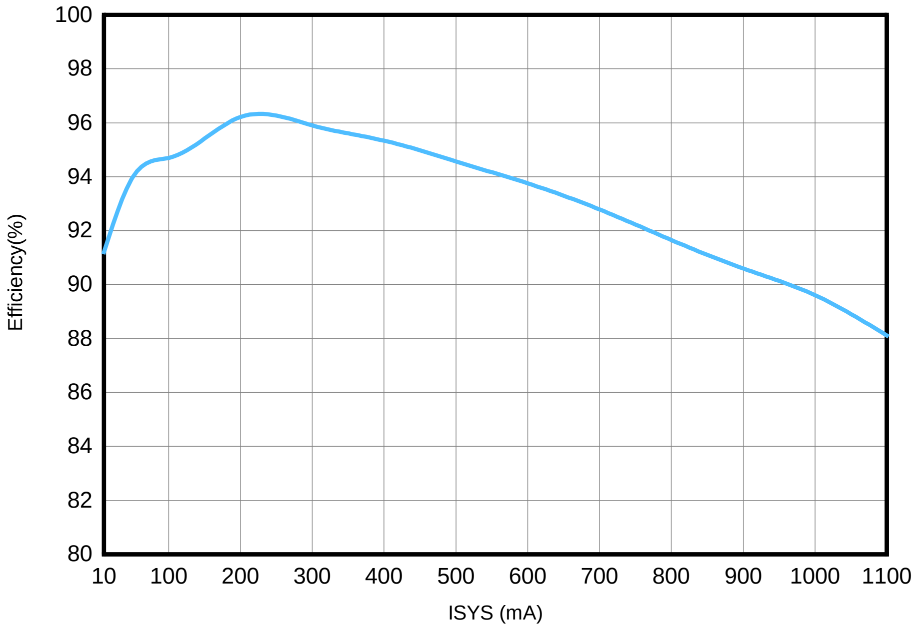


6.9 Boost converter characteristics

Table 6-9 Boost converter characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Operation battery voltage	—	3.0	3.7	4.5	V
V_{BATLOW}	Minimum battery	I_{SYS} = 1.0 A	2.9	—	—	V
I_{BAT}	Boost operation current	V_{BAT} = 3.7 V	—	4.0	6.0	mA
V_{SYS}	Output voltage	I_{SYS} = 0 mA	4.90	5.05	5.15	V
		I_{SYS} = 1.0 A	4.80	5.00	5.15	V
ΔV_{SYS}	Output ripple	—	—	100	—	mV
I_{SYS}	Output current	—	—	—	1.0	A
R_{HS}	High Side PMOS on resistance	V_{CC} = 3.3 V, T_A = 25 °C	—	150	—	mΩ
R_{LS}	Low Side NMOS on resistance	V_{CC} = 3.3 V, T_A = 25 °C	—	150	—	mΩ
I_{LIM}	Peak current limit	V_{BAT} = 3.7 V, T_A = 25 °C	—	2.0	—	A
	Peak current limit during startup	V_{BAT} = 3.7 V, T_A = 25 °C	—	0.6	—	A
f_{SW}	Switching frequency	—	0.9	1.0	1.1	MHz
I_{SW}	Switching node leakage	—	—	—	1.0	uA
D_{max}	Maximum Duty Cycle	—	90	—	—	%

Figure 6-3. Boost conversion efficiency



6.10 ADC characteristics

Table 6-10 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	Operation battery voltage	—	3.0	3.7	4.5	V
f_{ADC}	ADC clock frequency	—	—	2.0	—	MHz
f_S	Sampling rate	—	—	0.08	—	MSPS
V_{REFP}	Positive Reference Voltage	—	2.49	2.5	2.51	V
V_{REFN}	Negative Reference Voltage	—	—	0	—	V
t_S	Sampling time	f_{ADC} = 2 MHz	—	6	—	us
			—	12	—	1/ f_{ADC}
t_{CONV}	Total conversion time(including sampling time)	—	—	25	—	1/ f_{ADC}
t_{STAB}	Power-up time	—	—	—	1	us
ENOB	Effective number of bits	f_{ADC} = 2 MHz Input Frequency = 2 kHz Temperature = 25 °C	—	10.3	—	bits
SNDR	Signal-to-noise and distortion ratio		—	63.8	—	dB
SNR	Signal-to-noise ratio		—	64.5	—	
THD	Total harmonic distortion		—	-71.0	—	
Offset	Offset error	f_{ADC} = 2 MHz	±1	—	—	LSB
DNL	Differential linearity error		±1.5	—	—	

6.11 Timing characteristics

Table 6-11 Timing characteristics

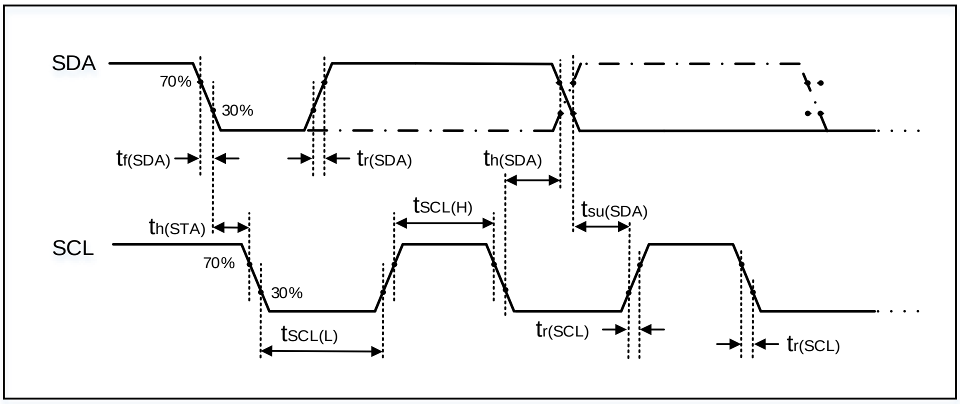
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PCH_FAULT}	Pre-charge fault time	—	—	30	—	min
t_{CH_TO}	Charge Time Out	—	—	180	—	min

6.12 I²C characteristics

Table 6-12 I²C characteristics

Symbol	Parameter	Conditions	Standard mode		Fast mode		Unit
			Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time	—	4.0	—	0.6	—	μs
$t_{SCL(L)}$	SCL clock low time	—	4.7	—	1.3	—	μs
$t_{su(SDA)}$	SDA setup time	—	250	—	100	—	ns
$t_{h(SDA)}$	SDA data hold time	—	0	3450	0	900	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time	—	—	1000	—	300	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time	—	—	300	3	300	ns
$t_{h(STA)}$	Start condition hold time	—	4.0	—	0.6	—	μs

Figure 6-4. I²C bus timing diagram



6.13 Protection features

Protection features include over current protection, under voltage, over voltage and thermal shutdown.

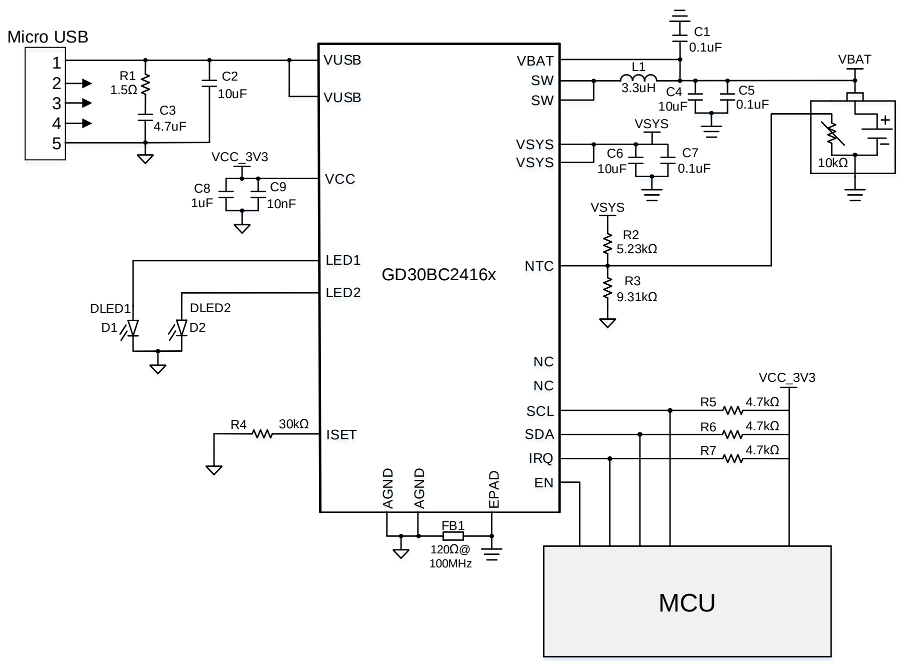
Table 6-13 Protection features characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{USB} Switch						
V_{USB_UVP}	V_{USB} under voltage Protection Threshold	V_{USB} falling	—	4.3	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{USB_OVP}	V_{USB} over voltage Protection Threshold	V_{USB} rising	—	5.6	—	V
I_{USB_Limit}	V_{USB} input current limit	—	—	0.5 + I_{CCCH}	—	A
V_{SYS_short}	V_{SYS} short voltage Protection Threshold	V_{SYS} falling	—	4.0	—	V
Charge						
V_{BAT_OVP}	V_{BAT} over voltage Protection Threshold	VCCCHT_SET = 000	—	4.3	—	V
		VCCCHT_SET = 001	—	4.2	—	
		VCCCHT_SET = 010	—	4.4	—	
		VCCCHT_SET = 011	—	4.45	—	
		VCCCHT_SET = 100	—	4.5	—	
		VCCCHT_SET = 101	—	4.3	—	
		VCCCHT_SET = 110	—	4.3	—	
		VCCCHT_SET = 111	—	4.3	—	
V_{SYS_DPM}	V_{SYS} voltage regulation limit	—	—	4.6	—	V
Boost						
V_{BAT_UVP}	V_{BAT} under voltage Protection Threshold	V_{BAT} Falling	—	2.8	—	V
V_{BATUVP_HSY}	V_{BAT} under voltage Protection hysteresis	—	—	0.1	—	V
V_{SYS_short}	V_{SYS} short Protection Threshold	—	—	4.3	—	V
V_{SYS_UVP}	V_{SYS} over voltage Protection Threshold	—	—	5.5	—	V
Temperature						
T_{OT}	Thermal shutdown temperature	Die temperature, T_J	—	150	—	°C
T_{HYS}	Thermal hysteresis	Die temperature, T_J	—	20	—	°C

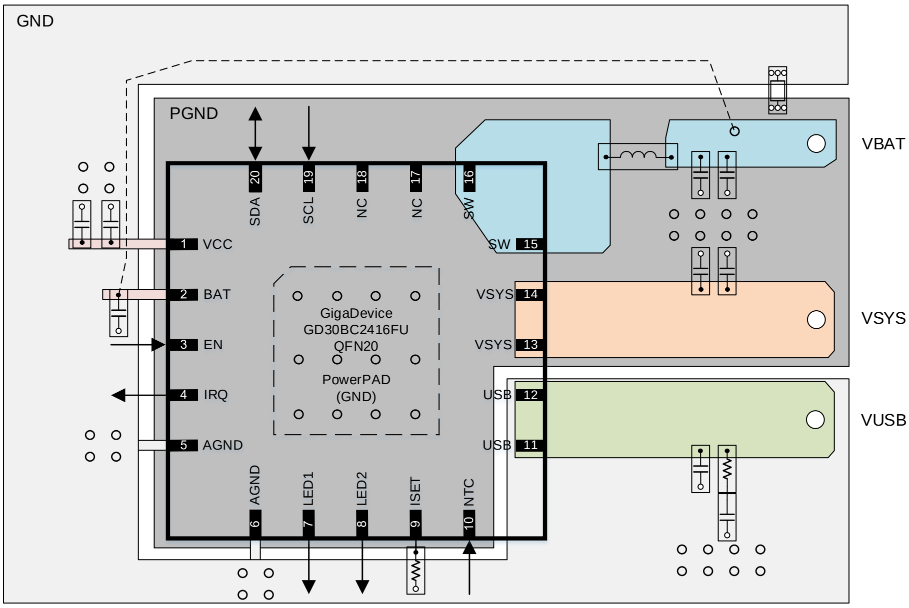
7 Typical application circuit

Figure 7-1 Typical GD30BC2416x application circuit



8 Layout guideline

Figure 8-1 Typical GD30BC2416x layout guideline



Notes:

1. The VBAT bypass capacitor should be connected to AGND to ensure the stability of the analog loop. The VBAT bypass capacitors should be connected to PGND to ensure the stability of the power loop.
2. The SW inductor should be as close to the pin as possible to reduce parasitic parameters.
3. The VSYS and bypass capacitor should be as close to the pin as possible to ensure the stability of the output power supply.

9 Package information

9.1 QFN20 package information

Figure 9-1 QFN20 package outline

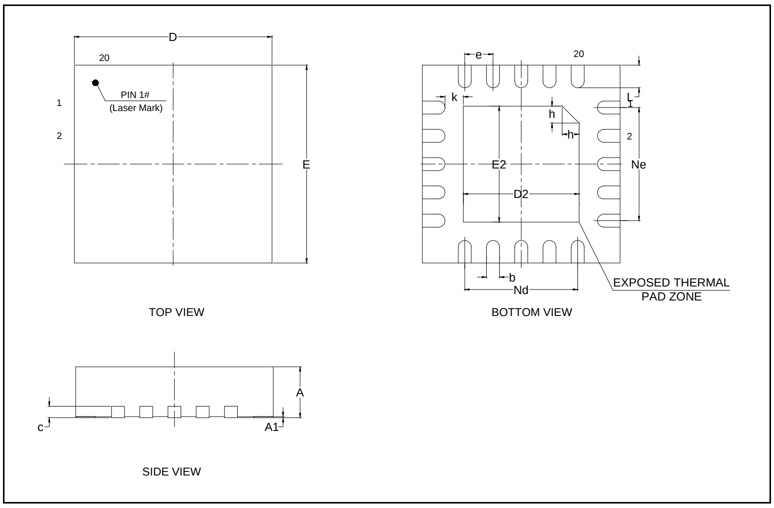
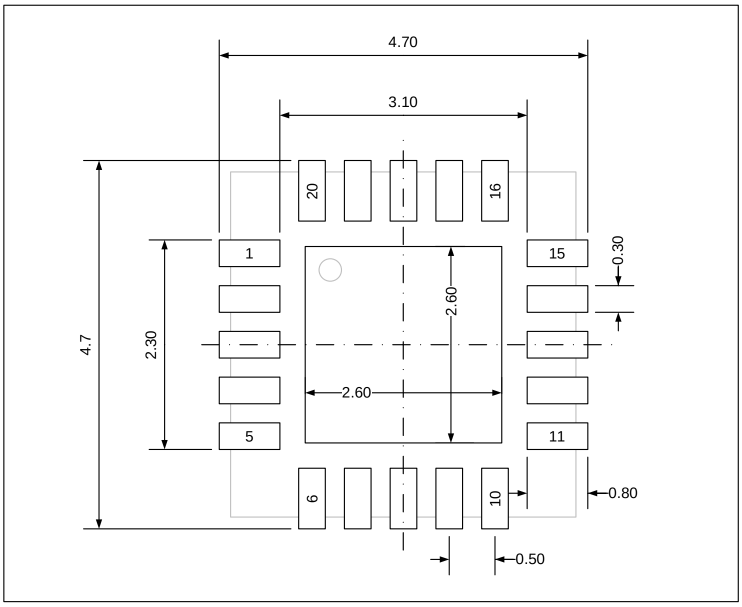


Table 9-1. QFN20 dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.55	2.65	2.75
E	3.90	4.00	4.10
E2	2.55	2.65	2.75
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Nd	—	2.00	—
Ne	—	2.00	—

(Original dimensions are in millimeters)

Figure 9-2 QFN20 recommended footprint



(All dimensions are in millimeters)

9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J – T_B)/P_D$

$\Theta_{JC} = (T_J – T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-2. Package thermal characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	QFN20	47.51	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	QFN20	14.9	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	QFN20	20.99	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	QFN20	15.05	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	QFN20	0.86	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

10 Ordering information

Table 10-1 Part ordering code for GD30BC2416x devices

Ordering Code	Package	Package Type	Temperature Operating Range
GD30BC2416FUTR	QFN20	Green	Industrial -20°C to +85°C

11 Revision history

Table 11-1 Revision history

Revision No.	Description	Date
1.0	Initial Release	May. 18, 2022

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