

**GigaDevice Semiconductor Inc.**

**GD30DR8306x**  
**3-Phase Motor Driver with Buck controller**

Datasheet

# Table of Contents

<b>Table of Contents</b> .....	<b>2</b>
<b>List of Figures</b> .....	<b>4</b>
<b>List of Tables</b> .....	<b>5</b>
<b>1. Features</b> .....	<b>6</b>
<b>2. Applications</b> .....	<b>6</b>
<b>3. General description</b> .....	<b>6</b>
<b>4. Device overview</b> .....	<b>8</b>
<b>4.1. Block diagram</b> .....	<b>8</b>
<b>4.2. Pinout and pin assignment</b> .....	<b>9</b>
<b>4.3. Pin definitions</b> .....	<b>9</b>
<b>5. Functional description</b> .....	<b>12</b>
<b>5.1. Power module</b> .....	<b>12</b>
5.1.1. Charge pump and VGLS_LDO .....	12
5.1.2. VDD_LDO .....	13
<b>5.2. Gate driver architecture</b> .....	<b>13</b>
<b>5.3. Gate driver control mode</b> .....	<b>14</b>
5.3.1. 6xPWM Mode .....	14
5.3.2. 3xPWM Mode .....	15
<b>5.4. Gate driver slew rate control</b> .....	<b>16</b>
<b>5.5. Dead time</b> .....	<b>16</b>
<b>5.6. Device configuration</b> .....	<b>16</b>
5.6.1. Hardware interface.....	17
<b>5.7. Over temperature protection</b> .....	<b>17</b>
<b>5.8. Buck Controller</b> .....	<b>17</b>
<b>6. Electrical characteristics</b> .....	<b>19</b>
<b>6.1. Absolute maximum ratings</b> .....	<b>19</b>
<b>6.2. Recommended operation conditions</b> .....	<b>20</b>
<b>6.3. Power supplies and current consumption</b> .....	<b>20</b>
<b>6.4. Logic inputs characteristics</b> .....	<b>21</b>
<b>6.5. Open drain outputs characteristics</b> .....	<b>21</b>



---

6.6.	Gate driver characteristics .....	21
6.7.	VDD LDO characteristics .....	22
6.8.	Buck controller characteristics .....	22
6.9.	Protection features.....	23
6.10.	Parameter conditions .....	23
7.	Typical application circuit.....	24
8.	Layout guideline .....	25
9.	Package information .....	26
9.1.	QFN32 package outline dimensions .....	26
9.2.	Thermal characteristics .....	28
10.	Ordering information .....	29
11.	Revision history .....	30

# List of Figures

Figure 4-1. Block diagram for GD30DR8306x .....	8
Figure 4-2. GD30DR8306x QFN32 pinouts .....	9
Figure 5-1. Charge pump and VGLS_LDO .....	12
Figure 5-2. VDD_LDO.....	13
Figure 5-3. Gate driver architecture.....	14
Figure 5-4. 6xPWM mode .....	15
Figure 5-5. 3xPWM mode .....	15
Figure 5-6. Dead time insertion .....	16
Figure 5-7. Buck controller application circuit .....	18
Figure 6-1. Buck controller efficiency diagram .....	23
Figure 7-1. Typical application circuit.....	24
Figure 8-1. Typical layout guideline.....	25
Figure 9-1. QFN32 package outline.....	26
Figure 9-2. QFN32 recommended footprint .....	27

## List of Tables

Table 4-1. GD30DR8306x pin configuration .....	9
Table 5-1. 6xPWM mode truth table .....	14
Table 5-2. 3xPWM mode truth table .....	15
Table 5-3. PWM mode configuration table .....	17
Table 5-4. Gate drive current configuration table.....	17
Table 6-1. Absolute maximum ratings .....	19
Table 6-2. Recommended operation conditions.....	20
Table 6-3. Power supplies and currents .....	20
Table 6-4. Logic input characteristics.....	21
Table 6-5. Open drain output characteristics.....	21
Table 6-6. Gate driver characteristics .....	21
Table 6-7. VDD LDO characteristics.....	22
Table 6-8. Buck controller characteristics .....	22
Table 6-9. Protection features characteristics .....	23
Table 9-1. QFN32 dimensions .....	26
Table 9-2. Package thermal characteristics <sup>(1)</sup> .....	28
Table 10-1. Part ordering code for GD30DR8306x device .....	29
Table 11-1. Revision history .....	30

## 1. Features

- 4.5-30V Supply Voltage
- Programmable gate drive current, peak 1A source and 1.2A sink current
- Smart high-side and low-side Slew-Rate Control
- PWM input control up to 200kHz
- 2 PWM modes (6x and 3x)
- Inside 5V/2A DC-DC buck controller
- 3.3V and 5V digital interface
- Integrated 5V LDO
- Thermally-Enhanced: QFN32 (5x5)
- Protection Features:
  - Dead time insertion
  - MOSFET Shoot-Through protection
  - Over temperature protection
  - Fault diagnostics
  - VP and VDD Under Voltage Lock-Out(UVLO)

## 2. Applications

- 3-Phase BLDC and PMSM Motors
- Power Tools
- Robotics and RC Toys
- Industrial Automation

## 3. General description

The versatile programmable features listed below allow GD30DR8306x to be used in a broad range of applications, such as 3-phase BLDC motors, electronic bikes, power tools, and etc.

The GD30DR8306x is a three-phase gate driver IC integrated with an optional DC/DC buck controller. The IC includes three half-bridge drivers, each is capable of driving two NMOSFETs and supports up to 1.2A source and 1A sink current capability. The drive currents will be adapted automatically to the optimized current according to different power MOSFET used in the application. A proprietary slew rate control is implemented to reduce the EMI of gate drive. The GD30DR8306x can operate with a single power supply ranging from 4.5V to 30V. A regulated charge pump supporting 100% duty cycle is integrated in the device to supply the gate drive current and the internal LDOs.

The device inserts fixed dead-time and uses automatic handshaking to prevent the high-side and low-side MOSFET from shoot-through when switching.

The optional integrated DC/DC buck controller operates with power supply of 4.5V to 30V and the output voltage is 5V. The driver can drive an external NMOSFET up to 2A.

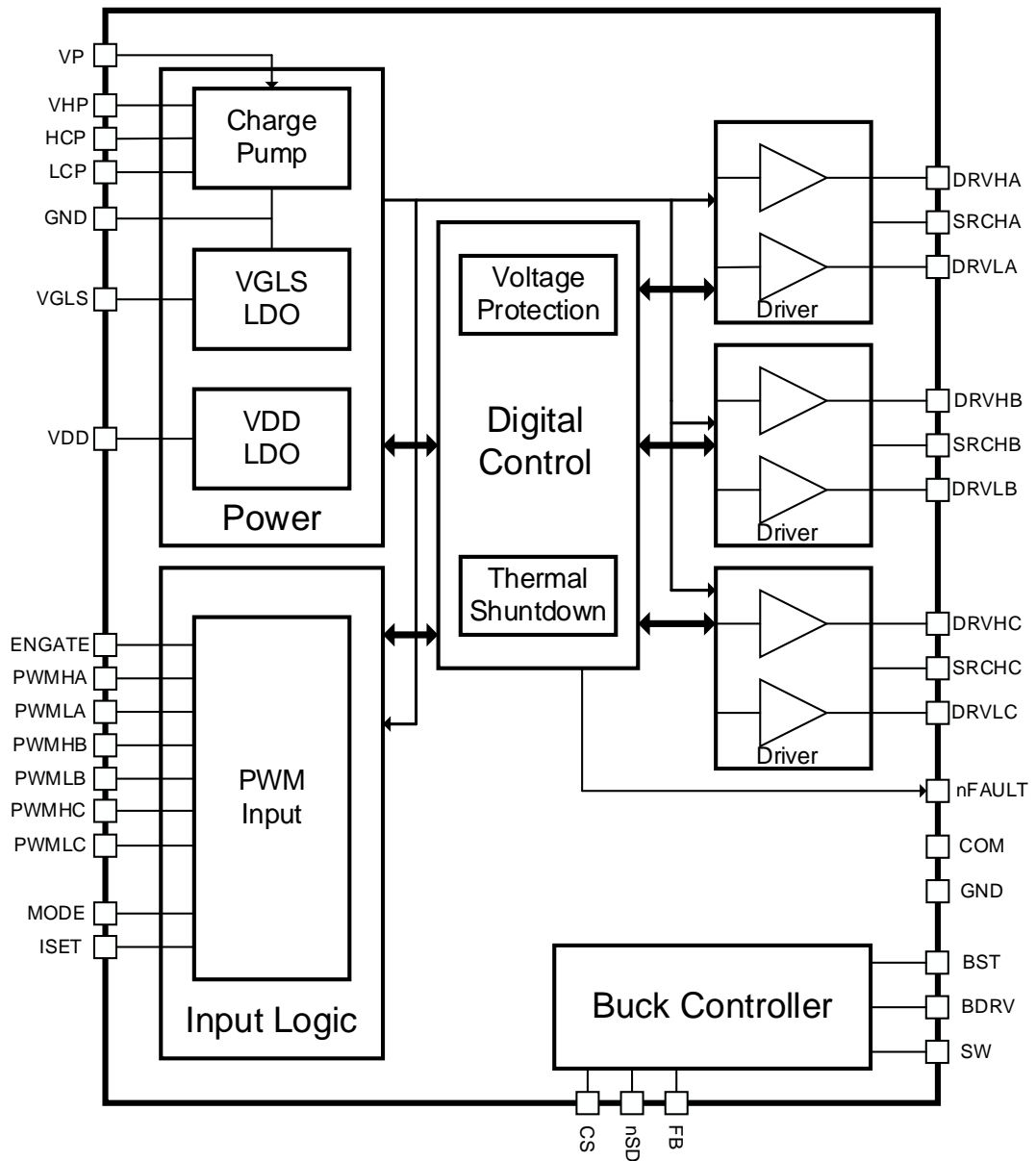
The versatile programmable features of the IC allow for it to be used in a broad range of applications, such as 3-phase BLDC motors, electronic bikes, power tools, and etc.

The GD30DR8306x is available in thermal enhanced package QFN32 with buck controller.

## 4. Device overview

### 4.1. Block diagram

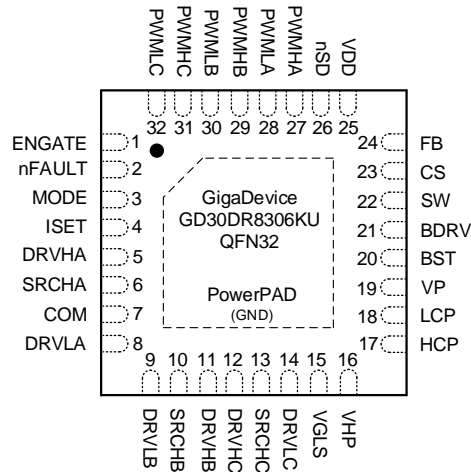
Figure 4-1. Block diagram for GD30DR8306x





## 4.2. Pinout and pin assignment

Figure 4-2. GD30DR8306x QFN32 pinouts



## 4.3. Pin definitions

The table below shows the pin definition of GD30DR8306x.

Table 4-1. GD30DR8306x pin configuration

Pin Name	Pins	Pin Type	Functions Description	
ENGATE	1	I	Enable gate driver	Enables the gate driver, internal pull-down.
nFAULT	2	OD	Fault indicator	The low level indicates a fault had occurred, external pull-up to MCU power supply is needed (1kΩ to 10kΩ).
MODE	3	I	PWM mode selection	PWM mode setting, set by an external resistor.
ISET	4	I	Driver current set	Gate driver output current setting, set by an external resistor.
DRVHA	5	O	Gate driver	Gate driver output for bridge A high-side.
SRCHA	6	I	Source connection	Source connection for bridge A high-side.
COM	7	I/O	Common for 3-driver	Common source connection for 3 lower side drivers, suggested to connect to power ground.

Pin Name	Pins	Pin Type	Functions Description	
DRVLA	8	O	Gate driver	Gate driver output for bridge A low-side.
DRVLB	9	O	Gate driver	Gate driver output for bridge B low-side.
SRCHB	10	I	Source connection	Source connection for bridge B high-side.
DRVHB	11	O	Gate driver	Gate driver output for bridge B high-side.
DRVHC	12	O	Gate driver	Gate driver output for bridge C high-side.
SRCHC	13	I	Source connection	Source connection for bridge C high-side.
DRVLC	14	O	Gate driver	Gate driver output for bridge C low-side.
VGLS	15	P	Low-side gate driver power supply	Internal voltage regulator for low-side gate driver, connecting 1 $\mu$ F and 10nF capacitor to GND.
VHP	16	P	High-side gate driver power supply	Internal charge pump for high-side gate driver, connecting 1 $\mu$ F capacitor to VP.
HCP	17	P	Charge pump flying capacitor	Flying capacitor for charge pump, connecting 47nF capacitor between HCP and LCP.
LCP	18			
VP	19	P	Power supply voltage	High-side MOSFET drain connection; common for all three half bridges, connecting 4.7 $\mu$ F capacitor to GND.
BST	20	P	Input for bootstrap capacitor	An external capacitor is required between the BST and the SW pins to provide bias to the MOSFET gate driver.
BDRV	21	O	Gate drive	Buck circuit, connecting to the gate terminal of the external MOSFET switch.
SW	22	P	Switching node	Buck circuit, connecting to the source terminal of the external MOSFET switch.
CS	23	I	Current sense	Buck circuit, current sense voltage input.
FB	24	I	Regulated output	Buck circuit, connecting directly to the regulated output voltage.
VDD	25	P	Voltage Regulator	5V internal supply regulator, connecting 6.3V, 1 $\mu$ F ceramic capacitor to GND.
nSD	26	I	Buck controller enable	Internal pull-down, pull above 2.2V to enable.
PWMHA	27	I	PWM input	Logic input signal for bridge A high-side.
PWMLA	28	I	PWM input	Logic input signal for bridge A low-side.
PWMHB	29	I	PWM input	Logic input signal for bridge B high-side.

Pin Name	Pins	Pin Type	Functions Description	
PWMLB	30	I	PWM input	Logic input signal for bridge B low-side.
PWMHC	31	I	PWM input	Logic input signal for bridge C high-side.
PWMLC	32	I	PWM input	Logic input signal for low-side bridge C.
GND	Thermal	P	Device ground	Must be connected to ground.

**Notes:**

Type: I = input, O = output, P = power, OD = open drain.

## 5. Functional description

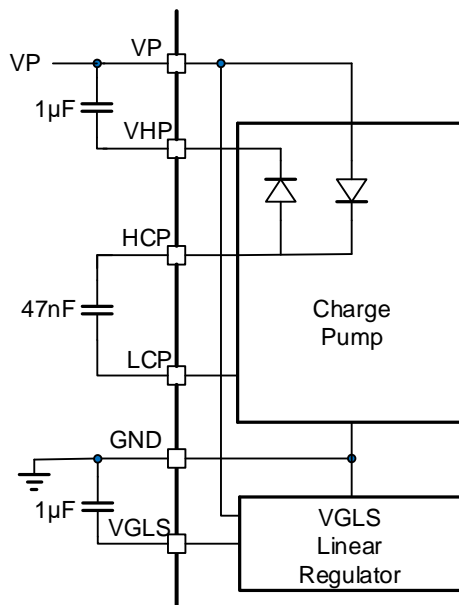
### 5.1. Power module

#### 5.1.1. Charge pump and VGLS\_LDO

A charge pump supplying voltage for the high-side gate driver is integrated to generate the appropriate gate to source bias voltage for the external high-side NMOSFET across a wide input supply voltage range. The charge pump generates  $V_{VHP} = 2 \times V_{VP} - 1.5V$  in doubled mode when  $V_{VP}$  is less than 11.5V and regulates the  $V_{VHP}$  supply to  $V_{VP} + 10V$  when  $V_{VP}$  is larger than 11.5V, respectively. The charge pump requires a  $1\mu F$  capacitor between the VP and VHP pins and a  $47nF$  capacitor between the HCP and LCP pins to act as the storage capacitor and flying capacitor, respectively. An undervoltage monitor for charge pump is integrated to detect the undervoltage condition.

A 11V linear regulator, which operates from the VP voltage supply input, supplying voltage for the low-side gate driver is integrated to generate the correct gate to source voltage for the external low-side NMOSFET. The linear regulator supporting an output current of 40 mA requires a  $1\mu F$  capacitor between the VGLS and GND pins to act as the regulated capacitor.

**Figure 5-1. Charge pump and VGLS\_LDO**



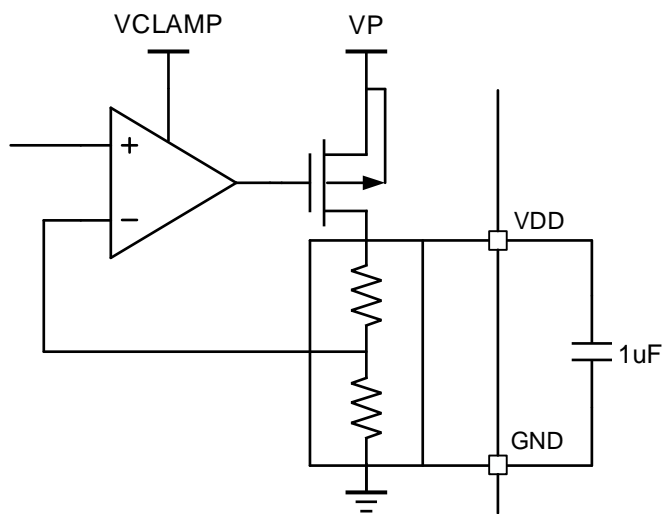
### 5.1.2. VDD\_LDO

A linear regulator outputting 5V, is integrated to supply part of the chip and external circuits or MCU.

The output driving current is 40mA, when output current exceeds 40mA, the output value will drop significantly.

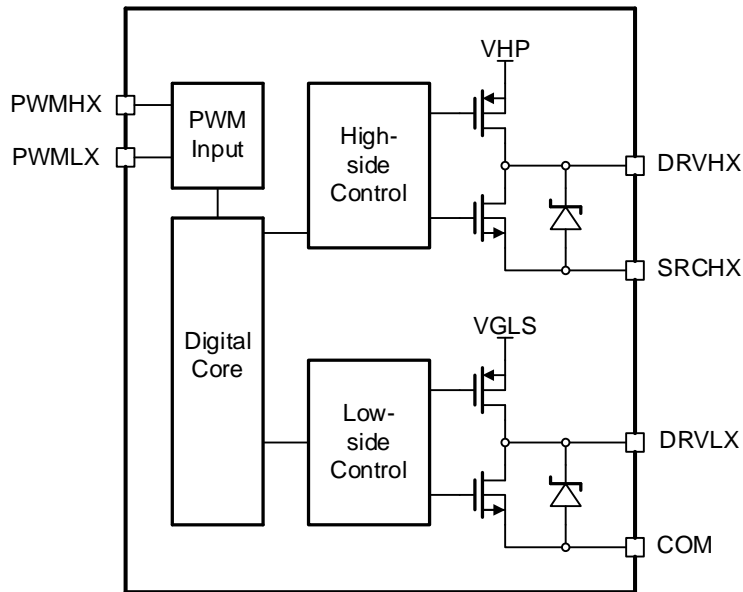
When the ENGATE pin is driven to low, the chip works in sleep mode to save power, which supplies 10mA current.

**Figure 5-2. VDD\_LDO**



## 5.2. Gate driver architecture

The gate driver uses a push-pull topology in both the high-side and low-side providing a strong pull up or down to the external NMOSFET gates. And it uses a programmable current control scheme through 4 level input pin to adjust the peak gate drive current, so the VDS slew rate of the external power MOSFETs can be smart-adaptable. Both sides of the gate driver incorporate Zener clamp diodes to protect the external NMOSFETs gates from overvoltage scenarios.

**Figure 5-3. Gate driver architecture**


### 5.3. Gate driver control mode

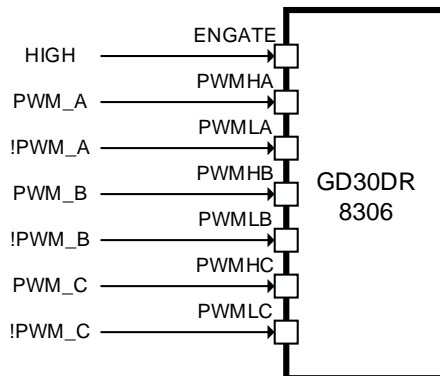
The GD30DR8306x is a gate driver IC designed for three-phase motor driver applications, operating in a wide range of 4.5V to 30V. This device integrates three half-bridge drivers, which can operate in three methods: 6xPWM mode and 3xPWM mode.

#### 5.3.1. 6xPWM Mode

The 6xPWM mode relates 6 inputs (PWMHx and PWMLx) to the 6 gate drives (DRVHx and DRVLx), and each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding PWMHx and PWMLx signals control the output state as listed in [Table 5-1. 6xPWM mode truth table.](#)

**Table 5-1. 6xPWM mode truth table**

PWMLx	PWMHx	DRVLx	DRVHx	SRCHx
0	0	L	L	Hi-Z
0	1	L	H	H
1	0	H	L	L
1	1	L	L	Hi-Z

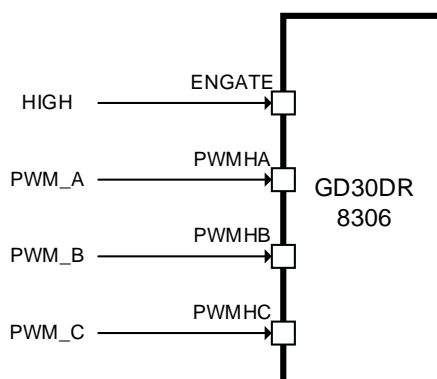
**Figure 5-4. 6xPWM mode**


### 5.3.2. 3xPWM Mode

The 3xPWM mode relates 3 inputs (PWMHx) to the 6 gate drives (DRVHx and DRVLx), one PWMHx pin controls two complementary half-bridge and supports two output states: low or high. The corresponding PWMHx signals control the output state as listed in [Table 5-2. 3xPWM mode truth table](#).

**Table 5-2. 3xPWM mode truth table**

PWMLx	PWMHx	DRVLx	DRVHx	SRCHx
X	0	H	L	L
X	1	L	H	H

**Figure 5-5. 3xPWM mode**


## 5.4. Gate driver slew rate control

The high-side and low-side peak gate drive currents are programmable through the external resistors connected to the level pin (ISET), so the VDS slew rate can be smart-adaptable to different external power MOSFETs. A proprietary slew rate is implemented to the MOSFETs to improve the system EMI.

## 5.5. Dead time

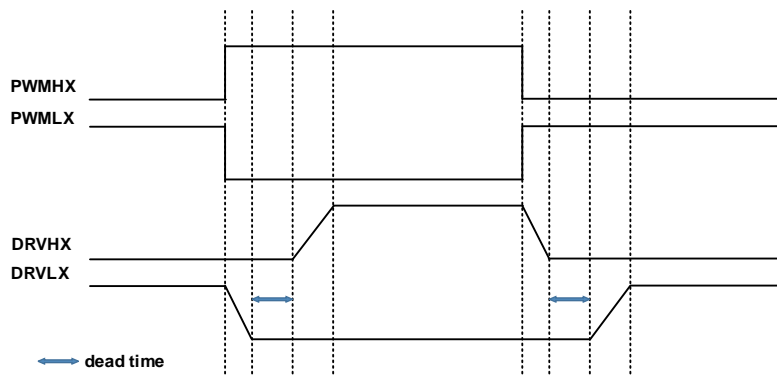
An internal handshaking scheme is used to prevent shoot-through and minimize the dead time when MOSFETs state in each half-bridge varies.

The dead time insertion is available in 6xPWM mode and 3xPWM mode.

The applying dead time can be expressed as below:

$$\text{dead time} = 200\text{ns}$$

**Figure 5-6. Dead time insertion**



## 5.6. Device configuration

The GD30DR8306x device can use external resistor connected to configuring pins to set the device configuration.



### 5.6.1. Hardware interface

The Hardware interface is available in GD30DR8306x device. That uses external resistor connected to designated pins to set the device configuration, such as PWM MODE and the gate driver current.

The MODE pin configures the PWM control mode.

**Table 5-3. PWM mode configuration table**

External interface	Mode selection
Hi-Z	6xPWM mode
Tied to GND	3xPWM mode

The ISET pin configures the gate driver source/sink current.

**Table 5-4. Gate drive current configuration table**

External interface	Sink	Source
Tied to GND	75mA	50mA
47KΩ±5% to GND	300mA	250mA
Hi-Z	600mA	500mA
Tied to VDD	1.2A	1A

### 5.7. Over temperature protection

If the die temperature exceeds the trip point of the thermal limit ( $T_{OTSD}$ ), the nFAULT pin is driven to low, which indicates a thermal event occurred until a clear fault command is issued through an effective falling edge on ENGATE pin ( $t_{RST}$ ).

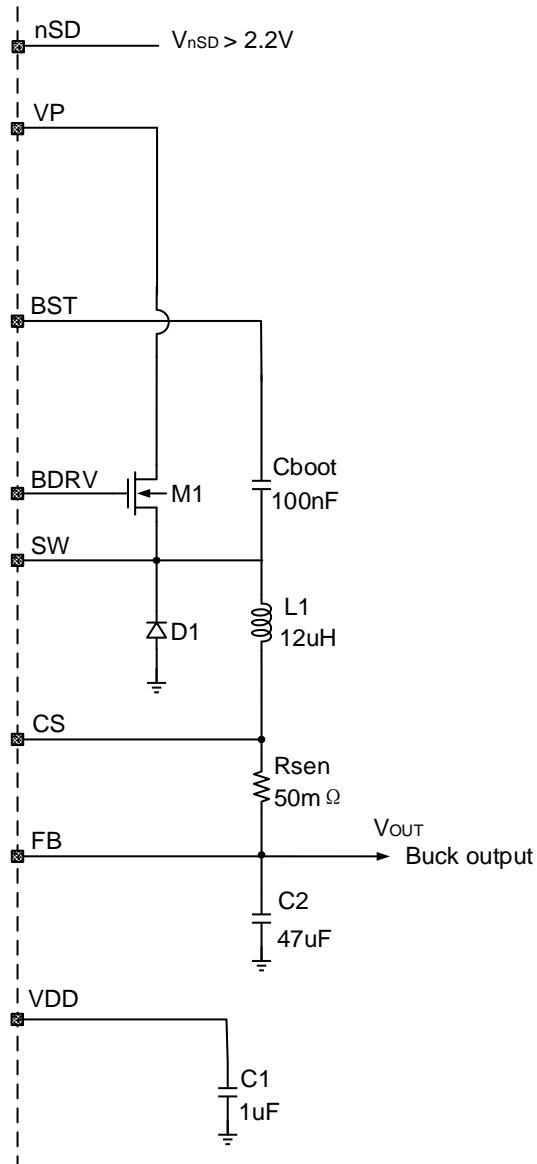
### 5.8. Buck Controller

A DC/DC buck controller is integrated in GD30DR8306x, the controller drives an external high side N-channel MOSFET for 2A output current, the output is regulated to 5V. The controller requires an external schottky diode to conduct current when the high side MOSFET is off.

The controller method is based upon peak current mode control and the switching frequency is 500kHz. A small ceramic capacitor Cboot is required between BST and SW pin to provide the gate drive voltage for the high side MOSFET. The Cboot capacitor is refreshed when the high side MOSFET is off and the low side diode conducts and the BST to SW voltage is charged to approximately 4.5V. When the voltage from BST to SW drops below 2.2V, the high side MOSFET is turned off using an UVLO circuit which allows the low side diode to conduct and refresh the charge on the Cboot capacitor. An internal circuit will also turn off the high side MOSFET and pull SW voltage to ground every four switching cycles for approximately 180ns to recharge the Cboot capacitor in maximum duty cycle applications or when the load is light.

The controller requires an external 50mΩ resistor between CS and FB pin for current sensing. To ensure the control loop stability, an output capacitor in the range of 20uF-100uF is recommended and the ESR should be less than 150 mΩ. [Figure 5-7. Buck controller application circuit](#) shows a typical application circuit.

**Figure 5-7. Buck controller application circuit**



## 6. Electrical characteristics

### 6.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 6-1. Absolute maximum ratings**

Symbol	Parameter	Min	Max	Unit
<b>Gate driver</b>				
$V_{VP}$	Power supply pin voltage (VP)	-0.3	30	V
$V_{VHP}$	Charge pump pin voltage (HCP, VHP)	-0.3	$V_{VP} + 12$	V
$V_{LCP}$	Charge pump negative-switching pin voltage (LCP)	-0.3	$V_{VP}$	V
$V_{VDD}$	Internal logic regulator pin voltage (VDD)	-0.3	5.5	V
$V_I$	Digital pin voltage (ENGATE, PWMHx, PWMLx, nFAULT, MODE, ISET)	-0.3	5.5	V
$V_{DRVH}$	Continuous high-side gate drive pin voltage (DRVHx)	-2	$V_{VHP} + 0.5$	V
$V_{DRVH}$	Transient 200-ns high-side gate drive pin voltage (DRVHx)	-3	$V_{VHP} + 0.5$	V
$V_{DRVH}$	High-side gate drive pin voltage with respect to SRCHx (DRVHx)	-0.3	13.5	V
$V_{SRCH}$	Continuous high-side source sense pin voltage (SRCHx)	-1	$V_{VP} + 5$	V
$V_{DRVL}$	Continuous low-side gate drive pin voltage (DRVLx)	0.5	13.5	V
$I_{SRC}$	Gate drive pin source current (DRVHx, DRVLx)	Internally limited		A
$I_{SNK}$	Gate drive pin sink current (DRVHx, DRVLx)	Internally limited		A
$V_{COM}$	Continuous low-side source sense pin voltage (COM)	-0.6	1	V
<b>Buck controller</b>				
$V_{BDRV}$	Power supply pin voltage (BDRV)	-0.3	30	V
$V_{nSD}$	Shutdown control pin voltage (nSD)	-0.3	$V_{VP}$	V
$V_{FB}$	Voltage feedback pin voltage (FB)	-0.3	7	V
$V_{BST}$	Bootstrap pin voltage with respect to SW (BST)	-0.3	7	V
$V_{SW}$	Switching node pin voltage (SW)	-0.3	$V_{VP}$	V
$V_{CS}$	Current Sense (CS)	-0.3	7	V
<b>Thermal characteristics</b>				
$T_J$	Operating junction temperature	-40	125	°C
$T_{stg}$	Storage temperature	-65	150	°C

## 6.2. Recommended operation conditions

**Table 6-2. Recommended operation conditions**

Symbol	Parameter	Min	Max	Unit
<b>Gate driver and current sense amplifier</b>				
$V_{VP}$	Power supply voltage (VP)	4.5	30	V
$V_I$	Input voltage (ENGATE, PWMHx, PWMLx, nFAULT, MODE, ISET)	0	5.5	V
$f_{PWM}$	Applied PWM signal (PWMHx, PWMLx)	0	200	kHz
$I_{GATE\_HS}$	High-side average gate drive current (DRVHx)	0	25	mA
$I_{GATE\_LS}$	Low-side average gate drive current (DRVLx)	0	25	mA
$I_{DVDD}$	External load current (VDD)	0	40	mA
$V_{VDD}$	Reference voltage input (VDD)	3	5.5	V
$V_{OD}$	Open drain pull-up voltage (nFAULT)	0	5.5	V
$I_{OD}$	Open drain output current (nFAULT)	0	5	mA
<b>Buck controller</b>				
$V_{BDRV}$	Drive voltage (BDRV)	4.5	30	V
$V_{nSD}$	Shutdown control input voltage (nSD)	0	30	V
<b>Thermal characteristics</b>				
$T_A$	Operating ambient temperature	-40	105	°C

## 6.3. Power supplies and current consumption

**Table 6-3. Power supplies and currents**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VP}$	VP operating supply current	$V_{VP} = 24\text{ V}$ , $EN = 3.3\text{ V}$ , $PWMHx/PWMLx = 0\text{ V}$	10.5	—	14	mA
$I_{VPQ}$	VP sleep mode supply current	$ENGATE = nSD = 0\text{ V}$ , $V_{VP} = 30\text{ V}$	108	144	200	μA
$t_{RST}$	Reset pulse time	$ENGATE = 0\text{ V}$ period to reset faults	8	—	40	μs
$t_{WAKE}$	Turn on time	$V_{VP} > V_{UVLO}$ , $ENGATE = 3.3\text{ V}$ to outputs ready	1	—	—	ms
$t_{SLEEP}$	Turn off time	$ENGATE = 0\text{ V}$ to device sleep mode	1	—	—	ms
$V_{VDD}$	VDD regulator voltage	$I_{VDD} = 0$ to 40 mA	—	5	—	V
$V_{VHP}$	VHP operating voltage with respect to VP	$V_{VP} = 12\text{ V}$ , $I_{VHP} = 0$ to 25 mA	8.4	11	12.5	V
		$V_{VP} = 8\text{ V}$ , $I_{VHP} = 0$ to 20 mA	6.3	9	10	
		$V_{VP} = 6\text{ V}$ , $I_{VHP} = 0$ to 15 mA	4	5	6	
		$V_{VP} = 4.5\text{ V}$ , $I_{VHP} = 0$ to 10 mA	4	5	6	
$V_{VGLS}$	Low-side gate drive voltage with respect to GND	$V_P = 16\text{ V}$	10.5	11.2	11.5	V

## 6.4. Logic inputs characteristics

Logic input pins include ENGATE, PWMHx, PWMLx.

**Table 6-4. Logic input characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	Input logic low voltage	—	0	—	0.8	V
$V_{IH}$	Input logic high voltage	—	1.5	—	5.5	V
$V_{HYS}$	Input logic hysteresis	—	100	—	—	mV
$I_{IL}$	Input logic low current	$V_{VIN} = 0\text{ V}$	-5.5	—	5.5	$\mu\text{A}$
$I_{IH}$	Input logic high current	$V_{VIN} = 5\text{ V}$	—	50	100	$\mu\text{A}$
$R_{PD}$	Pull-down resistance	To GND	100	—	—	k $\Omega$

## 6.5. Open drain outputs characteristics

Open drain output pins include nFAULT.

**Table 6-5. Open drain output characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OL}$	Output logic low voltage	$I_o = 5\text{ mA}$	—	—	0.1	V
$I_{OZ}$	Output high impedance leakage	$V_o = 5\text{ V}$	-5.5	0.01	5.5	$\mu\text{A}$

## 6.6. Gate driver characteristics

Gate driver pins include DRVHx, DRVLx.

**Table 6-6. Gate driver characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DTF}$	Gate drive dead time (Fixed)	—	—	200	—	ns
$I_{SRC}$	Peak source gate current	Tied to GND	—	50	—	mA
		47K $\Omega$ ±5% to GND	—	250	—	
		Hi-Z	—	500	—	
		Tied to VDD	—	1000	—	
$I_{SNK}$	Peak sink gate current	Tied to GND	—	75	—	mA
		47K $\Omega$ ±5% to GND	—	300	—	
		Hi-Z	—	600	—	
		Tied to VDD	—	1200	—	
$R_{OFF}$	Gate hold off resistor	DRVHx to SHx and DRVLx to GND	—	150	—	k $\Omega$

## 6.7. VDD LDO characteristics

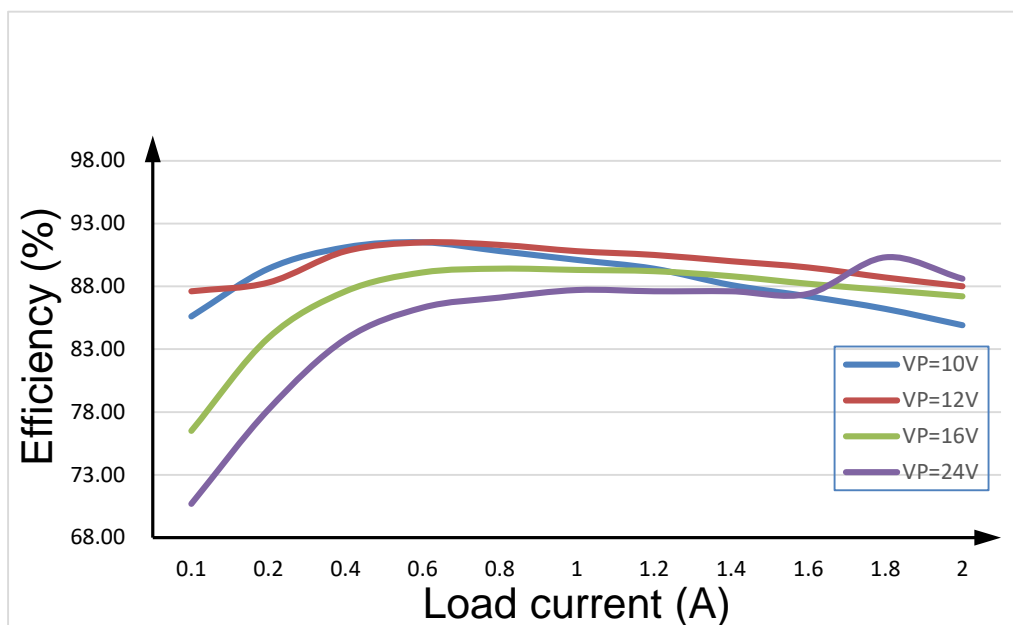
**Table 6-7. VDD LDO characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{VDD}$	LDO output voltage and Internal logic voltage	—	4.8	5.1	5.2	V
$V_{UVLO}$	VP undervoltage lockout	VP falling, UVLO	4.2	4.3	4.5	V
$V_{UVLO\_HYS}$	VP undervoltage hysteresis	Rising to falling threshold	—	200	—	mV
$t_{UVLO\_DEG}$	VP undervoltage deglitch time	VP falling, UVLO	—	10	—	$\mu$ s

## 6.8. Buck controller characteristics

**Table 6-8. Buck controller characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OUT}$	Buck Controller output voltage	—	—	5.0	—	V
$I_Q$	Shutdown supply current	$V_{nSD} = 0$ V	—	6	10	$\mu$ A
$V_{nSD\_H}$	Rising nSD threshold	—	—	2.2	—	V
$V_{nSD\_L}$	Falling nSD threshold	—	—	0.8	—	V
$R_{PD}$	nSD pull-down resistor	—	—	9	—	M $\Omega$
$T_{SS}$	Soft start time	—	—	1	—	ms
$T_{on\_min}$	Minimum on time	—	—	35	—	ns
$T_{OFF}$	Forced off time	—	—	180	—	ns
$T_R$	BDRV rise time(10%~90%)	$C_L = 1000$ pF	—	25	—	ns
$T_F$	BDRV fall time(90%~10%)	$C_L = 1000$ pF	—	20	—	ns
$I_{OH}$	Peak BDRV source current	—	—	300	—	mA
$I_{ol}$	Peak BDRV sink current	—	—	450	—	mA
$F_{SW}$	Switching frequency	—	450	500	550	kHz
$I_{LIMIT}$	Peak current limit	$V_{VP} = 24$ V	—	4.2	—	A
$V_{UVP}$	$V_{OUT}$ UVP threshold rise edge	—	—	3.24	—	V
	$V_{OUT}$ UVP threshold fall edge		—	3.0	—	V
$V_{OVP}$	$V_{OUT}$ OVP threshold	—	—	5.5	—	V
$V_{UVLO}$	BST UVLO voltage	BST to SW	—	2.2	—	V
$D_{MAX}$	Maximum duty cycle	—	—	97%	—	—

**Figure 6-1. Buck controller efficiency diagram**


## 6.9. Protection features

Protection features include over current protection, under voltage lockout and thermal shutdown.

**Table 6-9. Protection features characteristics**

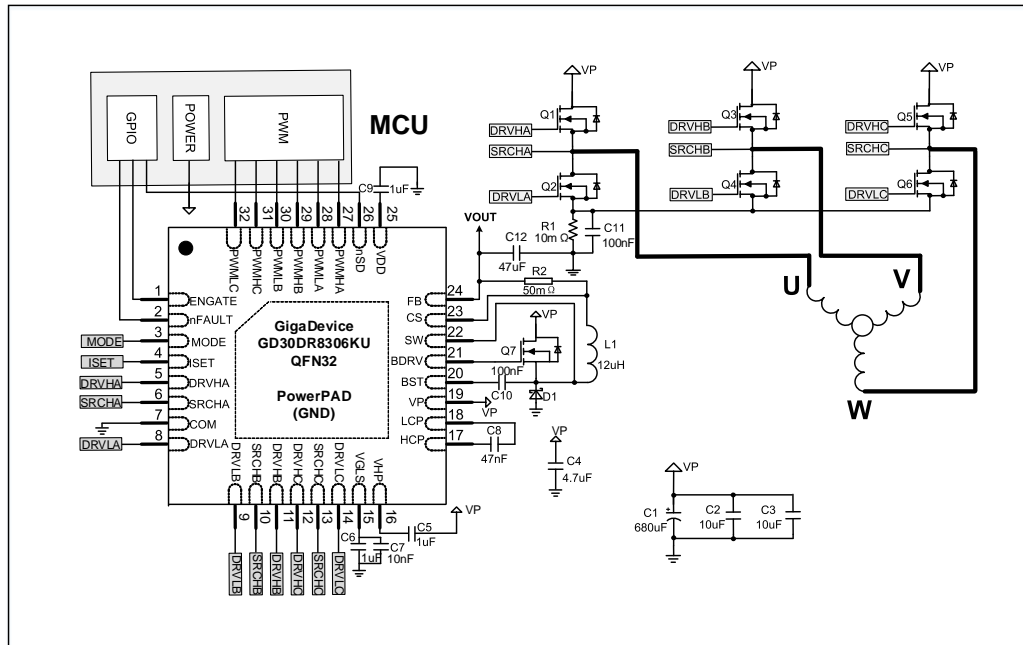
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{UVLO}$	VP undervoltage lockout	VP rising, UVLO	4.2	4.3	4.4	V
		VP falling, UVLO	4.0	4.1	4.2	
$V_{UVLO\_HYS}$	VP undervoltage hysteresis	Rising to falling threshold	—	200	—	mV
$t_{UVLO\_DEG}$	VP undervoltage deglitch time	VP falling, UVLO	—	100	—	$\mu$ s
$VHP_{UV}$	Charge pump undervoltage lockout	VHP falling, relative to VP	—	2.8	—	V
$VLP_{UV}$	Charge pump undervoltage lockout	VLP falling, relative to GND	—	2.8	—	V
$T_{OTSD}$	Thermal shutdown temperature	Die temperature, $T_J$	150	170	185	$^{\circ}$ C
$T_{HYS}$	Thermal hysteresis	Die temperature, $T_J$	—	20	—	$^{\circ}$ C

## 6.10. Parameter conditions

Unless otherwise specified, all values are given at  $T_A = 25^{\circ}$  C.

## 7. Typical application circuit

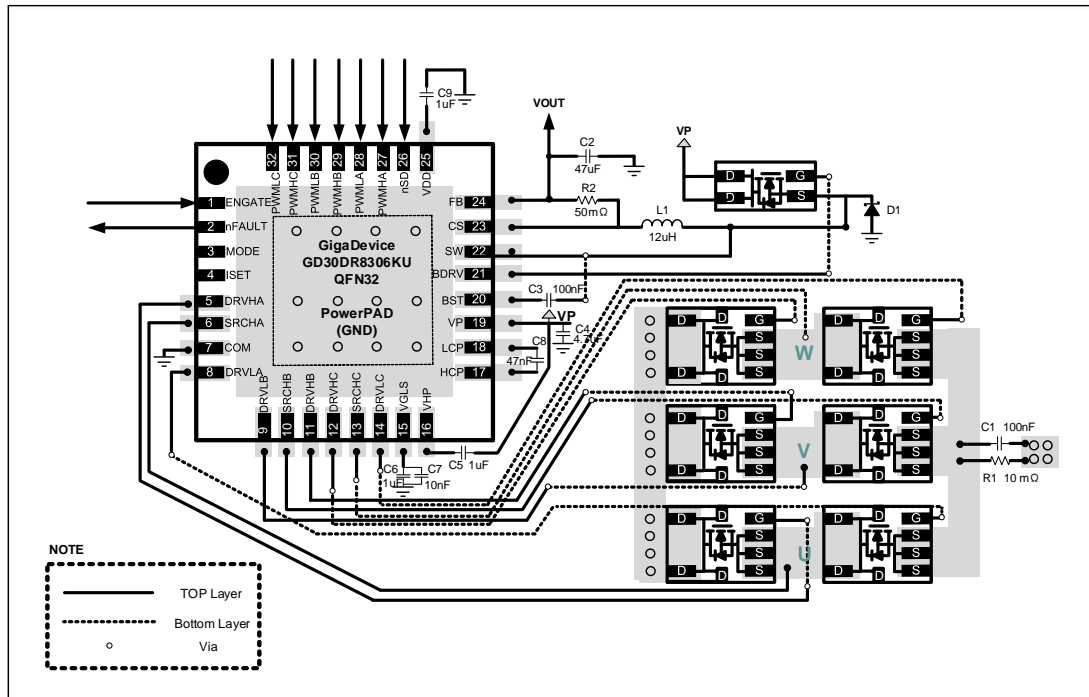
Figure 7-1. Typical application circuit





## 8. Layout guideline

Figure 8-1. Typical layout guideline



### Notes:

- 1) The VDD 1uF bypass capacitors should connect directly the VSS to ensure loop stability.
- 2) The VP 4.7uF bypass capacitor should be placed close to the supply pin with a direct path back to the GND pad.
- 3) The VP and VHP 1uF bypass capacitors should connect to the charge pump pins.
- 4) The VGLS 1uF and 10nF capacitor should connect directly the GND net to ensure loop stability.
- 5) The HCP and LCP 47nF flying capacitor should be placed directly next to the charge pump pins.
- 6) All capacitors should be as close to the chip pin as possible.

## 9. Package information

### 9.1. QFN32 package outline dimensions

Figure 9-1. QFN32 package outline

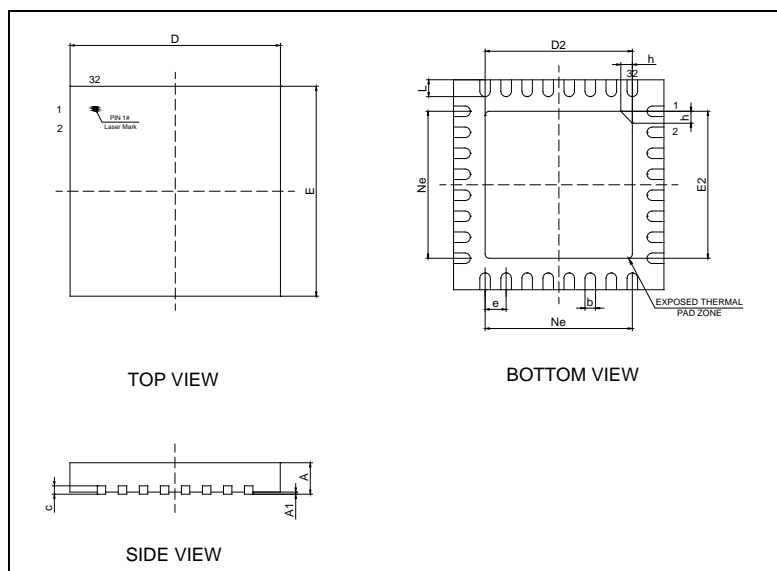
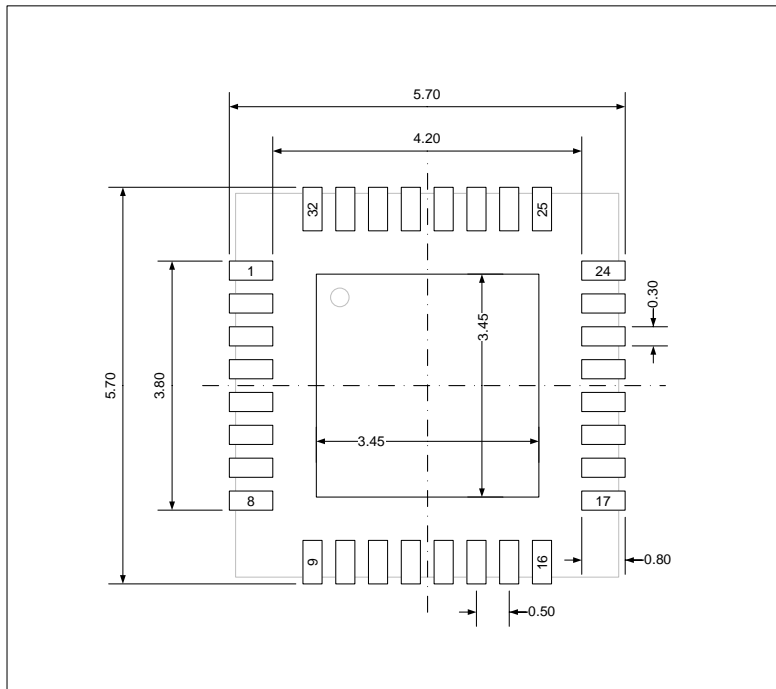


Table 9-1. QFN32 dimensions

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
e	—	0.50	—
h	0.30	0.35	0.40
L	0.35	0.40	0.45
Ne	—	3.50	—

(original dimensions are in millimeters)

Figure 9-2. QFN32 recommended footprint



(All dimensions are in millimeters)

## 9.2. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “ $\Theta$ ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

$\Theta_{JA}$ : Thermal resistance, junction-to-ambient.

$\Theta_{JB}$ : Thermal resistance, junction-to-board.

$\Theta_{JC}$ : Thermal resistance, junction-to-case.

$\Psi_{JB}$ : Thermal characterization parameter, junction-to-board.

$\Psi_{JT}$ : Thermal characterization parameter, junction-to-top center.

$$\Theta_{JA} = (T_J - T_A)/P_D$$

$$\Theta_{JB} = (T_J - T_B)/P_D$$

$$\Theta_{JC} = (T_J - T_C)/P_D$$

Where,  $T_J$  = Junction temperature.

$T_A$  = Ambient temperature

$T_B$  = Board temperature

$T_C$  = Case temperature which is monitoring on package surface

$P_D$  = Total power dissipation

$\Theta_{JA}$  represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower  $\Theta_{JA}$  can be considerate as better overall thermal performance.  $\Theta_{JA}$  is generally used to estimate junction temperature.

$\Theta_{JB}$  is used to measure the heat flow resistance between the chip surface and the PCB board.

$\Theta_{JC}$  represents the thermal resistance between the chip surface and the package top case.  $\Theta_{JC}$  is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

**Table 9-2. Package thermal characteristics<sup>(1)</sup>**

Symbol	Condition	Package	Value	Unit
$\Theta_{JA}$	Natural convection, 2S2P PCB	QFN32	38.5	°C/W
$\Theta_{JB}$	Cold plate, 2S2P PCB	QFN32	10.04	°C/W
$\Theta_{JC}$	Cold plate, 2S2P PCB	QFN32	14.67	°C/W
$\Psi_{JB}$	Natural convection, 2S2P PCB	QFN32	10.78	°C/W
$\Psi_{JT}$	Natural convection, 2S2P PCB	QFN32	0.46	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

## 10. Ordering information

Table 10-1. Part ordering code for GD30DR8306x device

Ordering Code	Interface	Package	Package Type	Temperature Operating Range
GD30DR8306KU	PWM mode configurable	QFN32	Green	Industrial -40°C to +105°C

## 11. Revision history

Table 11-1. Revision history

Revision No.	Description	Date
1.0	Initial Release	Mar.11, 2022

## Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the "Product"), is owned by the Company under the intellectual property laws and treaties of the People's Republic of China and other jurisdictions worldwide. The Company reserves all rights under such laws and treaties and does not grant any license under its patents, copyrights, trademarks, or other intellectual property rights. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no warranty of any kind, express or implied, with regard to this document or any Product, including, but not limited to, the implied warranties of merchantability and fitness for a particular purpose. The Company does not assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Except for customized products which has been expressly identified in the applicable agreement, the Products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only. The Products are not designed, intended, or authorized for use as components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, atomic energy control instruments, combustion control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or Product could cause personal injury, death, property or environmental damage ("Unintended Uses"). Customers shall take any and all actions to ensure using and selling the Products in accordance with the applicable laws and regulations. The Company is not liable, in whole or in part, and customers shall and hereby do release the Company as well as its suppliers and/or distributors from any claim, damage, or other liability arising from or related to all Unintended Uses of the Products. Customers shall indemnify and hold the Company as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Products.

Information in this document is provided solely in connection with the Products. The Company reserves the right to make changes, corrections, modifications or improvements to this document and Products and services described herein at any time, without notice.