GD3162

Advanced IGBT/SiC gate driver with dynamic gate strength adjust

Rev. 1 — 29 November 2022 Objective short data sheet

1 General description

The GD3162 is an advanced, galvanically isolated, single-channel gate driver designed to drive the latest SiC and IGBT modules for xEV traction inverters. The device does this while enabling space savings and performance improvements through advanced gate-drive functionality.

The GD3162 offers integrated galvanic isolation, a programmable interface via SPI, and advanced programmable protection features, such as overtemperature, desaturation, and current sense protection. GD3162 with integrated boost capability, can drive most SiC MOSFET and IGBT/SiC module gates directly and is able to shape the gate drive capability in order to improve the power device's switching performance and reduce voltage stress.

The control of the gate strength can be done using either SPI commands or the GS Enable Pins. GS_ENH logic controls the drive strength of the turn on, and GS_ENL controls the drive strength of the turn off. To further improve performance, these functions are designed to operate independent of each other. Three separate pullup drive strengths and three pulldown drive strengths are made available via trilevel functions on the input pins or commands in SPI.

The GD3162 autonomously manages faults and reports power device and gate driver status via the INTB pin. VCE/VDS monitoring, as well as VGE monitoring, can be selected to be output on the INTA/RTRPT pin.

The GD3162 includes self-test and control protection functions for design of high functional safety integrity level systems (ASIL C/D) and meets the stringent requirements of automotive applications, being fully AEC-Q100 grade 1 qualified.

2 Features and benefits

This section summarizes the key features, safety features, and regulatory approvals for the GD3162.

2.1 Key features

- Integrated galvanic signal isolation (up to 8 kV)
- Integrated boost capability for increased drive strength: Up to 10 A/ 20 A/ 30 A source/ sink current available by gate strength selection
- SPI or 3-state enabled GS_ENH and GS_ENL low-voltage domain pins to dynamically control gate drive strength. Adjustment of gate strength up to 20 KHz supported
- Dual gate pullup pins and dual gate pulldown pins for enhanced drive capability, synchronous adjustment of gate strength, reduced thermal loading during weak drive, and independent verification of each drive state operation
- SPI programmable ISEN/COMP setpoint, to allow the gate driver to automatically control gate drive strength based on high-voltage domain inputs.

- Temperature sense pins compatible with NTC and PTC thermistors allow for local control of temperature based gate-drive strength, as well as power device temperature monitoring via AOUT pin or SPI.
- Programmable ADC delay – Up to 8 µs sampling delay from rising or falling edge of PWM.
- Active Bus Discharge Functionality (PGD3162AM551EK and PGD3162AM581EK only) – Provides either MCU controlled or Safety Logic Controlled Gate drive to actively discharge the DC Link Capacitor.
- SPI interface for safety monitoring, configuration, and diagnostic reporting
- VCE power device monitoring via the low-voltage domain INTA/RTRPT pin
- Supports high PWM switching frequencies: PWM up to 100 kHz, thermally limited
- Fail-safe state management from LV and HV domain for user-selectable safe state
- Configurable desaturation and current sense optimized for protecting SiC and IGBTs against short circuit in less than 1 µs
- INTA/RTRPT and INTB Interrupt pins for current and voltage Fault Reporting and, if selected, VCE or VGE real-time reporting.
- Advanced two-level turn-off (2LTO) in combination with soft shut down gate current to reduce current and voltage stress associated with rapid turnoff.
- CMTI > 100 V/ns

2.2 Safety features

- Certified compliant with ISO 26262, supporting ASIL D level functional safety
- Error checking of SPI and configuration data with 8-bit CRC
- Autonomously manages severe faults and reports status via configurable INTB and/or INTA/RTRPT pins, and SPI interface
- VCE/VGE real-time cycle-by-cycle monitoring and reporting for feedback of power device status.
- Built-in self-test (BIST) of all analog and digital circuits
- Continuous watchdog of communications across isolation barrier
- Deadtime enforcement
- Overvoltage and undervoltage supervision of 5 V bias supply for LV circuitry
- Overvoltage and undervoltage supervision of VCC supply for HV circuitry
- Dedicated fail-safe state management pins on both low-voltage and high-voltage sides

2.3 Safety and regulatory approvals

- Reinforced isolation per DIN V VDE V 0884-10
- Withstand 5000 V rms (1 minute) isolation per UL 1577
- AEC-Q100 grade 1 automotive qualified

3 Ordering information

Table 1. Orderable part variations

Part number [1]	VDD (V)	External clearance and creepage distance (mm)	Material (isolation) group	Temperature (T_J) (°C)	Package
PGD3162AM550EK (without DC Link Discharge Mode)	5.0	>7.72[2]	II[3]	−40 to 150	32-pin wide body SOIC, 0.65 mm pitch
PGD3162AM551EK (with DC Link Discharge Mode)	5.0	>7.72[2]	II[3]	−40 to 150	32-pin wide body SOIC, 0.65 mm pitch
PGD3162AM580EK (without DC Link Discharge Mode)	5.0	>8.00[2]	I[3]	−40 to 150	32-pin wide body SOIC, 0.65 mm pitch
PGD3162AM581EK (with DC Link Discharge Mode)	5.0	>8.00[2]	I[3]	−40 to 150	32-pin wide body SOIC, 0.65 mm pitch

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] per IEC 60950-1 Tables 2K and 2N
[3] per IEC 60664-1

4 Block diagram

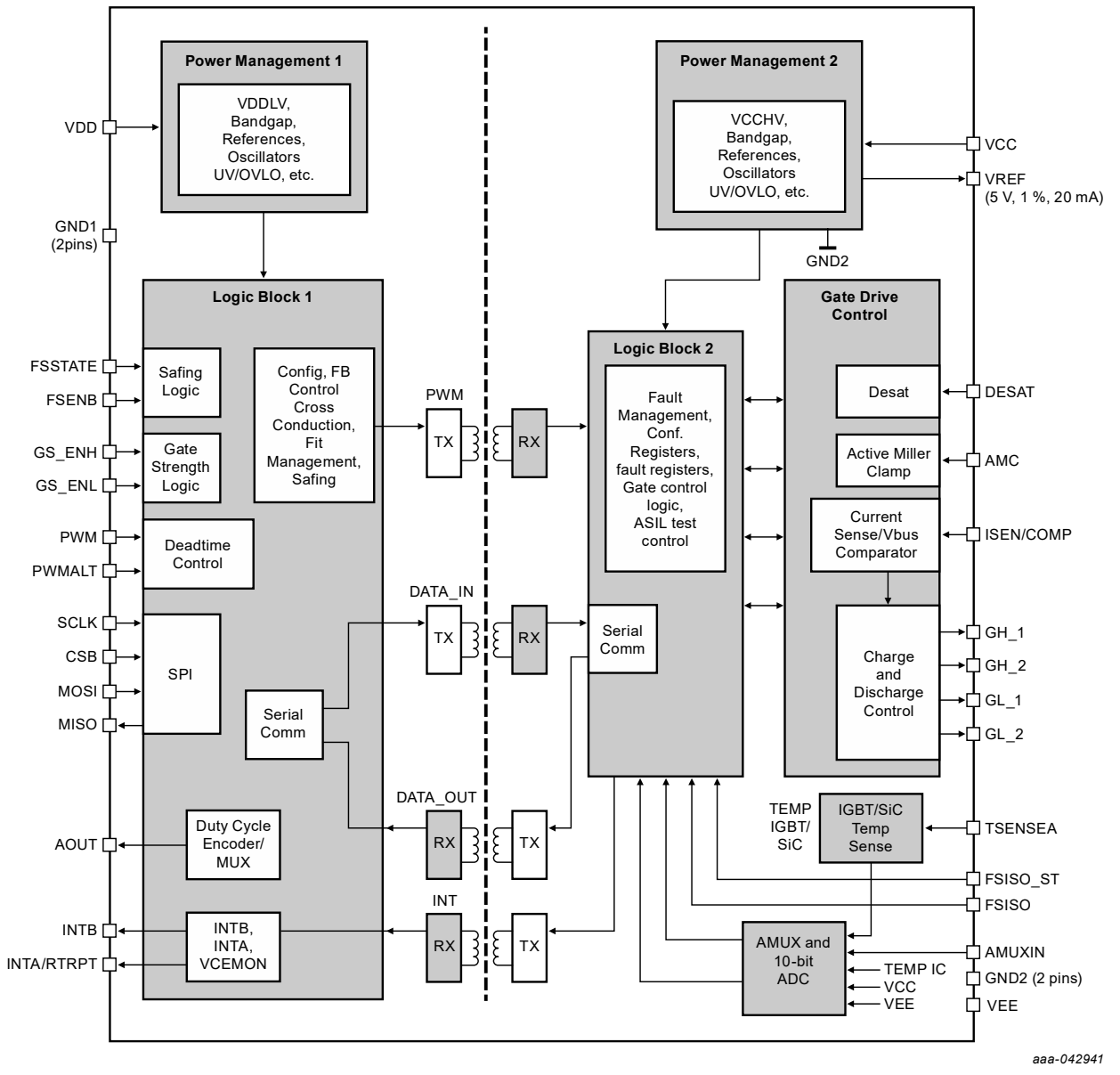

Figure 1. Internal block diagram

5 Limiting values

Table 2. Absolute maximum ratings

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). T_J = −40 to +150 °C, unless otherwise specified. Currents are positive into and negative out of the specified pins.

Symbol	Description (Rating)	Min	Max	Unit
Power supplies and current references				
V_{VDD}	Low-voltage domain logic supply voltage, 5.0 V [1]	−0.3	6.0	V
V_{VCC}	High-voltage domain positive supply voltage [2]	−0.3	25	V
V_{VEE}	High-voltage domain negative supply voltage [2]	−12	0.3	V
$V_{VCC-VEE}$	High-voltage domain positive/negative supply	−0.3	35	V
V_{VREF}	VREF voltage [2]	−0.3	6.0	V
I_{VREF}	VREF output current	—	–20	mA
Logic pins				
V_{IN}	Logic input pin voltage (FSSTATE, FSENB, PWM, PWMALT, GS_ENH, GS_ENL, SCLK, CSB, MOSI) [1]	−0.3	18	V
V_{OUT}	Logic output pin voltage (MISO, INTB, INTA/RTRPT, AOUT) [1]	−0.3	V_{VDD} + 0.3	V
V_{FSISO}	Logic input pin voltage (FSISO) [2]	−0.3	12	V
V_{FSISO_ST}	Logic input pin voltage (FSISO_ST) [2]	−0.3	12	V
Gage drive output stage				
$V_{GH\_1,2}$	GH_1,2 voltage [2]	V_{VEE} − 0.3	V_{VCC} + 0.3	V
$V_{GL\_1,2}$	GL_1,2 voltage [2]	V_{VEE} − 0.3	V_{VCC} + 0.3	V
V_{AMC}	AMC voltage [2]	V_{VEE} − 0.3	V_{VCC} + 0.3	V
$I_{SOURCEMAX1}$	GH_1 max. source current [3]	—	–14	A
$I_{SOURCEMAX2}$	GH_2 max. source current [3]	—	–5	A
$I_{SINKMAX1}$	GL_1, AMC max. sink current [3]	—	14	A
$I_{SINKMAX2}$	GL_2 max. sink current [3]	—	5	A
V_{DESAT}	DESAT voltage [2]	−0.3	V_{VCC} + 0.3	V
Temperature sense pin				
$V_{TSENSEA}$	TSENSEA voltage [2]	−0.3	6.0	V
Interrupt pins				
$I_{INTA/RTRPT}$	Open drain DC output current [4]	—	–20	mA
I_{INTB}	Open drain DC output current [4]	—	–20	mA
ISENSE sense pin				
$V_{ISEN/COMP}$	ISEN/COMP voltage [2]	−2.0	V_{VCC} + 0.3 V	V
AMUXIN pin				
V_{AMUXIN}	AMUXIN voltage [2]	−0.3	6.0	V
ESD ratings				
V_{ESDHBM}	ESD voltage (HBM) [5] All pins	 −2.0	 2.0	kV
V_{ESDCDM}	ESD voltage (CDM) [6] Corner pins Other pins	 −750 −500	 750 500	V

Table 2. Absolute maximum ratings...*continued*

All voltages referenced to GND1 (LV domain) or GND2 (HV domain). T_J = −40 to +150 °C, unless otherwise specified. Currents are positive into and negative out of the specified pins.

Symbol	Description (Rating)	Min	Max	Unit
$V_{ESDModule}$	ESD voltage (module level) [7]			kV
	GND1, GND2 pins	−8.0	8.0	
IMMUNITY				
dV_{ISO}/dt	Common mode transient immunity [8]	—	100	V/ns

[1] Ref = GND1
[2] Ref = GND2
[3] 50 %, 100 nF, 10 kHz
[4] V_{INTB}, $V_{INTA/RTRPT}$ < 1.0 V
[5] **Human Body Model (HBM) at device level**
ANSI/ESDA/JEDEC JS-001: 2010 Model HBM (human body model)
Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
Test points: pin to GND1 and pin to GND2
[6] **Charged Device Model (CDM)**
ANSI/ESD S5.3.1-2009
ESD Association Standard for Electrostatic Discharge Sensitivity Testing - Charged Device Model (CDM) - Component Level
[7] **Module Level ESD Tests**
ISO 10605:2008/Cor. 1:2010(E)
Road vehicles - Test methods for electrical disturbances from electrostatic discharge
[8] Pulse width = 10 ns

Revision history

Table 3. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
v.1.0	20221129	Objective	—	—
Modifications	—			

6 Legal information

6.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

6.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

6.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

6.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

SafeAssure — is a trademark of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com

Date of release: 29 November 2022
Document identifier: SDS_GD3162