

GigaDevice Semiconductor Inc.

GD32F107xx

Arm[®] Cortex[®]-M3 32-bit MCU

Datasheet

Revision 1.9

(Jun. 2023)



Table of Contents

| | |
|---|----|
| Table of Contents..... | 1 |
| List of Figures | 4 |
| List of Tables | 5 |
| 1. General description | 7 |
| 2. Device overview | 8 |
| 2.1. Device information..... | 8 |
| 2.2. Block diagram..... | 11 |
| 2.3. Pinouts and pin assignment..... | 12 |
| 2.4. Memory map..... | 15 |
| 2.5. Clock tree | 19 |
| 2.6. Pin definitions..... | 20 |
| 2.6.1. GD32F107Zx LQFP144 pin definitions | 20 |
| 2.6.2. GD32F107Vx LQFP100 pin definitions | 30 |
| 2.6.3. GD32F107Rx LQFP64 pin definitions..... | 38 |
| 3. Functional description | 43 |
| 3.1. Arm® Cortex®-M3 core..... | 43 |
| 3.2. On-chip memory..... | 43 |
| 3.3. Clock, reset and supply management..... | 44 |
| 3.4. Boot modes | 44 |
| 3.5. Power saving modes..... | 45 |
| 3.6. Analog to digital converter (ADC)..... | 45 |
| 3.7. Digital to analog converter (DAC)..... | 46 |
| 3.8. DMA..... | 46 |
| 3.9. General-purpose inputs/outputs (GPIOs)..... | 46 |
| 3.10. Timers and PWM generation | 47 |
| 3.11. Real time clock (RTC) | 48 |
| 3.12. Inter-integrated circuit (I2C)..... | 48 |
| 3.13. Serial peripheral interface (SPI)..... | 49 |
| 3.14. Universal synchronous asynchronous receiver transmitter (USART) | 49 |
| 3.15. Inter-IC sound (I2S)..... | 49 |



| | | |
|-------|--|----|
| 3.16. | Universal serial bus full-speed (USBFS)..... | 50 |
| 3.17. | Controller area network (CAN) | 50 |
| 3.18. | Ethernet MAC interface..... | 50 |
| 3.19. | External memory controller (EXMC)..... | 50 |
| 3.20. | Debug mode..... | 51 |
| 3.21. | Package and operation temperature | 51 |
| 4. | Electrical characteristics | 52 |
| 4.1. | Absolute maximum ratings..... | 52 |
| 4.2. | Operating conditions characteristics..... | 52 |
| 4.3. | Power consumption | 54 |
| 4.4. | EMC characteristics | 58 |
| 4.5. | Power supply supervisor characteristics..... | 58 |
| 4.6. | Electrical sensitivity..... | 59 |
| 4.7. | External clock characteristics | 59 |
| 4.8. | Internal clock characteristics | 62 |
| 4.9. | PLL characteristics | 62 |
| 4.10. | Memory characteristics | 63 |
| 4.11. | NRST pin characteristics..... | 64 |
| 4.12. | GPIO characteristics..... | 64 |
| 4.13. | Temperature sensor characteristics..... | 66 |
| 4.14. | ADC characteristics..... | 66 |
| 4.15. | DAC characteristics..... | 67 |
| 4.16. | I2C characteristics | 68 |
| 4.17. | SPI characteristics..... | 69 |
| 4.18. | I2S characteristics | 71 |
| 4.19. | USART characteristics..... | 73 |
| 4.20. | CAN characteristics..... | 73 |
| 4.21. | USBFS characteristics..... | 73 |
| 4.22. | EXMC characteristics | 74 |
| 4.23. | TIMER characteristics..... | 76 |
| 4.24. | WDGT characteristics..... | 76 |



| | |
|--|----|
| 4.25. Parameter condition | 77 |
| 5. Package information..... | 78 |
| 5.1. LQFP144 package outline dimensions..... | 78 |
| 5.2. LQFP100 package outline dimensions..... | 80 |
| 5.3. LQFP64 package outline dimensions..... | 82 |
| 5.4. Thermal characteristics | 84 |
| 6. Ordering information | 86 |
| 7. Revision history | 87 |



List of Figures

| | |
|--|----|
| Figure 2-1. GD32F107xx block diagram..... | 11 |
| Figure 2-2. GD32F107Zx LQFP144 pinouts..... | 12 |
| Figure 2-3. GD32F107Vx LQFP100 pinouts..... | 13 |
| Figure 2-4. GD32F107Rx LQFP64 pinouts | 14 |
| Figure 2-5. GD32F107xx clock tree | 19 |
| Figure 4-1. Recommended power supply decoupling capacitors ⁽¹⁾⁽²⁾ | 53 |
| Figure 4-2. Typical supply current consumption in Run mode..... | 57 |
| Figure 4-3. Typical supply current consumption in Sleep mode..... | 57 |
| Figure 4-4. Recommended external NRST pin circuit ⁽¹⁾ | 64 |
| Figure 4-5. I2C bus timing diagram..... | 69 |
| Figure 4-6. SPI timing diagram - master mode | 70 |
| Figure 4-7. SPI timing diagram - slave mode | 71 |
| Figure 4-8. I2S timing diagram - master mode | 72 |
| Figure 4-9. I2S timing diagram - slave mode..... | 73 |
| Figure 4-10. USBFS timings: definition of data signal rise and fall time..... | 74 |
| Figure 5-1. LQFP144 package outline | 78 |
| Figure 5-2. LQFP144 recommended footprint..... | 79 |
| Figure 5-3. LQFP100 package outline | 80 |
| Figure 5-4. LQFP100 recommended footprint..... | 81 |
| Figure 5-5. LQFP64 package outline | 82 |
| Figure 5-6. LQFP64 recommended footprint..... | 83 |



List of Tables

| | |
|--|----|
| Table 2-1. GD32F107xx devices features and peripheral list | 8 |
| Table 2-2. GD32F107xx devices features and peripheral list (continued) | 10 |
| Table 2-3. GD32F107xx memory map | 15 |
| Table 2-4. GD32F107Zx LQFP144 pin definitions | 20 |
| Table 2-5. GD32F107Vx LQFP100 pin definitions | 30 |
| Table 2-6. GD32F107Rx LQFP64 pin definitions | 38 |
| Table 4-1. Absolute maximum ratings ⁽¹⁾⁽⁴⁾ | 52 |
| Table 4-2. DC operating conditions | 52 |
| Table 4-3. Clock frequency ⁽¹⁾ | 53 |
| Table 4-4. Operating conditions at Power up/ Power down ⁽¹⁾ | 53 |
| Table 4-5. Start-up timings of Operating conditions ⁽¹⁾⁽²⁾⁽³⁾ | 53 |
| Table 4-6. Power saving mode wakeup timings characteristics ⁽¹⁾⁽²⁾ | 53 |
| Table 4-7. Power consumption characteristics ⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾ | 54 |
| Table 4-8. EMS characteristics ⁽¹⁾ | 58 |
| Table 4-9. Power supply supervisor characteristics | 58 |
| Table 4-10. ESD characteristics ⁽¹⁾ | 59 |
| Table 4-11. Static latch-up characteristics ⁽¹⁾ | 59 |
| Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics | 59 |
| Table 4-13. High speed external clock characteristics (HXTAL in bypass mode) | 60 |
| Table 4-14. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics | 60 |
| Table 4-15. Low speed external user clock characteristics (LXTAL in bypass mode) | 61 |
| Table 4-16. High speed internal clock (IRC8M) characteristics | 62 |
| Table 4-17. Low speed internal clock (IRC40K) characteristics | 62 |
| Table 4-18. PLL characteristics | 62 |
| Table 4-19. PLL1 characteristics | 63 |
| Table 4-20. PLL2 characteristics | 63 |
| Table 4-21. Flash memory characteristics | 63 |
| Table 4-22. NRST pin characteristics | 64 |
| Table 4-23. I/O port DC characteristics ⁽¹⁾⁽³⁾ | 64 |
| Table 4-24. I/O port AC characteristics ⁽¹⁾⁽²⁾⁽⁴⁾ | 66 |
| Table 4-25. Temperature sensor characteristics ⁽¹⁾ | 66 |
| Table 4-26. ADC characteristics | 66 |
| Table 4-27. ADC $R_{AIN\ max}$ for $f_{ADC} = 14\ MHz$ | 67 |
| Table 4-28. DAC characteristics | 67 |
| Table 4-29. I2C characteristics ⁽¹⁾⁽²⁾⁽³⁾ | 68 |
| Table 4-30. Standard SPI characteristics ⁽¹⁾ | 69 |
| Table 4-31. I2S characteristics ⁽¹⁾⁽²⁾ | 71 |
| Table 4-32. USART characteristics ⁽¹⁾ | 73 |
| Table 4-33. USBFS start up time | 73 |
| Table 4-34. USBFS DC electrical characteristics | 74 |



| | |
|--|----|
| Table 4-35. USBFS full speed-electrical characteristics ⁽¹⁾ | 74 |
| Table 4-36. Synchronous multiplexed PSRAM/NOR read timings ⁽¹⁾⁽²⁾⁽³⁾ | 74 |
| Table 4-37. Synchronous multiplexed PSRAM write timings ⁽¹⁾⁽²⁾⁽³⁾ | 75 |
| Table 4-38. Synchronous non-multiplexed PSRAM/NOR read timings ⁽¹⁾⁽²⁾⁽³⁾ | 75 |
| Table 4-39. Synchronous non-multiplexed PSRAM write timings ⁽¹⁾⁽²⁾⁽³⁾ | 76 |
| Table 4-40. TIMER characteristics ⁽¹⁾ | 76 |
| Table 4-41. FWDGT min/max timeout period at 40 kHz (IRC40K) ⁽¹⁾ | 76 |
| Table 4-42. WWDGT min-max timeout value at 54 MHz (f _{PCLK1}) ⁽¹⁾ | 77 |
| Table 5-1. LQFP144 package dimensions..... | 78 |
| Table 5-2. LQFP100 package dimensions..... | 80 |
| Table 5-3. LQFP64 package dimensions | 82 |
| Table 5-4. Package thermal characteristics ⁽¹⁾ | 84 |
| Table 6-1. Part ordering code for GD32F107xx devices | 86 |
| Table 7-1. Revision history..... | 87 |

1. General description

The GD32F107xx device belongs to the connectivity line of GD32 MCU Family. It is a 32-bit general-purpose microcontroller based on the Arm® Cortex®-M3 RISC core with enhanced connectivity performance and best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F107xx device incorporates the Arm® Cortex®-M3 32-bit processor core operating at 108 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 1 MB on-chip Flash memory and 96 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to two 12-bit ADCs, up to two 12-bit DACs, up to four general-purpose 16-bit timers, two basic timers plus one PWM advanced-control timer, as well as standard and advanced communication interfaces: up to three SPIs, two I²Cs, three USARTs, two UARTs, two I²Ss, two CANs, an USBFS and an Ethernet MAC.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F107xx devices suitable for a wide range of interconnection applications, especially in areas such as industrial control, motor drives, power monitor and alarm systems, consumer and handheld equipment, POS, vehicle GPS, LED display and so on.

2. Device overview

2.1. Device information

Table 2-1. GD32F107xx devices features and peripheral list

| Part Number | | GD32F107xx | | | | | | | |
|--------------|---------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| | | RB | RC | RD | RE | RF | RG | VB | VC |
| Flash | Code Area (KB) | 128 | 256 | 256 | 256 | 256 | 256 | 128 | 256 |
| | Data Area (KB) | 0 | 0 | 128 | 256 | 512 | 768 | 0 | 0 |
| | Total (KB) | 128 | 256 | 384 | 512 | 768 | 1024 | 128 | 256 |
| SRAM (KB) | | 96 | 96 | 96 | 96 | 96 | 96 | 96 | 96 |
| Timers | GPTM(16 bit) | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> |
| | Advanced TM(16 bit) | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic TM(16 bit) | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | U(S)ART | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| | I2C | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> |
| | SPI | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> |
| | I2S | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> |
| | CAN 2.0B | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | USBFS | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ethernet MAC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 51 | 51 | 51 | 51 | 51 | 51 | 80 | 80 |
| EXMC | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |



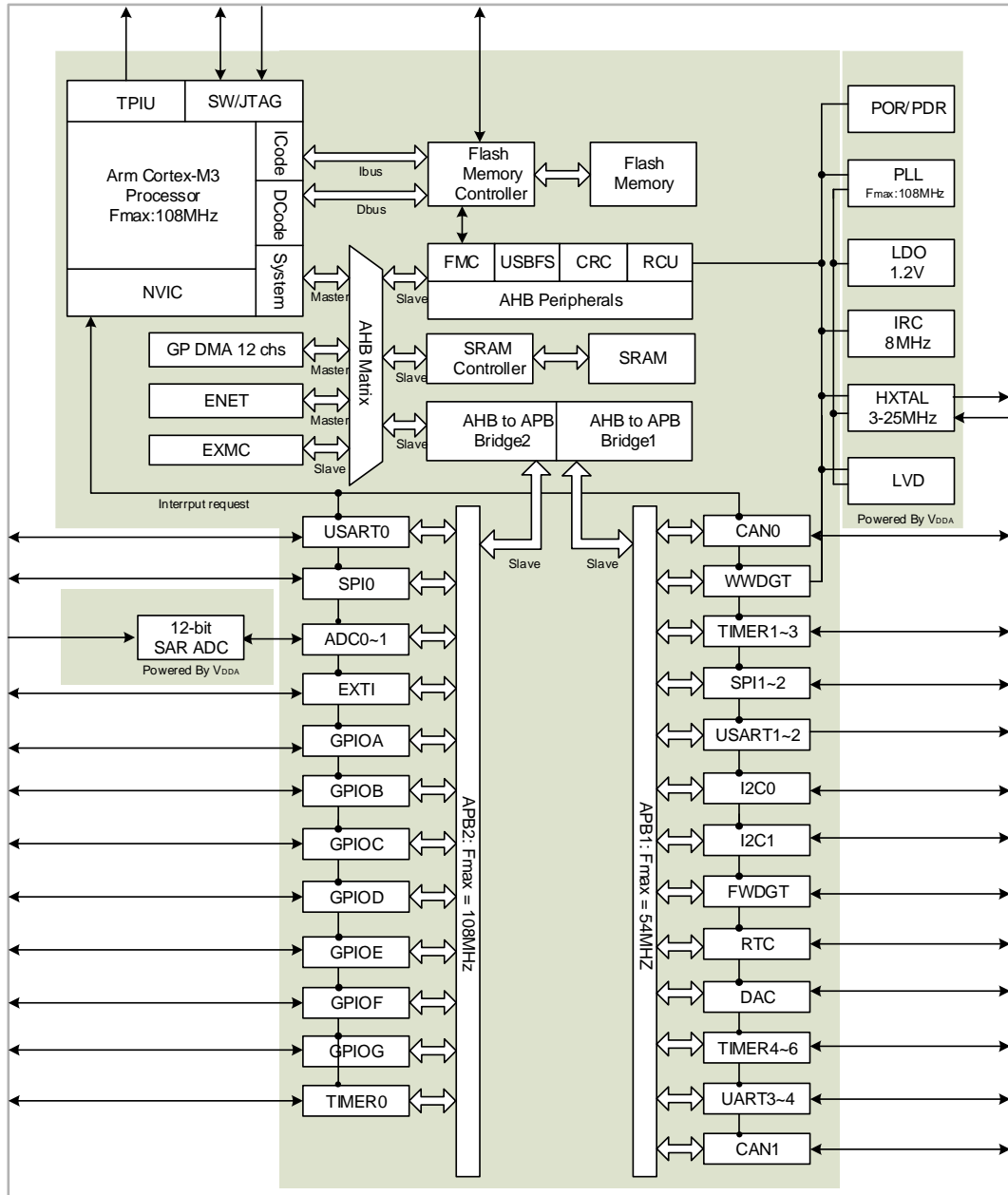
| Part Number | | GD32F107xx | | | | | | | |
|-------------|----------|------------|----|----|----|----|----|---------|----|
| | | RB | RC | RD | RE | RF | RG | VB | VC |
| ADC | Units | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Channels | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| DAC | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | | LQFP64 | | | | | | LQFP100 | |

Table 2-2. GD32F107xx devices features and peripheral list (continued)

| Part Number | | GD32F107xx | | | | | | | | |
|--------------|---------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| | | VD | VE | VF | VG | ZC | ZD | ZE | ZF | ZG |
| Flash | Code Area (KB) | 256 | 256 | 256 | 256 | 256 | 256 | 256 | 256 | 256 |
| | Data Area (KB) | 128 | 256 | 512 | 768 | 0 | 128 | 256 | 512 | 768 |
| | Total (KB) | 384 | 512 | 768 | 1024 | 256 | 384 | 512 | 768 | 1024 |
| SRAM (KB) | | 96 | 96 | 96 | 96 | 96 | 96 | 96 | 96 | 96 |
| Timers | GPTM(16 bit) | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> |
| | Advanced TM(16 bit) | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic TM(16 bit) | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | U(S)ART | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| | I2C | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | SPI | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> |
| | I2S | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> |
| | CAN 2.0B | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | USBFS | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Ethernet MAC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 80 | 80 | 80 | 80 | 112 | 112 | 112 | 112 | 112 |
| EXMC | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Channels | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| DAC | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| Package | | LQFP100 | | | | LQFP144 | | | | |

2.2. Block diagram

Figure 2-1. GD32F107xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F107Zx LQFP144 pinouts

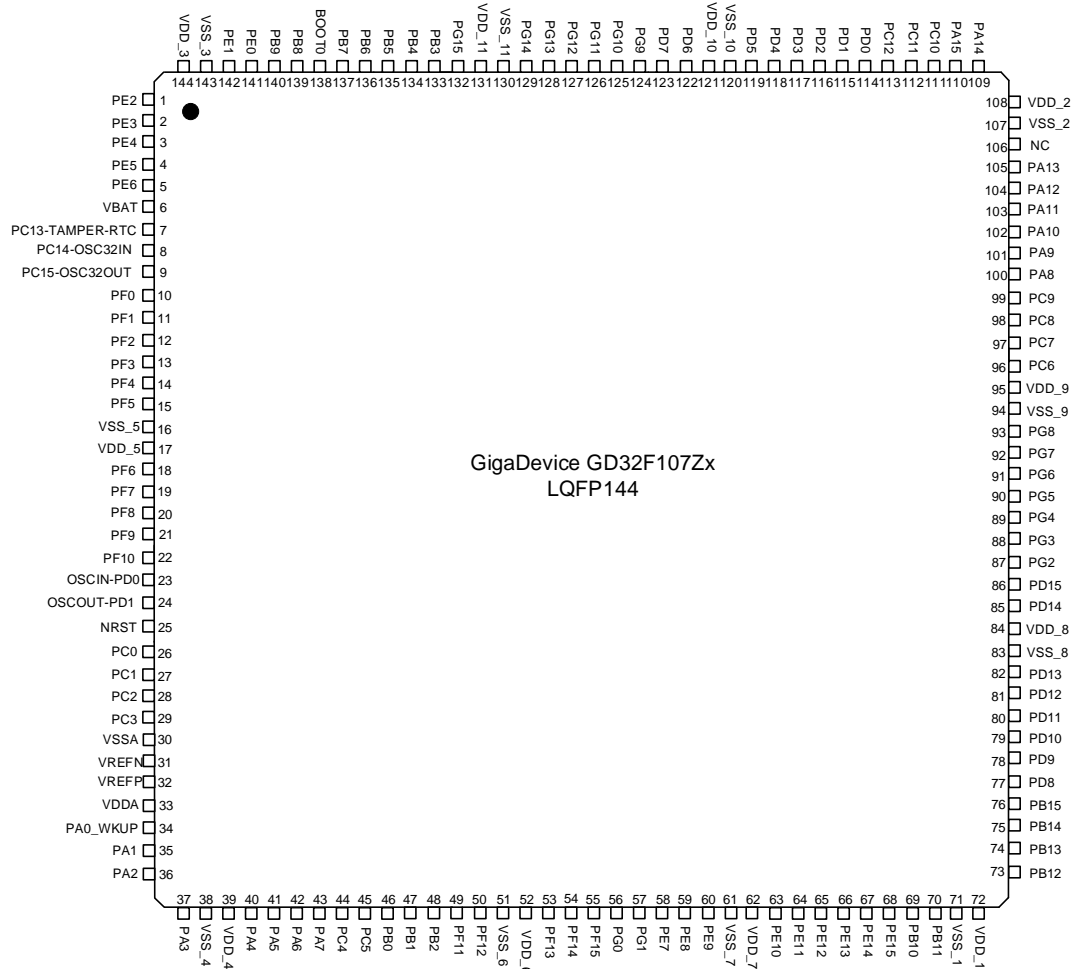


Figure 2-3. GD32F107Vx LQFP100 pinouts

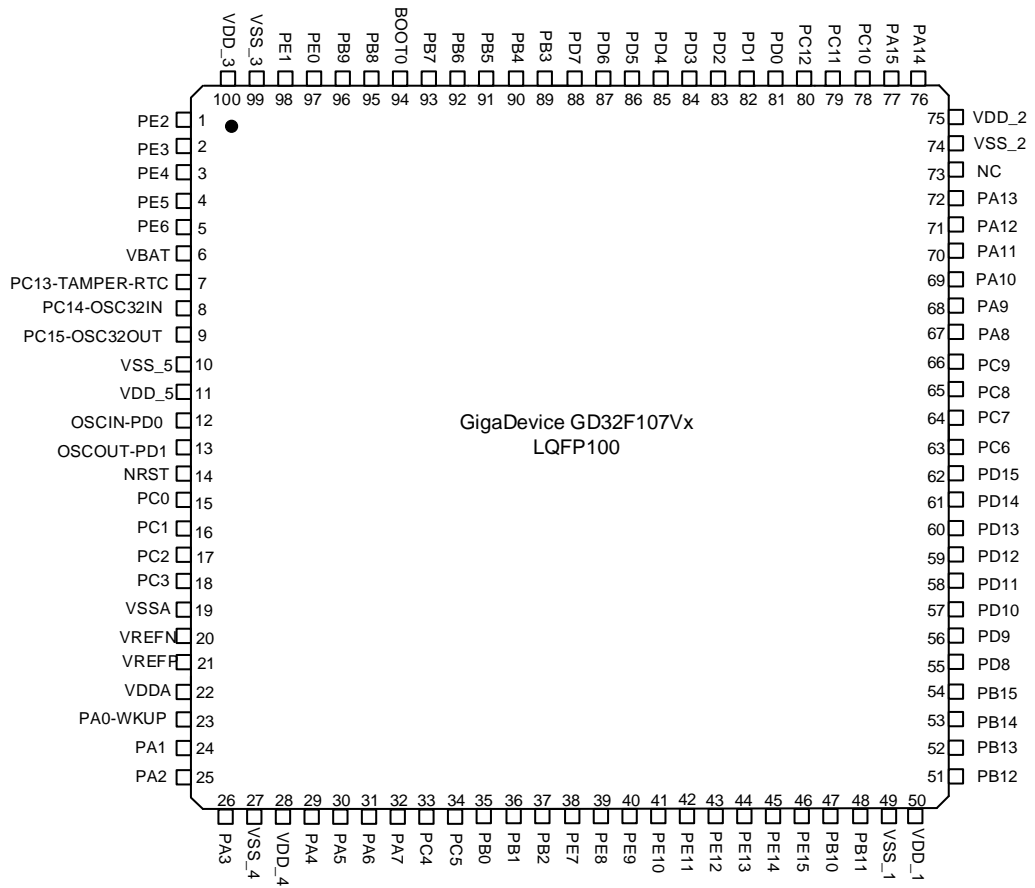
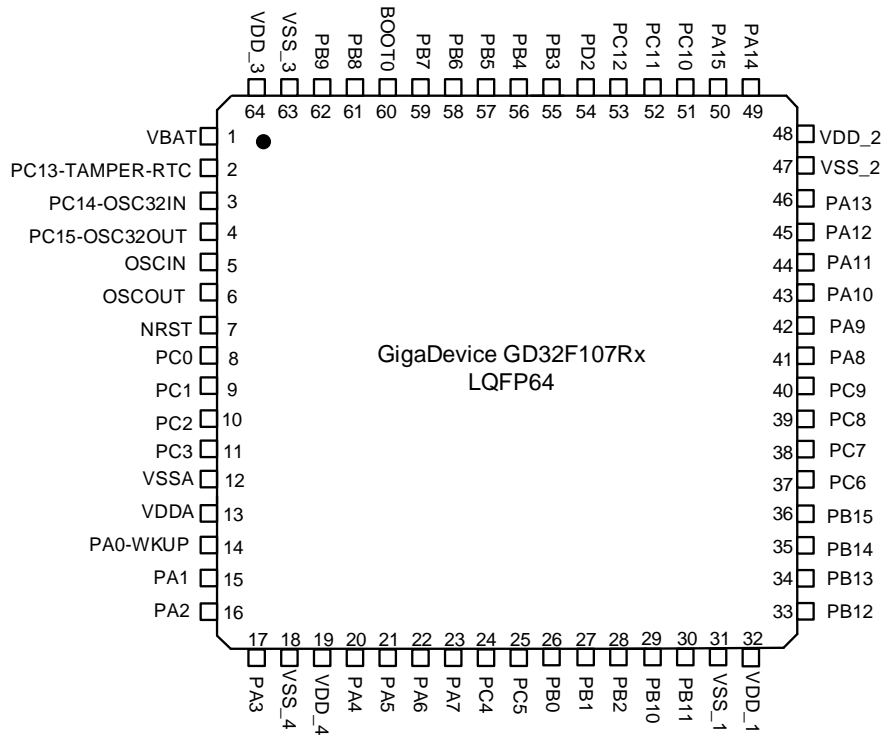


Figure 2-4. GD32F107Rx LQFP64 pinouts



2.4. Memory map

Table 2-3. GD32F107xx memory map

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------------|----------|---------------------------|-----------------------|
| External device | AHB | 0xA000 0000 - 0xA000 0FFF | EXMC - SWREG |
| External RAM | | 0x9000 0000 - 0x9FFF FFFF | EXMC - PC CARD |
| | | 0x7000 0000 - 0x8FFF FFFF | EXMC - NAND |
| | | 0x6000 0000 - 0x6FFF FFFF | EXMC - NOR/PSRAM/SRAM |
| Peripheral | AHB | 0x5000 0000 - 0x5003 FFFF | USBFS |
| | | 0x4008 0000 - 0x4FFF FFFF | Reserved |
| | | 0x4004 0000 - 0x4007 FFFF | Reserved |
| | | 0x4002 BC00 - 0x4003 FFFF | Reserved |
| | | 0x4002 B000 - 0x4002 BBFF | Reserved |
| | | 0x4002 A000 - 0x4002 AFFF | Reserved |
| | | 0x4002 8000 - 0x4002 9FFF | ENET |
| | | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | | 0x4002 6400 - 0x4002 67FF | Reserved |
| | | 0x4002 6000 - 0x4002 63FF | Reserved |
| | | 0x4002 5000 - 0x4002 5FFF | Reserved |
| | | 0x4002 4000 - 0x4002 4FFF | Reserved |
| | | 0x4002 3C00 - 0x4002 3FFF | Reserved |
| | | 0x4002 3800 - 0x4002 3BFF | Reserved |
| | | 0x4002 3400 - 0x4002 37FF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2C00 - 0x4002 2FFF | Reserved |
| | | 0x4002 2800 - 0x4002 2BFF | Reserved |
| | | 0x4002 2400 - 0x4002 27FF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | FMC |
| | | 0x4002 1C00 - 0x4002 1FFF | Reserved |
| | | 0x4002 1800 - 0x4002 1BFF | Reserved |
| | | 0x4002 1400 - 0x4002 17FF | Reserved |
| | | 0x4002 1000 - 0x4002 13FF | RCU |
| | | 0x4002 0C00 - 0x4002 0FFF | Reserved |
| | | 0x4002 0800 - 0x4002 0BFF | Reserved |
| | | 0x4002 0400 - 0x4002 07FF | DMA1 |
| | | 0x4002 0000 - 0x4002 03FF | DMA0 |
| 0x4001 8400 - 0x4001 FFFF | Reserved | | |



| Pre-defined Regions | Bus | Address | Peripherals | |
|---------------------|---------------------------|---------------------------|---------------------------|----------|
| | | 0x4001 8000 - 0x4001 83FF | Reserved | |
| | APB2 | 0x4001 7C00 - 0x4001 7FFF | Reserved | |
| | | 0x4001 7800 - 0x4001 7BFF | Reserved | |
| | | 0x4001 7400 - 0x4001 77FF | Reserved | |
| | | 0x4001 7000 - 0x4001 73FF | Reserved | |
| | | 0x4001 6C00 - 0x4001 6FFF | Reserved | |
| | | 0x4001 6800 - 0x4001 6BFF | Reserved | |
| | | 0x4001 5C00 - 0x4001 67FF | Reserved | |
| | | 0x4001 5800 - 0x4001 5BFF | Reserved | |
| | | 0x4001 5400 - 0x4001 57FF | Reserved | |
| | | 0x4001 5000 - 0x4001 53FF | Reserved | |
| | | 0x4001 4C00 - 0x4001 4FFF | Reserved | |
| | | 0x4001 4800 - 0x4001 4BFF | Reserved | |
| | | 0x4001 4400 - 0x4001 47FF | Reserved | |
| | | 0x4001 4000 - 0x4001 43FF | Reserved | |
| | | 0x4001 3C00 - 0x4001 3FFF | Reserved | |
| | | 0x4001 3800 - 0x4001 3BFF | USART0 | |
| | | 0x4001 3400 - 0x4001 37FF | Reserved | |
| | | 0x4001 3000 - 0x4001 33FF | SPI0 | |
| | | 0x4001 2C00 - 0x4001 2FFF | TIMER0 | |
| | | 0x4001 2800 - 0x4001 2BFF | ADC1 | |
| | | 0x4001 2400 - 0x4001 27FF | ADC0 | |
| | | 0x4001 2000 - 0x4001 23FF | GPIOG | |
| | | 0x4001 1C00 - 0x4001 1FFF | GPIOF | |
| | | 0x4001 1800 - 0x4001 1BFF | GPIOE | |
| | | 0x4001 1400 - 0x4001 17FF | GPIOD | |
| | | 0x4001 1000 - 0x4001 13FF | GPIOC | |
| | | 0x4001 0C00 - 0x4001 0FFF | GPIOB | |
| | | 0x4001 0800 - 0x4001 0BFF | GPIOA | |
| | | 0x4001 0400 - 0x4001 07FF | EXTI | |
| | | 0x4001 0000 - 0x4001 03FF | AFIO | |
| | | APB1 | 0x4000 CC00 - 0x4000 FFFF | Reserved |
| | | | 0x4000 C800 - 0x4000 CBFF | Reserved |
| | 0x4000 C400 - 0x4000 C7FF | | Reserved | |
| | 0x4000 C000 - 0x4000 C3FF | | Reserved | |
| | 0x4000 8000 - 0x4000 BFFF | | Reserved | |
| | 0x4000 7C00 - 0x4000 7FFF | | Reserved | |
| | 0x4000 7800 - 0x4000 7BFF | | Reserved | |
| | 0x4000 7400 - 0x4000 77FF | | DAC | |
| | 0x4000 7000 - 0x4000 73FF | | PMU | |



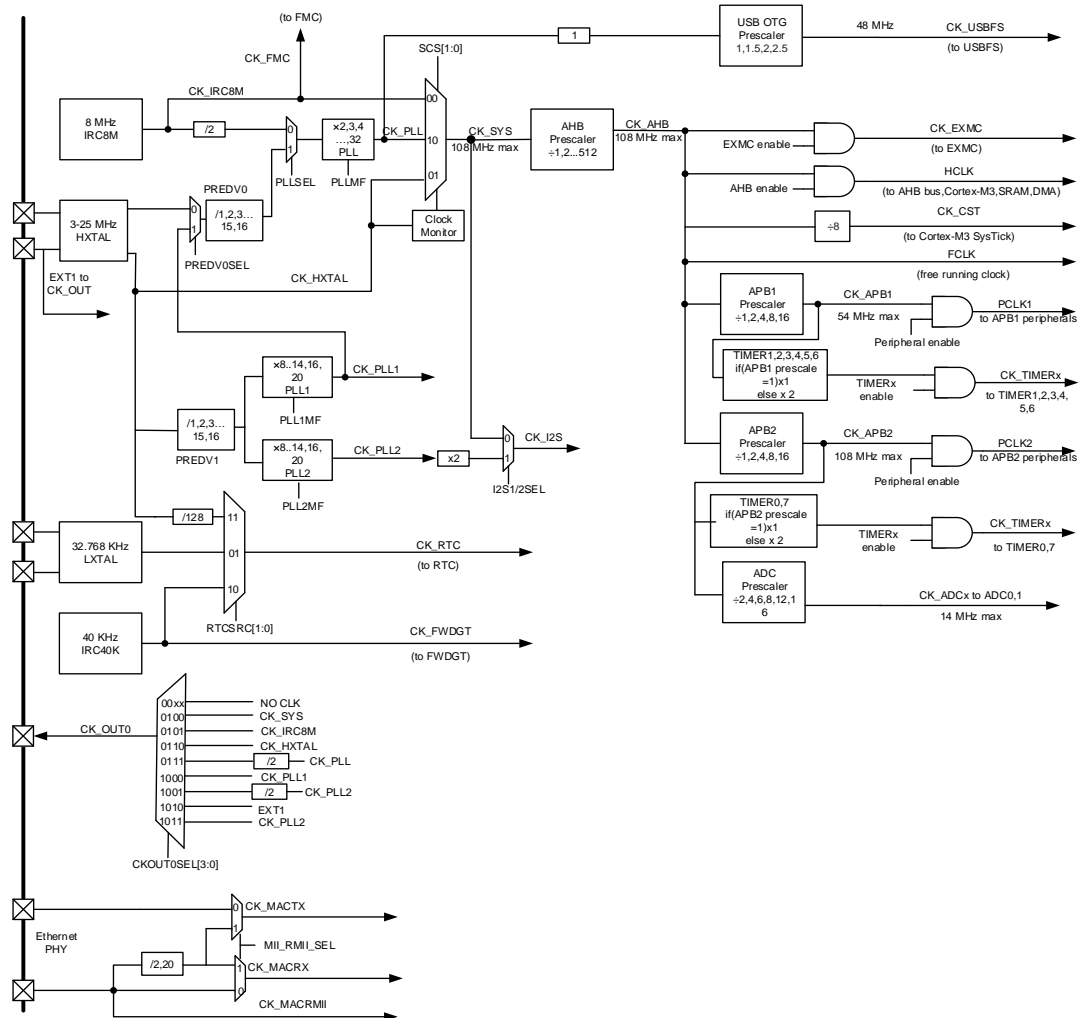
| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|-----|---------------------------|------------------------------|
| | | 0x4000 6C00 - 0x4000 6FFF | BKP |
| | | 0x4000 6800 - 0x4000 6BFF | CAN1 |
| | | 0x4000 6400 - 0x4000 67FF | CAN0 |
| | | 0x4000 6000 - 0x4000 63FF | Shared CAN SRAM 512 bytes |
| | | 0x4000 5C00 - 0x4000 5FFF | Reserved |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 5000 - 0x4000 53FF | UART4 |
| | | 0x4000 4C00 - 0x4000 4FFF | UART3 |
| | | 0x4000 4800 - 0x4000 4BFF | USART2 |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | Reserved |
| | | 0x4000 3C00 - 0x4000 3FFF | SP2/I2S2 |
| | | 0x4000 3800 - 0x4000 3BFF | SP1/I2S1 |
| | | 0x4000 3400 - 0x4000 37FF | Reserved |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | Reserved |
| | | 0x4000 1C00 - 0x4000 1FFF | Reserved |
| | | 0x4000 1800 - 0x4000 1BFF | Reserved |
| | | 0x4000 1400 - 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 - 0x4000 0FFF | TIMER4 |
| | | 0x4000 0800 - 0x4000 0BFF | TIMER3 |
| | | 0x4000 0400 - 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | AHB | 0x2007 0000 - 0x3FFF FFFF | Reserved |
| | | 0x2006 0000 - 0x2006 FFFF | Reserved |
| | | 0x2003 0000 - 0x2005 FFFF | Reserved |
| | | 0x2002 0000 - 0x2002 FFFF | Reserved |
| | | 0x2001 C000 - 0x2001 FFFF | Reserved |
| | | 0x2001 8000 - 0x2001 BFFF | Reserved |
| | | 0x2000 5000 - 0x2001 7FFF | SRAM |
| | | 0x2000 0000 - 0x2000 4FFF | |
| Code | AHB | 0x1FFF F810 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF F800 - 0x1FFF F80F | Option Bytes |
| | | 0x1FFF B000 - 0x1FFF F7FF | Boot loader |



| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|-----|---------------------------|---|
| | | 0x1FFF 7A10 - 0x1FFF AFFF | Reserved |
| | | 0x1FFF 7800 - 0x1FFF 7A0F | Reserved |
| | | 0x1FFF 0000 - 0x1FFF 77FF | Reserved |
| | | 0x1FFE C010 - 0x1FFE FFFF | Reserved |
| | | 0x1FFE C000 - 0x1FFE C00F | Reserved |
| | | 0x1001 0000 - 0x1FFE BFFF | Reserved |
| | | 0x1000 0000 - 0x1000 FFFF | Reserved |
| | | 0x083C 0000 - 0x0FFF FFFF | Reserved |
| | | 0x0830 0000 - 0x083B FFFF | Reserved |
| | | 0x0810 0000 - 0x082F FFFF | Reserved |
| | | 0x0802 0000 - 0x080F FFFF | Main Flash |
| | | 0x0800 0000 - 0x0801 FFFF | |
| | | 0x0030 0000 - 0x07FF FFFF | Reserved |
| | | 0x0010 0000 - 0x002F FFFF | Aliased to Main Flash or Boot loader |
| | | 0x0002 0000 - 0x000F FFFF | |
| | | 0x0000 0000 - 0x0001 FFFF | |

2.5. Clock tree

Figure 2-5. GD32F107xx clock tree



Legend:

- HXTAL: High speed external clock
- LXTAL: Low speed external clock
- IRC8M: High speed internal clock
- IRC40K: Low speed internal clock

2.6. Pin definitions

2.6.1. GD32F107Zx LQFP144 pin definitions

Table 2-4. GD32F107Zx LQFP144 pin definitions

| GD32F107Zx LQFP144 | | | | |
|-------------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PE2 | 1 | I/O | 5VT | Default: PE2 Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3 Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4 Alternate: TRACED1, EXMC_A20 |
| PE5 | 4 | I/O | 5VT | Default: PE5 Alternate: TRACED2, EXMC_A21 |
| PE6 | 5 | I/O | 5VT | Default: PE6 Alternate: TRACED3, EXMC_A22 |
| VBAT | 6 | P | | Default: VBAT |
| PC13- TAMPER- RTC | 7 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14- OSC32IN | 8 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15- OSC32OUT | 9 | I/O | | Default: PC15 Alternate: OSC32OUT |
| PF0 | 10 | I/O | 5VT | Default: PF0 Alternate: EXMC_A0 |
| PF1 | 11 | I/O | 5VT | Default: PF1 Alternate: EXMC_A1 |
| PF2 | 12 | I/O | 5VT | Default: PF2 Alternate: EXMC_A2 |
| PF3 | 13 | I/O | 5VT | Default: PF3 Alternate: EXMC_A3 |
| PF4 | 14 | I/O | 5VT | Default: PF4 Alternate: EXMC_A4 |
| PF5 | 15 | I/O | 5VT | Default: PF5 Alternate: EXMC_A5 |
| VSS_5 | 16 | P | | Default: VSS_5 |
| VDD_5 | 17 | P | | Default: VDD_5 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PF6 | 18 | I/O | | Default: PF6 Alternate: EXMC_NIORD |
| PF7 | 19 | I/O | | Default: PF7 Alternate: EXMC_NREG |
| PF8 | 20 | I/O | | Default: PF8 Alternate: EXMC_NIOWR |
| PF9 | 21 | I/O | | Default: PF9 Alternate: EXMC_CD |
| PF10 | 22 | I/O | | Default: PF10 Alternate: EXMC_INTR |
| OSCIN-PD0 | 23 | I | | Default: OSCIN Remap: PD0 |
| OSCOU-PD1 | 24 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 25 | I/O | | Default: NRST |
| PC0 | 26 | I/O | | Default: PC0 Alternate: ADC01_IN10 |
| PC1 | 27 | I/O | | Default: PC1 Alternate: ADC01_IN11, ETH_MII_MDC, ETH_RMII_MDC |
| PC2 | 28 | I/O | | Default: PC2 Alternate: ADC01_IN12, ETH_MII_TXD2 |
| PC3 | 29 | I/O | | Default: PC3 Alternate: ADC01_IN13, ETH_MII_TX_CLK |
| VSSA | 30 | P | | Default: VSSA |
| VREFN | 31 | P | | Default: VREFN |
| VREFP | 32 | P | | Default: VREFP |
| VDDA | 33 | P | | Default: VDDA |
| PA0-WKUP | 34 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, ETH_MII_CRS |
| PA1 | 35 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1, ETH_MII_RX_CLK, ETH_RMII_REF_CLK |
| PA2 | 36 | I/O | | Default: PA2 Alternate: USART1_TX, ADC01_IN2, |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | TIMER1_CH2, TIMER4_CH2, ETH_MII_MDIO, ETH_RMII_MDIO |
| PA3 | 37 | I/O | | Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, ETH_MII_COL |
| VSS_4 | 38 | P | | Default: VSS_4 |
| VDD_4 | 39 | P | | Default: VDD_4 |
| PA4 | 40 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap: SPI2_NSS, I2S2_WS |
| PA5 | 41 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1 |
| PA6 | 42 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BKIN |
| PA7 | 43 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, ETH_MII_RX_DV, ETH_RMII_CRS_DV Remap: TIMER0_CH0_ON |
| PC4 | 44 | I/O | | Default: PC4 Alternate: ADC01_IN14, ETH_MII_RXD0, ETH_RMII_RXD0 |
| PC5 | 45 | I/O | | Default: PC5 Alternate: ADC01_IN15, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PB0 | 46 | I/O | | Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, ETH_MII_RXD2 Remap: TIMER0_CH1_ON |
| PB1 | 47 | I/O | | Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, ETH_MII_RXD3 Remap: TIMER0_CH2_ON |
| PB2 | 48 | I/O | 5VT | Default: PB2, BOOT1 |
| PF11 | 49 | I/O | 5VT | Default: PF11 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: EXMC_NIOS16 |
| PF12 | 50 | I/O | 5VT | Default: PF12 Alternate: EXMC_A6 |
| VSS_6 | 51 | P | | Default: VSS_6 |
| VDD_6 | 52 | P | | Default: VDD_6 |
| PF13 | 53 | I/O | 5VT | Default: PF13 Alternate: EXMC_A7 |
| PF14 | 54 | I/O | 5VT | Default: PF14 Alternate: EXMC_A8 |
| PF15 | 55 | I/O | 5VT | Default: PF15 Alternate: EXMC_A9 |
| PG0 | 56 | I/O | 5VT | Default: PG0 Alternate: EXMC_A10 |
| PG1 | 57 | I/O | 5VT | Default: PG1 Alternate: EXMC_A11 |
| PE7 | 58 | I/O | 5VT | Default: PE7 Alternate: EXMC_D4 Remap: TIMER0_ETI |
| PE8 | 59 | I/O | 5VT | Default: PE8 Alternate: EXMC_D5 Remap: TIMER0_CH0_ON |
| PE9 | 60 | I/O | 5VT | Default: PE9 Alternate: EXMC_D6 Remap: TIMER0_CH0 |
| VSS_7 | 61 | P | | Default: VSS_7 |
| VDD_7 | 62 | P | | Default: VDD_7 |
| PE10 | 63 | I/O | 5VT | Default: PE10 Alternate: EXMC_D7 Remap: TIMER0_CH1_ON |
| PE11 | 64 | I/O | 5VT | Default: PE11 Alternate: EXMC_D8 Remap: TIMER0_CH1 |
| PE12 | 65 | I/O | 5VT | Default: PE12 Alternate: EXMC_D9 Remap: TIMER0_CH2_ON |
| PE13 | 66 | I/O | 5VT | Default: PE13 Alternate: EXMC_D10 Remap: TIMER0_CH2 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PE14 | 67 | I/O | 5VT | Default: PE14 Alternate: EXMC_D11 Remap: TIMER0_CH3 |
| PE15 | 68 | I/O | 5VT | Default: PE15 Alternate: EXMC_D12 Remap: TIMER0_BKIN |
| PB10 | 69 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL, USART2_TX, ETH_MII_RX_ER Remap: TIMER1_CH2 |
| PB11 | 70 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA, USART2_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN Remap: TIMER1_CH3 |
| VSS_1 | 71 | P | | Default: VSS_1 |
| VDD_1 | 72 | P | | Default: VDD_1 |
| PB12 | 73 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK, TIMER0_BKIN, I2S1_WS, CAN1_RX, ETH_MII_TXD0, ETH_RMII_TXD0 |
| PB13 | 74 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX, ETH_MII_TXD1, ETH_RMII_TXD1 |
| PB14 | 75 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON |
| PB15 | 76 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD |
| PD8 | 77 | I/O | 5VT | Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX, ETH_MII_RX_DV, ETH_RMII_CRS_DV |
| PD9 | 78 | I/O | 5VT | Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX, ETH_MII_RXD0, ETH_RMII_RXD0 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PD10 | 79 | I/O | 5VT | Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PD11 | 80 | I/O | 5VT | Default: PD11 Alternate: EXMC_A16/EXMC_CLE Remap: USART2_CTS, ETH_MII_RXD2 |
| PD12 | 81 | I/O | 5VT | Default: PD12 Alternate: EXMC_A17/EXMC_ALE Remap: TIMER3_CH0, USART2_RTS, ETH_MII_RXD3 |
| PD13 | 82 | I/O | 5VT | Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1 |
| VSS_8 | 83 | P | | Default: VSS_8 |
| VDD_8 | 84 | P | | Default: VDD_8 |
| PD14 | 85 | I/O | 5VT | Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2 |
| PD15 | 86 | I/O | 5VT | Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3 |
| PG2 | 87 | I/O | 5VT | Default: PG2 Alternate: EXMC_A12 |
| PG3 | 88 | I/O | 5VT | Default: PG3 Alternate: EXMC_A13 |
| PG4 | 89 | I/O | 5VT | Default: PG4 Alternate: EXMC_A14 |
| PG5 | 90 | I/O | 5VT | Default: PG5 Alternate: EXMC_A15 |
| PG6 | 91 | I/O | 5VT | Default: PG6 Alternate: EXMC_INT1 |
| PG7 | 92 | I/O | 5VT | Default: PG7 Alternate: EXMC_INT2 |
| PG8 | 93 | I/O | 5VT | Default: PG8 |
| VSS_9 | 94 | P | | Default: VSS_9 |
| VDD_9 | 95 | P | | Default: VDD_9 |
| PC6 | 96 | I/O | 5VT | Default: PC6 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: I2S1_MCK Remap: TIMER2_CH0 |
| PC7 | 97 | I/O | 5VT | Default: PC7 Alternate: I2S2_MCK Remap: TIMER2_CH1 |
| PC8 | 98 | I/O | 5VT | Default: PC8 Remap: TIMER2_CH2 |
| PC9 | 99 | I/O | 5VT | Default: PC9 Remap: TIMER2_CH3 |
| PA8 | 100 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF |
| PA9 | 101 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS |
| PA10 | 102 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID |
| PA11 | 103 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 |
| PA12 | 104 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI |
| PA13 | 105 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| NC | 106 | | | - |
| VSS_2 | 107 | P | | Default: VSS_2 |
| VDD_2 | 108 | P | | Default: VDD_2 |
| PA14 | 109 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 110 | I/O | 5VT | Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 111 | I/O | 5VT | Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PC11 | 112 | I/O | 5VT | Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO |
| PC12 | 113 | I/O | 5VT | Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD0 | 114 | I/O | 5VT | Default: PD0 Alternate: EXMC_D2 Remap: CAN0_RX |
| PD1 | 115 | I/O | 5VT | Default: PD1 Alternate: EXMC_D3 Remap: CAN0_TX |
| PD2 | 116 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI, UART4_RX |
| PD3 | 117 | I/O | 5VT | Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS |
| PD4 | 118 | I/O | 5VT | Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS |
| PD5 | 119 | I/O | 5VT | Default: PD5 Alternate: EXMC_NWE Remap: USART1_TX |
| VSS_10 | 120 | | | Default: VSS_10 |
| VDD_10 | 121 | | | Default: VDD_10 |
| PD6 | 122 | I/O | 5VT | Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX |
| PD7 | 123 | I/O | 5VT | Default: PD7 Alternate: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK |
| PG9 | 124 | I/O | 5VT | Default: PG9 Alternate: EXMC_NE1, EXMC_NCE2 |
| PG10 | 125 | I/O | 5VT | Default: PG10 Alternate: EXMC_NCE3_0, EXMC_NE2 |
| PG11 | 126 | I/O | 5VT | Default: PG11 Alternate: EXMC_NCE3_1 |
| PG12 | 127 | I/O | 5VT | Default: PG12 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: EXMC_NE3 |
| PG13 | 128 | I/O | 5VT | Default: PG13 Alternate: EXMC_A24 |
| PG14 | 129 | I/O | 5VT | Default: PG14 Alternate: EXMC_A25 |
| VSS_11 | 130 | P | | Default: VSS_11 |
| VDD_11 | 131 | P | | Default: VDD_11 |
| PG15 | 132 | I/O | 5VT | Default: PG15 |
| PB3 | 133 | I/O | 5VT | Default: JTDO Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 134 | I/O | 5VT | Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 135 | I/O | | Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ETH_PPS_OUT Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX |
| PB6 | 136 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX |
| PB7 | 137 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1, EXMC_NADV Remap: USART0_RX |
| BOOT0 | 138 | I | | Default: BOOT0 |
| PB8 | 139 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2, ETH_MII_TXD3 Remap: I2C0_SCL, CAN0_RX |
| PB9 | 140 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3 Remap: I2C0_SDA, CAN0_TX |
| PE0 | 141 | I/O | 5VT | Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0 |
| PE1 | 142 | I/O | 5VT | Default: PE1 Alternate: EXMC_NBL1 |
| VSS_3 | 143 | P | | Default: VSS_3 |



| GD32F107Zx LQFP144 | | | | |
|--------------------|------|-------------------------|--------------------------|-----------------------|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| VDD_3 | 144 | P | | Default: VDD_3 |

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.



2.6.2. GD32F107Vx LQFP100 pin definitions

Table 2-5. GD32F107Vx LQFP100 pin definitions

| GD32F107Vx LQFP100 | | | | |
|-------------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PE2 | 1 | I/O | 5VT | Default: PE2 Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3 Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4 Alternate: TRACED1, EXMC_A20 |
| PE5 | 4 | I/O | 5VT | Default: PE5 Alternate: TRACED2, EXMC_A21 |
| PE6 | 5 | I/O | 5VT | Default: PE6 Alternate: TRACED3, EXMC_A22 |
| VBAT | 6 | P | | Default: VBAT |
| PC13- TAMPER- RTC | 7 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14- OSC32IN | 8 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15- OSC32OUT | 9 | I/O | | Default: PC15 Alternate: OSC32OUT |
| VSS_5 | 10 | P | | Default: VSS_5 |
| VDD_5 | 11 | P | | Default: VDD_5 |
| OSCIN-PD0 | 12 | I | | Default: OSCIN Remap: PD0 |
| OSCOU- PD1 | 13 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 14 | I/O | | Default: NRST |
| PC0 | 15 | I/O | | Default: PC0 Alternate: ADC01_IN10 |
| PC1 | 16 | I/O | | Default: PC1 Alternate: ADC01_IN11, ETH_MII_MDC, ETH_RMII_MDC |
| PC2 | 17 | I/O | | Default: PC2 Alternate: ADC01_IN12, ETH_MII_TXD2 |
| PC3 | 18 | I/O | | Default: PC3 Alternate: ADC01_IN13, ETH_MII_TX_CLK |
| VSSA | 19 | P | | Default: VSSA |



| GD32F107Vx LQFP100 | | | | |
|--------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| VREFN | 20 | P | | Default: VREFN |
| VREFP | 21 | P | | Default: VREFP |
| VDDA | 22 | P | | Default: VDDA |
| PA0-WKUP | 23 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, ETH_MII_CRS |
| PA1 | 24 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1, ETH_MII_RX_CLK, ETH_RMII_REF_CLK |
| PA2 | 25 | I/O | | Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2, ETH_MII_MDIO, ETH_RMII_MDIO |
| PA3 | 26 | I/O | | Default: PA3 Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, ETH_MII_COL |
| VSS_4 | 27 | P | | Default: VSS_4 |
| VDD_4 | 28 | P | | Default: VDD_4 |
| PA4 | 29 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap: SPI2_NSS, I2S2_WS |
| PA5 | 30 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1 |
| PA6 | 31 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BKIN |
| PA7 | 32 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, ETH_MII_RX_DV, ETH_RMII_CRS_DV Remap: TIMER0_CH0_ON |
| PC4 | 33 | I/O | | Default: PC4 Alternate: ADC01_IN14, ETH_MII_RXD0, ETH_RMII_RXD0 |



| GD32F107Vx LQFP100 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PC5 | 34 | I/O | | Default: PC5 Alternate: ADC01_IN15, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PB0 | 35 | I/O | | Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, ETH_MII_RXD2 Remap: TIMER0_CH1_ON |
| PB1 | 36 | I/O | | Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, ETH_MII_RXD3 Remap: TIMER0_CH2_ON |
| PB2 | 37 | I/O | 5VT | Default: PB2, BOOT1 |
| PE7 | 38 | I/O | 5VT | Default: PE7 Alternate: EXMC_D4 Remap: TIMER0_ETI |
| PE8 | 39 | I/O | 5VT | Default: PE8 Alternate: EXMC_D5 Remap: TIMER0_CH0_ON |
| PE9 | 40 | I/O | 5VT | Default: PE9 Alternate: EXMC_D6 Remap: TIMER0_CH0 |
| PE10 | 41 | I/O | 5VT | Default: PE10 Alternate: EXMC_D7 Remap: TIMER0_CH1_ON |
| PE11 | 42 | I/O | 5VT | Default: PE11 Alternate: EXMC_D8 Remap: TIMER0_CH1 |
| PE12 | 43 | I/O | 5VT | Default: PE12 Alternate: EXMC_D9 Remap: TIMER0_CH2_ON |
| PE13 | 44 | I/O | 5VT | Default: PE13 Alternate: EXMC_D10 Remap: TIMER0_CH2 |
| PE14 | 45 | I/O | 5VT | Default: PE14 Alternate: EXMC_D11 Remap: TIMER0_CH3 |
| PE15 | 46 | I/O | 5VT | Default: PE15 Alternate: EXMC_D12 |



| GD32F107Vx LQFP100 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Remap: TIMER0_BKIN |
| PB10 | 47 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL ⁽³⁾ , USART2_TX, ETH_MII_RX_ER Remap: TIMER1_CH2 |
| PB11 | 48 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA ⁽³⁾ , USART2_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN Remap: TIMER1_CH3 |
| VSS_1 | 49 | P | | Default: VSS_1 |
| VDD_1 | 50 | P | | Default: VDD_1 |
| PB12 | 51 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA ⁽³⁾ , USART2_CK, TIMER0_BKIN, I2S1_WS, CAN1_RX, ETH_MII_TXD0, ETH_RMII_TXD0 |
| PB13 | 52 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX, ETH_MII_TXD1, ETH_RMII_TXD1 |
| PB14 | 53 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON |
| PB15 | 54 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD |
| PD8 | 55 | I/O | 5VT | Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX, ETH_MII_RX_DV, ETH_RMII_CRS_DV |
| PD9 | 56 | I/O | 5VT | Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX, ETH_MII_RXD0, ETH_RMII_RXD0 |
| PD10 | 57 | I/O | 5VT | Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PD11 | 58 | I/O | 5VT | Default: PD11 |



| GD32F107Vx LQFP100 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: EXMC_A16/EXMC_CLE Remap: USART2_CTS, ETH_MII_RXD2 |
| PD12 | 59 | I/O | 5VT | Default: PD12 Alternate: EXMC_A17/EXMC_ALE Remap: TIMER3_CH0, USART2_RTS, ETH_MII_RXD3 |
| PD13 | 60 | I/O | 5VT | Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1 |
| PD14 | 61 | I/O | 5VT | Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2 |
| PD15 | 62 | I/O | 5VT | Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3 |
| PC6 | 63 | I/O | 5VT | Default: PC6 Alternate: I2S1_MCK Remap: TIMER2_CH0 |
| PC7 | 64 | I/O | 5VT | Default: PC7 Alternate: I2S2_MCK Remap: TIMER2_CH1 |
| PC8 | 65 | I/O | 5VT | Default: PC8 Remap: TIMER2_CH2 |
| PC9 | 66 | I/O | 5VT | Default: PC9 Remap: TIMER2_CH3 |
| PA8 | 67 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF |
| PA9 | 68 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS |
| PA10 | 69 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, USBFS_ID |
| PA11 | 70 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 |
| PA12 | 71 | I/O | 5VT | Default: PA12 |



| GD32F107Vx LQFP100 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI |
| PA13 | 72 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| NC | 73 | | | - |
| VSS_2 | 74 | P | | Default: VSS_2 |
| VDD_2 | 75 | P | | Default: VDD_2 |
| PA14 | 76 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 77 | I/O | 5VT | Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 78 | I/O | 5VT | Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK |
| PC11 | 79 | I/O | 5VT | Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO |
| PC12 | 80 | I/O | 5VT | Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD0 | 81 | I/O | 5VT | Default: PD0 Alternate: EXMC_D2 Remap: CAN0_RX |
| PD1 | 82 | I/O | 5VT | Default: PD1 Alternate: EXMC_D3 Remap: CAN0_TX |
| PD2 | 83 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI, UART4_RX |
| PD3 | 84 | I/O | 5VT | Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS |
| PD4 | 85 | I/O | 5VT | Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS |
| PD5 | 86 | I/O | 5VT | Default: PD5 Alternate: EXMC_NWE |



| GD32F107Vx LQFP100 | | | | |
|--------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Remap: USART1_TX |
| PD6 | 87 | I/O | 5VT | Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX |
| PD7 | 88 | I/O | 5VT | Default: PD7 Alternate: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK |
| PB3 | 89 | I/O | 5VT | Default: JTDO Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 90 | I/O | 5VT | Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 91 | I/O | | Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ETH_PPS_OUT Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX |
| PB6 | 92 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX |
| PB7 | 93 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1, EXMC_NADV Remap: USART0_RX |
| BOOT0 | 94 | I | | Default: BOOT0 |
| PB8 | 95 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2, ETH_MII_TXD3 Remap: I2C0_SCL, CAN0_RX |
| PB9 | 96 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3 Remap: I2C0_SDA, CAN0_TX |
| PE0 | 97 | I/O | 5VT | Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0 |
| PE1 | 98 | I/O | 5VT | Default: PE1 Alternate: EXMC_NBL1 |
| VSS_3 | 99 | P | | Default: VSS_3 |
| VDD_3 | 100 | P | | Default: VDD_3 |



Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available in GD32F107VD/E/F/G devices.

2.6.3. GD32F107Rx LQFP64 pin definitions

Table 2-6. GD32F107Rx LQFP64 pin definitions

| GD32F107Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| VBAT | 1 | P | | Default: VBAT |
| PC13-TAMPER-RTC | 2 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14-OSC32IN | 3 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | | Default: PC15 Alternate: OSC32OUT |
| OSCIN | 5 | I | | Default: OSCIN |
| OSCOUT | 6 | O | | Default: OSCOUT |
| NRST | 7 | I/O | | Default: NRST |
| PC0 | 8 | I/O | | Default: PC0 Alternate: ADC01_IN10 |
| PC1 | 9 | I/O | | Default: PC1 Alternate: ADC01_IN11, ETH_MII_MDC, ETH_RMII_MDC |
| PC2 | 10 | I/O | | Default: PC2 Alternate: ADC01_IN12, ETH_MII_TXD2 |
| PC3 | 11 | I/O | | Default: PC3 Alternate: ADC01_IN13, ETH_MII_TX_CLK |
| VSSA | 12 | P | | Default: VSSA |
| VDDA | 13 | P | | Default: VDDA |
| PA0-WKUP | 14 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, ETH_MII_CRS |
| PA1 | 15 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC01_IN1, TIMER1_CH1, TIMER4_CH1, ETH_MII_RX_CLK, ETH_RMII_REF_CLK |
| PA2 | 16 | I/O | | Default: PA2 Alternate: USART1_TX, ADC01_IN2, TIMER1_CH2, TIMER4_CH2, ETH_MII_MDIO, ETH_RMII_MDIO |
| PA3 | 17 | I/O | | Default: PA3 |



| GD32F107Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: USART1_RX, ADC01_IN3, TIMER1_CH3, TIMER4_CH3, ETH_MII_COL |
| VSS_4 | 18 | P | | Default: VSS_4 |
| VDD_4 | 19 | P | | Default: VDD_4 |
| PA4 | 20 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4, DAC_OUT0 Remap: SPI2_NSS, I2S2_WS |
| PA5 | 21 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC01_IN5, DAC_OUT1 |
| PA6 | 22 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC01_IN6, TIMER2_CH0 Remap: TIMER0_BKIN |
| PA7 | 23 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7, TIMER2_CH1, ETH_MII_RX_DV, ETH_RMII_CRS_DV Remap: TIMER0_CH0_ON |
| PC4 | 24 | I/O | | Default: PC4 Alternate: ADC01_IN14, ETH_MII_RXD0, ETH_RMII_RXD0 |
| PC5 | 25 | I/O | | Default: PC5 Alternate: ADC01_IN15, ETH_MII_RXD1, ETH_RMII_RXD1 |
| PB0 | 26 | I/O | | Default: PB0 Alternate: ADC01_IN8, TIMER2_CH2, ETH_MII_RXD2 Remap: TIMER0_CH1_ON |
| PB1 | 27 | I/O | | Default: PB1 Alternate: ADC01_IN9, TIMER2_CH3, ETH_MII_RXD3 Remap: TIMER0_CH2_ON |
| PB2 | 28 | I/O | 5VT | Default: PB2, BOOT1 |
| PB10 | 29 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL ⁽³⁾ , USART2_TX, ETH_MII_RX_ER Remap: TIMER1_CH2 |



| GD32F107Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PB11 | 30 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA ⁽³⁾ , USART2_RX, ETH_MII_TX_EN, ETH_RMII_TX_EN Remap: TIMER1_CH3 |
| VSS_1 | 31 | P | | Default: VSS_1 |
| VDD_1 | 32 | P | | Default: VDD_1 |
| PB12 | 33 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA ⁽³⁾ , USART2_CK, TIMER0_BKIN, I2S1_WS, CAN1_RX, ETH_MII_TXD0, ETH_RMII_TXD0 |
| PB13 | 34 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK, USART2_CTS, TIMER0_CH0_ON, I2S1_CK, CAN1_TX, ETH_MII_TXD1, ETH_RMII_TXD1 |
| PB14 | 35 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON |
| PB15 | 36 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD |
| PC6 | 37 | I/O | 5VT | Default: PC6 Alternate: I2S1_MCK Remap: TIMER2_CH0 |
| PC7 | 38 | I/O | 5VT | Default: PC7 Alternate: I2S2_MCK Remap: TIMER2_CH1 |
| PC8 | 39 | I/O | 5VT | Default: PC8 Remap: TIMER2_CH2 |
| PC9 | 40 | I/O | 5VT | Default: PC9 Remap: TIMER2_CH3 |
| PA8 | 41 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, CK_OUT0, USBFS_SOF |
| PA9 | 42 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, USBFS_VBUS |
| PA10 | 43 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, |



| GD32F107Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | USBFS_ID |
| PA11 | 44 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, CAN0_RX, USBFS_DM, TIMER0_CH3 |
| PA12 | 45 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS, USBFS_DP, CAN0_TX, TIMER0_ETI |
| PA13 | 46 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| VSS_2 | 47 | P | | Default: VSS_2 |
| VDD_2 | 48 | P | | Default: VDD_2 |
| PA14 | 49 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 50 | I/O | 5VT | Default: JTDI Alternate: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 51 | I/O | 5VT | Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK |
| PC11 | 52 | I/O | 5VT | Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO |
| PC12 | 53 | I/O | 5VT | Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD |
| PD2 | 54 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI, UART4_RX |
| PB3 | 55 | I/O | 5VT | Default: JTDO Alternate: SPI2_SCK, I2S2_CK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 56 | I/O | 5VT | Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 57 | I/O | | Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI, I2S2_SD, ETH_PPS_OUT |



| GD32F107Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX |
| PB6 | 58 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX, CAN1_TX |
| PB7 | 59 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1 Remap: USART0_RX |
| BOOT0 | 60 | I | | Default: BOOT0 |
| PB8 | 61 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2, ETH_MII_TXD3 Remap: I2C0_SCL, CAN0_RX |
| PB9 | 62 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3 Remap: I2C0_SDA, CAN0_TX |
| VSS_3 | 63 | P | | Default: VSS_3 |
| VDD_3 | 64 | P | | Default: VDD_3 |

Notes:

- (1) Type: I = input, O = output, P = power.
(2) I/O Level: 5VT = 5 V tolerant.
(3) Functions are available in GD32F107RD/E/F/G devices.

3. Functional description

3.1. Arm® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of Arm® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit Arm® Cortex®-M3 processor core
- Up to 108 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Memory Protection Unit (MPU)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 1024 Kbytes of Flash memory
- The region of the MCU executing instructions without waiting time is up to 256K bytes (in case that Flash size less than or equal to 256K, all memory is no waiting time). A long delay when CPU fetches the instructions out of the range.
- 96 Kbytes of SRAM

The Arm® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 1024 Kbytes of inner Flash at most, which includes code Flash and data Flash, is available for storing programs and data, and there is no waiting time within code Flash area when CPU executes instructions. The [Table 2-3. GD32F107xx memory map](#) shows the memory map of the GD32F107xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 3 to 25 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and the high-speed APB domains is 108 MHz. The maximum allowed frequency of the low-speed APB domain is 54 MHz. See [Figure 2-5. GD32F107xx clock tree](#) for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), USART1 (PD5 and PD6), USBFS in device mode (PA9, PA11 and PA12). It also can be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 1 of Flash memory by

setting a bit in option bytes.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the Deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine
- Up to 1 MSPS conversion rate
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to two 12-bit 1 μ s multi-channel ADCs are integrated in the device. Each is a total of up to 21 multiplexed external channels. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADCs can be triggered from the events generated by the general-purpose timers (TIMERx) and the advanced-control timer (TIMER0) with internal connection. The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2.6\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage

into a digital value.

To ensure a high accuracy on ADC and DAC, the ADC/DAC independent external reference voltage should be connected to V_{REF+}/V_{REF-} pins. According to the different packages, V_{REF+} pin can be connected to V_{DDA} pin, or external reference voltage, V_{REF-} pin must be connected to V_{SSA} pin. The V_{REF+} pin is only available on no less than 100-pin packages. On less than 100-pin packages, the V_{REF+} pin is not available and it is internally connected to V_{DDA} . The V_{REF-} pin is internally connected to V_{SSA} .

3.7. Digital to analog converter (DAC)

- Two 12-bit DAC converters of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The two 12-bit buffered DAC channels are used to generate variable analog outputs. The DACs are designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. In dual DAC channel operation, conversions could be done independently or simultaneously. The maximum output value of the DAC is V_{REF+} .

3.8. DMA

- 7 channel DMA0 controller and 5 channel DMA1 controller
- Peripherals supported: Timers, ADC, SPIs, I²Cs, USARTs, DAC, I²S
- Dedicated DMA controller with the Ethernet application

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Four types of access method are supported: peripheral to peripheral, peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 112 general purpose I/O pins (GPIO) in GD32F107xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0-PF15, PG0-PG15 to implement logic input/output functions. Each of the GPIO ports has related control and

configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- One 16-bit advanced-control timer (TIMER0), four 16-bit general-purpose timers (GPTM), and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each GPTM and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog timer and window watchdog timer)

The advanced-control timer (TIMER0) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for

- Input capture
- Output compare
- PWM generation (edge- or center-aligned counting modes)
- Single pulse mode output

If configured as a general-purpose 16-bit timer, it has the same functions as the TIMER x timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM), known as TIMER1 ~ TIMER4 can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 and TIMER6 are mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F107xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and an 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz from external crystal oscillator.

3.12. Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the

situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs and two UARTs with operating frequency up to 6.75 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART0, USART1 and USART2) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication except UART4.

3.15. Inter-IC sound (I2S)

- Two I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F107xx contain two I2S-bus interfaces that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1 and SPI2. The audio sampling frequency from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

3.16. Universal serial bus full-speed (USBFS)

- One USB device/host/OTG full-speed Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus with 4 bidirectional endpoints. The device controller enables 12 Mbit/s data exchange with integrated transceivers in device/host/OTG mode. Full-speed peripheral is compliant with the USB 2.0 specification. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HXTAL crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.17. Controller area network (CAN)

- Two CAN2.0B interface with communication frequency up to 1 Mbit/s
- Internal main PLL for USB CLK compliantly

Controller area network (CAN) is a method for enabling serial communication in field bus. The CAN protocol has been used extensively in industrial automation and automotive applications. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. Each CAN has three mailboxes for transmission and two FIFOs of three message deep for reception. It also provides 14 scalable/configurable identifier filter banks for selecting the incoming messages needed and discarding the others.

3.18. Ethernet MAC interface

- IEEE 802.3 compliant media access controller (MAC) for Ethernet LAN
- 10/100 Mbit/s rates with dedicated DMA controller and SRAM
- Support hardware precision time protocol (PTP) with conformity to IEEE 1588

The Ethernet media access controller (MAC) conforms to IEEE 802.3 specifications and fully supports IEEE 1588 standards. The embedded MAC provides the interface to the required external network physical interface (PHY) for LAN bus connection via an internal media independent interface (MII) or a reduced media independent interface (RMII). The number of MII signals provided up to 17 with 25 MHz output and RMII up to 9 with 50 MHz output. The function of 32-bit CRC checking is also available.

3.19. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and

CF card

- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.20. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21. Package and operation temperature

- LQFP144 (GD32F107Zx), LQFP100 (GD32F107Vx), LQFP64 (GD32F107Rx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings⁽¹⁾⁽⁴⁾

| Symbol | Parameter | Min | Max | Unit |
|------------------------------------|---|------------------------|------------------------|------|
| V _{DD} | External voltage range ⁽²⁾ | V _{SS} - 0.3 | V _{SS} + 3.6 | V |
| V _{DDA} | External analog supply voltage | V _{SSA} - 0.3 | V _{SSA} + 3.6 | V |
| V _{BAT} | External battery supply voltage | V _{SS} - 0.3 | V _{SS} + 3.6 | V |
| V _{IN} | Input voltage on 5V tolerant pin ⁽³⁾ | V _{SS} - 0.3 | V _{DD} + 3.6 | V |
| | Input voltage on other I/O | V _{SS} - 0.3 | 3.6 | V |
| ΔV _{DDx} | Variations between different VDD power pins | — | 50 | mV |
| V _{SSx} - V _{SS} | Variations between different ground pins | — | 50 | mV |
| I _O | Maximum current for GPIO pins | — | ±25 | mA |
| T _A | Operating temperature range | -40 | +85 | °C |
| P _D | Power dissipation at T _A = 85°C of LQFP144 | — | 820 | mW |
| | Power dissipation at T _A = 85°C of LQFP100 | — | 697 | |
| | Power dissipation at T _A = 85°C of LQFP64 | — | 647 | |
| T _{STG} | Storage temperature range | -65 | +150 | °C |
| T _J | Maximum junction temperature | — | 125 | °C |

(1) Guaranteed by design, not tested in production.

(2) All main power and ground pins should be connected to an external power source within the allowable range.

(3) V_{IN} maximum value cannot exceed 5.5 V.

(4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

4.2. Operating conditions characteristics

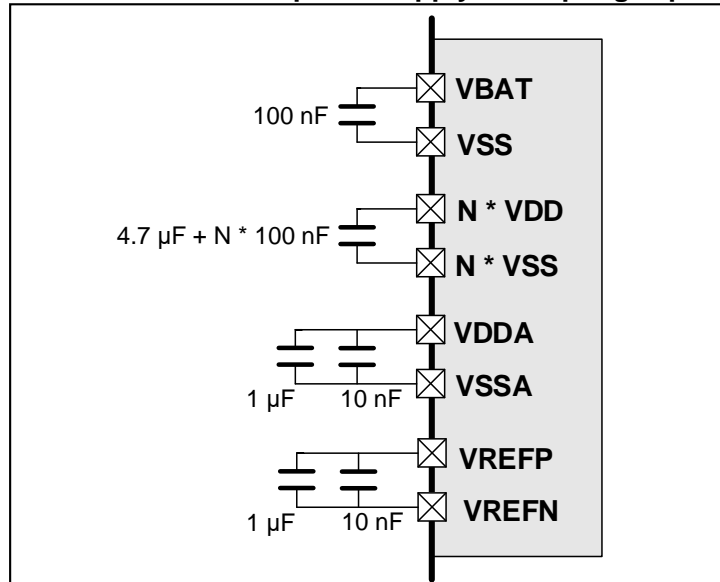
Table 4-2. DC operating conditions

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|------------------|------------------------|-------------------------|--------------------|-----|--------------------|------|
| V _{DD} | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| V _{DDA} | Analog supply voltage | Same as V _{DD} | 2.6 | 3.3 | 3.6 | V |
| V _{BAT} | Battery supply voltage | — | 1.8 ⁽²⁾ | — | 3.6 | V |

(1) Based on characterization, not tested in production.

(2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

Figure 4-1. Recommended power supply decoupling capacitors⁽¹⁾⁽²⁾



- (1) The VREFP and VREFN pins are only available on no less than 100-pin packages, or else the VREFP and VREFN pins are not available and internally connected to VDDA and VSSA pins. More details refer to **AN076 GD32F10x Hardware Development Guide**.
- (2) All decoupling capacitors need to be as close as possible to the pin on the PCB board.

Table 4-3. Clock frequency⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|----------------------|------------|-----|-----|------|
| f _{HCLK} | AHB clock frequency | — | — | 108 | MHz |
| f _{APB1} | APB1 clock frequency | — | — | 54 | MHz |
| f _{APB2} | APB2 clock frequency | — | — | 108 | MHz |

- (1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--------------------------------|------------|-----|-----|-------|
| t _{VDD} | V _{DD} rise time rate | — | 0 | ∞ | μs/ V |
| | V _{DD} fall time rate | | 20 | ∞ | |

- (1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Conditions | Typ | Unit |
|-----------------------|---------------|-------------------------|-----|------|
| t _{start-up} | Start-up time | Clock source from HXTAL | 132 | ms |
| | | Clock source from IRC8M | 132 | |

- (1) Based on characterization, not tested in production.
- (2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.
- (3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics⁽¹⁾⁽²⁾

| Symbol | Parameter | Typ | Unit |
|-------------------------|---|-----|------|
| t _{Sleep} | Wakeup from Sleep mode | 4.5 | μs |
| t _{Deep-sleep} | Wakeup from Deep-sleep mode (LDO On) | 6 | |
| | Wakeup from Deep-sleep mode (LDO in low power mode) | 6 | |
| t _{Standby} | Wakeup from Standby mode | 119 | ms |

- (1) Based on characterization, not tested in production.
 (2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD} = V_{DDA} = 3.3\text{ V}$, IRC8M = System clock = 8 MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾⁽⁶⁾

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|-----------------------------------|------------------------------|---|-----|--------------------|-----|------|
| I _{DD} +I _{DDA} | Supply current (Run mode) | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, All peripherals enabled | — | 63.8 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, All peripherals disabled | — | 37.6 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, All peripherals enabled | — | 57.1 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, All peripherals disabled | — | 33.8 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled | — | 43.6 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled | — | 26.2 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled | — | 30.2 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled | — | 18.6 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled | — | 23.4 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled | — | 14.8 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled | — | 16.7 | — | mA |



| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--------|-----------------------------|--|-----|--------------------|-----|------|
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled | — | 10.9 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled | — | 12.1 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled | — | 8 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled | — | 7.4 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled | — | 5.4 | — | mA |
| | Supply current (Sleep mode) | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled | — | 38.7 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled | — | 9.1 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled | — | 34.7 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled | — | 8.4 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 72 MHz, CPU clock off, All peripherals enabled | — | 26.9 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 72 MHz, CPU clock off, All peripherals disabled | — | 6.7 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled | — | 18.6 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled | — | 5.5 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled | — | 14.7 | — | mA |



| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|---|--|---|--|--------------------|-----|------|
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled | — | 4.8 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 24 MHz, CPU clock off, All peripherals enabled | — | 10.8 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 24 MHz, CPU clock off, All peripherals disabled | — | 4.2 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 16 MHz, CPU clock off, All peripherals enabled | — | 8.1 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 16 MHz, CPU clock off, All peripherals disabled | — | 3.7 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled | — | 5.5 | — | mA |
| | | V _{DD} = V _{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled | — | 3.3 | — | mA |
| | | Supply current (Deep-Sleep mode) | V _{DD} = V _{DDA} = 3.3 V, LDO in normal power mode, IRC40K off, RTC off, All GPIOs analog mode | — | 585 | — |
| V _{DD} = V _{DDA} = 3.3 V, LDO in low power mode, IRC40K off, RTC off, All GPIOs analog mode | — | | 573 | — | μA | |
| Supply current (Standby mode) | V _{DD} = V _{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on | — | 7.8 | — | μA | |
| | V _{DD} = V _{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off | — | 7.4 | — | μA | |
| | V _{DD} = V _{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off | — | 6.2 | — | μA | |
| I _{BAT} | Battery supply current (Backup mode) | V _{DD} off, V _{DDA} off, V _{BAT} = 3.6 V, LXTAL on with external crystal, RTC on | — | 16.6 | — | μA |
| | | V _{DD} off, V _{DDA} off, V _{BAT} = 3.3 V, LXTAL on with external crystal, RTC on | — | 12.6 | — | μA |
| | | V _{DD} off, V _{DDA} off, V _{BAT} = 2.6 V, LXTAL on with external crystal, RTC on | — | 5.9 | — | μA |
| | | V _{DD} off, V _{DDA} off, V _{BAT} = 1.8 V, LXTAL on with external crystal, RTC on | — | 2 | — | μA |

(1) Based on characterization, not tested in production.

- (2) Unless otherwise specified, all values given for $T_A = 25\text{ }^\circ\text{C}$ and test result is mean value.
- (3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.
- (4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.
- (5) When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.
- (6) All GPIOs are configured as analog mode except standby mode.

Figure 4-2. Typical supply current consumption in Run mode

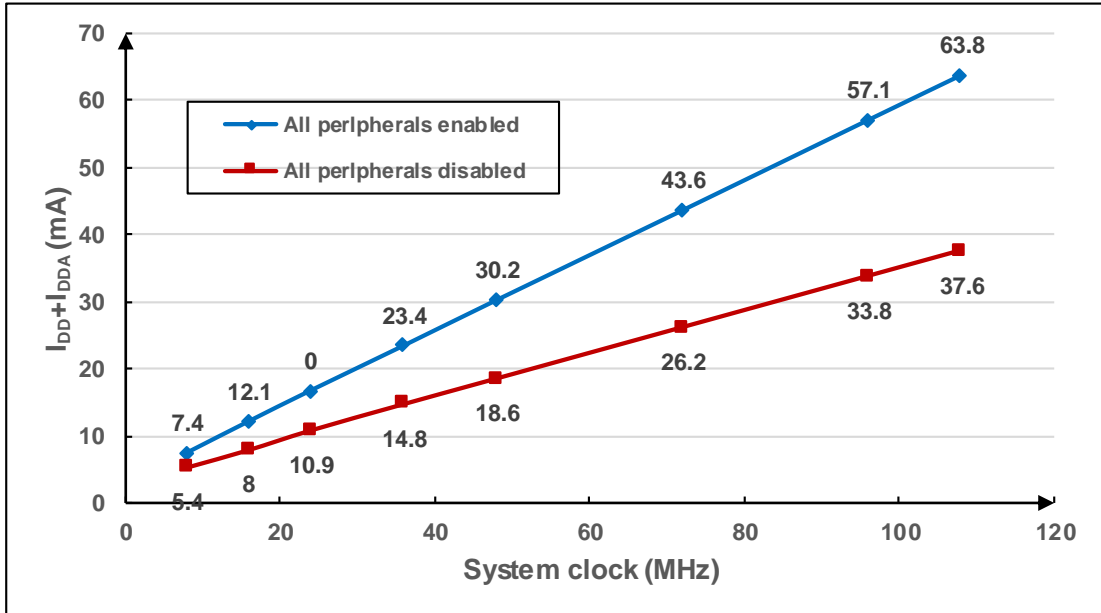
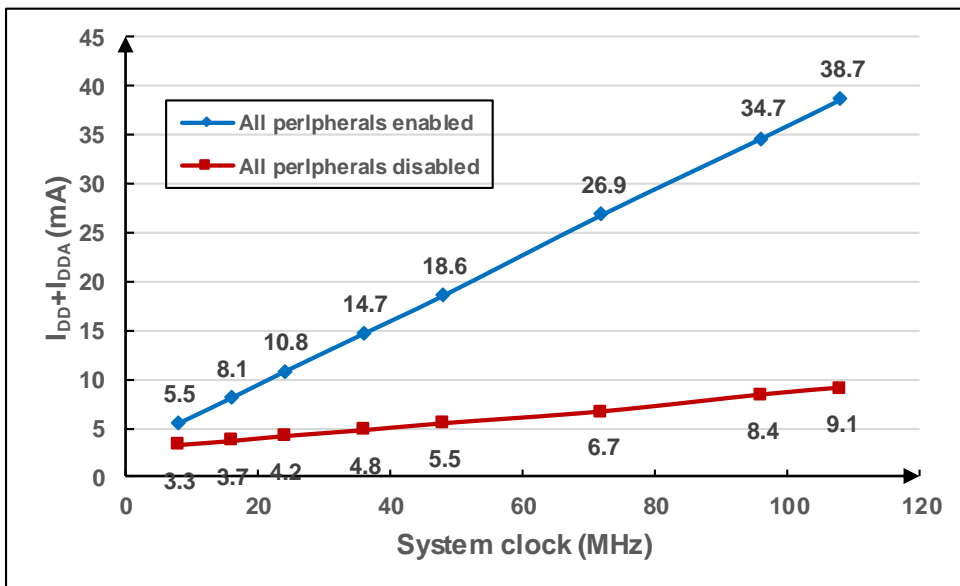


Figure 4-3. Typical supply current consumption in Sleep mode



4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in [Table 4-8. EMS characteristics](#), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-8. EMS characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Level/Class |
|------------------|--|--|-------------|
| V _{ESD} | Voltage applied to all device pins to induce a functional disturbance | V _{DD} = 3.3 V, T _A = 25 °C LQFP144, f _{HCLK} = 108 MHz conforms to IEC 61000-4-2 | 3B |
| V _{FTB} | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and VSS pins | V _{DD} = 3.3 V, T _A = 25 °C LQFP144, f _{HCLK} = 108 MHz conforms to IEC 61000-4-4 | 4A |

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-9. Power supply supervisor characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|--------------------------------------|-------------------------------|-----|------|-----|------|
| V _{LVD} ⁽¹⁾ | Low voltage Detector level selection | LVDT<2:0> = 000(rising edge) | — | 2.19 | — | V |
| | | LVDT<2:0> = 000(falling edge) | — | 2.08 | — | |
| | | LVDT<2:0> = 001(rising edge) | — | 2.29 | — | |
| | | LVDT<2:0> = 001(falling edge) | — | 2.19 | — | |
| | | LVDT<2:0> = 010(rising edge) | — | 2.39 | — | |
| | | LVDT<2:0> = 010(falling edge) | — | 2.29 | — | |
| | | LVDT<2:0> = 011(rising edge) | — | 2.5 | — | |
| | | LVDT<2:0> = 011(falling edge) | — | 2.39 | — | |
| | | LVDT<2:0> = 100(rising edge) | — | 2.6 | — | |
| | | LVDT<2:0> = 100(falling edge) | — | 2.48 | — | |
| | | LVDT<2:0> = 101(rising edge) | — | 2.68 | — | |
| | | LVDT<2:0> = 101(falling edge) | — | 2.58 | — | |
| | | LVDT<2:0> = 110(rising edge) | — | 2.79 | — | |
| | | LVDT<2:0> = 110(falling edge) | — | 2.68 | — | |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|----------------------------|-------------------------------|-----|------|-----|------|
| | | LVDT<2:0> = 111(rising edge) | — | 2.89 | — | |
| | | LVDT<2:0> = 111(falling edge) | — | 2.78 | — | |
| V _{LVDhyst} ⁽²⁾ | LVD hysteresis | — | — | 100 | — | mV |
| V _{POR} ⁽¹⁾ | Power on reset threshold | — | — | 2.40 | — | V |
| V _{PDR} ⁽¹⁾ | Power down reset threshold | | — | 1.85 | — | V |
| V _{PDRhyst} ⁽²⁾ | PDR hysteresis | | — | 550 | — | mV |
| t _{RSTEMPO} ⁽²⁾ | Reset temporization | | — | 2 | — | ms |

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-10. ESD characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---|---------------------------------------|-----|-----|------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A =25 °C; JS-001-2014 | — | — | 3000 | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | T _A =25 °C; JS-002-2014 | — | — | 500 | V |

- (1) Based on characterization, not tested in production.

Table 4-11. Static latch-up characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|----------------------------------|-------------------------------|-----|-----|------|------|
| LU | I-test | T _A =25 °C; JESD78 | — | — | ±100 | mA |
| | V _{supply} over voltage | | — | — | 5.4 | V |

- (1) Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-12. High speed external clock (HXTAL) generated from a crystal/ceramic

characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|--|---|-----|------|-----|------------|
| $f_{\text{HXTAL}}^{(1)}$ | Crystal or ceramic frequency | $2.6 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | 3 | 8 | 25 | MHz |
| $R_{\text{F}}^{(2)}$ | Feedback resistor | $V_{\text{DD}} = 3.3 \text{ V}$ | — | 400 | — | k Ω |
| $C_{\text{HXTAL}}^{(2)(3)}$ | Recommended load capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| $\text{Ducy}_{(\text{HXTAL})}^{(2)}$ | Crystal or ceramic duty cycle | — | 30 | 50 | 70 | % |
| $g_{\text{m}}^{(2)}$ | Oscillator transconductance | Startup | — | 35 | — | mA/V |
| $I_{\text{DDHXTAL}}^{(1)}$ | Crystal or ceramic operating current | $V_{\text{DD}} = 3.3 \text{ V}$, $T_{\text{A}} = 25 \text{ }^{\circ}\text{C}$ | — | 1.6 | — | mA |
| $t_{\text{SUHXTAL}}^{(1)}$ | Crystal or ceramic startup time | $V_{\text{DD}} = 3.3 \text{ V}$, $T_{\text{A}} = 25 \text{ }^{\circ}\text{C}$ | — | 0.65 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{\text{HXTAL1}} = C_{\text{HXTAL2}} = 2 \cdot (C_{\text{LOAD}} - C_{\text{S}})$, For C_{HXTAL1} and C_{HXTAL2} , it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_{S} , it is PCB and MCU pin stray capacitance.

Table 4-13. High speed external clock characteristics (HXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------------|---|---|---------------------|-----|---------------------|------|
| $f_{\text{HXTAL_ext}}^{(1)}$ | External clock source or oscillator frequency | $2.6 \text{ V} \leq V_{\text{DD}} \leq 3.6 \text{ V}$ | 1 | — | 50 | MHz |
| $V_{\text{HXTALH}}^{(2)}$ | OSCIN input pin high level voltage | $V_{\text{DD}} = 3.3 \text{ V}$ | $0.7 V_{\text{DD}}$ | — | V_{DD} | V |
| $V_{\text{HXTALL}}^{(2)}$ | OSCIN input pin low level voltage | | V_{SS} | — | $0.3 V_{\text{DD}}$ | V |
| $t_{\text{H/L(HXTAL)}}^{(2)}$ | OSCIN high or low time | — | 5 | — | — | ns |
| $t_{\text{R/F(HXTAL)}}^{(2)}$ | OSCIN rise or fall time | — | — | — | 10 | ns |
| $C_{\text{IN}}^{(2)}$ | OSCIN input capacitance | — | — | 5 | — | pF |
| $\text{Ducy}_{(\text{HXTAL})}^{(2)}$ | Duty cycle | — | 40 | — | 60 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-14. Low speed external clock (LXTAL) generated from a crystal/ceramic

characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--|-------------------------|-----|--------|-----|-----------------|
| $f_{LXTAL}^{(1)}$ | Crystal or ceramic frequency | $V_{DD} = 3.3\text{ V}$ | — | 32.768 | — | kHz |
| $C_{LXTAL}^{(2)(3)}$ | Recommended matching capacitance on OSC32IN and OSC32OUT | — | — | 10 | — | pF |
| $D_{ucy(LXTAL)}^{(2)}$ | Crystal or ceramic duty cycle | — | 30 | — | 70 | % |
| $g_m^{(2)}$ | Oscillator transconductance | — | — | 23 | — | $\mu\text{A/V}$ |
| $I_{DDLXTAL}^{(1)}$ | Crystal or ceramic operating current | — | — | 11.6 | — | μA |
| $t_{SULXTAL}^{(1)(4)}$ | Crystal or ceramic startup time | — | — | 0.39 | — | s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2 * (C_{LOAD} - C_s)$, For C_{LXTAL1} and C_{LXTAL2} , it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_s , it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flag is SET. This value varies significantly with the crystal manufacturer.

Table 4-15. Low speed external user clock characteristics (LXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|-------------------------|--------------|--------|--------------|------|
| $f_{LXTAL_ext}^{(1)}$ | External clock source or oscillator frequency | $V_{DD} = 3.3\text{ V}$ | — | 32.768 | 1000 | kHz |
| $V_{LXTALH}^{(2)}$ | OSC32IN input pin high level voltage | — | $0.7 V_{DD}$ | — | V_{DD} | V |
| $V_{LXTALL}^{(2)}$ | OSC32IN input pin low level voltage | — | V_{SS} | — | $0.3 V_{DD}$ | |
| $t_{H/L(LXTAL)}^{(2)}$ | OSC32IN high or low time | — | 450 | — | — | ns |
| $t_{R/F(LXTAL)}^{(2)}$ | OSC32IN rise or fall time | — | — | — | 50 | |
| $C_{IN}^{(2)}$ | OSC32IN input capacitance | — | — | 5 | — | pF |
| $D_{ucy(LXTAL)}^{(2)}$ | Duty cycle | — | 30 | 50 | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.



4.8. Internal clock characteristics

Table 4-16. High speed internal clock (IRC8M) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|---|------|------|------|---------------|
| f_{IRC8M} | High Speed Internal Oscillator (IRC8M) frequency | $V_{DD} = V_{DDA} = 3.3\text{ V}$ | — | 8 | — | MHz |
| ACC_{IRC8M} | IRC8M oscillator Frequency accuracy, Factory-trimmed | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = -40\text{ °C} \sim +85\text{ °C}^{(1)}$ | -2.5 | — | 2.5 | % |
| | | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ °C}$ | -1.0 | — | +1.0 | % |
| | IRC8M oscillator Frequency accuracy, User trimming step ⁽¹⁾ | — | — | 0.5 | — | % |
| $Ducy_{IRC8M}^{(2)}$ | IRC8M oscillator duty cycle | $V_{DD} = V_{DDA} = 3.3\text{ V}$ | 45 | 50 | 55 | % |
| $I_{DDAIRC8M}^{(1)}$ | IRC8M oscillator operating current | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ °C}$ | — | 62 | — | μA |
| $t_{SUIRC8M}^{(1)}$ | IRC8M oscillator startup time | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ °C}$ | — | 0.64 | — | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-17. Low speed internal clock (IRC40K) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|---|-----|-----|-----|---------------|
| $f_{IRC40K}^{(1)}$ | Low Speed Internal oscillator (IRC40K) frequency | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = -40\text{ °C} \sim +85\text{ °C}$ | — | 40 | — | kHz |
| $I_{DDAIRC40K}^{(2)}$ | IRC40K oscillator operating current | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ °C}$ | — | 1.2 | — | μA |
| $t_{SUIRC40K}^{(2)}$ | IRC40K oscillator startup time | $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ °C}$ | — | 124 | — | μs |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

4.9. PLL characteristics

Table 4-18. PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--------------------------------|------------|-----|-----|-----|---------------|
| $f_{PLLIN}^{(1)}$ | PLL input clock frequency | — | 1 | — | 25 | MHz |
| $f_{PLLOUT}^{(2)}$ | PLL output clock frequency | — | 16 | — | 108 | MHz |
| $f_{VCO}^{(2)}$ | PLL VCO output clock frequency | — | 32 | — | 216 | MHz |
| $t_{LOCK}^{(2)}$ | PLL lock time | — | — | — | 300 | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-19. PLL1 characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--------------------------------|------------|-----|-----|-----|---------|
| $f_{PLLIN}^{(1)}$ | PLL input clock frequency | — | 1 | — | 25 | MHz |
| $f_{PLLOUT}^{(2)}$ | PLL output clock frequency | — | 16 | — | 120 | MHz |
| $f_{VCO}^{(2)}$ | PLL VCO output clock frequency | — | 32 | — | 200 | MHz |
| $t_{LOCK}^{(2)}$ | PLL lock time | — | — | — | 300 | μ s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-20. PLL2 characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|--------------------------------|------------|-----|-----|-----|---------|
| $f_{PLLIN}^{(1)}$ | PLL input clock frequency | — | 1 | — | 25 | MHz |
| $f_{PLLOUT}^{(2)}$ | PLL output clock frequency | — | 16 | — | 120 | MHz |
| $f_{VCO}^{(2)}$ | PLL VCO output clock frequency | — | 32 | — | 200 | MHz |
| $t_{LOCK}^{(2)}$ | PLL lock time | — | — | — | 300 | μ s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.10. Memory characteristics

Table 4-21. Flash memory characteristics

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|--------------------|---|--|--------------------|--------------------|------------------------|---------|
| $P_{E}CYC$ | Number of guaranteed program /erase cycles before failure (Endurance) | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | 100 | — | — | kcycles |
| t_{RET} | Data retention time | — | — | 20 | — | years |
| t_{PROG} | Word programming time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 37.5 | 105/170 ⁽³⁾ | μ s |
| t_{ERASE} | Page erase time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 50 | 400/500 ⁽⁴⁾ | ms |
| $t_{MERASE(64K)}$ | Mass erase time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 0.6 | 6 | s |
| $t_{MERASE(128K)}$ | Mass erase time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 1.2 | 12 | s |
| $t_{MERASE(256K)}$ | Mass erase time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 2.4 | 24 | s |
| $t_{MERASE(512K)}$ | Mass erase time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 8 | 64 | s |
| $t_{MERASE(1MB)}$ | Mass erase time | $T_A = -40\text{ }^\circ\text{C} \sim +85\text{ }^\circ\text{C}$ | — | 16 | 128 | s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Flash memory $\leq 256\text{K}$ is 105 μ s and flash memory $>256\text{K}$ is 170 μ s.

(4) Flash memory $\leq 256\text{K}$ is 400 ms and flash memory $>256\text{K}$ is 500 ms.

4.11. NRST pin characteristics

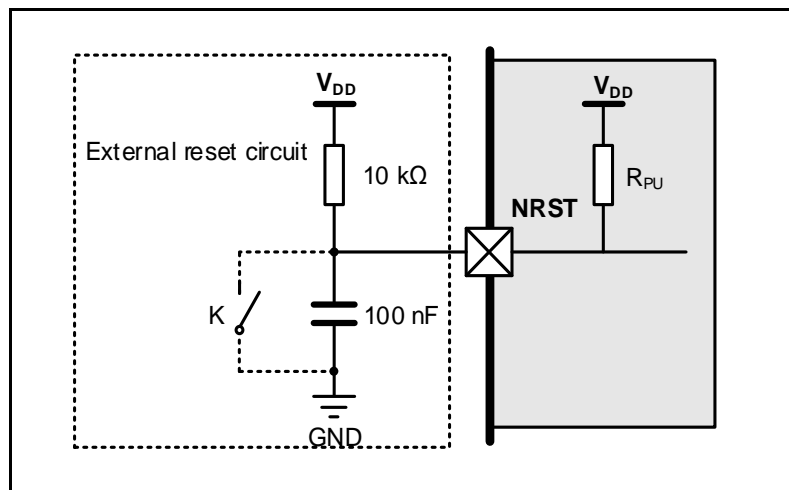
Table 4-22. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|------------------------------------|-----------------------------------|--------------|-----|----------------|------------|
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD} = V_{DDA} = 2.6\text{ V}$ | -0.3 | — | $0.3 V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | $0.7 V_{DD}$ | — | $V_{DD} + 0.3$ | |
| $V_{hyst}^{(1)}$ | Schmidt trigger Voltage hysteresis | | — | 350 | — | |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD} = V_{DDA} = 3.3\text{ V}$ | -0.3 | — | $0.3 V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | $0.7 V_{DD}$ | — | $V_{DD} + 0.3$ | |
| $V_{hyst}^{(1)}$ | Schmidt trigger Voltage hysteresis | | — | 360 | — | |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD} = V_{DDA} = 3.6\text{ V}$ | -0.3 | — | $0.3 V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | $0.7 V_{DD}$ | — | $V_{DD} + 0.3$ | |
| $V_{hyst}^{(1)}$ | Schmidt trigger Voltage hysteresis | | — | 370 | — | |
| $R_{pu}^{(2)}$ | Pull-up equivalent resistor | — | — | 40 | — | k Ω |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit⁽¹⁾



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.12. GPIO characteristics

Table 4-23. I/O port DC characteristics⁽¹⁾⁽³⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--|--|--------------|-----|--------------|------|
| V_{IL} | Standard IO Low level input voltage | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.6\text{ V}$ | — | — | $0.3 V_{DD}$ | V |
| | 5V-tolerant IO Low level input voltage | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.6\text{ V}$ | — | — | $0.3 V_{DD}$ | V |
| V_{IH} | Standard IO Low level input voltage | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.6\text{ V}$ | $0.7 V_{DD}$ | — | — | V |
| | 5V-tolerant IO Low level | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.6\text{ V}$ | $0.7 V_{DD}$ | — | — | V |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-----------------------|--|-------------------------|-----------------------------------|------|-----|------|----|
| | input voltage | | | | | | |
| R _{PU} (2) | Internal pull-up resistor | All pins | V _{IN} = V _{SS} | — | 40 | — | kΩ |
| | | PA10 | — | — | 10 | — | |
| R _{PD} (2) | Internal pull-down resistor | All pins | V _{IN} = V _{DD} | — | 40 | — | kΩ |
| | | PA10 | — | — | 10 | — | |
| IO_Speed=50MHz | | | | | | | |
| V _{OL} | Low level output voltage for an IO Pin (I _{IO} = +8 mA) | V _{DD} = 2.6V | — | 0.27 | — | V | |
| | | V _{DD} = 3.3 V | — | 0.23 | — | | |
| | | V _{DD} = 3.6V | — | 0.22 | — | | |
| | Low level output voltage for an IO Pin (I _{IO} = +12mA) | V _{DD} = 2.6V | — | 0.43 | — | | |
| | | V _{DD} = 3.3 V | — | 0.66 | — | | |
| | Low level output voltage for an IO Pin (I _{IO} = +20 mA) | V _{DD} = 3.6V | — | 0.61 | — | | |
| | | | | | | | |
| V _{OH} | High level output voltage for an IO Pin (I _{IO} = +8 mA) | V _{DD} = 2.6V | — | 2.3 | — | V | |
| | | V _{DD} = 3.3 V | — | 3.05 | — | | |
| | | V _{DD} = 3.6V | — | 3.36 | — | | |
| | High level output voltage for an IO Pin (I _{IO} = +10 mA) | V _{DD} = 2.6V | — | 2.21 | — | | |
| | | V _{DD} = 3.3 V | — | 2.59 | — | | |
| | High level output voltage for an IO Pin (I _{IO} = +20 mA) | V _{DD} = 3.6V | — | 2.95 | — | | |
| | | | | | | | |
| IO_Speed=10MHz | | | | | | | |
| V _{OL} | Low level output voltage for an IO Pin (I _{IO} = +8 mA) | V _{DD} = 2.6V | — | 0.43 | — | V | |
| | | V _{DD} = 3.3 V | — | 0.36 | — | | |
| | | V _{DD} = 3.6V | — | 0.34 | — | | |
| | Low level output voltage for an IO Pin (I _{IO} = +15 mA) | V _{DD} = 2.6V | — | — | — | | |
| | | V _{DD} = 3.3 V | — | 0.78 | — | | |
| | | V _{DD} = 3.6V | — | 0.72 | — | | |
| V _{OH} | High level output voltage for an IO Pin (I _{IO} = +8 mA) | V _{DD} = 2.6V | — | 2.06 | — | V | |
| | | V _{DD} = 3.3 V | — | 2.87 | — | | |
| | | V _{DD} = 3.6V | — | 3.2 | — | | |
| | High level output voltage for an IO Pin (I _{IO} = +15mA) | V _{DD} = 2.6V | — | — | — | | |
| | | V _{DD} = 3.3 V | — | 2.39 | — | | |
| | | V _{DD} = 3.6V | — | 2.77 | — | | |
| IO_Speed=2MHz | | | | | | | |
| V _{OL} | Low level output voltage for an IO Pin (I _{IO} = +4 mA) | V _{DD} = 2.6V | — | 0.44 | — | V | |
| | | V _{DD} = 3.3 V | — | 0.36 | — | | |
| | | V _{DD} = 3.6V | — | 0.34 | — | | |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---|-------------------------|-----|------|-----|------|
| V _{OH} | High level output voltage for an IO Pin (I _O = +4mA) | V _{DD} = 2.6V | — | 2.22 | — | V |
| | | V _{DD} = 3.3 V | — | 2.99 | — | |
| | | V _{DD} = 3.6V | — | 3.31 | — | |

- (1) Based on characterization, not tested in production.
- (2) Guaranteed by design, not tested in production.
- (3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current, the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode (maximum load: 30 pF).

Table 4-24. I/O port AC characteristics⁽¹⁾⁽²⁾⁽⁴⁾

| GPIOx_MDy[1:0] bit value ⁽³⁾ | Parameter | Conditions | Typ | Unit |
|--|--------------------------------------|---|------|------|
| GPIOx_CTL->MDy[1:0]=10 (IO_Speed = 2MHz) | T _{Rise} /T _{Fall} | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 10 pF | 49.2 | ns |
| | | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 30 pF | 60 | |
| | | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 50 pF | 70.4 | |
| GPIOx_CTL->MDy[1:0] = 01 (IO_Speed = 10MHz) | T _{Rise} /T _{Fall} | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 10 pF | 23.4 | ns |
| | | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 30 pF | 27 | |
| | | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 50 pF | 32 | |
| GPIOx_CTL->MDy[1:0]=11 (IO_Speed = 50MHz) | T _{Rise} /T _{Fall} | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 10 pF | 3.3 | ns |
| | | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 30 pF | 3.5 | |
| | | 2.6 ≤ V _{DD} ≤ 3.6 V, C _L = 50 pF | 3.6 | |

- (1) Based on characterization, not tested in production.
- (2) Unless otherwise specified, all test results given for T_A = 25 °C.
- (3) The I/O speed is configured using the GPIOx_CTL->MDy[1:0] bits.
- (4) Only for reference, Depending on user's design.

4.13. Temperature sensor characteristics

Table 4-25. Temperature sensor characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------------------|--|-----|------|-----|-------|
| T _L | V _{SENSE} linearity with temperature | — | ±1.5 | — | °C |
| Avg_Slope | Average slope | — | 4.1 | — | mV/°C |
| V ₂₅ | Voltage at 25 °C | — | 1.45 | — | V |
| t _{S_temp} ⁽²⁾ | ADC sampling time when reading the temperature | — | 17.1 | — | µs |

- (1) Based on characterization, not tested in production.
- (2) Shortest sampling time can be determined in the application by multiple iterations.

4.14. ADC characteristics

Table 4-26. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------------|----------------------------|-------------------------|-----|-----|-------------------|------|
| V _{DDA} ⁽¹⁾ | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| V _{IN} ⁽¹⁾ | ADC input voltage range | 16 external; 2 internal | 0 | — | V _{REFP} | V |
| V _{REFP} ⁽²⁾ | Positive Reference Voltage | — | 2.6 | — | V _{DDA} | V |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------------|--|---------------------------------|------|------------------|-------|--------------------|
| V _{REFN} ⁽²⁾ | Negative Reference Voltage | — | — | V _{SSA} | — | V |
| f _{ADC} ⁽¹⁾ | ADC clock | — | 0.6 | — | 14 | MHz |
| f _S ⁽¹⁾ | Sampling rate | 12-bit | 0.04 | — | 1 | MSPS |
| R _{AIN} ⁽²⁾ | External input impedance | See Equation 1 | — | — | 219.8 | kΩ |
| R _{ADC} ⁽²⁾ | Input sampling switch resistance | — | — | — | 0.5 | kΩ |
| C _{ADC} ⁽²⁾ | Input sampling capacitance | No pin/pad capacitance included | — | — | 8 | pF |
| t _{CAL} ⁽²⁾ | Calibration time | f _{ADC} = 14 MHz | — | 7.28 | — | μs |
| t _S ⁽²⁾ | Sampling time | f _{ADC} = 14 MHz | 0.11 | — | 17.11 | μs |
| t _{CONV} ⁽²⁾ | Total conversion time(including sampling time) | 12-bit | — | 14 | — | 1/f _{ADC} |
| t _{SU} ⁽²⁾ | Startup time | — | — | — | 1 | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Equation 1: R_{AIN max} formula $R_{AIN} < \frac{T_s}{f_{ADC} \cdot C_{ADC} \cdot \ln(2^{N+2})} - R_{ADC}$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 4-27. ADC R_{AIN max} for f_{ADC} = 14 MHz

| T _s (cycles) | t _s (μs) | R _{AIN max} (kΩ) |
|-------------------------|---------------------|---------------------------|
| 1.5 | 0.11 | 0.8 |
| 7.5 | 0.54 | 6.4 |
| 13.5 | 0.96 | 11.9 |
| 28.5 | 2.04 | 25.7 |
| 41.5 | 2.96 | 37.6 |
| 55.5 | 3.96 | 50.5 |
| 71.5 | 5.11 | 65.2 |
| 239.5 | 17.11 | 219.8 |

4.15. DAC characteristics

Table 4-28. DAC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------------|----------------------------|------------|-----|-----|------------------|------|
| V _{DDA} ⁽¹⁾ | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| V _{REFP} ⁽²⁾ | Positive Reference Voltage | — | 2.6 | — | V _{DDA} | V |



| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|---|-----|-----------|----------------|------------|
| $V_{REFN}^{(2)}$ | Negative Reference Voltage | — | — | V_{SSA} | — | V |
| $R_{LOAD}^{(2)}$ | Load resistance | Resistive load with buffer ON | 5 | — | — | k Ω |
| $R_o^{(2)}$ | Impedance output with buffer OFF | — | — | — | 15 | k Ω |
| $C_{LOAD}^{(2)}$ | Load capacitance | No pin/pad capacitance included | — | — | 50 | pF |
| $DAC_OUT_{min}^{(2)}$ | Lower DAC_OUT voltage with buffer ON | — | 0.2 | — | — | V |
| $DAC_OUT_{max}^{(2)}$ | Higher DAC_OUT voltage with buffer ON | — | — | — | $V_{DDA}-0.2$ | V |
| $DAC_OUT_{min}^{(2)}$ | Lower DAC_OUT voltage with buffer OFF | — | — | 0.5 | — | mV |
| $DAC_OUT_{max}^{(2)}$ | Higher DAC_OUT voltage with buffer OFF | — | — | — | $V_{DDA}-1LSB$ | V |
| $I_{DDA}^{(1)}$ | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REFP} = 3.6$ V | — | 550 | — | μ A |
| | | With no load, worst code(0xF1C) on the input, $V_{REFP} = 3.6$ V | — | 600 | — | μ A |
| $I_{DDVREFP}^{(1)}$ | DAC current consumption in quiescent mode | With no load, middle code(0x800) on the input, $V_{REFP} = 3.6$ V | — | 86 | — | μ A |
| | | With no load, worst code(0xF1C) on the input, $V_{REFP} = 3.6$ V | — | 298 | — | μ A |
| $T_{setting}^{(1)}$ | Settling time | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω | — | 0.3 | 1 | μ s |
| $T_{wakeup}^{(2)}$ | Wakeup from off state | — | — | 5 | 10 | μ s |
| Update rate ⁽²⁾ | Max frequency for a correct DAC_OUT change from code i to $\pm 1LSBs$ | $C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ k Ω | — | — | 4 | MS/s |
| PSRR ⁽²⁾ | Power supply rejection ratio (to V_{DDA}) | — | 55 | 80 | — | dB |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.16. I2C characteristics

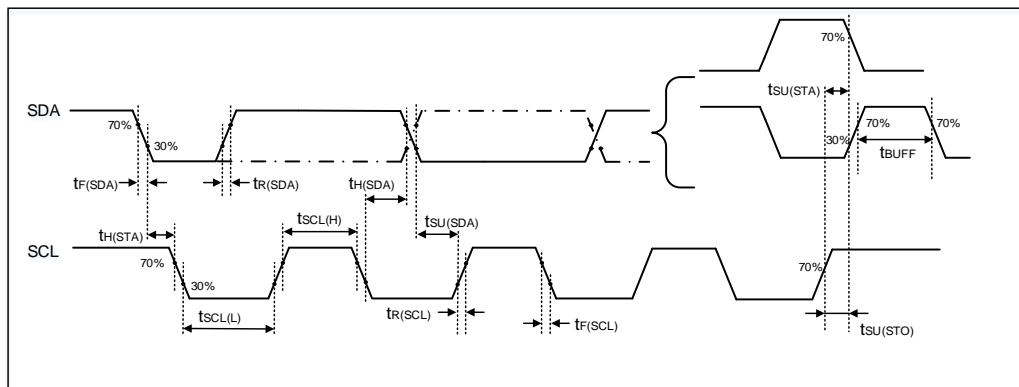
Table 4-29. I2C characteristics⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|--------------|---------------------|------------|---------------|-----|-----------|-----|---------|
| | | | Min | Max | Min | Max | |
| $t_{SCL(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | μ s |

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|------------------|---|------------|------------------|------|-----------|-----|---------------|
| | | | Min | Max | Min | Max | |
| $t_{SCL(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | μs |
| $t_{SU(SDA)}$ | SDA setup time | — | 250 | — | 100 | — | ns |
| $t_H(SDA)$ | SDA data hold time | — | 0 ⁽³⁾ | 3450 | 0 | 900 | ns |
| $t_{R(SDA/SCL)}$ | SDA and SCL rise time | — | — | 1000 | — | 300 | ns |
| $t_{F(SDA/SCL)}$ | SDA and SCL fall time | — | — | 300 | — | 300 | ns |
| $t_H(STA)$ | Start condition hold time | — | 4.0 | — | 0.6 | — | μs |
| $t_{SU(STA)}$ | Repeated Start condition setup time | — | 4.7 | — | 0.6 | — | μs |
| $t_{SU(STO)}$ | Stop condition setup time | — | 4.0 | — | 0.6 | — | μs |
| t_{BUFF} | Stop to Start condition time (bus free) | — | 4.7 | — | 1.3 | — | μs |

- (1) Guaranteed by design, not tested in production.
- (2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz.
- (3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

Figure 4-5. I2C bus timing diagram



4.17. SPI characteristics

Table 4-30. Standard SPI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---------------------|---|-------|-------|-------|------|
| f_{SCK} | SCK clock frequency | — | — | — | 27 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | Master mode, $f_{PCLKx} = 108 \text{ MHz}$, presc = 4 | 35.13 | 37.13 | 39.13 | ns |
| $t_{SCK(L)}$ | SCK clock low time | Master mode, $f_{PCLKx} = 108 \text{ MHz}$, presc = 4 | 35.13 | 37.13 | 39.13 | ns |
| SPI master mode | | | | | | |



| | | | | | | |
|-----------------------|--------------------------|---|---|----|---|----|
| $t_{V(MO)}$ | Data output valid time | — | — | — | 8 | ns |
| $t_{SU(MI)}$ | Data input setup time | — | 1 | — | — | ns |
| $t_{H(MI)}$ | Data input hold time | — | 0 | — | — | ns |
| SPI slave mode | | | | | | |
| $t_{SU(NSS)}$ | NSS enable setup time | — | 0 | — | — | ns |
| $t_{H(NSS)}$ | NSS enable hold time | — | 1 | — | — | ns |
| $t_{A(SO)}$ | Data output access time | — | — | 9 | — | ns |
| $t_{DIS(SO)}$ | Data output disable time | — | — | 11 | — | ns |
| $t_{V(SO)}$ | Data output valid time | — | — | 11 | — | ns |
| $t_{SU(SI)}$ | Data input setup time | — | 0 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | — | 1 | — | — | ns |

(1) Based on characterization, not tested in production.

Figure 4-6. SPI timing diagram - master mode

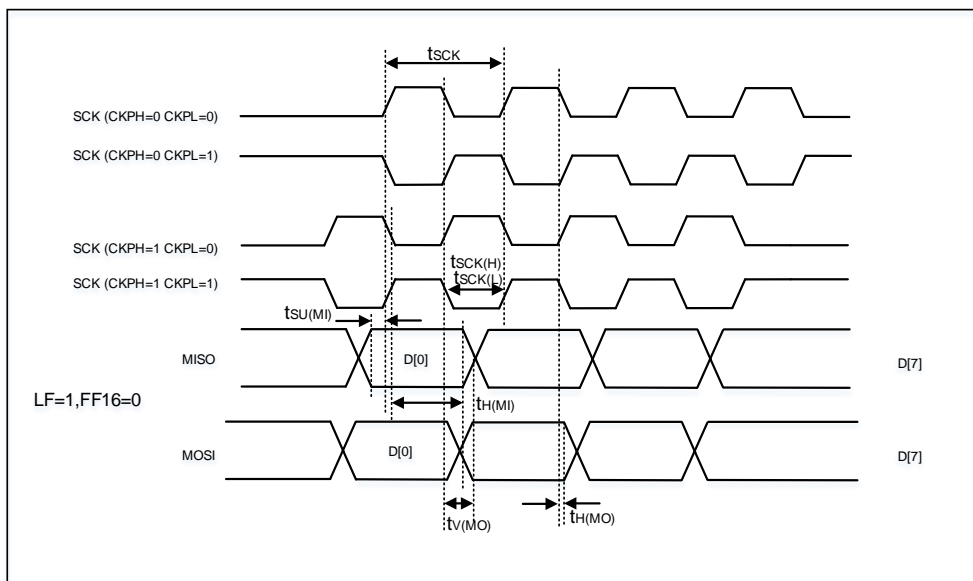
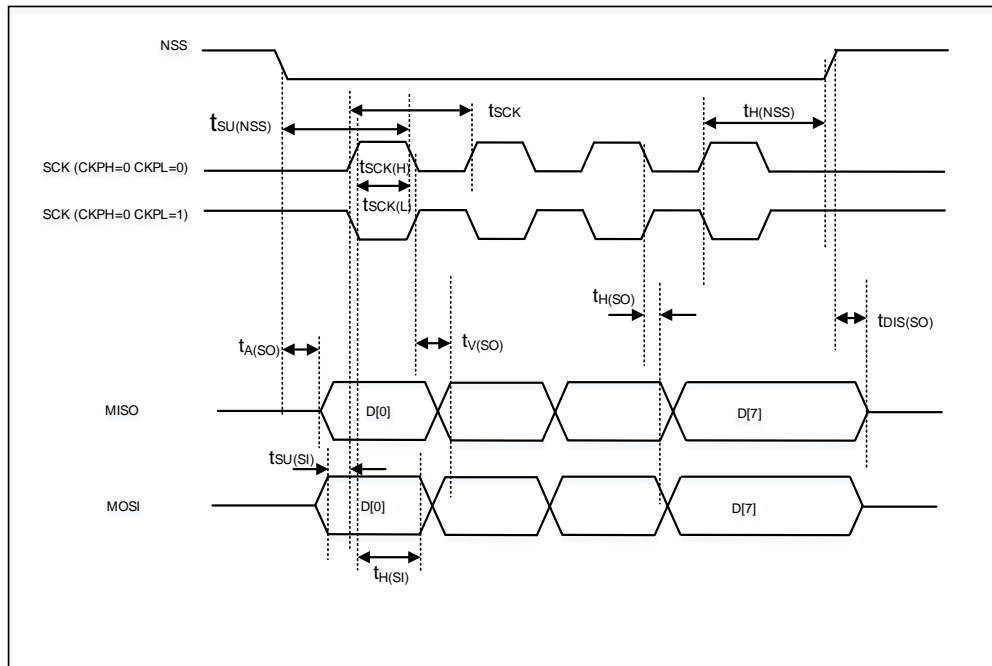


Figure 4-7. SPI timing diagram - slave mode



4.18. I2S characteristics

Table 4-31. I2S characteristics⁽¹⁾⁽²⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|--|-----|------|------|------|
| f_{CK} | Clock frequency | Master mode (data: 32 bits, Audio frequency = 96 kHz) | — | 6.25 | — | MHz |
| | | Slave mode | 0 | — | 12.5 | |
| t_H | Clock high time | — | — | 80 | — | ns |
| t_L | Clock low time | | — | 80 | — | ns |
| $t_{V(WS)}$ | WS valid time | Master mode | — | 3 | — | ns |
| $t_{H(WS)}$ | WS hold time | Master mode | — | 3 | — | ns |
| $t_{SU(WS)}$ | WS setup time | Slave mode | 0 | — | — | ns |
| $t_{H(WS)}$ | WS hold time | Slave mode | 2 | — | — | ns |
| $D_{ucy(SCK)}$ | I2S slave input clock duty cycle | Slave mode | — | 50 | — | % |
| $t_{SU(SD_MR)}$ | Data input setup time | Master mode | 1 | — | — | ns |
| $t_{SU(SD_SR)}$ | Data input setup time | Slave mode | 0 | — | — | ns |
| $t_{H(SD_MR)}$ | Data input hold time | Master receiver | 0 | — | — | ns |
| $t_{H(SD_SR)}$ | | Slave receiver | 1 | — | — | ns |
| $t_{V(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | — | — | 5 | ns |
| $t_{H(SD_ST)}$ | Data output hold time | Slave transmitter | 6 | — | — | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|------------------------|---|-----|-----|-----|------|
| | | (after enable edge) | | | | |
| $t_{V(SD_MT)}$ | Data output valid time | Master transmitter (after enable edge) | — | — | 5 | ns |
| $t_{H(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | — | — | ns |

- (1) Guaranteed by design, not tested in production.
 (2) Based on characterization, not tested in production

Figure 4-8. I2S timing diagram - master mode

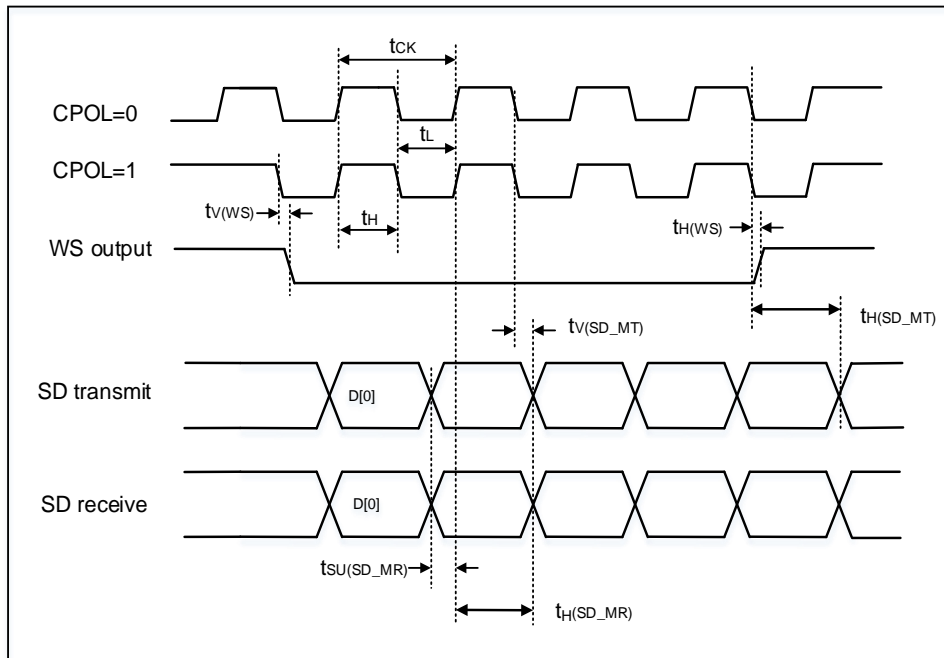
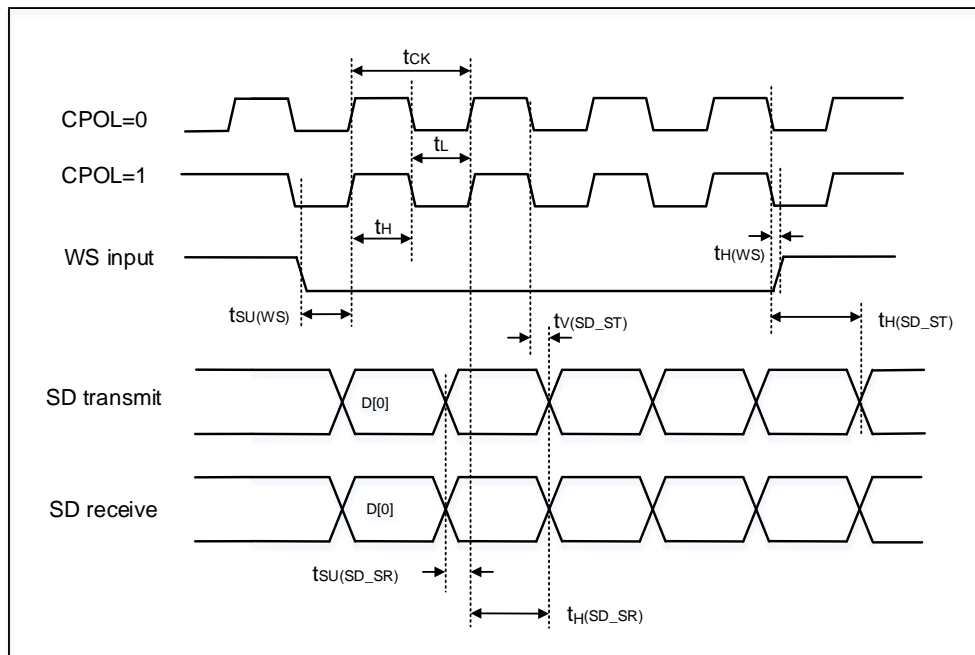


Figure 4-9. I2S timing diagram - slave mode



4.19. USART characteristics

Table 4-32. USART characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---------------------|-------------------------------|------|-----|------|------|
| f_{SCK} | SCK clock frequency | $f_{PCLKX} = 108 \text{ MHz}$ | — | — | 13.5 | MHz |
| $t_{SCK(H)}$ | SCK clock high time | $f_{PCLKX} = 108 \text{ MHz}$ | 37.0 | — | — | ns |
| $t_{SCK(L)}$ | SCK clock low time | $f_{PCLKX} = 108 \text{ MHz}$ | 37.0 | — | — | ns |

(1) Guaranteed by design, not tested in production.

4.20. CAN characteristics

Refer to [Table 4-23. I/O port DC characteristics^{\(1\)}](#) for more details on the input/output alternate function characteristics (CANTX and CANRX).

4.21. USBFS characteristics

Table 4-33. USBFS start up time

| Symbol | Parameter | Max | Unit |
|---------------------|--------------------|-----|---------------|
| $t_{STARTUP}^{(1)}$ | USBFS startup time | 1 | μs |

(1) Guaranteed by design, not tested in production.

Table 4-34. USBFS DC electrical characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|--------------------------------|------------------------|-----------------------------------|--|--------|-------|------|---|
| Input levels ⁽¹⁾ | V _{DD} | USBFS operating voltage | — | 3 | — | 3.6 | V |
| | V _{DI} | Differential input sensitivity | — | 0.2 | — | — | |
| | V _{CM} | Differential common mode range | Includes V _{DI} range | 0.8 | — | 2.5 | |
| | V _{SE} | Single ended receiver threshold | — | 0.8 | — | 2.0 | |
| Output levels ⁽²⁾ | V _{OL} | Static output level low | R _L of 1.0 kΩ to 3.6 V | — | 0.064 | 0.3 | V |
| | V _{OH} | Static output level high | R _L of 15 kΩ to V _{SS} | 2.8 | 3.3 | 3.6 | |
| R _{PD} ⁽²⁾ | PA 11, PA12(USB_DM/DP) | V _{IN} = V _{DD} | 17 | 20.574 | 24 | kΩ | |
| | PA9(USB_VBUS) | | 0.65 | — | 2.0 | | |
| R _{PU} ⁽²⁾ | PA 11, PA12(USB_DM/DP) | V _{IN} = V _{SS} | 1.5 | 1.585 | 2.1 | | |
| | PA9(USB_VBUS) | | 0.25 | 0.326 | 0.55 | | |

(1) Guaranteed by design, not tested in production.

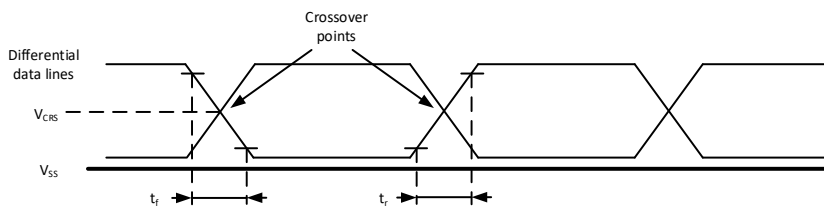
(2) Based on characterization, not tested in production.

Table 4-35. USBFS full speed-electrical characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------------------|---------------------------------|-----|-----|-----|------|
| t _R | Rise time | CL = 50 pF | 4 | — | 20 | ns |
| t _F | Fall time | CL = 50 pF | 4 | — | 20 | ns |
| t _{RFM} | Rise/fall time matching | t _R / t _F | 90 | — | 110 | % |
| V _{CRS} | Output signal crossover voltage | — | 1.3 | — | 2.0 | V |

(1) Guaranteed by design, not tested in production.

Figure 4-10. USBFS timings: definition of data signal rise and fall time



4.2.2. EXMC characteristics

Table 4-36. Synchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Min | Max | Unit |
|--|--------------------------------|------|-----|------|
| t _w (CLK) | EXMC_CLK period | 36.8 | — | ns |
| t _d (CLKL-NExL) | EXMC_CLK low to EXMC_NEx low | 0 | — | ns |
| t _d (CLKH-NExH) | EXMC_CLK high to EXMC_NEx high | 18.4 | — | ns |
| t _d (CLKL-NADV _L) | EXMC_CLK low to EXMC_NADV low | 0 | — | ns |
| t _d (CLKL-NADV _H) | EXMC_CLK low to EXMC_NADV high | 0 | — | ns |
| t _d (CLKL-AV) | EXMC_CLK low to EXMC_Ax valid | 0 | — | ns |



| Symbol | Parameter | Min | Max | Unit |
|--------------------|----------------------------------|------|-----|------|
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 18.4 | — | ns |
| $t_{d(CLKL-NOEL)}$ | EXMC_CLK low to EXMC_NOE low | 0 | — | ns |
| $t_{d(CLKH-NOEH)}$ | EXMC_CLK high to EXMC_NOE high | 18.4 | — | ns |
| $t_{d(CLKL-ADV)}$ | EXMC_CLK low to EXMC_AD valid | 0 | — | ns |
| $t_{d(CLKL-ADIV)}$ | EXMC_CLK low to EXMC_AD invalid | 0 | — | ns |

- (1) $C_L = 30$ pF.
- (2) Guaranteed by design, not tested in production.
- (3) Based on configure: $f_{HCLK} = 108$ MHz, BurstAccessMode = Enable; Memory Type = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); Data Latency = 1.

Table 4-37. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------------|--|------|-----|------|
| $t_w(CLK)$ | EXMC_CLK period | 36.8 | — | ns |
| $t_{d(CLKL-NE\bar{L})}$ | EXMC_CLK low to EXMC_NEx low | 0 | — | ns |
| $t_{d(CLKH-NE\bar{H})}$ | EXMC_CLK high to EXMC_NEx high | 18.4 | — | ns |
| $t_{d(CLKL-NAD\bar{V}L)}$ | EXMC_CLK low to EXMC_NA DV low | 0 | — | ns |
| $t_{d(CLKL-NAD\bar{V}H)}$ | EXMC_CLK low to EXMC_NA DV high | 0 | — | ns |
| $t_{d(CLKL-AV)}$ | EXMC_CLK low to EXMC_Ax valid | 0 | — | ns |
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 18.4 | — | ns |
| $t_{d(CLKL-NWEL)}$ | EXMC_CLK low to EXMC_NWE low | 0 | — | ns |
| $t_{d(CLKH-NWEH)}$ | EXMC_CLK high to EXMC_NWE high | 18.4 | — | ns |
| $t_{d(CLKL-ADIV)}$ | EXMC_CLK low to EXMC_AD invalid | 0 | — | ns |
| $t_{d(CLKL-DATA)}$ | EXMC_A/D valid data after EXMC_CLK low | 0 | — | ns |
| $t_h(CLKL-NBLH)$ | EXMC_CLK low to EXMC_NBL high | 0 | — | ns |

- (1) $C_L = 30$ pF.
- (2) Guaranteed by design, not tested in production.
- (3) Based on configure: $f_{HCLK} = 108$ MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-38. Synchronous non-multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------------|----------------------------------|------|-----|------|
| $t_w(CLK)$ | EXMC_CLK period | 36.8 | — | ns |
| $t_{d(CLKL-NE\bar{L})}$ | EXMC_CLK low to EXMC_NEx low | 0 | — | ns |
| $t_{d(CLKH-NE\bar{H})}$ | EXMC_CLK high to EXMC_NEx high | 18.4 | — | ns |
| $t_{d(CLKL-NAD\bar{V}L)}$ | EXMC_CLK low to EXMC_NA DV low | 0 | — | ns |
| $t_{d(CLKL-NAD\bar{V}H)}$ | EXMC_CLK low to EXMC_NA DV high | 0 | — | ns |
| $t_{d(CLKL-AV)}$ | EXMC_CLK low to EXMC_Ax valid | 0 | — | ns |
| $t_{d(CLKH-AIV)}$ | EXMC_CLK high to EXMC_Ax invalid | 18.4 | — | ns |
| $t_{d(CLKL-NOEL)}$ | EXMC_CLK low to EXMC_NOE low | 0 | — | ns |
| $t_{d(CLKH-NOEH)}$ | EXMC_CLK high to EXMC_NOE high | 18.4 | — | ns |

- (1) $C_L = 30$ pF.
- (2) Guaranteed by design, not tested in production.
- (3) Based on configure: HCLK=108 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

Table 4-39. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Min | Max | Unit |
|---------------------------|--|------|-----|------|
| $t_{w(CLK)}$ | EXMC_CLK period | 36.8 | — | ns |
| $t_{d(CLKL-NE\bar{x}L)}$ | EXMC_CLK low to EXMC_NEx low | 0 | — | ns |
| $t_{d(CLKH-NE\bar{x}H)}$ | EXMC_CLK high to EXMC_NEx high | 18.4 | — | ns |
| $t_{d(CLKL-NAD\bar{V}L)}$ | EXMC_CLK low to EXMC_NA DV low | 0 | — | ns |
| $t_{d(CLKL-NAD\bar{V}H)}$ | EXMC_CLK low to EXMC_NA DV high | 0 | — | ns |
| $t_{d(CLKL-A\bar{V})}$ | EXMC_CLK low to EXMC_Ax valid | 0 | — | ns |
| $t_{d(CLKH-A\bar{I}V)}$ | EXMC_CLK high to EXMC_Ax invalid | 18.4 | — | ns |
| $t_{d(CLKL-NW\bar{E}L)}$ | EXMC_CLK low to EXMC_NWE low | 0 | — | ns |
| $t_{d(CLKH-NW\bar{E}H)}$ | EXMC_CLK high to EXMC_NWE high | 18.4 | — | ns |
| $t_{d(CLKL-DATA)}$ | EXMC_A/D valid data after EXMC_CLK low | 0 | — | ns |
| $t_{h(CLKL-NBLH)}$ | EXMC_CLK low to EXMC_NBL high | 0 | — | ns |

(1) $C_L = 30$ pF.

(2) Guaranteed by design, not tested in production.

(3) Based on configure: HCLK = 108 MHz, BurstAccessMode = Enable; MemoryType = PSRAM; WriteBurst = Enable; CLKDivision = 3 (EXMC_CLK is 4 divided by HCLK); DataLatency = 1.

4.23. TIMER characteristics

Table 4-40. TIMER characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---|---------------------------|--------|----------------------|-----------------|
| t_{res} | Timer resolution time | — | 1 | — | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK} = 108$ MHz | 9.3 | — | ns |
| f_{EXT} | Timer external clock frequency | — | 0 | $f_{TIMERxCLK}/2$ | MHz |
| | | $f_{TIMERxCLK} = 108$ MHz | 0 | 54 | MHz |
| RES | Timer resolution | — | — | 16 | bit |
| $t_{COUNTER}$ | 16-bit counter clock period when internal clock is selected | — | 1 | 65536 | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK} = 108$ MHz | 0.0093 | 607 | μ s |
| t_{MAX_COUNT} | Maximum possible count | — | — | 65536×65536 | $t_{TIMERxCLK}$ |
| | | $f_{TIMERxCLK} = 108$ MHz | — | 39.8 | s |

(1) Guaranteed by design, not tested in production.

4.24. WDG_T characteristics

Table 4-41. FWDGT min/max timeout period at 40 kHz (IRC40K)⁽¹⁾

| Prescaler divider | PR[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFF | Unit |
|-------------------|--------------|-------------------------------|-------------------------------|------|
| 1/4 | 000 | 0.025 | 409.525 | ms |
| 1/8 | 001 | 0.025 | 819.025 | |
| 1/16 | 010 | 0.025 | 1638.025 | |
| 1/32 | 011 | 0.025 | 3276.025 | |



| Prescaler divider | PR[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFF | Unit |
|-------------------|--------------|----------------------------------|----------------------------------|------|
| 1/64 | 100 | 0.025 | 6552.025 | |
| 1/128 | 101 | 0.025 | 13104.025 | |
| 1/256 | 110 or 111 | 0.025 | 26208.025 | |

(1) Guaranteed by design, not tested in production.

Table 4-42. WWDGT min-max timeout value at 54 MHz (f_{PCLK1})⁽¹⁾

| Prescaler divider | PSC[2:0] | Min timeout value CNT[6:0] = 0x40 | Unit | Max timeout value CNT[6:0] = 0x7F | Unit |
|-------------------|----------|--------------------------------------|------|--------------------------------------|------|
| 1/1 | 00 | 75.8 | μs | 4.8 | ms |
| 1/2 | 01 | 151.7 | | 9.7 | |
| 1/4 | 10 | 303.4 | | 19.4 | |
| 1/8 | 11 | 606.8 | | 38.8 | |

(1) Guaranteed by design, not tested in production.

4.25. Parameter condition

Unless otherwise specified, all values given for $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

5. Package information

5.1. LQFP144 package outline dimensions

Figure 5-1. LQFP144 package outline

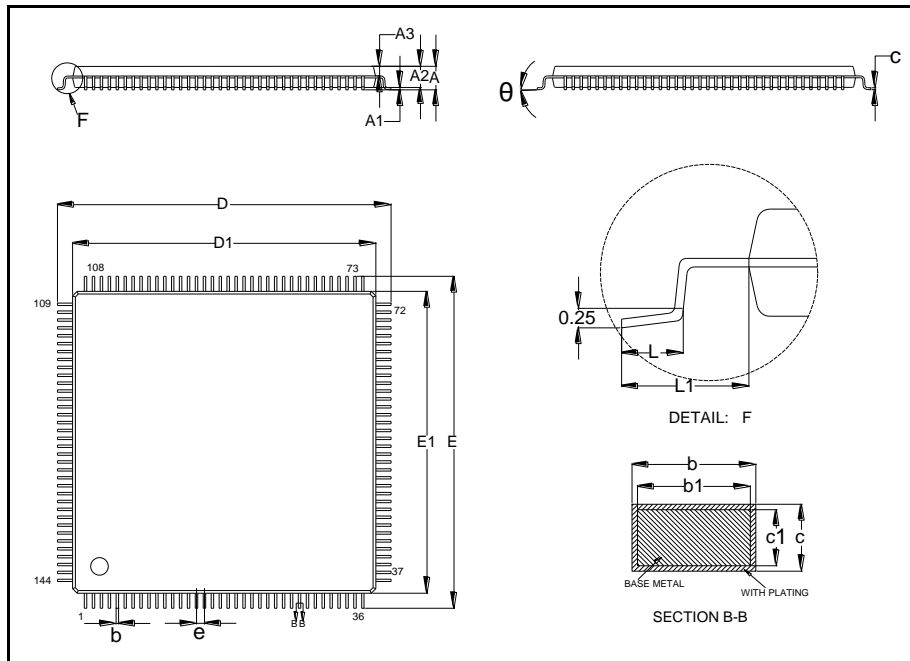


Table 5-1. LQFP144 package dimensions

| Symbol | Min | Typ | Max |
|----------|-------|-------|-------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 21.80 | 22.00 | 22.20 |
| D1 | 19.90 | 20.00 | 20.10 |
| E | 21.80 | 22.00 | 22.20 |
| E1 | 19.90 | 20.00 | 20.10 |
| e | — | 0.50 | — |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

5.2. LQFP100 package outline dimensions

Figure 5-3. LQFP100 package outline

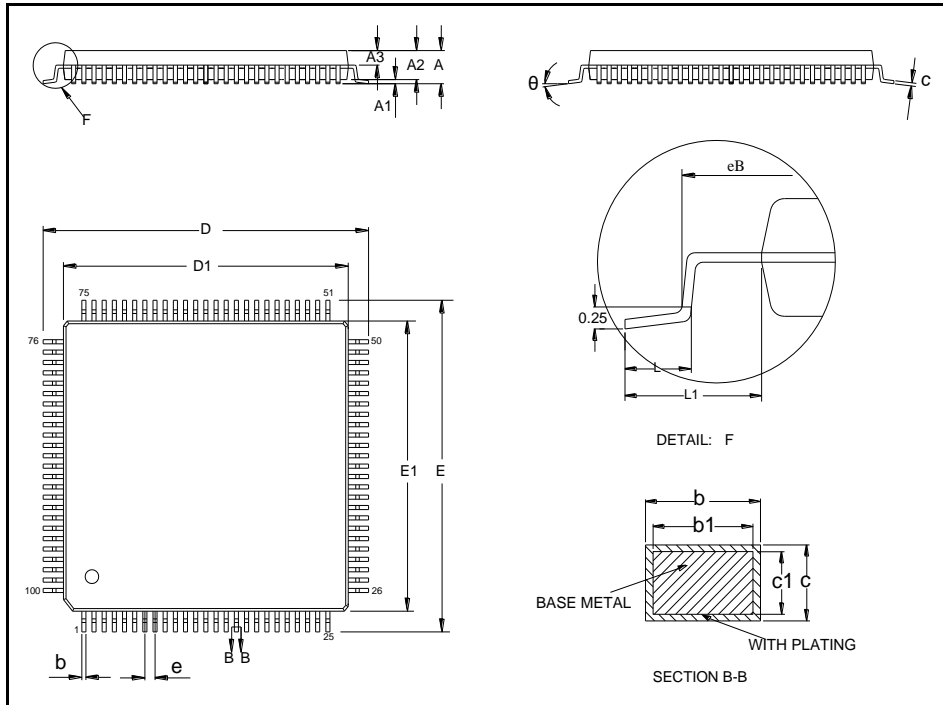
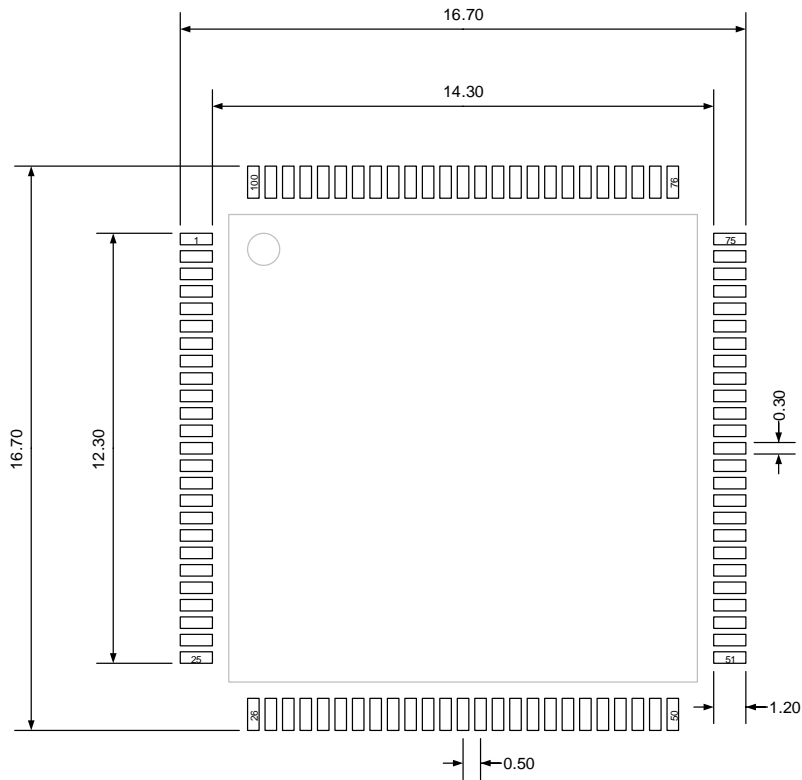


Table 5-2. LQFP100 package dimensions

| Symbol | Min | Typ | Max |
|----------|-------|-------|-------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.10 |
| e | — | 0.50 | — |
| eB | 15.05 | — | 15.35 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-4. LQFP100 recommended footprint



(Original dimensions are in millimeters)

5.3. LQFP64 package outline dimensions

Figure 5-5. LQFP64 package outline

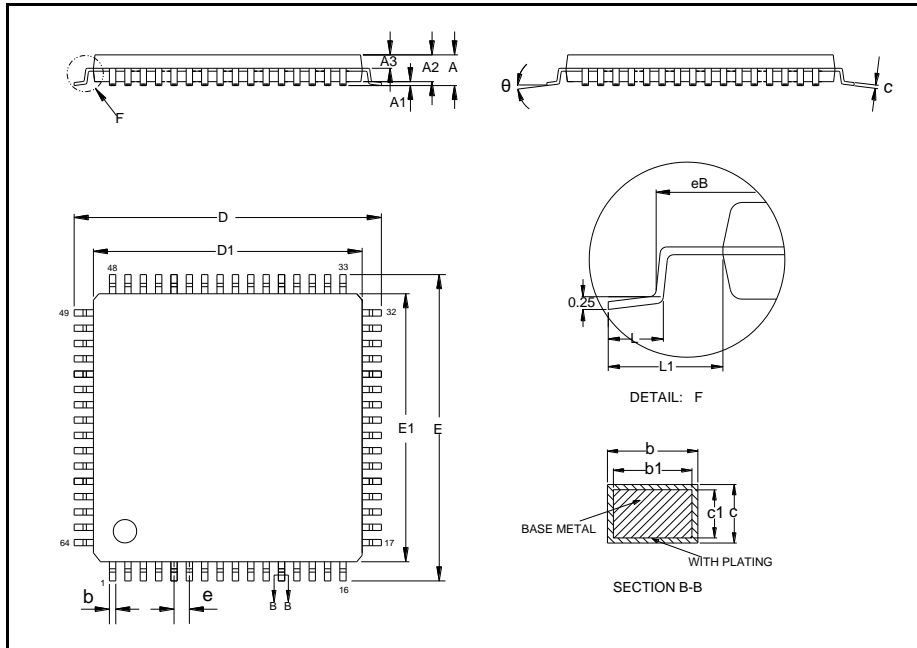
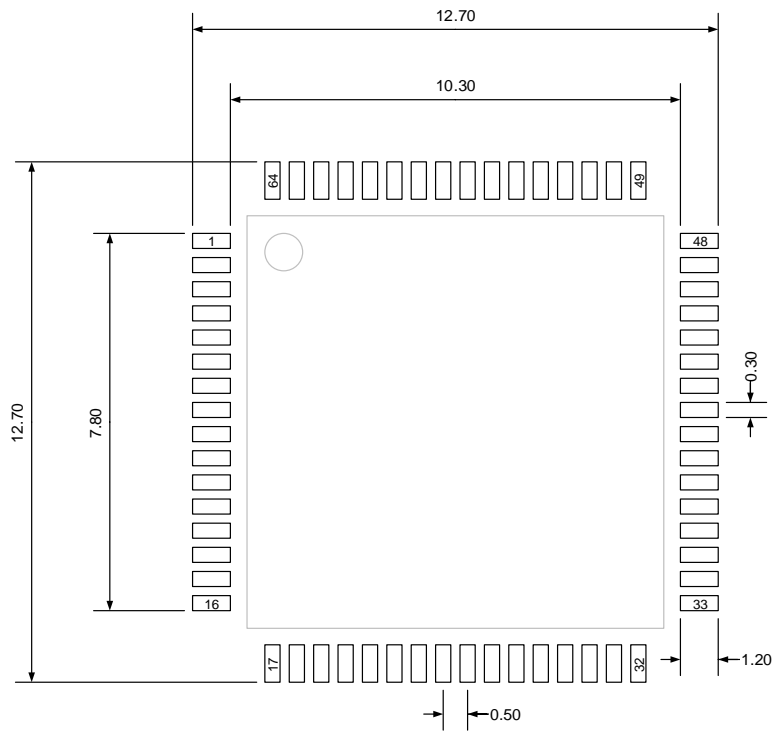


Table 5-3. LQFP64 package dimensions

| Symbol | Min | Typ | Max |
|----------|-------|-------|-------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | — | 0.50 | — |
| eB | 11.25 | — | 11.45 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-6. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.4. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “ θ ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA} : Thermal resistance, junction-to-ambient.

θ_{JB} : Thermal resistance, junction-to-board.

θ_{JC} : Thermal resistance, junction-to-case.

Ψ_{JB} : Thermal characterization parameter, junction-to-board.

Ψ_{JT} : Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5-1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5-2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5-3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-4. Package thermal characteristics⁽¹⁾

| Symbol | Condition | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| θ_{JA} | Natural convection, 2S2P PCB | LQFP144 | 48.76 | °C/W |
| | | LQFP100 | 57.42 | |
| | | LQFP64 | 61.80 | |
| θ_{JB} | Cold plate, 2S2P PCB | LQFP144 | 35.00 | °C/W |
| | | LQFP100 | 31.68 | |
| | | LQFP64 | 42.83 | |



| Symbol | Condition | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| θ_{JC} | Cold plate, 2S2P PCB | LQFP144 | 12.03 | °C/W |
| | | LQFP100 | 13.85 | |
| | | LQFP64 | 21.98 | |
| Ψ_{JB} | Natural convection, 2S2P PCB | LQFP144 | 35.32 | °C/W |
| | | LQFP100 | 41.28 | |
| | | LQFP64 | 43.05 | |
| Ψ_{JT} | Natural convection, 2S2P PCB | LQFP144 | 1.86 | °C/W |
| | | LQFP100 | 0.75 | |
| | | LQFP64 | 1.58 | |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.



6. Ordering information

Table 6-1. Part ordering code for GD32F107xx devices

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---------------|------------|---------|--------------|------------------------------|
| GD32F107ZGT6 | 1024 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZFT6 | 768 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZET6 | 512 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZDT6 | 384 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107ZCT6 | 256 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F107VGT6 | 1024 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VFT6 | 768 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VET6 | 512 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VDT6 | 384 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VCT6 | 256 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107VBT6 | 128 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F107RGT6 | 1024 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RFT6 | 768 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RET6 | 512 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RDT6 | 384 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RCT6 | 256 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F107RBT6 | 128 | LQFP64 | Green | Industrial -40°C to +85°C |

7. Revision history

Table 7-1. Revision history

| Revision No. | Description | Date |
|--------------|---|--------------|
| 1.0 | Initial Release | Oct.25, 2013 |
| 1.1 | 1. Characteristics values modified, refers to <u>Electrical characteristics</u> . | Nov.10, 2013 |
| 1.2 | 1. Repair history accumulation error. | Jan.24, 2018 |
| 1.3 | 1. Delete the PD0, PD1 remap to OSC pins information in packages no less than 100 pins, refers to <u>Pin definitions</u> . | Feb.15, 2020 |
| 1.4 | 1. Integrate the boot loader address in chapter <u>Memory map</u> together. 2. Add description of V _{REF+} and V _{REF-} connection in chapter <u>Analog to digital converter (ADC)</u> . 3. Remove all TIMER7 information from GD32F107xx datasheet. 4. Arm® Cortex® w ritten format modification. | Sep.18, 2020 |
| 1.5 | 1. Table 4-3 update, refers to <u>Table 4-3. Power consumption characteristics</u> . | Apr.12, 2021 |
| 1.6 | 1. Delete PD0 / PD1 from OSCIN / OSCOUT remap information in chapter 2.6.3, refers to <u>Pin definitions</u> . 2. Modify pinouts, refers to <u>Pinouts and pin assignment</u> . 3. Characteristics values modified, refers to <u>Electrical characteristics</u> . 4. Package information and Ordering information update, refer to <u>Package information</u> and <u>Ordering information</u> . 5. Modify the notes under <u>Table 4-1. Absolute maximum ratings⁽¹⁾⁽⁴⁾</u> . 6. Modify Vesd (HBM) and Vesd (CDM) standards, refers to <u>Electrical characteristics</u> . 7. Modify WDGT characteristics, refers to <u>WDGT characteristics</u> . 8. Modify SPI/I2S diagrams, refer to <u>SPI characteristics</u> and <u>I2S characteristics</u> . 9. Modify I2C characteristics, refer to <u>I2C characteristics</u> . 10. Modify LQFP64 package information, refer to <u>LQFP64</u> . | Jun.30, 2022 |



| | | |
|-----|---|--------------|
| | <p><u>package outline dimensions.</u></p> <p>11. Delete related static parameter in <u>DAC characteristics.</u></p> <p>12. Update NRST external pin circuit, refer to <u>Figure 4-4. Recommended external NRST pin circuit⁽¹⁾.</u></p> <p>13. EXMC related pin update, refer to <u>Pin definitions.</u></p> | |
| 1.7 | <p>1. Modify gm value in table <u>Table 4-14. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics.</u></p> | Sep.13, 2022 |
| 1.8 | <p>1. Pin name modification in <u>Pin definitions</u> and <u>Pinouts and pin assignment.</u></p> <p>2. Add comments to <u>Power consumption.</u></p> <p>3. Modify <u>I2C characteristics</u> diagram <u>Figure 4-5. I2C bus timing diagram.</u></p> <p>4. Modify <u>I2S characteristics</u> diagram <u>Figure 4-8. I2S timing diagram - master mode</u> and <u>Figure 4-9. I2S timing diagram - slave mode.</u></p> | Dec.6, 2022 |
| 1.9 | <p>1. Format modification: VREFP / VREFN / VDD / VDDA / VSS.</p> <p>2. Modify <u>I2C characteristics</u> diagram <u>Figure 4-3. I2C bus timing diagram.</u></p> <p>3. Add version number and date to cover.</p> <p>4. Add chip type in pin definitions table <u>Table 24. GD32F107Zx LQFP144 pin definitions/ Table 2 5. GD32F107Vx LQFP100 pin definitions/ Table 2 6. GD32F107Rx LQFP64 pin definitions.</u></p> | Jun.20, 2023 |

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