

GigaDevice Semiconductor Inc.

GD32F150xx

Arm[®] Cortex[®]-M3 32-bit MCU

Datasheet

Revision 3.8

(Dec. 2024)

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1. General description

The GD32F150xx device belongs to the value line of GD32 MCU family. It is a 32-bit general-purpose microcontroller based on the high performance Arm® Cortex®-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex®-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F150xx device incorporates the Arm® Cortex®-M3 32-bit processor core operating at 72 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 64 KB on-chip Flash memory and up to 8 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer one 12-bit ADC, one 12-bit DAC and two comparators, up to five general-purpose 16-bit timers, a general-purpose 32-bit timer, a basic timer, a PWM advanced-control timer, as well as standard and advanced communication interfaces: up to two SPIs, two I²Cs, two USARTs, a I²S, a HDMI-CEC a TSI and an USB D.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F150xx devices suitable for a wide range of applications, especially in areas such as industrial control, motor drives, user interface, power monitor and alarm systems, consumer and handheld equipment, gaming and GPS, E-bike and so on.

2. Device overview

2.1. Device information

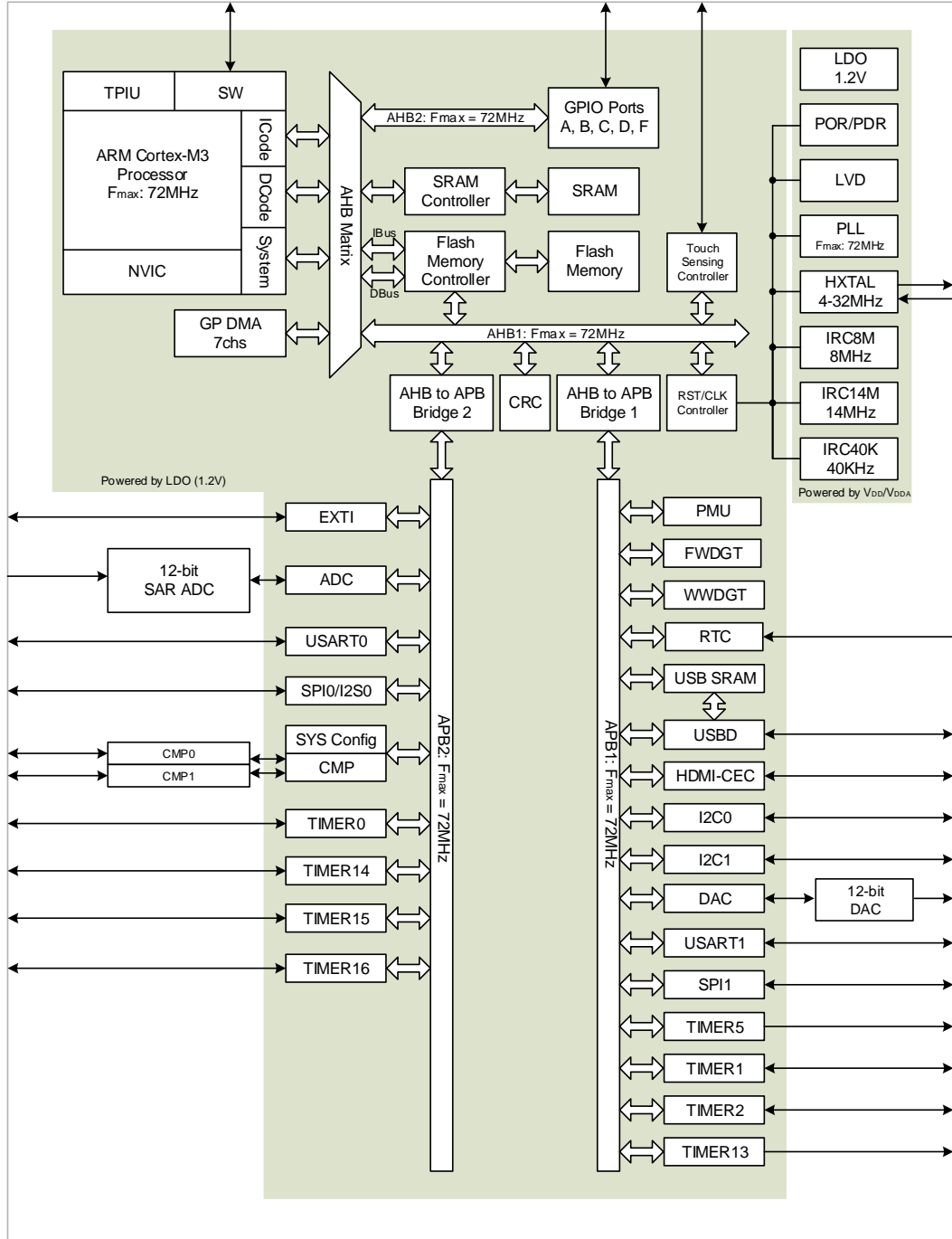
Table 2-1. GD32F150xx devices features and peripheral list

| Part Number | | GD32F150xx | | | | | | | | | | | |
|---------------------------|---------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| | | G4 | G6 | G8 | K4 | K6 | K8 | C4 | C6 | C8 | R4 | R6 | R8 |
| Flash | Code area (KB) | 16 | 32 | 32 | 16 | 32 | 32 | 16 | 32 | 32 | 16 | 32 | 32 |
| | Data area (KB) | 0 | 0 | 32 | 0 | 0 | 32 | 0 | 0 | 32 | 0 | 0 | 32 |
| | Total (KB) | 16 | 32 | 64 | 16 | 32 | 64 | 16 | 32 | 64 | 16 | 32 | 64 |
| SRAM (KB) | | 4 | 6 | 8 | 4 | 6 | 8 | 4 | 6 | 8 | 4 | 6 | 8 |
| Timers | GPTM(32 bit) | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ | 1 ⁽¹⁾ |
| | GPTM(16 bit) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) | 5 ^(2,13-16) |
| | Advanced TM(16 bit) | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ |
| | Basic TM(16 bit) | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ | 1 ⁽⁵⁾ |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 2 ⁽⁰⁻¹⁾ |
| | I2C | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ |
| | SPI | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 2 ⁽⁰⁻¹⁾ |
| | I2S | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ | 1 ⁽⁰⁾ |
| | USB D | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | HDMI CEC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| GPIO | | 24 | 24 | 24 | 27 | 27 | 27 | 39 | 39 | 39 | 55 | 55 | 55 |
| Capacitive Touch Channels | | 14 | 14 | 14 | 14 | 14 | 14 | 17 | 17 | 17 | 18 | 18 | 18 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |

| Part Number | | GD32F150xx | | | | | | | | | | | |
|-------------------|-----------------|------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|
| | | G4 | G6 | G8 | K4 | K6 | K8 | C4 | C6 | C8 | R4 | R6 | R8 |
| Analog Comparator | | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| ADC | Units | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Channels (Ext.) | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 16 | 16 | 16 |
| | Channels (Int.) | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| DAC | | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) | 1 (0) |
| Package | | QFN28 | | | QFN32 | | | LQFP48 | | | LQFP64 | | |

2.2. Block diagram

Figure 2-1. GD32F150xx block diagram



2.3. Pinouts and pin assignment

Figure 2-2. GD32F150Rx LQFP64 pinouts

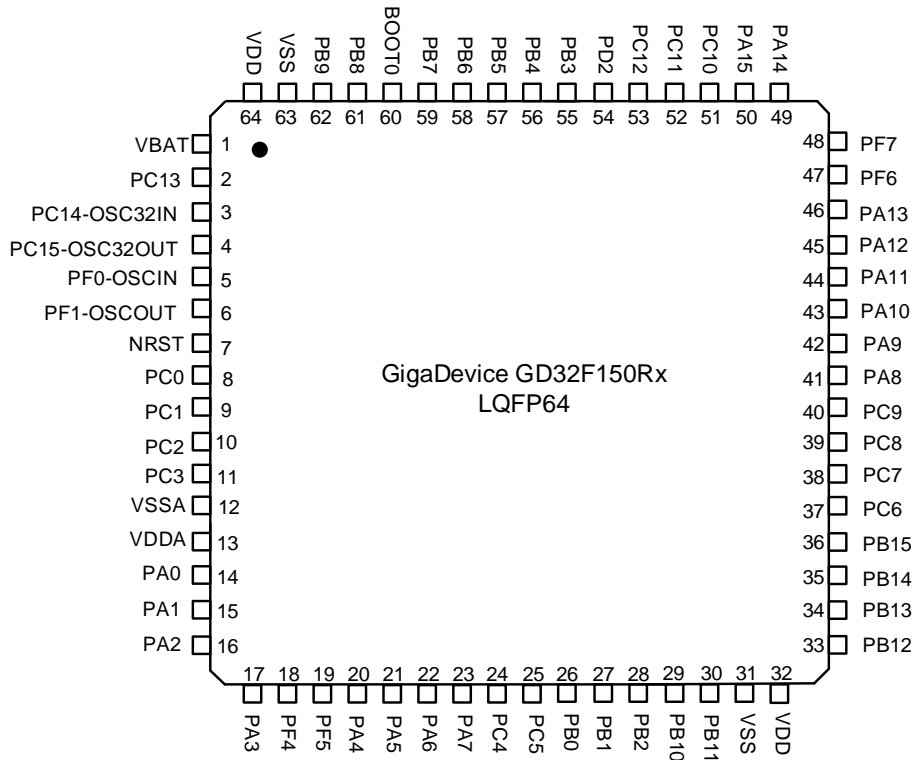


Figure 2-3. GD32F150Cx LQFP48 pinouts

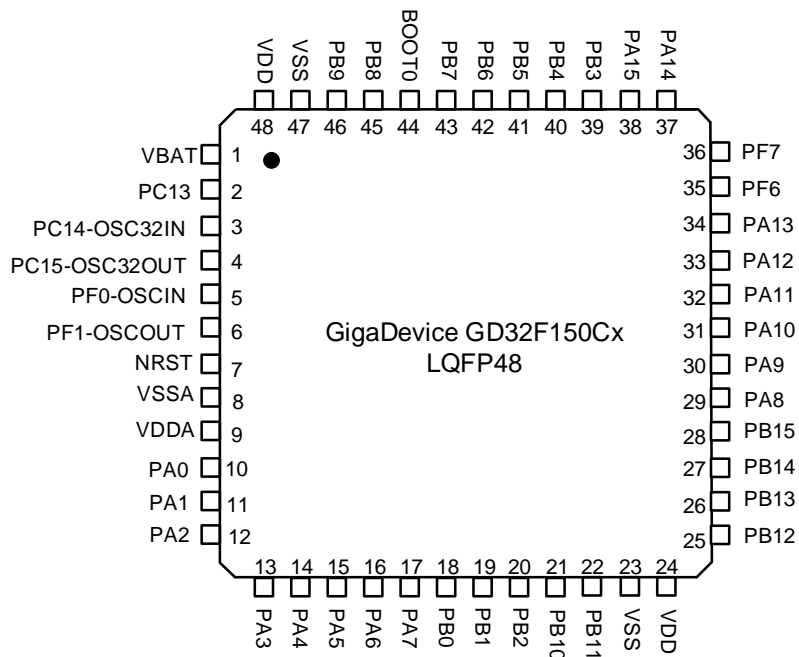


Figure 2-4. GD32F150Kx QFN32 pinouts

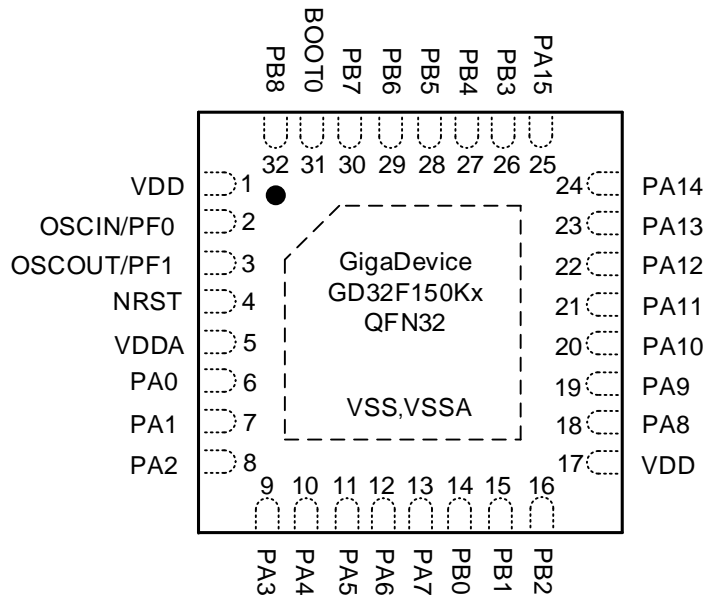
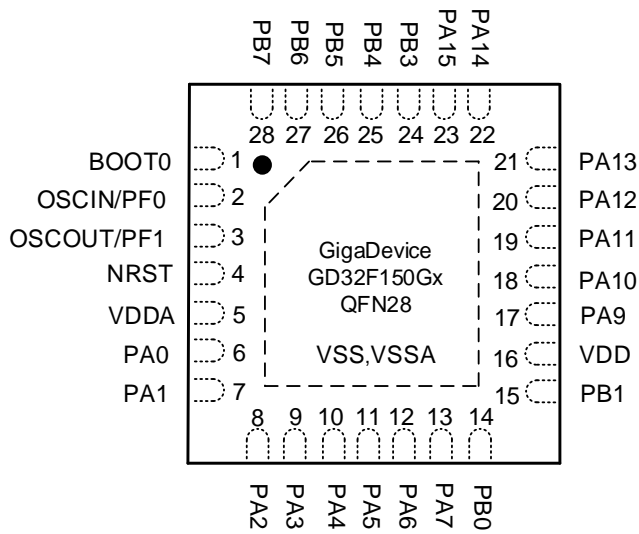


Figure 2-5. GD32F150Gx QFN28 pinouts



2.4. Memory map

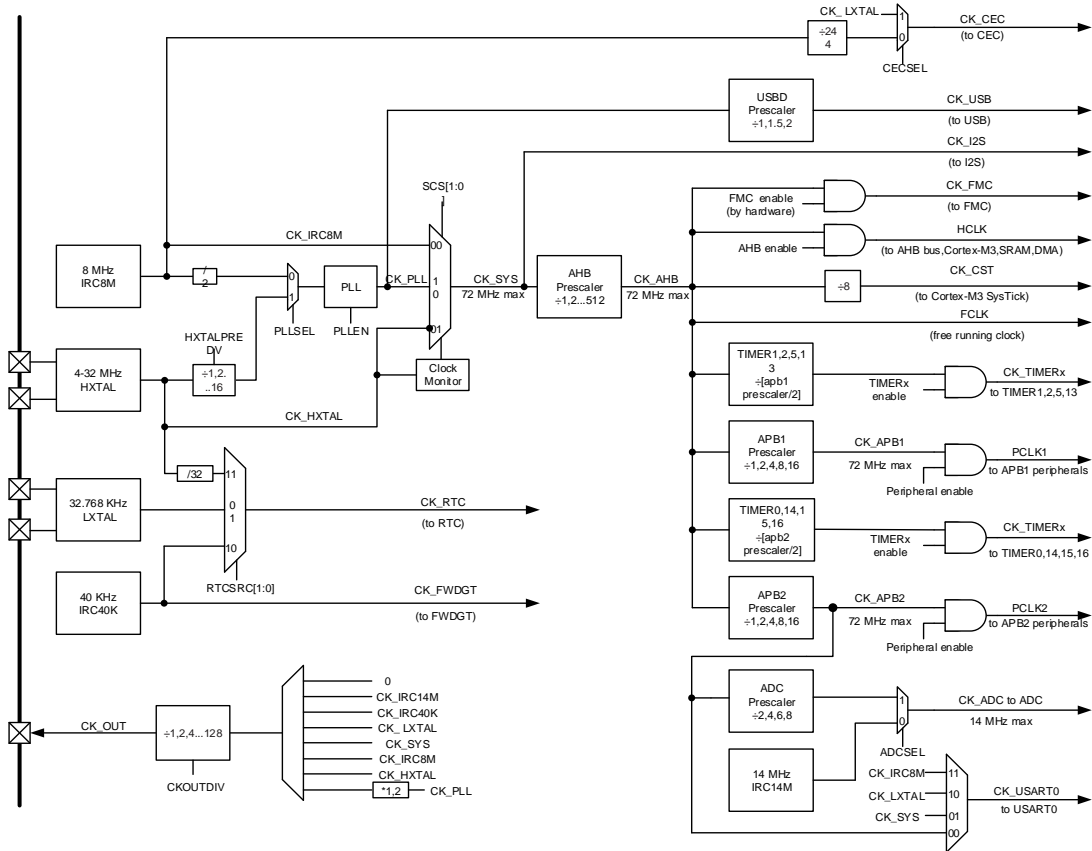
Table 2-2. GD32F150xx memory map

| Pre-defined Regions | Bus | ADDRESS | Peripherals |
|---------------------------|------|---------------------------|--------------------------------|
| | | 0xE000 0000 - 0xE00F FFFF | Cortex-M3 internal peripherals |
| External Device | | 0xA000 0000 - 0xDFFF FFFF | Reserved |
| External RAM | | 0x6000 0000 - 0x9FFF FFFF | Reserved |
| Peripherals | AHB1 | 0x5000 0000 - 0x5FFF FFFF | Reserved |
| | AHB2 | 0x4800 1800 - 0x4FFF FFFF | Reserved |
| | | 0x4800 1400 - 0x4800 17FF | GPIOF |
| | | 0x4800 1000 - 0x4800 13FF | Reserved |
| | | 0x4800 0C00 - 0x4800 0FFF | GPIOD |
| | | 0x4800 0800 - 0x4800 0BFF | GPIOC |
| | | 0x4800 0400 - 0x4800 07FF | GPIOB |
| | | 0x4800 0000 - 0x4800 03FF | GPIOA |
| | AHB1 | 0x4002 4400 - 0x47FF FFFF | Reserved |
| | | 0x4002 4000 - 0x4002 43FF | TSI |
| | | 0x4002 3400 - 0x4002 3FFF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2400 - 0x4002 2FFF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | FMC |
| | | 0x4002 1400 - 0x4002 1FFF | Reserved |
| | | 0x4002 1000 - 0x4002 13FF | RCU |
| | | 0x4002 0400 - 0x4002 0FFF | Reserved |
| | | 0x4002 0000 - 0x4002 03FF | DMA |
| | APB2 | 0x4001 4C00 - 0x4001 FFFF | Reserved |
| | | 0x4001 4800 - 0x4001 4BFF | TIMER16 |
| | | 0x4001 4400 - 0x4001 47FF | TIMER15 |
| | | 0x4001 4000 - 0x4001 43FF | TIMER14 |
| | | 0x4001 3C00 - 0x4001 3FFF | Reserved |
| | | 0x4001 3800 - 0x4001 3BFF | USART0 |
| | | 0x4001 3400 - 0x4001 37FF | Reserved |
| | | 0x4001 3000 - 0x4001 33FF | SPI0/I2S0 |
| | | 0x4001 2C00 - 0x4001 2FFF | TIMER0 |
| | | 0x4001 2800 - 0x4001 2BFF | Reserved |
| | | 0x4001 2400 - 0x4001 27FF | ADC |
| | | 0x4001 0800 - 0x4001 23FF | Reserved |
| | | 0x4001 0400 - 0x4001 07FF | EXTI |
| | | 0x4001 0000 - 0x4001 03FF | SYSCFG+CMP |
| | APB1 | 0x4000 C400 - 0x4000 FFFF | Reserved |
| 0x4000 C000 - 0x4000 C3FF | | Reserved | |

| Pre-defined Regions | Bus | ADDRESS | Peripherals |
|---------------------|-----|---------------------------|-----------------------------------|
| | | 0x4000 8000 - 0x4000 BFFF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | Reserved |
| | | 0x4000 7800 - 0x4000 7BFF | CEC |
| | | 0x4000 7400 - 0x4000 77FF | DAC |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| | | 0x4000 6400 - 0x4000 6FFF | Reserved |
| | | 0x4000 6000 - 0x4000 63FF | USB SRAM |
| | | 0x4000 5C00 - 0x4000 5FFF | USB registers |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 4800 - 0x4000 53FF | Reserved |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | Reserved |
| | | 0x4000 3C00 - 0x4000 3FFF | Reserved |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1 |
| | | 0x4000 3400 - 0x4000 37FF | Reserved |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | TIMER13 |
| | | 0x4000 1400 - 0x4000 1FFF | Reserved |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0800 - 0x4000 0FFF | Reserved |
| | | 0x4000 0400 - 0x4000 07FF | TIMER2 |
| | | 0x4000 0000 - 0x4000 03FF | TIMER1 |
| SRAM | | 0x2000 2000 - 0x3FFF FFFF | Reserved |
| | | 0x2000 0000 - 0x2000 1FFF | SRAM |
| Code | | 0x1FFF F80F - 0x1FFF FFFF | Reserved |
| | | 0x1FFF F800 - 0x1FFF F80E | Option bytes |
| | | 0x1FFF EC00 - 0x1FFF F7FF | System memory |
| | | 0x0801 0000 - 0x1FFF EBFF | Reserved |
| | | 0x0800 0000 - 0x0800 FFFF | Main Flash memory |
| | | 0x0000 0000 - 0x07FF FFFF | Aliased to Flash or system memory |

2.5. Clock tree

Figure 2-6. GD32F150xx clock tree



Legend:

- HXTAL: High speed crystal oscillator
- LXTAL: Low speed crystal oscillator
- IRC8M: Internal 8M RC oscillators
- IRC40K: Internal 40K RC oscillator

2.6. Pin definitions

2.6.1. GD32F150Rx LQFP64 pin definitions

Table 2-3. GD32F150Rx LQFP64 pin definitions

| GD32F150Rx LQFP64 | | | | |
|---------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| VBAT | 1 | P | | Default: VBAT |
| PC13-TAM PER-RTC | 2 | I/O | | Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1 |
| PC14-OSC 32IN | 3 | I/O | | Default: PC14 Additional: OSC32IN |
| PC15- OSC32OUT | 4 | I/O | | Default: PC15 Additional: OSC32OUT |
| PF0-OSCIN | 5 | I/O | 5VT | Default: PF0 Additional: OSCIN |
| PF1-OSCO UT | 6 | I/O | 5VT | Default: PF1 Additional: OSCOUT |
| NRST | 7 | I/O | | Default: NRST |
| PC0 | 8 | I/O | | Default: PC0 Alternate: EVENTOUT Additional: ADC_IN10 |
| PC1 | 9 | I/O | | Default: PC1 Alternate: EVENTOUT Additional: ADC_IN11 |
| PC2 | 10 | I/O | | Default: PC2 Alternate: EVENTOUT Additional: ADC_IN12 |
| PC3 | 11 | I/O | | Default: PC3 Alternate: EVENTOUT Additional: ADC_IN13 |
| V _{SSA} | 12 | P | | Default: V _{SSA} |
| V _{DDA} | 13 | P | | Default: V _{DDA} |
| PA0-WKUP | 14 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, CMP0_OUT, TSI_G0_IO0, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP0_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 15 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ /USART0_DE ⁽³⁾ , |

| GD32F150Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | USART1_RTS ⁽⁴⁾ /USART1_DE ⁽⁴⁾ , TIMER1_CH1, TSI_G0_IO1, I2C1_SDA ⁽⁵⁾ , EVENTOUT Additional: ADC_IN1, CMP0_IP |
| PA2 | 16 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER1_CH2, TIMER14_CH0, CMP1_OUT, TSI_G0_IO2 Additional: ADC_IN2, CMP1_IM6 |
| PA3 | 17 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH3, TIMER14_CH1, TSI_G0_IO3 Additional: ADC_IN3, CMP1_IP |
| PF4 | 18 | I/O | 5VT | Default: PF4 Alternate: SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PF5 | 19 | I/O | 5VT | Default: PF5 Alternate: EVENTOUT |
| PA4 | 20 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER13_CH0, TSI_G1_IO0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT |
| PA5 | 21 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK, CEC, TIMER1_CH0, TIMER1_ETI, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5 |
| PA6 | 22 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, CMP0_OUT, TSI_G1_IO2, EVENTOUT Additional: ADC_IN6 |
| PA7 | 23 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, CMP1_OUT, TSI_G1_IO3, EVENTOUT Additional: ADC_IN7 |
| PC4 | 24 | I/O | | Default: PC4 Alternate: EVENTOUT Additional: ADC_IN14 |
| PC5 | 25 | I/O | | Default: PC5 Alternate: TSI_G2_IO0 Additional: ADC_IN15 |

| GD32F150Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PB0 | 26 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, TSI_G2_IO1, USART1_RX, EVENTOUT Additional: ADC_IN8 |
| PB1 | 27 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, TSI_G2_IO2, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| PB2 | 28 | I/O | 5VT | Default: PB2 Alternate: TSI_G2_IO3 |
| PB10 | 29 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL ⁽⁵⁾ , CEC, TIMER1_CH2, TSITG |
| PB11 | 30 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA ⁽⁵⁾ , TIMER1_CH3, TSI_G5_IO0, EVENTOUT |
| VSS | 31 | P | | Default: VSS |
| VDD | 32 | P | | Default: VDD |
| PB12 | 33 | I/O | 5VT | Default: PB12 Alternate: SPI0_NSS ⁽³⁾ , SPI1_NSS ⁽⁵⁾ , TIMER0_BRKIN, TSI_G5_IO1, I2C1_SMBA ⁽⁵⁾ , EVENTOUT |
| PB13 | 34 | I/O | 5VT | Default: PB13 Alternate: SPI0_SCK ⁽³⁾ , SPI1_SCK ⁽⁵⁾ , TIMER0_CH0_ON, TSI_G5_IO2 |
| PB14 | 35 | I/O | 5VT | Default: PB14 Alternate: SPI0_MISO ⁽³⁾ , SPI1_MISO ⁽⁵⁾ , TIMER0_CH1_ON, TIMER14_CH0, TSI_G5_IO3 |
| PB15 | 36 | I/O | 5VT | Default: PB15 Alternate: SPI0_MOSI ⁽³⁾ , SPI1_MOSI ⁽⁵⁾ , TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN |
| PC6 | 37 | I/O | 5VT | Default: PC6 Alternate: TIMER2_CH0 |
| PC7 | 38 | I/O | 5VT | Default: PC7 Alternate: TIMER2_CH1 |
| PC8 | 39 | I/O | 5VT | Default: PC8 Alternate: TIMER2_CH2 |
| PC9 | 40 | I/O | 5VT | Default: PC9 Alternate: TIMER2_CH3 |
| PA8 | 41 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, MCO, USART1_TX, |

| GD32F150Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | EVENTOUT |
| PA9 | 42 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, TSI_G3_IO0, I2C0_SCL |
| PA10 | 43 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, TSI_G3_IO1, I2C0_SDA |
| PA11 | 44 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP0_OUT, TSI_G3_IO2, EVENTOUT Additional: USBDM |
| PA12 | 45 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, CMP1_OUT, TSI_G3_IO3, EVENTOUT Additional: USBDP |
| PA13 | 46 | I/O | 5VT | Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO ⁽⁵⁾ |
| PF6 | 47 | I/O | 5VT | Default: I2C1_SCL ⁽⁵⁾ |
| PF7 | 48 | I/O | 5VT | Default: I2C1_SDA ⁽⁵⁾ |
| PA14 | 49 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 50 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PC10 | 51 | I/O | 5VT | Default: PC10 |
| PC11 | 52 | I/O | 5VT | Default: PC11 |
| PC12 | 53 | I/O | 5VT | Default: PC12 |
| PD2 | 54 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI |
| PB3 | 55 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH1, TSI_G4_IO0, EVENTOUT |
| PB4 | 56 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TSI_G4_IO1, EVENTOUT |
| PB5 | 57 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 |

| GD32F150Rx LQFP64 | | | | |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| PB6 | 58 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2 |
| PB7 | 59 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON, TSI_G4_IO3 |
| BOOT0 | 60 | I | | Default: BOOT0 |
| PB8 | 61 | I/O | 5VT | Default: PB8 Alternate: I2C0_SCL, CEC, TIMER15_CH0, TSITG |
| PB9 | 62 | I/O | 5VT | Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT |
| VSS | 63 | P | | Default: VSS |
| VDD | 64 | P | | Default: VDD |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F150R4 devices only.
- (4) Functions are available on GD32F150R8/6 devices.
- (5) Functions are available on GD32F150R8 devices.

2.6.2. GD32F150Cx LQFP48 pin definitions

Table 2-4. GD32F150Cx LQFP48 pin definitions

| GD32F150Cx LQFP48 | | | | |
|---------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| VBAT | 1 | P | | Default: VBAT |
| PC13-TAMP ER-RTC | 2 | I/O | | Default: PC13 Additional: RTC_TAMP0, RTC_TS, RTC_OUT, WKUP1 |
| PC14-OSC3 2IN | 3 | I/O | | Default: PC14 Additional: OSC32IN |
| PC15- OSC32OUT | 4 | I/O | | Default: PC15 Additional: OSC32OUT |
| PF0-OSCIN | 5 | I/O | 5VT | Default: PF0 Additional: OSCIN |
| PF1-OSCOU T | 6 | I/O | 5VT | Default: PF1 Additional: OSCOUT |
| NRST | 7 | I/O | | Default: NRST |
| VSSA | 8 | P | | Default: VSSA |
| VDDA | 9 | P | | Default: VDDA |
| PA0-WKUP | 10 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI,CMP0_OUT, TSI_G0_IO0, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP0_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 11 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ /USART0_DE ⁽³⁾ , USART1_RTS ⁽⁴⁾ /USART1_DE ⁽⁴⁾ , TIMER1_CH1, TSI_G0_IO1, I2C1_SDA ⁽⁵⁾ , EVENTOUT Additional: ADC_IN1, CMP0_IP |
| PA2 | 12 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER1_CH2, TIMER14_CH0, CMP1_OUT, TSI_G0_IO2 Additional: ADC_IN2, CMP1_IM6 |
| PA3 | 13 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH3, TIMER14_CH1, TSI_G0_IO3 Additional: ADC_IN3,CMP1_IP |
| PA4 | 14 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER13_CH0, TSI_G1_IO0, SPI1_NSS ⁽⁵⁾ |

| GD32F150Cx LQFP48 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT |
| PA5 | 15 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK, CEC, TIMER1_CH0, TIMER1_ETI, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5 |
| PA6 | 16 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, CMP0_OUT, TSI_G1_IO2, EVENTOUT Additional: ADC_IN6 |
| PA7 | 17 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, CMP1_OUT, TSI_G1_IO3, EVENTOUT Additional: ADC_IN7 |
| PB0 | 18 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, TSI_G2_IO1, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 19 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, TSI_G2_IO2, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| PB2 | 20 | I/O | 5VT | Default: PB2 Alternate: TSI_G2_IO3 |
| PB10 | 21 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL ⁽⁵⁾ , CEC, TIMER1_CH2, TSITG |
| PB11 | 22 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA ⁽⁵⁾ , TIMER1_CH3, TSI_G5_IO0, EVENTOUT |
| VSS | 23 | P | | Default: VSS |
| VDD | 24 | P | | Default: VDD |
| PB12 | 25 | I/O | 5VT | Default: PB12 Alternate: SPI0_NSS ⁽³⁾ , SPI1_NSS ⁽⁵⁾ , TIMER0_BRKIN, TSI_G5_IO1, I2C1_SMBA ⁽⁵⁾ , EVENTOUT |
| PB13 | 26 | I/O | 5VT | Default: PB13 Alternate: SPI0_SCK ⁽³⁾ , SPI1_SCK ⁽⁵⁾ , TIMER0_CH0_ON, TSI_G5_IO2 |
| PB14 | 27 | I/O | 5VT | Default: PB14 Alternate: SPI0_MISO ⁽³⁾ , SPI1_MISO ⁽⁵⁾ , TIMER0_CH1_ON, |

| GD32F150Cx LQFP48 | | | | |
|-------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | TIMER14_CH0, TSI_G5_IO3 |
| PB15 | 28 | I/O | 5VT | Default: PB15 Alternate: SPI0_MOSI ⁽³⁾ , SPI1_MOSI ⁽⁵⁾ , TIMER0_CH2_ON, TIMER14_CH0_ON, TIMER14_CH1 Additional: RTC_REFIN |
| PA8 | 29 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, MCO, USART1_TX ⁽⁴⁾ , EVENTOUT |
| PA9 | 30 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, TSI_G3_IO0, I2C0_SCL |
| PA10 | 31 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, TSI_G3_IO1, I2C0_SDA |
| PA11 | 32 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP0_OUT, TSI_G3_IO2, EVENTOUT Additional: USBDM |
| PA12 | 33 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, CMP1_OUT, TSI_G3_IO3, EVENTOUT Additional: USBDP |
| PA13 | 34 | I/O | 5VT | Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO ⁽⁵⁾ |
| PF6 | 35 | I/O | 5VT | Default: I2C1_SCL ⁽⁵⁾ |
| PF7 | 36 | I/O | 5VT | Default: I2C1_SDA ⁽⁵⁾ |
| PA14 | 37 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 38 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 39 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH1, TSI_G4_IO0, EVENTOUT |
| PB4 | 40 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TSI_G4_IO1, EVENTOUT |
| PB5 | 41 | I/O | 5VT | Default: PB5 |

| GD32F150Cx LQFP48 | | | | |
|-------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: SPI0_MOSI,I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 |
| PB6 | 42 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2 |
| PB7 | 43 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON, TSI_G4_IO3 |
| BOOT0 | 44 | I | | Default: BOOT0 |
| PB8 | 45 | I/O | 5VT | Default: PB8 Alternate: I2C0_SCL, CEC, TIMER15_CH0, TSITG |
| PB9 | 46 | I/O | 5VT | Default: PB9 Alternate: I2C0_SDA, IFRP_OUT, TIMER16_CH0, EVENTOUT |
| VSS | 47 | P | | Default: VSS |
| VDD | 48 | P | | Default: VDD |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F150C4 devices only.
- (4) Functions are available on GD32F150C8/6 devices.
- (5) Functions are available on GD32F150C8 devices.

2.6.3. GD32F150Kx QFN32 pin definitions

Table 2-5. GD32F150Kx QFN32 pin definitions

| GD32F150Kx QFN32 | | | | |
|------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| VDD | 1 | P | | Default: VDD |
| PF0-OSCIN | 2 | I/O | 5VT | Default: PF0 Additional: OSCIN |
| PF1-OSCOU T | 3 | I/O | 5VT | Default: PF1 Additional: OSCOUT |
| NRST | 4 | I/O | | Default: NRST |
| VDDA | 5 | P | | Default: VDDA |
| PA0-WKUP | 6 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, CMP0_OUT, TSI_G0_IO0, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP0_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 7 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ /USART0_DE ⁽³⁾ , USART1_RTS ⁽⁴⁾ /USART1_DE ⁽⁴⁾ , TIMER1_CH1, TSI_G0_IO1, I2C1_SDA ⁽⁵⁾ , EVENTOUT Additional: ADC_IN1, CMP0_IP |
| PA2 | 8 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER1_CH2, TIMER14_CH0, CMP1_OUT, TSI_G0_IO2 Additional: ADC_IN2, CMP1_IM6 |
| PA3 | 9 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH3, TIMER14_CH1, TSI_G0_IO3 Additional: ADC_IN3, CMP1_IP |
| PA4 | 10 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER13_CH0, TSI_G1_IO0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT |
| PA5 | 11 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK, CEC, TIMER1_CH0, TIMER1_ETI, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5 |
| PA6 | 12 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, CMP0_OUT, TSI_G1_IO2, EVENTOUT |

| GD32F150Kx QFN32 | | | | |
|------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Additional: ADC_IN6 |
| PA7 | 13 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, CMP1_OUT, TSI_G1_IO3, EVENTOUT Additional: ADC_IN7 |
| PB0 | 14 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, TSI_G2_IO1, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 15 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, TSI_G2_IO2, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| PB2 | 16 | I/O | 5VT | Default: PB2 Alternate: TSI_G2_IO3 |
| VDD | 17 | P | | Default: VDD |
| PA8 | 18 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, TIMER0_CH0, MCO, USART1_TX ⁽⁴⁾ , EVENTOUT |
| PA9 | 19 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, TSI_G3_IO0, I2C0_SCL |
| PA10 | 20 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, TSI_G3_IO1, I2C0_SDA |
| PA11 | 21 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP0_OUT, TSI_G3_IO2, EVENTOUT Additional: USBDM |
| PA12 | 22 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, CMP1_OUT, TSI_G3_IO3, EVENTOUT Additional: USBDP |
| PA13 | 23 | I/O | 5VT | Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO ⁽⁵⁾ |
| PA14 | 24 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 25 | I/O | 5VT | Default: PA15 |

| GD32F150Kx QFN32 | | | | |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 26 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH1, TSI_G4_IO0, EVENTOUT |
| PB4 | 27 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TSI_G4_IO1, EVENTOUT |
| PB5 | 28 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI, I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 |
| PB6 | 29 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2 |
| PB7 | 30 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON, TSI_G4_IO3 |
| BOOT0 | 31 | I | | Default: BOOT0 |
| PB8 | 32 | I/O | 5VT | Default: PB8 Alternate: I2C0_SCL, CEC, TIMER15_CH0, TSITG |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F150K4 devices only.
- (4) Functions are available on GD32F150K8/6 devices.
- (5) Functions are available on GD32F150K8 devices.

2.6.4. GD32F150Gx QFN28 pin definitions

Table 2-6. GD32F150Gx QFN28 pin definitions

| GD32F150Gx QFN28 | | | | |
|------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| BOOT0 | 1 | I | | Default: BOOT0 |
| PF0-OSCIN | 2 | I/O | 5VT | Default: PF0 Additional: OSCIN |
| PF1-OSCOU T | 3 | I/O | 5VT | Default: PF1 Additional: OSCOUT |
| NRST | 4 | I/O | | Default: NRST |
| VDDA | 5 | P | | Default: VDDA |
| PA0-WKUP | 6 | I/O | | Default: PA0 Alternate: USART0_CTS ⁽³⁾ , USART1_CTS ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, CMP0_OUT, TSI_G0_IO0, I2C1_SCL ⁽⁵⁾ Additional: ADC_IN0, CMP0_IM6, RTC_TAMP1, WKUP0 |
| PA1 | 7 | I/O | | Default: PA1 Alternate: USART0_RTS ⁽³⁾ /USART0_DE ⁽³⁾ , USART1_RTS ⁽⁴⁾ /USART1_DE ⁽⁴⁾ , TIMER1_CH1, TSI_G0_IO1, I2C1_SDA ⁽⁵⁾ , EVENTOUT Additional: ADC_IN1, CMP0_IP |
| PA2 | 8 | I/O | | Default: PA2 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , TIMER1_CH2, TIMER14_CH0, CMP1_OUT, TSI_G0_IO2 Additional: ADC_IN2, CMP1_IM6 |
| PA3 | 9 | I/O | | Default: PA3 Alternate: USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH3, TIMER14_CH1, TSI_G0_IO3 Additional: ADC_IN3, CMP1_IP |
| PA4 | 10 | I/O | | Default: PA4 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER13_CH0, TSI_G1_IO0, SPI1_NSS ⁽⁵⁾ Additional: ADC_IN4, CMP0_IM4, CMP1_IM4, DAC0_OUT |
| PA5 | 11 | I/O | | Default: PA5 Alternate: SPI0_SCK, I2S0_CK, CEC, TIMER1_CH0, TIMER1_ETI, TSI_G1_IO1 Additional: ADC_IN5, CMP0_IM5, CMP1_IM5 |
| PA6 | 12 | I/O | | Default: PA6 Alternate: SPI0_MISO, I2S0_MCK, TIMER2_CH0, TIMER0_BRKIN, TIMER15_CH0, CMP0_OUT, TSI_G1_IO2, EVENTOUT |

| GD32F150Gx QFN28 | | | | |
|------------------|------|-------------------------|--------------------------|---|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | Additional: ADC_IN6 |
| PA7 | 13 | I/O | | Default: PA7 Alternate: SPI0_MOSI, I2S0_SD, TIMER2_CH1, TIMER13_CH0, TIMER0_CH0_ON, TIMER16_CH0, CMP1_OUT, TSI_G1_IO3, EVENTOUT Additional: ADC_IN7 |
| PB0 | 14 | I/O | | Default: PB0 Alternate: TIMER2_CH2, TIMER0_CH1_ON, TSI_G2_IO1, USART1_RX ⁽⁴⁾ , EVENTOUT Additional: ADC_IN8 |
| PB1 | 15 | I/O | | Default: PB1 Alternate: TIMER2_CH3, TIMER13_CH0, TIMER0_CH2_ON, TSI_G2_IO2, SPI1_SCK ⁽⁵⁾ Additional: ADC_IN9 |
| VDD | 16 | P | | Default: VDD |
| PA9 | 17 | I/O | 5VT | Default: PA9 Alternate: USART0_TX, TIMER0_CH1, TIMER14_BRKIN, TSI_G3_IO0, I2C0_SCL |
| PA10 | 18 | I/O | 5VT | Default: PA10 Alternate: USART0_RX, TIMER0_CH2, TIMER16_BRKIN, TSI_G3_IO1, I2C0_SDA |
| PA11 | 19 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS, TIMER0_CH3, CMP0_OUT, TSI_G3_IO2, EVENTOUT Additional: USBDM |
| PA12 | 20 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS/USART0_DE, TIMER0_ETI, CMP1_OUT, TSI_G3_IO3, EVENTOUT Additional: USBDP |
| PA13 | 21 | I/O | 5VT | Default: PA13 Alternate: IFRP_OUT, SWDIO, SPI1_MISO ⁽⁵⁾ |
| PA14 | 22 | I/O | 5VT | Default: PA14 Alternate: USART0_TX ⁽³⁾ , USART1_TX ⁽⁴⁾ , SWCLK, SPI1_MOSI ⁽⁵⁾ |
| PA15 | 23 | I/O | 5VT | Default: PA15 Alternate: SPI0_NSS, I2S0_WS, USART0_RX ⁽³⁾ , USART1_RX ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, SPI1_NSS ⁽⁵⁾ , EVENTOUT |
| PB3 | 24 | I/O | 5VT | Default: PB3 Alternate: SPI0_SCK, I2S0_CK, TIMER1_CH1, TSI_G4_IO0, |

| GD32F150Gx QFN28 | | | | |
|------------------|------|-------------------------|--------------------------|--|
| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
| | | | | EVENTOUT |
| PB4 | 25 | I/O | 5VT | Default: PB4 Alternate: SPI0_MISO,I2S0_MCK, TIMER2_CH0, TSI_G4_IO1, EVENTOUT |
| PB5 | 26 | I/O | 5VT | Default: PB5 Alternate: SPI0_MOSI,I2S0_SD, I2C0_SMBA, TIMER15_BRKIN, TIMER2_CH1 |
| PB6 | 27 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, USART0_TX, TIMER15_CH0_ON, TSI_G4_IO2 |
| PB7 | 28 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, USART0_RX, TIMER16_CH0_ON,TSI_G4_IO3 |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available on GD32F150G4 devices only.
- (4) Functions are available on GD32F150G8/6 devices.
- (5) Functions are available on GD32F150G8 devices.

2.6.5. GD32F150xx pin alternate functions

Table 2-7. Port A alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|--------------------------------|--|-----------------------------|--------------|---------------------------|-----------------|-----------------------------|---------------|
| PA0 | | USART0_ CTS ⁽¹⁾ USART1_ CTS ⁽²⁾ | TIMER1_ CH0, TIMER1_ ETI | TSI_G0_I O0 | I2C1_SCL ⁽³⁾ | | | CMP0_ O UT |
| PA1 | EVENTO UT | USART0_ RTS ⁽¹⁾ /US ART0_DE ⁽¹⁾ USART1_ RTS ⁽²⁾ /US ART1_DE ⁽²⁾ | TIMER1_ CH1 | TSI_G0_I O1 | I2C1_SDA ⁽³⁾ | | | |
| PA2 | TIMER14 _CH0 | USART0_ TX ⁽¹⁾ USART1_ TX ⁽²⁾ | TIMER1_ CH2 | TSI_G0_I O2 | | | | CMP1_ O UT |
| PA3 | TIMER14 _CH1 | USART0_ RX ⁽¹⁾ USART1_ RX ⁽²⁾ | TIMER1_ CH3 | TSI_G0_I O3 | | | | |
| PA4 | SPI0_NS S/ I2S0_WS | USART0_ CK ⁽¹⁾ USART1_ CK ⁽²⁾ | | TSI_G1_I O0 | TIMER13 _CH0 | | SPI1_NS S ⁽³⁾ | |
| PA5 | SPI0_SC K/ I2S0_CK | CEC | TIMER1_ CH0, TIMER1_ ETI | TSI_G1_I O1 | | | | |
| PA6 | SPI0_MIS O/ I2S0_MC K | TIMER2_ CH0 | TIMER0_ BRKIN | TSI_G1_I O2 | | TIMER15 _CH0 | EVENTO UT | CMP0_ O UT |
| PA7 | SPI0_MO SI/ I2S0_SD | TIMER2_ CH1 | TIMER0_ CH0_ON | TSI_G1_I O3 | TIMER13 _CH0 | TIMER16 _CH0 | EVENTO UT | CMP1_ O UT |
| PA8 | MCO | USART0_ CK | TIMER0_ CH0 | EVENTO UT | USART1_ TX ⁽²⁾ | | | |
| PA9 | TIMER14 _BRKIN | USART0_ TX | TIMER0_ CH1 | TSI_G3_I O1 | I2C0_SCL | | | |

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|--------------------------|--|-----------------------------------|----------------|--------------|-----|------------------------------|--------------|
| PA10 | TIMER16 _BRKIN | USART0_ RX | TIMER0_ CH2 | TSI_G3_I O1 | I2C0_SD A | | | |
| PA11 | EVENTO UT | USART0_ CTS | TIMER0_ CH3 | TSI_G3_I O2 | | | | CMP0_O UT |
| PA12 | EVENTO UT | USART0_ RTS/USA RT0_DE | TIMER0_ ETI | TSI_G3_I O3 | | | | CMP1_O UT |
| PA13 | SWDIO | IFRP_OU T | | | | | SPI1_MIS O ⁽³⁾ | |
| PA14 | SWCLK | USART0_ TX ⁽¹⁾ USART1_ TX ⁽²⁾ | | | | | SPI1_MO SI ⁽³⁾ | |
| PA15 | SPI0_NS S, I2S0_WS | USART0_ RX ⁽¹⁾ USART1_ RX ⁽²⁾ | TIMER1_ CH0, TIMER1_ ETI | EVENTO UT | | | SPI1_NS S ⁽³⁾ | |

Notes:

- (1) Functions are available on GD32F150x4 devices only.
- (2) Functions are available on GD32F150x8/6 devices.
- (3) Functions are available on GD32F150x8 devices.

Table 2-8. Port B alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
|----------|--|-------------------------|--------------------|--------------------|------------------------------|-----|-------------------------|
| PB0 | EVENTO T | TIMER2_C H2 | TIMER0_C H1_ON | TSI_G2_IO 1 | USART1_R X ⁽²⁾ | | |
| PB1 | TIMER13_ CH0 | TIMER2_C H3 | TIMER0_C H2_ON | TSI_G2_IO 2 | | | SPI1_SCK ⁽³⁾ |
| PB2 | | | | TSI_G2_IO 3 | | | |
| PB3 | SPI0_SCK / I2S0_CK | EVENTO T | TIMER1_C H1 | TSI_G4_IO 0 | | | |
| PB4 | SPI0_MISO / I2S0_MCK | TIMER2_C H0 | EVENTO T | TSI_G4_IO 1 | | | |
| PB5 | SPI0_MOSI / I2S0_SD | TIMER2_C H1 | TIMER15_ BRKIN | I2C0_SMB A | | | |
| PB6 | USART0_T X | I2C0_SCL | TIMER15_ CH0_ON | TSI_G4_IO 2 | | | |
| PB7 | USART0_R X | I2C0_SDA | TIMER16_ CH0_ON | TSI_G4_IO 3 | | | |
| PB8 | CEC | I2C0_SCL | TIMER15_ CH0 | TSITG | | | |
| PB9 | IFRP_OUT | I2C0_SDA | TIMER16_ CH0 | EVENTO T | | | |
| PB10 | CEC | I2C1_SCL ⁽³⁾ | TIMER1_C H2 | TSITG | | | |
| PB11 | EVENTO T | I2C1_SDA ⁽³⁾ | TIMER1_C H3 | TSI_G5_IO 0 | | | |
| PB12 | SPI0_NSS ⁽¹⁾ SPI1_NSS ⁽³⁾ | EVENTO T | TIMER0_B RKIN | TSI_G5_IO 1 | I2C1_SMB A ⁽³⁾ | | |
| PB13 | SPI0_SCK ⁽¹⁾ SPI1_SCK ⁽³⁾ | | TIMER0_C H0_ON | TSI_G5_IO 2 | | | |
| PB14 | SPI0_MISO ⁽¹⁾ SPI1_MISO ⁽³⁾ | TIMER14_ CH0 | TIMER0_C H1_ON | TSI_G5_IO 3 | | | |
| PB15 | SPI0_MOSI ⁽¹⁾ SPI1_MOSI ⁽³⁾ | TIMER14_ CH1 | TIMER0_C H2_ON | TIMER14_ CH0_ON | | | |

Notes:

- (1) Functions are available on GD32F150x4 devices only.
- (2) Functions are available on GD32F150x8/6 devices.
- (3) Functions are available on GD32F150x8 devices.

Table 2-9. Port C & D & F alternate functions summary

| Pin Name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 |
|----------|--------------------------|-----|-----|-----|-----|-----|-----|
| PC0 | EVENTO T | | | | | | |
| PC1 | EVENTO T | | | | | | |
| PC2 | EVENTO T | | | | | | |
| PC3 | EVENTO T | | | | | | |
| PC4 | EVENTO T | | | | | | |
| PC5 | TSI_G2_IO 0 | | | | | | |
| PC6 | TIMER2_C H0 | | | | | | |
| PC7 | TIMER2_C H1 | | | | | | |
| PC8 | TIMER2_C H2 | | | | | | |
| PC9 | TIMER2_C H3 | | | | | | |
| PD2 | TIMER2_E TI | | | | | | |
| PF0 | OSCIN | | | | | | |
| PF1 | OSCOU | | | | | | |
| PF4 | SPI1_NSS, EVENTO T | | | | | | |
| PF5 | EVENTO T | | | | | | |

3. Functional description

3.1. Arm® Cortex®-M3 core

The Cortex®-M3 processor is the latest generation of Arm® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit Arm® Cortex®-M3 processor core
- Up to 72 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is based on the Armv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex®-M3:

- Internal Bus Matrix connected with ICode bus, DCode bus, system bus, Private Peripheral Bus (PPB) and debug accesses (AHB-AP)
- Nested Vectored Interrupt Controller (NVIC)
- Flash Patch and Breakpoint (FPB)
- Data Watchpoint and Trace (DWT)
- Instrument Trace Macrocell (ITM)
- Serial Wire JTAG Debug Port (SWJ-DP)
- Trace Port Interface Unit (TPIU)

3.2. On-chip memory

- Up to 64 Kbytes of Flash memory
- The region of the MCU executing instructions without waiting time is up to 32K bytes (in case that the Flash size equal to 16K or 32K, all memory is no waiting time). A long time delay when CPU fetches the instructions out of the range.
- Up to 8 Kbytes of SRAM with hardware parity checking

The Arm® Cortex®-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 64 Kbytes of inner Flash at most, which includes code Flash and data Flash is available for storing programs and data, and there is no waiting time within code Flash area when CPU executes instructions. The [Table 2-2. GD32F150xx memory map](#) shows the memory map of the GD32F150xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control Unit (CCU) provides a range of oscillator and clock functions. These include speed internal RC oscillator and external crystal oscillator, high speed and low speed two types. Several prescalers allow the frequency configuration of the AHB and two APB domains. The maximum frequency of the AHB and two APB domains is 72 MHz. See [Figure 2-6. GD32F150xx clock tree](#) for details on the clock tree.

The Reset Control Unit (RCU) controls three kinds of reset: system reset resets the processor core and peripheral IP components. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from 2.6 V and down to 1.8V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through VDD pins.
- V_{SSA} , V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main Flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

In default condition, boot from main Flash memory is selected. The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10) or USART1 (PA2 and PA3, PA14 and PA15) in device mode.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only the clock of CPU core is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of the high speed crystal oscillator (IRC8M, HXTAL) and PLL are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, and USB wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC's conversion rate is up to 1 MSPS.
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

One 12-bit 1 MSPS multi-channel ADCs are integrated in the device. It is a total of up to 16 multiplexed external channels, 1 channel for internal temperature sensor (V_{SENSE}), 1 channel for internal reference voltage (V_{REFINT}) and 1 channel for battery voltage (V_{BAT}). The input voltage range is between V_{SSA} and V_{DDA} . An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced use.

The ADC can be triggered from the events generated by the general timers (TIMERx, x=1,2,14) and the advanced timers (TIMER0) with internal connection. The temperature sensor can be used to generate a voltage that varies linearly with temperature. It is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

3.7. Digital to analog converter (DAC)

- 12-bit DAC converter of independent output channel
- 8-bit or 12-bit mode in conjunction with the DMA controller

The 12-bit buffered DAC channel is used to generate variable analog outputs. The DAC is designed with integrated resistor strings structure. The DAC channels can be triggered by the timer update outputs or EXTI with DMA support. The maximum output value of the DAC is V_{REF+} .

3.8. DMA

- 7 channel DMA controller
- Peripherals supported: Timers, ADC, SPIs, I²Cs, USARTs, DAC and I²S

The flexible general-purpose DMA controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.9. General-purpose inputs/outputs (GPIOs)

- Up to 55 fast GPIOs, all mappable on 16 external interrupt vectors (EXTI)
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 55 general purpose I/O pins (GPIO) in GD32F150xx, named PA0 ~ PA15 and PB0 ~ PB15, PC0 ~ PC15, PD2, PF0, PF1, PF4-PF7 to implement logic input/output functions. Each of the GPIO ports has related control and configuration registers to satisfy the requirements of specific applications. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current capable except for analog inputs.

3.10. Timers and PWM generation

- One 16-bit advanced-control timer (TIMER0), one 32-bit general-purpose timer (TIMER1), five 16-bit general-purpose timers (TIMER2, TIMER13 ~ TIMER16), and one 16-bit basic timer (TIMER5)
- Up to 4 independent channels of PWM, output compare or input capture for each general-purpose timer (GPTM) and external trigger input
- 16-bit, motor control PWM advanced-control timer with programmable dead-time generation for output match
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (free watchdog timer and window watchdog timer)

The advanced-control timer (TIMER0) can be used as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time generation. It can also be used as a complete general-purpose timer. The 4 independent channels can be used for input capture, output compare, PWM generation (edge-aligned or center-aligned mode) and single pulse mode output. If configured as a general-purpose 16-bit timer, it has the same functions as the TIMEx timer. It can be synchronized with external signals or to interconnect with other GPTMs together which have the same architecture and features.

The general-purpose timer (GPTM) can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM output, up to 4 independent channels for input capture/output compare. TIMER1 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER2 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. TIMER13 ~ TIMER16 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. The GPTM also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5, is mainly used for DAC trigger generation. They can also be used as a simple 16-bit time base.

The GD32F150xx have two watchdog peripherals, free watchdog and window watchdog. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer includes a 12-bit down-counting counter and a 8-bit prescaler, It is clocked from an independent 40 kHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wake up interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.11. Real time clock (RTC)

- Independent binary-coded decimal (BCD) format timer/counter with five 32-bit backup registers.
- Calendar with subsecond, seconds, minutes, hours, week day, date, year and month automatically correction
- Alarm function with wake up from deep-sleep and standby mode capability
- On-the-fly correction for synchronization with master clock. Digital calibration with 1 ppm resolution for compensation of quartz crystal inaccuracy.

The real time clock is an Independent timer which provides a set of continuously running counters in backup registers to provide a real calendar function, and provides an alarm interrupt or an expected interrupt. It is not reset by a system or power reset, or when the device wakes up from standby mode. In the RTC unit, there are two prescalers used for implementing the calendar and other functions. One prescaler is a 7-bit asynchronous prescaler and the other is a 15-bit synchronous prescaler.

3.12. Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 kHz
- Provide arbitration function, optional PEC (packet error checking) generation and checking
- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.13. Serial peripheral interface (SPI)

- Up to two SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.14. Universal synchronous asynchronous receiver transmitter (USART)

- Up to two USARTs with operating speed up to 9 Mbit/s
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- ISO 7816-3 compliant smart card interface

The USART (USART0, USART1) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication.

3.15. Inter-IC sound (I2S)

- One I2S bus Interfaces with sampling frequency from 8 kHz to 192 kHz, multiplexed with SPI1
- Support either master or slave mode

The Inter-IC sound (I2S) bus provides a standard communication interface for digital audio applications by 3-wire serial lines. GD32F150xx contain an I2S-bus interface that can be operated with 16/32 bit resolution in master or slave mode, pin multiplexed with SPI1. The audio sampling frequency from 8 kHz to 192 kHz is supported with less than 0.5% accuracy error.

3.16. HDMI CEC

- Hardware support Consumer Electronics Control (CEC) protocol (HDMI standard rev1.4)

The CEC protocol provides high-level control functions between the audiovisual products linked with HDMI cables. GD32F150xx contain a HDMI-CEC controller which has an Independent clock domain and can wake up the MCU from deep-sleep mode on data reception.

3.17. Universal serial bus full-speed (USBD)

- One full-speed USB Interface with frequency up to 12 Mbit/s
- Internal main PLL for USB CLK compliantly

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between one or more devices. Full-speed peripheral is compliant with the USB 2.0 specification. The device controller enables 12 Mbit/s data exchange with a USB Host controller. Transaction formatting is performed by the hardware, including CRC generation and checking. The status of a completed USB transfer or error condition is indicated by status registers. An interrupt is also generated if enabled. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HXTAL crystal oscillator) and the operating frequency divided from APB1 should be 12 MHz above.

3.18. Touch sensing interface (TSI)

- Supports up to 18 external electrodes by the sensing channels distributed over 6 analog I/O groups
- Programmable charging frequency and I/O pins
- Capability to wake up the MCU from power saving modes

Capacitive sensing technology can be used for the detection of a finger (or any conductive object) presence near an electrode. The capacitive variation of the electrode introduced by the finger can be measured by charging and detecting the voltage across the sampling capacitor. GD32F150xx contain a hardware touch sensing interface (TSI) and only requires few external components to operate. The sensing channels are distributed over 6 analog I/O groups including: Group1 (PA0 ~ PA3), Group2 (PA4 ~ PA7), Group3 (PC5, PB0 ~ PB2), Group4 (PA9 ~ PA12), Group5 (PB3, PB4, PB6, PA7) and Group6 (PB11 ~ PB14),

3.19. Comparators (CMP)

- Two fast rail-to-rail low-power comparators with software configurable
- Programmable reference voltage (internal, external I/O or DAC output pin)

Two Comparators (CMP) are implemented within the devices. Both comparators can wake up from deep-sleep mode to generate interrupts and breaks for the timers and also can be combined as a window comparator. The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

3.20. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The Arm® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.21. Package and operation temperature

- LQFP64 (GD32F150Rx), LQFP48 (GD32F150Cx), QFN32 (GD32F150Kx) and QFN28 (GD32F150Gx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly over the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings⁽¹⁾⁽⁴⁾

| Symbol | Parameter | Min | Max | Unit |
|----------------------|---|-----------------|-----------------|------|
| V_{DD} | External voltage range ⁽²⁾ | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{DDA} | External analog supply voltage | $V_{SSA} - 0.3$ | $V_{SSA} + 3.6$ | V |
| V_{BAT} | External battery supply voltage | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{IN} | Input voltage on 5V tolerant pin ⁽³⁾ | $V_{SS} - 0.3$ | $V_{DD} + 3.6$ | V |
| | Input voltage on other I/O | $V_{SS} - 0.3$ | 3.6 | V |
| $ \Delta V_{DDX} $ | Variations between different VDD power pins | — | 50 | mV |
| $ V_{SSX} - V_{SS} $ | Variations between different ground pins | — | 50 | mV |
| I_{IO} | Maximum current for GPIO pins | — | ± 25 | mA |
| T_A | Operating temperature range | -40 | +85 | °C |
| P_D | Power dissipation at $T_A = 85^\circ\text{C}$ of LQFP64 | — | 629 | mW |
| | Power dissipation at $T_A = 85^\circ\text{C}$ of LQFP48 | — | 621 | |
| | Power dissipation at $T_A = 85^\circ\text{C}$ of QFN32 | — | 825 | |
| | Power dissipation at $T_A = 85^\circ\text{C}$ of QFN28 | — | 605 | |
| T_{STG} | Storage temperature range | -65 | +150 | °C |
| T_J | Maximum junction temperature | — | +125 | °C |

- (1) Guaranteed by design, not tested in production.
- (2) All main power and ground pins should be connected to an external power source within the allowable range.
- (3) V_{IN} maximum value cannot exceed 5.5 V.
- (4) It is recommended that V_{DD} and V_{DDA} are powered by the same source. The maximum difference between V_{DD} and V_{DDA} does not exceed 300 mV during power-up and operation.

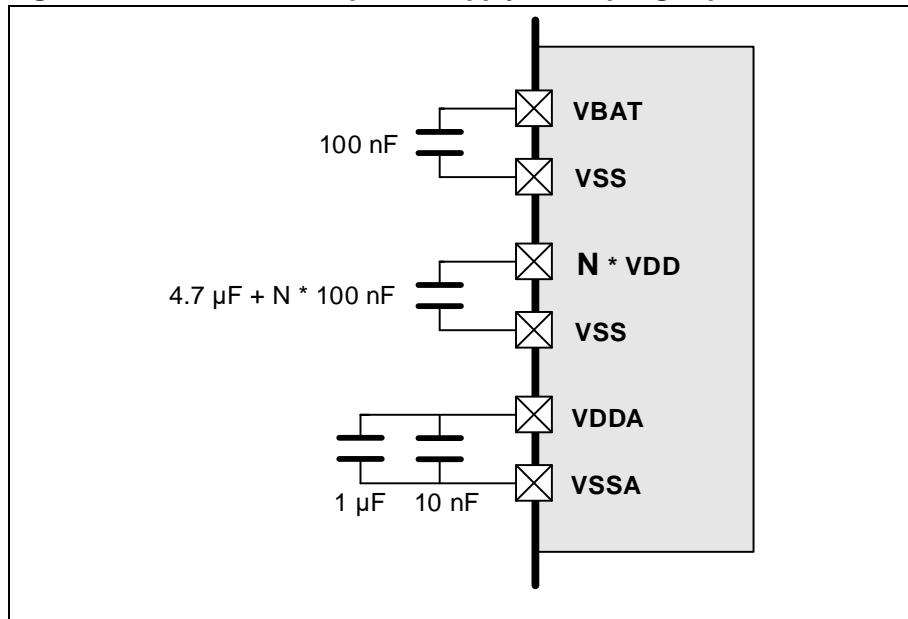
4.2. Operating conditions characteristics

Table 4-2. DC operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max ⁽¹⁾ | Unit |
|-----------|------------------------|------------------|--------------------|-----|--------------------|------|
| V_{DD} | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| V_{DDA} | Analog supply voltage | Same as V_{DD} | 2.6 | 3.3 | 3.6 | V |
| V_{BAT} | Battery supply voltage | — | 1.8 ⁽²⁾ | — | 3.6 | V |

- (1) Based on characterization, not tested in production.
- (2) In the application which V_{BAT} supply the backup domains, if the V_{BAT} voltage drops below the minimum value, when V_{DD} is powered on again, it is necessary to refresh the registers of backup domains and enable LXTAL again.

Figure 4-1. Recommended power supply decoupling capacitors⁽¹⁾



(1) All decoupling capacitors need to be as close as possible to the pins on the PCB board. More details refer to **AN108 GD32F1x0 Hardware Development Guide**.

Table 4-3. Clock frequency⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------|----------------------|------------|-----|-----|------|
| f _{HCLK1} | AHB1 clock frequency | — | — | 72 | MHz |
| f _{HCLK2} | AHB2 clock frequency | — | — | 72 | MHz |
| f _{APB1} | APB1 clock frequency | — | — | 72 | MHz |
| f _{APB2} | APB2 clock frequency | — | — | 72 | MHz |

(1) Guaranteed by design, not tested in production.

Table 4-4. Operating conditions at Power up/ Power down⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--------------------------------|------------|-----|-----|------|
| t _{VDD} | V _{DD} rise time rate | — | 0 | ∞ | μs/v |
| | V _{DD} fall time rate | | 20 | ∞ | |

(1) Guaranteed by design, not tested in production.

Table 4-5. Start-up timings of Operating conditions⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Conditions | Typ | Unit |
|-----------------------|---------------|-------------------------|-----|------|
| t _{start-up} | Start-up time | Clock source from HXTAL | 19 | ms |
| | | Clock source from IRC8M | 19 | ms |

(1) Based on characterization, not tested in production.

(2) After power-up, the start-up time is the time between the rising edge of NRST high and the main function.

(3) PLL is off.

Table 4-6. Power saving mode wakeup timings characteristics⁽¹⁾⁽²⁾

| Symbol | Parameter | Typ | Unit |
|-------------------------|---|-----|------|
| t _{Sleep} | Wakeup from Sleep mode | 3.3 | μs |
| t _{Deep-sleep} | Wakeup from Deep-sleep mode (LDO in run mode) | 4.9 | |
| | Wakeup from Deep-sleep mode (LDO in low power mode) | 4.9 | |
| t _{Standby} | Wakeup from Standby mode | 21 | ms |

- (1) Based on characterization, not tested in production.
(2) The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction under the below conditions: $V_{DD} = V_{DDA} = 3.3\text{ V}$, IRC8M = System clock = 8MHz.

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-7. Power consumption characteristics⁽²⁾⁽³⁾⁽³⁾⁽⁴⁾⁽⁵⁾⁽⁶⁾

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|-----------------------------------|--------------------------------|---|-----|--------------------|-----|------|
| I _{DD} +I _{DDA} | Supply current (Run mode) | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=72 MHz, All peripherals enabled | — | 26.8 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System clock =72 MHz, All peripherals disabled | — | 18.9 | — | mA |
| | | V _{DD} =V _{DDA} =3.3V, HXTAL=8MHz, System clock=48 MHz, All peripherals enabled | — | 18.5 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System clock =48 MHz, All peripherals disabled | — | 13.2 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System clock =36 MHz, All peripherals enabled | — | 14.6 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System Clock =36 MHz, All peripherals disabled | — | 10.5 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System clock =24 MHz, All peripherals enabled | — | 10.3 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System Clock =24 MHz, All peripherals disabled | — | 7.5 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System clock =16 MHz, All peripherals enabled | — | 7.4 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System Clock =16 MHz, All peripherals disabled | — | 5.6 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System clock =8 MHz, All peripherals enabled | — | 4.5 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, System Clock =8 MHz, All peripherals disabled | — | 3.6 | — | mA |
| | Supply current (Sleep mode) | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =72 MHz, All peripherals enabled | — | 15.9 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =72 MHz, All peripherals disabled | — | 6.3 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =48 MHz, All peripherals enabled | — | 11.6 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock | — | 5.1 | — | mA |

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|------------------|----------------------------------|---|-----|--------------------|------|------|
| | | off, System clock =48 MHz, All peripherals disabled | | | | |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =36 MHz, All peripherals enabled | — | 9.1 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =36 MHz, All peripherals disabled | — | 4.2 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =24 MHz, All peripherals enabled | — | 6.6 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =24 MHz, All peripherals disabled | — | 3.4 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =16 MHz, All peripherals enabled | — | 5.0 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =16 MHz, All peripherals disabled | — | 2.8 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =8 MHz, All peripherals enabled | — | 3.3 | — | mA |
| | | V _{DD} = V _{DDA} =3.3V, HXTAL=8MHz, CPU clock off, System clock =8 MHz, All peripherals disabled | — | 2.2 | — | mA |
| | Supply current (Deep-Sleep mode) | V _{DD} = V _{DDA} =3.3V, Regulator in run mode, IRC40K off, RTC off | — | 263 | 1100 | μA |
| | | V _{DD} = V _{DDA} =3.3V, Regulator in low power mode, IRC40K off, RTC off | — | 255 | — | μA |
| | Supply current (Standby mode) | V _{DD} = V _{DDA} =3.3V, LXTAL off, IRC40K on, RTC on | — | 7.3 | — | μA |
| | | V _{DD} = V _{DDA} =3.3V, LXTAL off, IRC40K on, RTC off | — | 6.8 | — | μA |
| | | V _{DD} = V _{DDA} =3.3V, LXTAL off, IRC40K off, RTC off | — | 5.5 | 27.5 | μA |
| I _{BAT} | Battery supply current | V _{DD} and V _{DDA} not available, V _{BAT} =3.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving | — | 2.6 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving | — | 2.4 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =2.6 V, LXTAL on with external crystal, RTC on, LXTAL High driving | — | 1.9 | — | μA |

| Symbol | Parameter | Conditions | Min | Typ ⁽¹⁾ | Max | Unit |
|--------|-----------|--|-----|--------------------|-----|------|
| | | driving | | | | |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =1.8 V, LXTAL on with external crystal, RTC on, LXTAL High driving | — | 1.3 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | — | 2.6 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | — | 2.3 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | — | 1.8 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving | — | 1.3 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | — | 1.5 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | — | 1.4 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =2.6 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | — | 1.2 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving | — | 1.0 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | — | 1.4 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | — | 1.3 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =2.6 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | — | 1.1 | — | μA |
| | | V _{DD} and V _{DDA} not available, V _{BAT} =1.8 V, LXTAL on with external crystal, RTC on, LXTAL Low driving | — | 0.9 | — | μA |

(1) Based on characterization, not tested in production.

(2) Unless otherwise specified, all values given for T_A = 25 °C and test result is mean value.

(3) When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.

(4) When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed,

- using PLL.
- (5) When analog peripheral blocks such as ADCs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.
 - (6) All GPIOs are configured as analog mode except standby mode.

Figure 4-2. Typical supply current consumption in Run mode

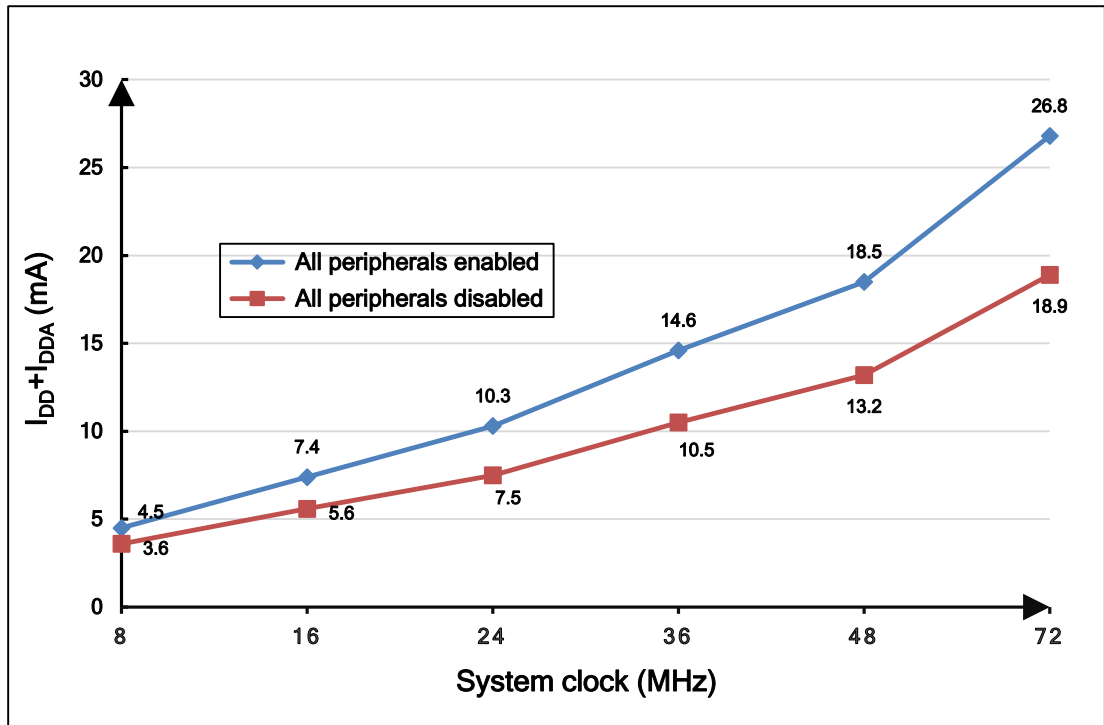
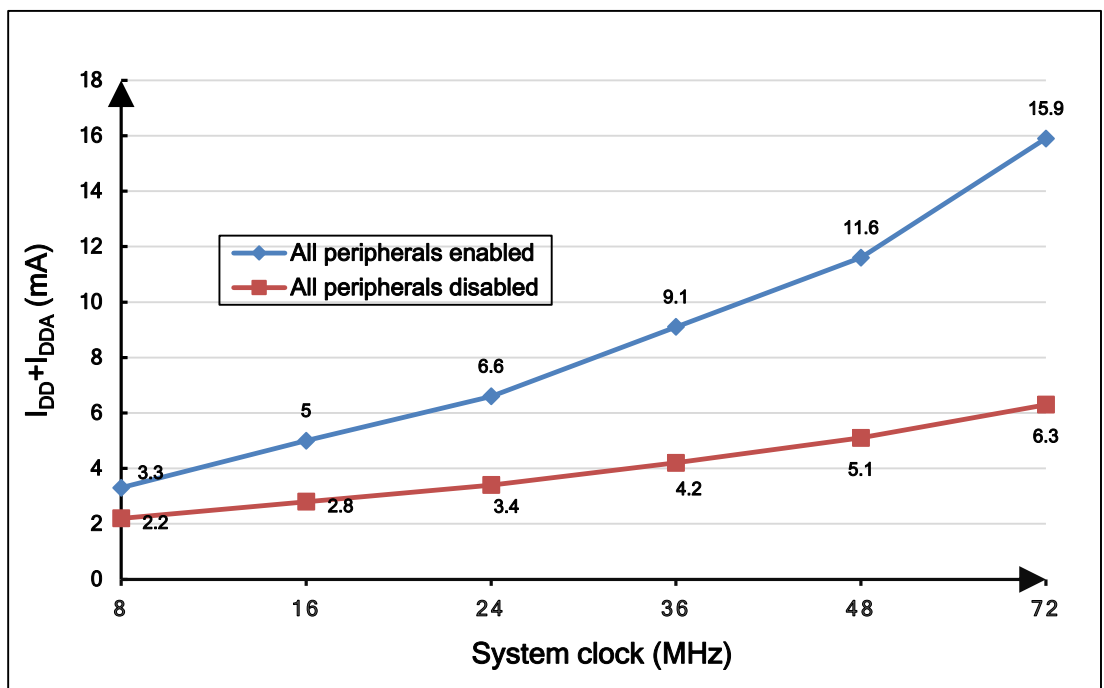


Figure 4-3. Typical supply current consumption in Sleep mode



4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the [Table 4-8. EMS characteristics](#), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-8. EMS characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Level/Class |
|------------------|--|---|-------------|
| V _{ESD} | Voltage applied to all device pins to induce a functional disturbance | V _{DD} = 3.3 V, T _A = +25 °C conforms to IEC 61000-4-2 | 3B |
| V _{FTB} | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on VDD and VSS pins | V _{DD} = 3.3 V, T _A = +25 °C conforms to IEC 61000-4-4 | 4A |

(1) Based on characterization, not tested in production.

EMI (Electromagnetic Interference) emission test result is given in the [Table 4-9. EMI characteristics^{\(1\)}](#), The electromagnetic field emitted by the device are monitored while an application, executing EEMBC code, is running. The test is compliant with SAE J1752-3:2017 standard which specifies the test board and the pin loading.

Table 4-9. EMI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Tested frequency band | Max vs. [f _{HXTAL} /f _{HCLK}] | Unit |
|------------------|------------|---|-----------------------|---|------|
| | | | | 8/72 MHz | |
| S _{EMI} | Peak level | V _{DD} = 3.6 V, T _A = +25 °C, LQFP64, f _{HCLK} = 72 MHz, conforms to SAE J1752-3:2017 | 0.15 to 30 MHz | 8.41 | dBμV |
| | | | 30 to 130 MHz | 8.12 | |
| | | | 130 MHz to 1GHz | 12.84 | |

(1) Based on characterization, not tested in production.

4.5. Power supply supervisor characteristics

Table 4-10. Power supply supervisor characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|-----------------------------------|-------------------------------|-----|-------|-----|------|
| V _{LVD} ⁽¹⁾ | Low Voltage Detector Threshold | LVDT<2:0> = 000(rising edge) | — | 2.123 | — | V |
| | | LVDT<2:0> = 000(falling edge) | — | 2.019 | — | V |
| | | LVDT<2:0> = 001(rising edge) | — | 2.213 | — | V |
| | | LVDT<2:0> = 001(falling edge) | — | 2.181 | — | V |
| | | LVDT<2:0> = 010(rising edge) | — | 2.31 | — | V |
| | | LVDT<2:0> = 010(falling edge) | — | 2.194 | — | V |

| | | | | | | |
|--------------------------------------|----------------------------|-------------------------------|-----------|-------|-----|----|
| | | LVDT<2:0> = 011(rising edge) | — | 2.404 | — | V |
| | | LVDT<2:0> = 011(falling edge) | — | 2.304 | — | V |
| | | LVDT<2:0> = 100(rising edge) | — | 2.505 | — | V |
| | | LVDT<2:0> = 100(falling edge) | — | 2.382 | — | V |
| | | LVDT<2:0> = 101(rising edge) | — | 2.604 | — | V |
| | | LVDT<2:0> = 101(falling edge) | — | 2.498 | — | V |
| | | LVDT<2:0> = 110(rising edge) | — | 2.702 | — | V |
| | | LVDT<2:0> = 110(falling edge) | — | 2.59 | — | V |
| | | LVDT<2:0> = 111(rising edge) | — | 2.803 | — | V |
| | | LVDT<2:0> = 111(falling edge) | — | 2.684 | — | V |
| V _{LVDhyst} ⁽²⁾ | LVD hysteresis | — | — | 100 | — | mV |
| V _{POR} ⁽¹⁾ | Power on reset threshold | PDRVS = 0 | — | 2.4 | — | V |
| V _{PDR} ⁽¹⁾ | Power down reset threshold | | — | 2.35 | — | V |
| V _{PDRhyst} ⁽²⁾ | PDR hysteresis | | — | 0.05 | — | V |
| t _{RSTTEMPO} ⁽²⁾ | Reset temporization | | — | 2 | — | ms |
| V _{POR} ⁽¹⁾ | Power on reset threshold | | PDRVS = 1 | — | 2.4 | — |
| V _{PDR} ⁽¹⁾ | Power down reset threshold | — | | 1.8 | — | V |
| V _{PDRhyst} ⁽²⁾ | PDR hysteresis | — | | 0.6 | — | V |
| t _{RSTTEMPO} ⁽²⁾ | Reset temporization | — | | 2 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-11. ESD characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|---------------------------------------|-----|-----|------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A =25 °C; JS-001-2014 | — | — | 5000 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|-----|------|
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A=25\text{ }^\circ\text{C}$; JS-002-2014 | — | — | 500 | V |

(1) Based on characterization, not tested in production.

Table 4-12. Static latch-up characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|---------------------------|---|-----|-----|-----------|------|
| LU | I-test | $T_A=25\text{ }^\circ\text{C}$; JESD78 | — | — | ± 100 | mA |
| | V_{supply} over voltage | | — | — | 5.4 | V |

(1) Based on characterization, not tested in production.

4.7. External clock characteristics

Table 4-13. High speed crystal oscillator (HXTAL) generated from a crystal/ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|---|-----|-----|-----|------------|
| $f_{HXTAL}^{(1)}$ | High Speed crystal oscillator (HXTAL) frequency | $V_{DD} = 3.3V$ | 4 | 8 | 32 | MHz |
| $R_F^{(2)}$ | Recommended external feedback resistor between XTALIN and XTALOUT | — | — | 200 | — | k Ω |
| $C_{HXTAL}^{(2)(3)}$ | Recommended matching capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| $D_{ucy}^{(HXTAL)(2)}$ | HXTAL oscillator duty cycle | — | 48 | 50 | 52 | % |
| $g_m^{(2)}$ | Oscillator transconductance | Startup | — | 25 | — | mA/V |
| $I_{DDHXTAL}^{(1)}$ | HXTAL oscillator operating current | $V_{DD} = 3.3V, T_A = 25^\circ\text{C}$ | — | 1.1 | — | mA |
| $t_{SUHXTAL}^{(1)}$ | HXTAL oscillator startup time | $V_{DD} = 3.3V, T_A = 25^\circ\text{C}$ | — | 1.5 | — | ms |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{HXTAL1} = C_{HXTAL2} = 2 \times (C_{LOAD} - C_S)$, For C_{HXTAL1} and C_{HXTAL2} , it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S , it is PCB and MCU pin stray capacitance.

Table 4-14. High speed external clock characteristics (HXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|------------------|--------------|-----|--------------|------|
| $f_{HXTAL_ext}^{(1)}$ | External clock source or oscillator frequency | $V_{DD} = 3.3 V$ | 1 | — | 50 | MHz |
| $V_{HXTALH}^{(2)}$ | OSCIN input pin high level voltage | $V_{DD} = 3.3 V$ | $0.7 V_{DD}$ | — | V_{DD} | V |
| $V_{HXTALL}^{(2)}$ | OSCIN input pin low level voltage | | V_{SS} | — | $0.3 V_{DD}$ | V |
| $t_{H/L}^{(HXTAL)(2)}$ | OSCIN high or low time | — | 5 | — | — | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------|-------------------------|------------|-----|-----|-----|------|
| $t_{R/F(HXTAL)}$ ⁽²⁾ | OSCIN rise or fall time | — | — | — | 10 | ns |
| $C_{IN}^{(2)}$ | OSCIN input capacitance | — | — | 5 | — | pF |
| $D_{ucy(HXTAL)}$ ⁽²⁾ | Duty cycle | — | 40 | — | 60 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-15. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--|---------------------------|-----|--------|-----|-----------|
| $f_{LXTAL}^{(1)}$ | Low Speed crystal oscillator (LXTAL) frequency | $V_{DD} = 3.3V$ | — | 32.768 | — | KHz |
| $C_{LXTAL}^{(2)(3)}$ | Recommended load capacitance on OSC32IN and OSC32OUT | — | — | 10 | — | pF |
| $D_{ucy(LXTAL)}^{(2)}$ | LXTAL oscillator duty cycle | — | 48 | 50 | 52 | % |
| $g_m^{(2)}$ | Oscillator transconductance | Lower driving capability | — | 4 | — | $\mu A/V$ |
| | | Higher driving capability | — | 18 | — | |
| $I_{DDLXTAL}^{(1)}$ | LXTAL oscillator operating current | Lower driving capability | — | 0.9 | — | μA |
| | | Higher driving capability | — | 1.9 | — | |
| $t_{SULXTAL}^{(1)(4)}$ | LXTAL oscillator startup time | Lower driving capability | — | 1.36 | — | s |
| | | Higher driving capability | — | 0.55 | — | s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) $C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S)$, For C_{LXTAL1} and C_{LXTAL2} , it is recommended matching capacitance on OSC32IN and OSC32OUT. For C_{LOAD} , it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S , it is PCB and MCU pin stray capacitance.

(4) $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4-16. Low speed external user clock characteristics (LXTAL in bypass mode)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|------------------|--------------|--------|--------------|------|
| $f_{LXTAL_ext}^{(1)}$ | External clock source or oscillator frequency | $V_{DD} = 3.3 V$ | — | 32.768 | 1000 | KHz |
| $V_{LXTALH}^{(2)}$ | OSC32IN input pin high level voltage | — | $0.7 V_{DD}$ | — | V_{DD} | V |
| $V_{LXTALL}^{(2)}$ | OSC32IN input pin low level voltage | — | V_{SS} | — | $0.3 V_{DD}$ | |
| $t_{H/L(LXTAL)}^{(2)}$ | OSC32IN high or low time | — | 450 | — | — | ns |
| $t_{R/F(LXTAL)}^{(2)}$ | OSC32IN rise or fall time | — | — | — | 50 | |
| $C_{IN}^{(2)}$ | OSC32IN input capacitance | — | — | 5 | — | pF |
| $D_{ucy(LXTAL)}^{(2)}$ | Duty cycle | — | 30 | 50 | 70 | % |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.8. Internal clock characteristics

Table 4-17. Internal 8 MHz RC oscillator (IRC8M) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|------|----------|------|---------|
| f_{IRC8M} | Internal 8 MHz RC oscillator (IRC8M) frequency | $V_{DD}=V_{DDA}=3.3V$ | — | 8 | — | MHz |
| ACC_{IRC8M} | IRC8M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}=V_{DDA}=3.3V$, $T_A=-40^{\circ}C \sim +85^{\circ}C$ | — | -1.7~1.4 | — | % |
| | | $V_{DD}=V_{DDA}=3.3V$, $T_A=25^{\circ}C$ | -1.0 | — | +1.0 | % |
| | IRC8M oscillator Frequency accuracy, User trimming step ⁽¹⁾ | — | — | 0.5 | — | % |
| $Ducy_{IRC8M}^{(2)}$ | IRC8M oscillator duty cycle | $V_{DD}=V_{DDA}=3.3V$, $f_{IRC8M}=8MHz$ | 48 | 50 | 52 | % |
| $I_{DDIRC8M}$ $+I_{DDAIRC8M}^{(1)}$ | IRC8M oscillator operating current | $V_{DD}=V_{DDA}=3.3V$, $f_{IRC8M}=8MHz$ | — | 39 | — | μA |
| $t_{SUIRC8M}^{(1)}$ | IRC8M oscillator startup time | $V_{DD}=V_{DDA}=3.3V$, $f_{IRC8M}=8MHz$ | — | 3.6 | — | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Table 4-18. Internal 40KHz RC oscillator (IRC40K) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|---|-----|-------|-----|---------|
| $f_{IRC40K}^{(1)}$ | Internal 40KHz RC oscillator (IRC40K) frequency | $V_{DD}=V_{DDA}=3.3V$ | 25 | 40 | 60 | KHz |
| $I_{DDIRC40KI}$ $+I_{DDAIRC40KI}^{(2)}$ | IRC40K oscillator operating current | $V_{DD}=V_{DDA}=3.3V$, $T_A=25^{\circ}C$ | — | 1.3 | — | μA |
| $t_{SUIRC40K}^{(2)}$ | IRC40K oscillator startup time | $V_{DD}=V_{DDA}=3.3V$, $T_A=25^{\circ}C$ | — | 115.7 | — | μs |

(1) Guaranteed by design, not tested in production.

(2) Based on characterization, not tested in production.

Table 4-19. High speed internal clock (IRC14M) characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|------|------------|------|------|
| f_{IRC14M} | Internal 14 MHz RC oscillator (IRC14M) frequency | $V_{DD}=V_{DDA}=3.3V$ | — | 14 | — | MHz |
| ACC_{IRC14M} | IRC14M oscillator Frequency accuracy, Factory-trimmed | $V_{DD}=V_{DDA}=3.3V$, $T_A=-40^{\circ}C \sim +85^{\circ}C$ | — | -0.9~0.029 | — | % |
| | | $V_{DD}=V_{DDA}=3.3V$, $T_A=25^{\circ}C$ | -1.0 | — | +1.0 | % |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|-----|-----|-----|------|
| | IRC14M oscillator Frequency accuracy, User trimming step ⁽¹⁾ | — | — | 0.5 | — | % |
| D _{IRC14M} ⁽²⁾ | IRC14M oscillator duty cycle | V _{DD} =V _{DDA} =3.3V, f _{IRC14M} =14MHz | 48 | 50 | 52 | % |
| I _{DDIRC14M} +I _{DDAIRC14M} ⁽¹⁾ | IRC14M oscillator operating current | V _{DD} =V _{DDA} =3.3V, f _{IRC14M} =14MHz | — | 54 | — | μA |
| t _{SUIRC14M} ⁽¹⁾ | IRC14M oscillator startup time | V _{DD} =V _{DDA} =3.3V, f _{IRC14M} =14MHz | — | 2.9 | — | us |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.9. PLL characteristics

Table 4-20. PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|-------------------|-----|-------|-----|------|
| f _{PLLIN} ⁽¹⁾ | PLL input clock frequency | — | 1 | — | 25 | MHz |
| f _{PLLOUT} ⁽²⁾ | PLL output clock frequency | — | 16 | — | 72 | MHz |
| f _{VCO} ⁽²⁾ | PLL VCO output clock frequency | — | — | — | 72 | MHz |
| t _{LOCK} ⁽²⁾ | PLL lock time | — | — | — | 300 | μs |
| I _{DDA} ⁽¹⁾ | Current consumption on V _{DDA} | VCO freq = 72 MHz | — | 270 | — | μA |
| Jitter _{PLL} ⁽¹⁾⁽³⁾ | Cycle to cycle Jitter (rms) | System clock | — | 32.1 | — | ps |
| | Cycle to cycle Jitter (peak to peak) | | — | 255.6 | — | |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

(3) Value given with main PLL running.

4.10. Memory characteristics

Table 4-21. Flash memory characteristics

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|--------------------|---|----------------------------------|--------------------|--------------------|--------------------|---------|
| P _{ECYC} | Number of guaranteed program /erase cycles before failure (Endurance) | T _A = -40 °C ~ +85 °C | 100 | — | — | kcycles |
| t _{RET} | Data retention time | — | — | 20 | — | years |
| t _{PROG} | Word programming time | T _A = -40°C ~ +85 °C | — | 37.5 | 105 | μs |
| t _{ERASE} | Page erase time | T _A = -40°C ~ +85 °C | — | 50 | 400 | ms |

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ ⁽¹⁾ | Max ⁽²⁾ | Unit |
|-------------------------|-----------------|--|--------------------|--------------------|--------------------|------|
| $t_{MERASE(16K)}^{(2)}$ | Mass erase time | $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | — | 0.3 | 3 | s |
| $t_{MERASE(32K)}^{(2)}$ | Mass erase time | $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | — | 0.6 | 6 | s |
| $t_{MERASE(64K)}^{(2)}$ | Mass erase time | $T_A = -40^{\circ}\text{C} \sim +85^{\circ}\text{C}$ | — | 1.2 | 12 | s |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.11. NRST pin characteristics

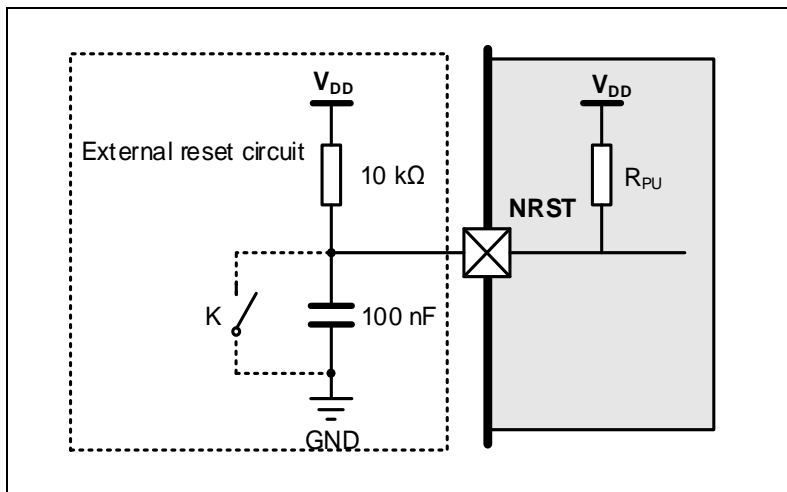
Table 4-22. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|------------------------------------|-----------------------------------|--------------|-----|----------------|------------|
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD} = V_{DDA} = 2.6\text{ V}$ | -0.3 | — | $0.3 V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | $0.7 V_{DD}$ | — | $V_{DD} + 0.3$ | |
| $V_{hyst}^{(2)}$ | Schmidt trigger Voltage hysteresis | | — | 330 | — | |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD} = V_{DDA} = 3.3\text{ V}$ | -0.3 | — | $0.3 V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | $0.7 V_{DD}$ | — | $V_{DD} + 0.3$ | |
| $V_{hyst}^{(2)}$ | Schmidt trigger Voltage hysteresis | | — | 340 | — | |
| $V_{IL(NRST)}^{(1)}$ | NRST Input low level voltage | $V_{DD} = V_{DDA} = 3.6\text{ V}$ | -0.3 | — | $0.3 V_{DD}$ | V |
| $V_{IH(NRST)}^{(1)}$ | NRST Input high level voltage | | $0.7 V_{DD}$ | — | $V_{DD} + 0.3$ | |
| $V_{hyst}^{(2)}$ | Schmidt trigger Voltage hysteresis | | — | 350 | — | |
| $R_{pu}^{(2)}$ | Pull-up equivalent resistor | — | — | 40 | — | k Ω |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

Figure 4-4. Recommended external NRST pin circuit⁽¹⁾



(1) Unless the voltage on NRST pin go below $V_{IL(NRST)}$ level, the device would not generate a reliable reset.

4.12. GPIO characteristics

Table 4-23. I/O port DC characteristics⁽¹⁾⁽³⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-----------------------|--|-----|-----|--------------|------|
| V_{IL} | Standard IO Low level | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | — | — | $0.3 V_{DD}$ | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--|--|--------------|------|--------------|------|
| V_{IH} | input voltage | | | | | |
| | 5V-tolerant IO Low level input voltage | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | — | — | $0.3 V_{DD}$ | |
| | Standard IO High level input voltage | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | $0.7 V_{DD}$ | — | — | |
| | 5 V-tolerant IO High level input voltage | $2.6\text{ V} \leq V_{DD} = V_{DDA} \leq 3.3\text{ V}$ | $0.7 V_{DD}$ | — | — | |
| IO_speed=50MHz | | | | | | |
| V_{OL} | Low level output voltage for an IO Pin ($I_{IO} = +8\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 0.24 | — | V |
| | | $V_{DD} = 3.3\text{ V}$ | — | 0.21 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 0.2 | — | |
| | Low level output voltage for an IO Pin ($I_{IO} = +20\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 0.66 | — | |
| | | $V_{DD} = 3.3\text{ V}$ | — | 0.56 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 0.54 | — | |
| V_{OH} | High level output voltage for an IO Pin ($I_{IO} = +8\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 2.25 | — | V |
| | | $V_{DD} = 3.3\text{ V}$ | | 2.94 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 3.23 | — | |
| | High level output voltage for an IO Pin ($I_{IO} = +20\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 2.16 | — | |
| | | $V_{DD} = 3.3\text{ V}$ | — | 2.36 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | | 2.83 | — | |
| IO_speed=10MHz | | | | | | |
| V_{OL} | Low level output voltage for an IO Pin ($I_{IO} = +4\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 0.35 | — | V |
| | | $V_{DD} = 3.3\text{ V}$ | | 0.29 | | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 0.28 | — | |
| | Low level output voltage for an IO Pin ($I_{IO} = +10\text{ mA}$) | $V_{DD} = 3.3\text{ V}$ | — | 0.82 | — | |
| V_{OH} | High level output voltage for an IO Pin ($I_{IO} = +4\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 2.21 | — | V |
| | | $V_{DD} = 3.3\text{ V}$ | — | 2.96 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 3.28 | — | |
| | High level output voltage for an IO Pin ($I_{IO} = +10\text{ mA}$) | $V_{DD} = 3.3\text{ V}$ | — | 2.49 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 2.85 | — | |
| IO_speed=2MHz | | | | | | |
| V_{OL} | Low level output voltage for an IO Pin ($I_{IO} = +4\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 0.91 | — | V |
| | | $V_{DD} = 3.3\text{ V}$ | — | 0.72 | — | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 0.69 | — | |
| V_{OH} | High level output voltage for an IO Pin ($I_{IO} = +4\text{ mA}$) | $V_{DD} = 2.6\text{ V}$ | — | 1.75 | — | |
| | | $V_{DD} = 3.3\text{ V}$ | | 2.70 | | |
| | | $V_{DD} = 3.6\text{ V}$ | — | 3.04 | — | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-----------------------------|-----------------|-----|-----|-----|------------|
| $R_{PU}^{(2)}$ | Internal pull-up resistor | $V_{IN}=V_{SS}$ | — | 40 | — | k Ω |
| $R_{PD}^{(2)}$ | Internal pull-down resistor | $V_{IN}=V_{DD}$ | — | 40 | — | k Ω |

- (1) Based on characterization, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) All pins except PC13 / PC14 / PC15. Since PC13 to PC15 are supplied through the Power Switch, which can only be obtained by a small current (typical source capability:3 mA shared between these IOs, but sink capability is same as other IO), the speed of GPIOs PC13 to PC15 should not exceed 2 MHz when they are in output mode(maximum load: 30 pF).

Table 4-24. I/O port AC characteristics⁽¹⁾⁽²⁾⁽⁴⁾

| GPIOx_OSPDy[1:0] bit value ⁽³⁾ | Parameter | Conditions | Typ | Unit |
|---|---------------------|---|------|------|
| GPIOx_OSPDy [1:0] = X0 (IO_Speed = 2 MHz) | T_{Rise}/T_{Fall} | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 10 pF$ | 65.2 | ns |
| | | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 30 pF$ | 55.4 | |
| | | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 50 pF$ | 45 | |
| GPIOx_OSPDy [1:0] = 01 (IO_Speed = 10 MHz) | T_{Rise}/T_{Fall} | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 10 pF$ | 18.4 | ns |
| | | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 30 pF$ | 25.6 | |
| | | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 50 pF$ | 30.4 | |
| GPIOx_OSPDy [1:0] = 11 (IO_Speed = 50 MHz) | T_{Rise}/T_{Fall} | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 10 pF$ | 2.6 | ns |
| | | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 30 pF$ | 3.4 | |
| | | $2.6 \leq V_{DD} \leq 3.6 V, C_L = 50 pF$ | 4.8 | |

- (1) Based on characterization, not tested in production.
(2) Unless otherwise specified, all test results given for $T_A = 25 \text{ }^\circ\text{C}$.
(3) The I/O speed is configured using the GPIOx_CTL -> MDy[1:0] bits.
(4) Only for reference, Depending on user's design.

4.13. ADC characteristics

Table 4-25. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|---------------------------------|------|-------|-----------|---------------|
| $V_{DDA}^{(1)}$ | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{IN}^{(1)}$ | ADC input voltage range | 16 external; 3 internal | 0 | — | V_{DDA} | V |
| $f_{ADC}^{(1)}$ | ADC clock | — | 0.6 | — | 14 | MHz |
| $f_s^{(1)}$ | Sampling rate | 12-bit | 0.04 | — | 1 | MSPS |
| $R_{AIN}^{(2)}$ | External input impedance | See Equation 1 | — | — | 54.8 | k Ω |
| $R_{ADC}^{(2)}$ | Input sampling switch resistance | — | — | — | 0.2 | k Ω |
| $C_{ADC}^{(2)}$ | Input sampling capacitance | No pin/pad capacitance included | — | 32 | — | pF |
| $t_{CAL}^{(2)}$ | Calibration time | $f_{ADC} = 14 \text{ MHz}$ | — | 5.928 | — | μs |
| $t_s^{(2)}$ | Sampling time | $f_{ADC} = 14 \text{ MHz}$ | 0.11 | — | 17.11 | μs |
| $t_{CONV}^{(2)}$ | Total conversion time(including sampling | 12-bit | — | 14 | — | $1/f_{ADC}$ |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--------------|------------|-----|-----|-----|---------|
| | time) | | | | | |
| $t_{SU}^{(2)}$ | Startup time | — | — | — | 1 | μs |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

$$\text{Equation 1: } R_{AIN \text{ max formula}} \quad R_{AIN} < \frac{T_s}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N=12 (from 12-bit resolution).

Table 4-26. ADC $R_{AIN \text{ max}}$ for $f_{ADC}=14 \text{ MHz}$

| T_s (cycles) | t_s (μs) | $R_{AIN \text{ max}}$ (k Ω) |
|----------------|-------------------|-------------------------------------|
| 1.5 | 0.11 | 0.14 |
| 7.5 | 0.54 | 1.5 |
| 13.5 | 0.96 | 2.9 |
| 28.5 | 2.04 | 6.3 |
| 41.5 | 2.96 | 9.3 |
| 55.5 | 3.96 | 12.5 |
| 71.5 | 5.11 | 16.2 |
| 239.5 | 17.11 | 54.8 |

4.14. Temperature sensor characteristics

Table 4-27. Temperature sensor characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|--|-----|-----------|-----|-----------------|
| T_L | VSENSE linearity with temperature | — | ± 1.5 | — | $^{\circ}C$ |
| Avg_Slope | Average slope | — | 4.1 | — | mV/ $^{\circ}C$ |
| V_{25} | Voltage at 25 $^{\circ}C$ | — | 1.45 | — | V |
| $t_{S_temp}^{(2)}$ | ADC sampling time when reading the temperature | — | 17.1 | — | μs |

(1) Based on characterization, not tested in production.

(2) Shortest sampling time can be determined in the application by multiple iterations.

4.15. DAC characteristics

Table 4-28. DAC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------|-------------------------------|-----|-----------|-----------|------------|
| $V_{DDA}^{(1)}$ | Operating voltage | — | 2.6 | 3.3 | 3.6 | V |
| $V_{REFP}^{(2)}$ | Positive Reference Voltage | — | 2.6 | — | V_{DDA} | V |
| $V_{REFN}^{(2)}$ | Negative Reference Voltage | — | — | V_{SSA} | — | V |
| $R_{LOAD}^{(2)}$ | Load resistance | Resistive load with buffer ON | 5 | — | — | k Ω |
| $R_o^{(2)}$ | Impedance output with | — | — | — | 15 | k Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|--|-----|-----|----------------|------|
| | buffer OFF | | | | | |
| $C_{LOAD}^{(2)}$ | Load capacitance | No pin/pad capacitance included | — | — | 50 | pF |
| DAC_OUT min ⁽²⁾ | Lower DAC_OUT voltage with buffer ON | — | 0.2 | — | — | V |
| DAC_OUT max ⁽²⁾ | Higher DAC_OUT voltage with buffer ON | — | — | — | $V_{DDA}-0.2$ | V |
| DAC_OUT min ⁽²⁾ | Lower DAC_OUT voltage with buffer OFF | — | — | 0.5 | — | mV |
| DAC_OUT max ⁽²⁾ | Higher DAC_OUT voltage with buffer OFF | — | — | — | $V_{DDA}-1LSB$ | V |
| $T_{wakeup}^{(2)}$ | Wakeup from off state | — | — | 5 | 10 | μs |
| Update rate ⁽²⁾ | Max frequency for a correct DAC_OUT change from code i to $i \pm 1LSBs$ | $C_{LOAD} \leq 50 \text{ pF}, R_{LOAD} \geq 5 \text{ k}\Omega$ | — | — | 4 | MS/s |
| PSRR ⁽²⁾ | Power supply rejection ratio (to V_{DDA}) | — | 55 | 80 | — | dB |

(1) Based on characterization, not tested in production.

(2) Guaranteed by design, not tested in production.

4.16. I2C characteristics

Table 4-29. I2C characteristics ^{(1) (2) (3)}

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|------------------|---|------------|------------------|------|-----------|-----|------|
| | | | Min | Max | Min | Max | |
| $t_{SCL(H)}$ | SCL clock high time | — | 4.0 | — | 0.6 | — | μs |
| $t_{SCL(L)}$ | SCL clock low time | — | 4.7 | — | 1.3 | — | μs |
| $t_{SU(SDA)}$ | SDA setup time | — | 250 | — | 100 | — | ns |
| $t_{H(SDA)}$ | SDA data hold time | — | 0 ⁽³⁾ | 3450 | 0 | 900 | ns |
| $t_{R(SDA/SCL)}$ | SDA and SCL rise time | — | — | 1000 | — | 300 | ns |
| $t_{F(SDA/SCL)}$ | SDA and SCL fall time | — | — | 300 | — | 300 | ns |
| $t_{H(STA)}$ | Start condition hold time | — | 4.0 | — | 0.6 | — | μs |
| $t_{SU(STA)}$ | Repeated Start condition setup time | — | 4.7 | — | 0.6 | — | μs |
| $t_{SU(STO)}$ | Stop condition setup time | — | 4.0 | — | 0.6 | — | μs |
| t_{BUFF} | Stop to Start condition time (bus free) | — | 4.7 | — | 1.3 | — | μs |

(1) Guaranteed by design, not tested in production.

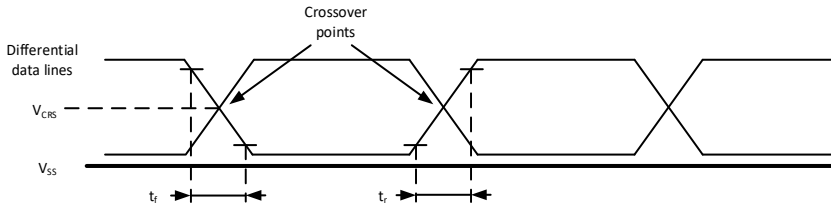
(2) To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz. To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz.

(3) The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

| | | | | | | |
|------------------|---------------------------------|------------|-----|---|-----|----|
| V _{CRS} | Output signal crossover voltage | — | 1.3 | — | 2.0 | V |
| t _R | Rise time | CL = 50 pF | 4 | 5 | 20 | ns |

(1) Guaranteed by design, not tested in production.

Figure 4-6. USB D timings: definition of data signal rise and fall time



4.19. TIMER characteristics

Table 4-34. TIMER characteristics ⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------------|---|---------------------------------|--------|---------------------------|------------------------|
| t _{res} | Timer resolution time | — | 1 | — | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 72 MHz | 13.9 | — | ns |
| f _{EXT} | Timer external clock frequency | — | 0 | f _{TIMERxCLK} /2 | MHz |
| | | f _{TIMERxCLK} = 72 MHz | 0 | 36 | MHz |
| RES | Timer resolution | — | — | 16 | bit |
| t _{COUNTER} | 16-bit counter clock period when internal clock is selected | — | 1 | 65536 | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 72 MHz | 0.0139 | 910 | μs |
| t _{MAX_COUNT} | Maximum possible count | — | — | 65536 × 65536 | t _{TIMERxCLK} |
| | | f _{TIMERxCLK} = 72 MHz | — | 59.6 | s |

(1) Guaranteed by design, not tested in production.

4.20. WDG_T characteristics

Table 4-35. FWDGT min/max timeout period at 40 kHz (IRC40K) ⁽¹⁾

| Prescaler divider | PR[2:0] bits | Min timeout RLD[11:0] = 0x000 | Max timeout RLD[11:0] = 0xFFF | Unit |
|-------------------|--------------|-------------------------------|-------------------------------|------|
| 1/4 | 000 | 0.025 | 409.525 | ms |
| 1/8 | 001 | 0.025 | 819.025 | |
| 1/16 | 010 | 0.025 | 1638.025 | |
| 1/32 | 011 | 0.025 | 3276.025 | |
| 1/64 | 100 | 0.025 | 6552.025 | |
| 1/128 | 101 | 0.025 | 13104.025 | |
| 1/256 | 110 or 111 | 0.025 | 26208.025 | |

(1) Guaranteed by design, not tested in production.

Table 4-36. WWDGT min-max timeout value at 36 MHz (f_{PCLK1})⁽¹⁾

| Prescaler divider | PSC[1:0] | Min timeout value CNT[6:0] = 0x40 | Unit | Max timeout value CNT[6:0] = 0x7F | Unit |
|-------------------|----------|--------------------------------------|------|--------------------------------------|------|
| 1/1 | 00 | 56.89 | μs | 3.64 | ms |
| 1/2 | 01 | 113.78 | | 7.28 | |
| 1/4 | 10 | 227.56 | | 14.56 | |
| 1/8 | 11 | 455.11 | | 29.13 | |

(1) Guaranteed by design, not tested in production.

4.21. Parameter conditions

Unless otherwise specified, all values given for $V_{DD} = V_{DDA} = 3.3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$.

5. Package information

5.1. LQFP64 package outline dimensions

Figure 5-1. LQFP64 package outline

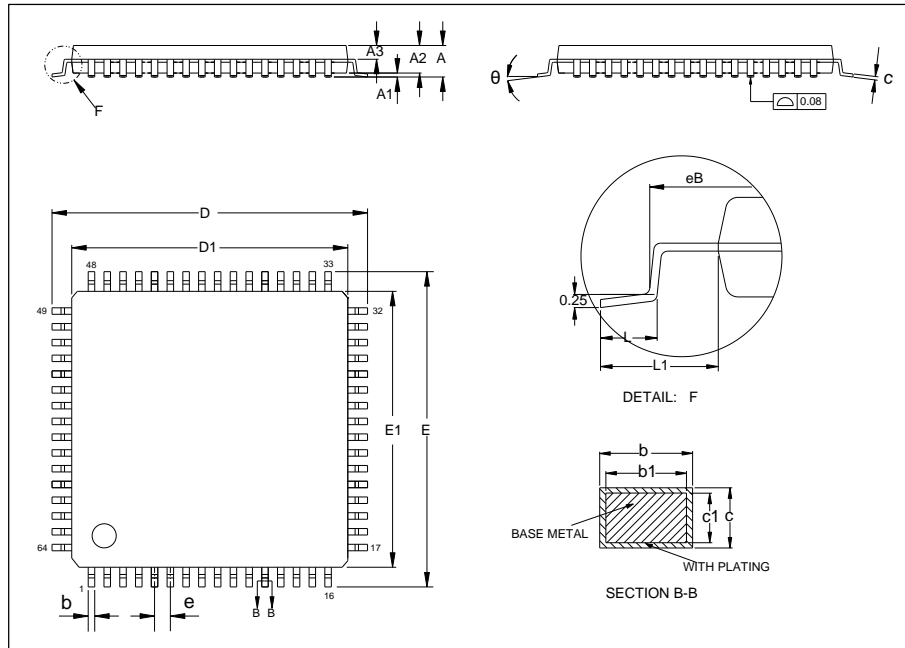
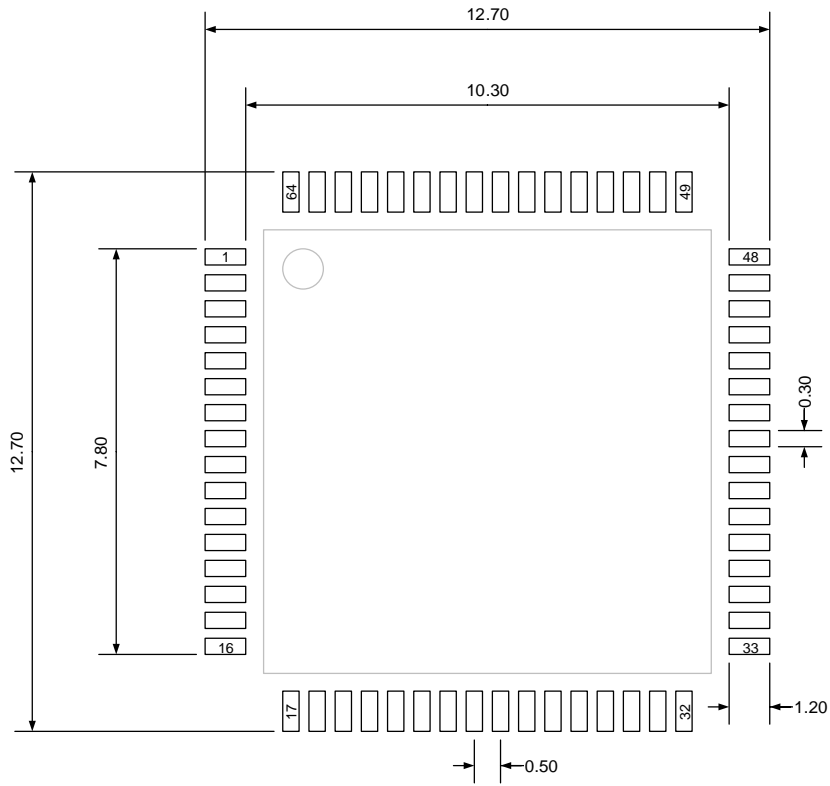


Table 5-1. LQFP64 package dimensions

| Symbol | Min | Typ | Max |
|--------|-------|-------|-------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | — | 0.50 | — |
| eB | 11.25 | — | 11.45 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-2. LQFP64 recommended footprint



(Original dimensions are in millimeters)

5.2. LQFP48 package outline dimensions

Figure 5-3. LQFP48 package outline

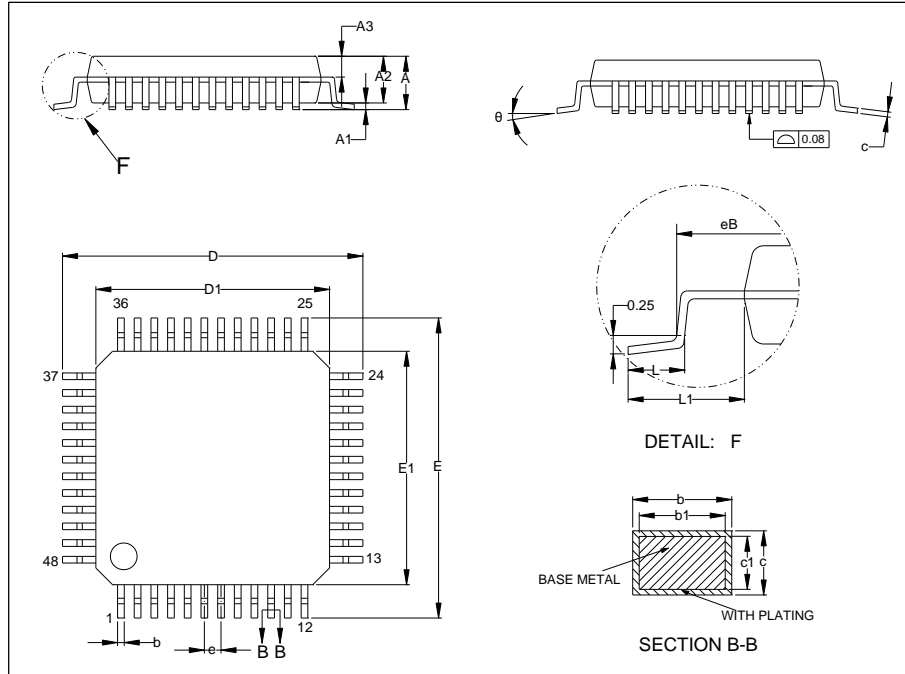
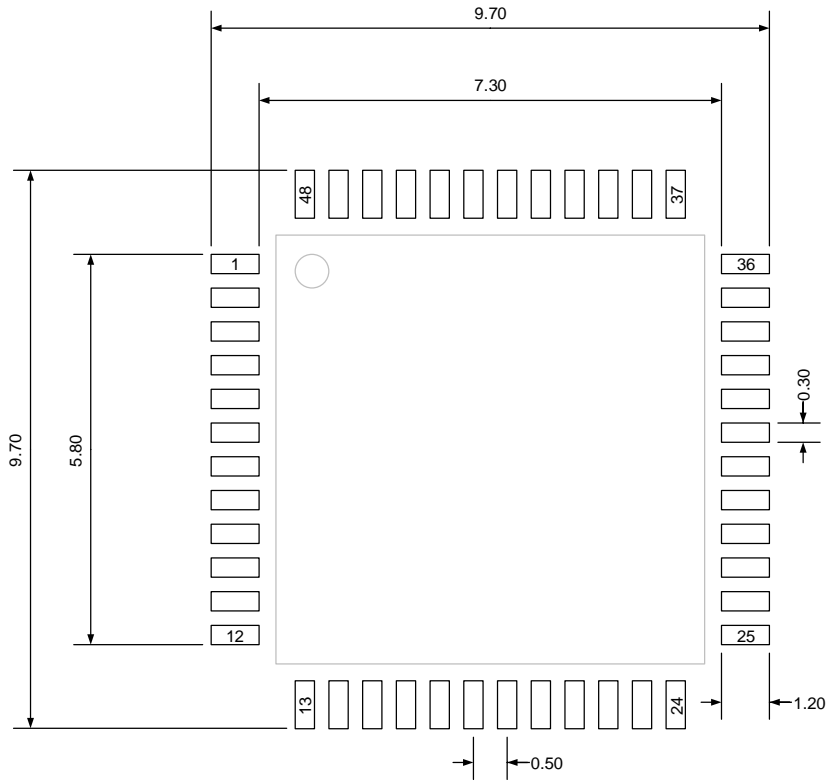


Table 5-2. LQFP48 package dimensions

| Symbol | Min | Typ | Max |
|----------|------|------|------|
| A | — | — | 1.60 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | — | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | — | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | — | 0.50 | — |
| eB | 8.10 | — | 8.25 |
| L | 0.45 | — | 0.75 |
| L1 | — | 1.00 | — |
| θ | 0° | — | 7° |

(Original dimensions are in millimeters)

Figure 5-4. LQFP48 recommended footprint



(Original dimensions are in millimeters)

5.3. QFN32 package outline dimensions

Figure 5-5. QFN32 package outline

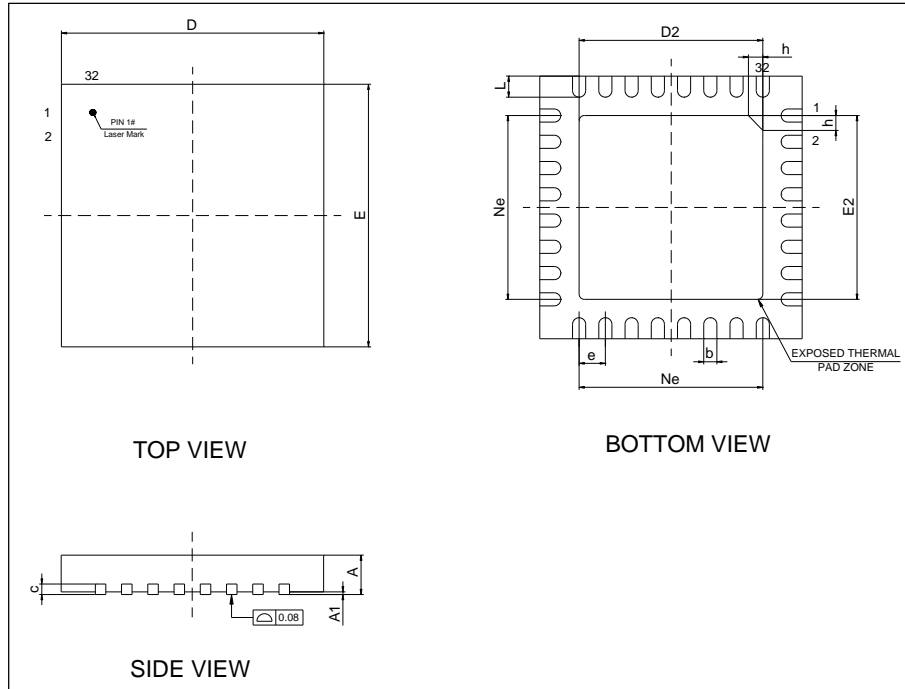
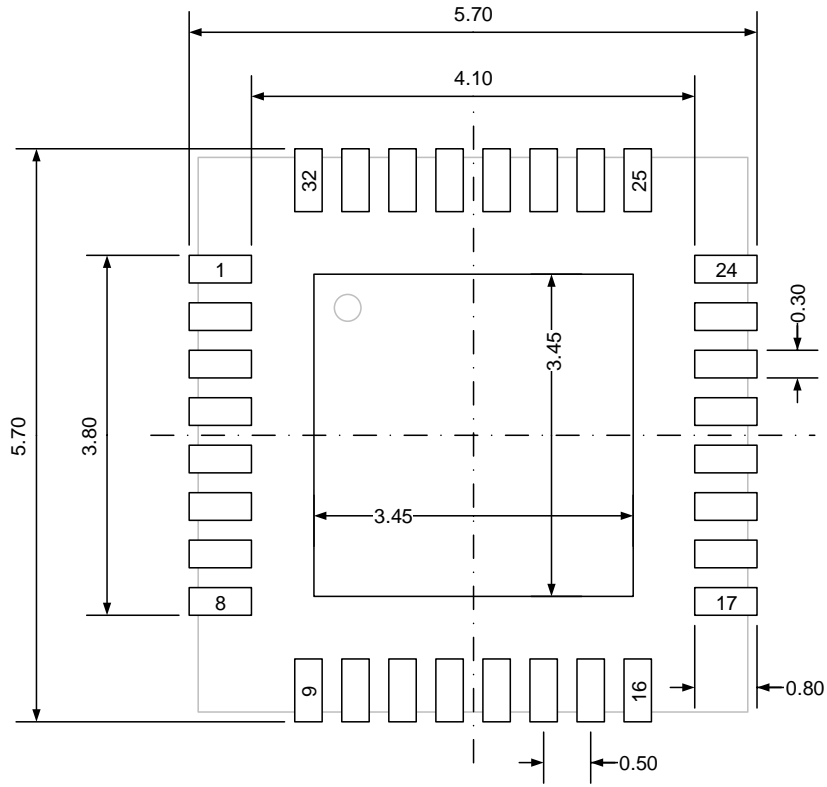


Table 5-3. QFN32 package dimensions

| Symbol | Min | Typ | Max |
|--------|------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.18 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.40 | 3.50 | 3.60 |
| e | — | 0.50 | — |
| h | 0.30 | 0.35 | 0.40 |
| L | 0.35 | 0.40 | 0.45 |
| Ne | — | 3.50 | — |

(Original dimensions are in millimeters)

Figure 5-6. QFN32 recommended footprint



(Original dimensions are in millimeters)

5.4. QFN28 package outline dimensions

Figure 5-7. QFN28 package outline

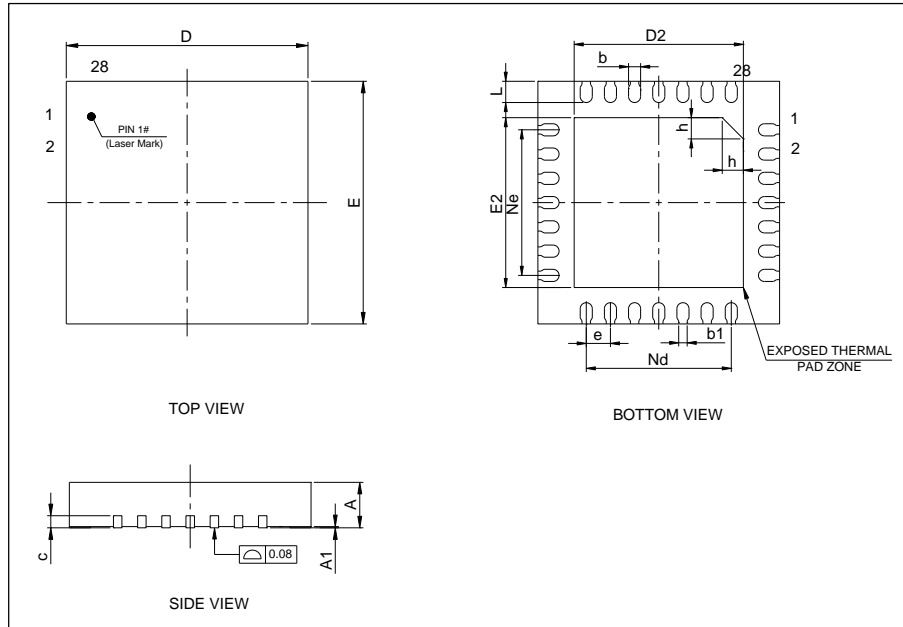
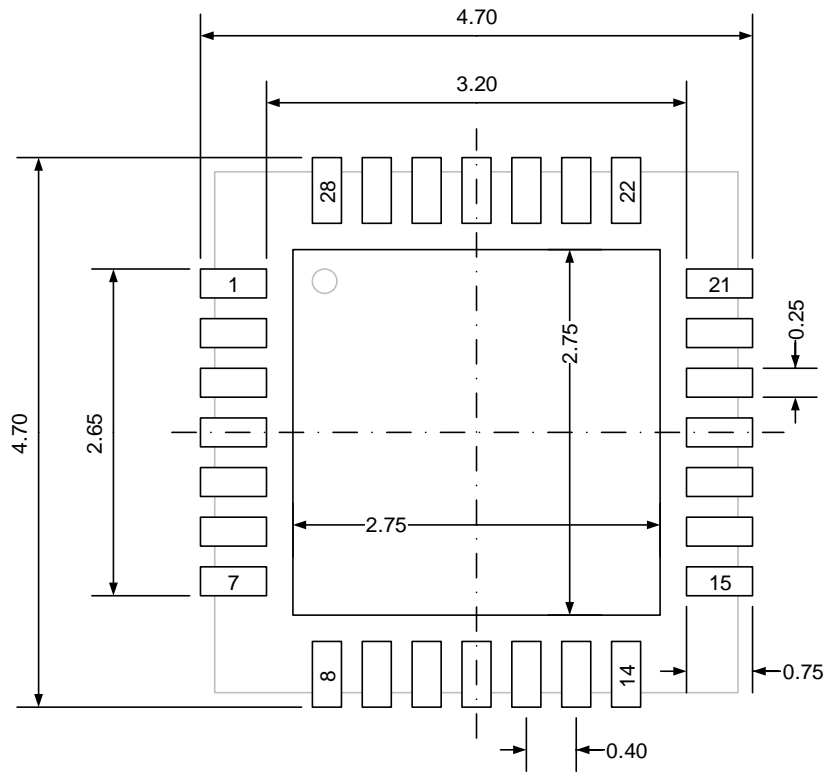


Table 5-4. QFN28 package dimensions

| Symbol | Min | Typ | Max |
|--------|------|------|------|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| b1 | — | 0.14 | — |
| c | 0.18 | 0.20 | 0.25 |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.70 | 2.80 | 2.90 |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.70 | 2.80 | 2.90 |
| e | — | 0.40 | — |
| h | 0.30 | 0.35 | 0.40 |
| L | 0.30 | 0.35 | 0.40 |
| Nd | — | 2.40 | — |
| Ne | — | 2.40 | — |

(Original dimensions are in millimeters)

Figure 5-8. QFN28 recommended footprint



(Original dimensions are in millimeters)

5.5. Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter “ θ ”. For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

θ_{JA} : Thermal resistance, junction-to-ambient.

θ_{JB} : Thermal resistance, junction-to-board.

θ_{JC} : Thermal resistance, junction-to-case.

ψ_{JB} : Thermal characterization parameter, junction-to-board.

ψ_{JT} : Thermal characterization parameter, junction-to-top center.

$$\theta_{JA}=(T_J-T_A)/P_D \quad (5-1)$$

$$\theta_{JB}=(T_J-T_B)/P_D \quad (5-2)$$

$$\theta_{JC}=(T_J-T_C)/P_D \quad (5-3)$$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower θ_{JA} can be considerate as better overall thermal performance. θ_{JA} is generally used to estimate junction temperature.

θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

θ_{JC} represents the thermal resistance between the chip surface and the package top case. θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 5-5. Package thermal characteristics⁽¹⁾

| Symbol | Condition | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| θ_{JA} | Natural convection, 2S2P PCB | LQFP64 | 63.57 | °C/W |
| | | LQFP48 | 64.40 | |
| | | QFN32 | 48.50 | |
| | | QFN28 | 66.07 | |
| θ_{JB} | Cold plate, 2S2P PCB | LQFP64 | 44.40 | °C/W |
| | | LQFP48 | 42.32 | |

| Symbol | Condition | Package | Value | Unit |
|---------------|------------------------------|---------|-------|------|
| | | QFN32 | 28.32 | |
| | | QFN28 | 32.52 | |
| θ_{JC} | Cold plate, 2S2P PCB | LQFP64 | 21.98 | °C/W |
| | | LQFP48 | 22.47 | |
| | | QFN32 | 24.07 | |
| | | QFN28 | 30.58 | |
| Ψ_{JB} | Natural convection, 2S2P PCB | LQFP64 | 44.64 | °C/W |
| | | LQFP48 | 42.42 | |
| | | QFN32 | 28.93 | |
| | | QFN28 | 32.55 | |
| Ψ_{JT} | Natural convection, 2S2P PCB | LQFP64 | 1.51 | °C/W |
| | | LQFP48 | 1.74 | |
| | | QFN32 | 3.33 | |
| | | QFN28 | 3.27 | |

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

6. Ordering information

Table 6-1. Part ordering code for GD32F150xx devices

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|----------------|------------|---------|--------------|------------------------------|
| GD32F150R8T6 | 64 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F150R6T6 | 32 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F150R4T6 | 16 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F150C8T6 | 64 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F150C6T6 | 32 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F150C4T6 | 16 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F150K8U6 | 64 | QFN32 | Green | Industrial -40°C to +85°C |
| GD32F150K6U6 | 32 | QFN32 | Green | Industrial -40°C to +85°C |
| GD32F150K4U6 | 16 | QFN32 | Green | Industrial -40°C to +85°C |
| GD32F150G8U6TR | 64 | QFN28 | Green | Industrial -40°C to +85°C |
| GD32F150G6U6TR | 32 | QFN28 | Green | Industrial -40°C to +85°C |
| GD32F150G4U6TR | 16 | QFN28 | Green | Industrial -40°C to +85°C |

7. Revision history

Table 7-1. Revision history

| Revision No. | Description | Date |
|--------------|---|---------------|
| 1.0 | 1. Initial Release | Mar.8, 2014 |
| 1.1 | 1. Package data updated in <u>Table 5-1. QFN package dimensions</u> and <u>Table 6-1. Part ordering code for GD32F150xx devices.</u> | Jun.18, 2014 |
| 2.1 | 1. Characteristics values updated in <u>Table 4-3. Power consumption characteristics.</u> | Oct.20, 2014 |
| 3.0 | 1. Adapt To New Name Convention. | Jan.24, 2018 |
| 3.1 | 1. Modify formats and descriptions. | Nov.21, 2019 |
| 3.2 | 1. Table 4-3 update, refers to <u>Table 4-3. Power consumption characteristics.</u> | Jun.16.2021 |
| 3.3 | 1. Update <u>Table 4-1. Absolute maximum ratings^{(1)(4).}</u> 2. Update electrical parameters in chapter <u>Electrical characteristics.</u> | Jul. 12. 2022 |
| 3.4 | 1. Add notes for <u>Table 4-2. DC operating conditions</u> and <u>Table 4-7. Power consumption characteristics⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾⁽⁶⁾</u> , and update <u>Table 4-7. Power consumption characteristics⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾⁽⁶⁾</u> . 2. Update <u>Figure 4-5. I2C bus timing diagram.</u> | Sep. 27, 2022 |
| 3.5 | 1. Add the TR suffix after the Ordering information QFN28 | Mar. 13, 2023 |
| 3.6 | 2. Add notes more details refer to AN108 GD32F3x0 Hardware Development Guide. 3. Add the pin definitions format requires that a new line be added to the pin definitions. | Jun.15.2023 |
| 3.7 | 1. Add specific ability description to backup domain IO driver current. 2. Convert all encapsulated POD plots to vector plots. | Dec. 31, 2023 |
| 3.8 | 1. All pods add coplanarity information. | Jun. 30, 2024 |

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