

GD4017B

5-STAGE JOHNSON COUNTER

DESCRIPTION — The 4017B is a 5-Stage Johnson Decade Counter with ten glitch free decoded active HIGH Outputs (O_0 – O_9), an active LOW Output from the most significant flip-flop (\overline{O}_{5-9}), active HIGH and active LOW Clock Inputs (CP_0 , \overline{CP}_1) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP_0 while \overline{CP}_1 is LOW or a HIGH-to-LOW transition at CP_1 while CP_0 is HIGH (see Functional Truth Table). When cascading 4017B counters, the \overline{O}_{5-9} output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next 4017B.

A HIGH on the Master Reset Input (MR) resets the counter to zero ($O_0 = \overline{O}_{5-9} = \text{HIGH}$, O_1 – $O_9 = \text{LOW}$) independent of the Clock Inputs (CP_0 , \overline{CP}_1).

- TYPICAL COUNT FREQUENCY OF 13.8 MHz AT $V_{DD} = 10\text{ V}$
- ACTIVE HIGH DECODED OUTPUTS
- TRIGGERS ON EITHER A HIGH-TO-LOW OR LOW-TO-HIGH TRANSITION
- CASCADABLE

PIN NAMES

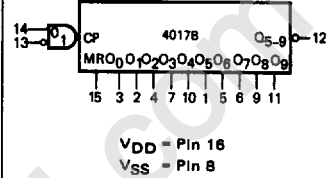
CP_0	Clock Input (L→H Triggered)
\overline{CP}_1	Clock Input (H→L Triggered)
MR	Master Reset Input
O_0 – O_9	Decoded Outputs
\overline{O}_{5-9}	Carry Output (Active LOW)

FUNCTIONAL TRUTH TABLE

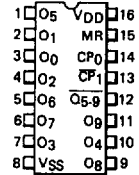
MR	CP_0	\overline{CP}_1	OPERATION
H	X	X	$O_0 = \overline{O}_{5-9} = \text{H}; O_1 - O_9 = \text{L}$
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	H→L	L	No Change

H = HIGH Level
 L = LOW Level
 L→H = LOW-to-HIGH Transition
 H→L = HIGH-to-LOW Transition
 X = Don't Care

LOGIC SYMBOL

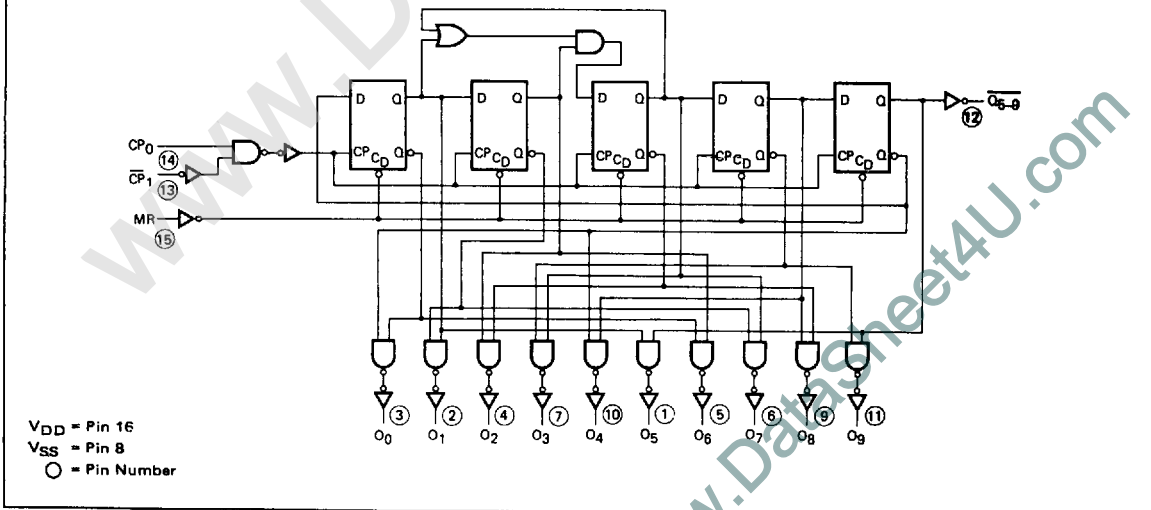


**CONNECTION DIAGRAM
 DIP (TOP VIEW)**



NOTE:
 The SO Package has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



GS CMOS - GD4017B

DC CHARACTERISTICS: V_{DD} as shown, $V_{SS} = 0$ V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power	XC			20			40			80	μ A	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
	Supply Current	XM			5			10			20	μ A	MIN, 25°C	
					150			300			600		MAX	

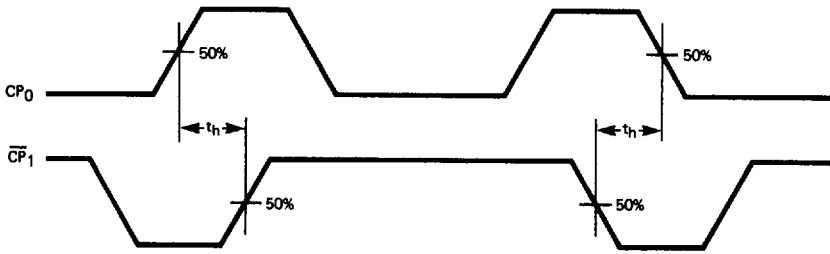
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, $V_{SS} = 0$ V, $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER		LIMITS									UNITS	TEST CONDITIONS
			$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP_0 or CP_1 to O_n			278	700		114	285		82	228	ns	$C_L = 60$ pF, $R_L = 200$ k Ω Input Transition Times ≤ 20 ns
t_{PHL}	Propagation Delay, CP_0 or CP_1 to \bar{O}_{5-g}			205	525		87	225		63	180	ns	
t_{PLH}	Propagation Delay, MR to O_n			261	650		105	250		73	200	ns	
t_{PHL}	Propagation Delay, MR to \bar{O}_{5-g}			170	430		80	175		52	140	ns	
t_{TLH}	Output Transition Time			125	300		65	130		40	104	ns	
t_{THL}	Output Transition Time			59	135		31	70		23	45	ns	
t_{wCP}	Min. CP_0 or CP_1 Pulse Width			63	135		26	70		19	45	ns	
t_{wMR}	Minimum MR Pulse Width		200	85		70	37		56	28		ns	
t_{rec}	MR Recovery Time		130	52		55	22		44	18		ns	
t_H	Hold Time, CP_0 to CP_1		50	16		25	6		20	3		ns	
t_H	Hold Time, CP_1 to CP_0		200	90		90	39		72	26		ns	
f_{MAX}	Input Count Frequency (Note 3)		200	89		90	39		72	22		ns	
			2.5	5.8		7	13.8		8	16		MHz	

NOTES:

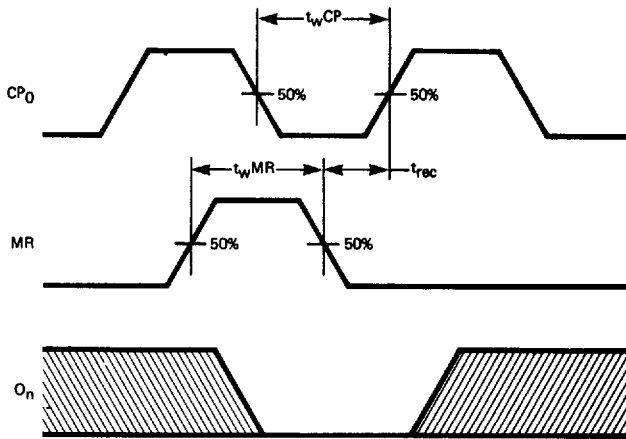
- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
- For f_{MAX} , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
- It is recommended that input rise and fall times to either Clock Input (CP_0 or CP_1) be less than 15 μ s at $V_{DD} = 5$ V, 4 μ s at $V_{DD} = 10$ V, and 3 μ s at $V_{DD} = 15$ V.

SWITCHING WAVEFORMS



HOLD TIMES, CP_0 TO \overline{CP}_1 AND \overline{CP}_1 TO CP_0

Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS FOR
CP AND MR AND RECOVERY TIME FOR MR

CONDITIONS: \overline{CP}_1 = LOW while CP_0 is triggered on a LOW-to-HIGH transition. t_wCP and t_{rec} also apply when CP_0 = HIGH and \overline{CP}_1 is triggered on a HIGH-to-LOW transition.