GD5FxGQ4xC

DATASHEET

Contents

1 FEATURE

◆1Gb SLC NAND Flash

◆Page Size
- 2048 bytes + 128 bytes with ECC disabled
- 2048 bytes + 64 bytes with ECC enabled

◆ Standard, Dual, Quad SPI
- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

◆ High Speed Clock Frequency
- 120MHz for fast read with 30PF load
- Quad I/O Data transfer up to 480Mbits/s

◆ Software/Hardware Write Protection
- Write protect all/portion of memory via software
- Register protection with WP# Pin
- Top or Bottom, Block selection combination

◆ Advanced security Features
- 8K-Byte OTP Region (4 page OTP)

◆Single Power Supply Voltage
- Full voltage range for 1.8V: 1.7V ~ 2.0V
- Full voltage range for 3.3V: 2.7V ~ 3.6V

◆Program/Erase/Read Speed
- Page Program time: 400us typical
- Block Erase time: 3ms typical
- Page read time: 80us maximum(w/I ECC)

◆Low Power Consumption
- 40mA maximum active current
- 90uA maximum standby current

◆ Enhanced access performance
- 2kbyte cache for fast random read
- Cache read and cache program

◆ Advanced Feature for NAND
- Internal ECC option, per 528bytes
- Internal data move by page with ECC

◆ The first block(Block0) is guaranteed to be a valid block at the time of shipment.

2 GENERAL DESCRIPTION

SPI (Serial Peripheral Interface) NAND Flash provides an ultra cost-effective while high density non-volatile memory storage solution for embedded systems, based on an industry-standard NAND Flash memory core. It is an attractive alternative to SPI-NOR and standard parallel NAND Flash, with advanced features:

- Total pin count is 8, including VCC and GND
- Density is 1Gbit
- Superior write performance and cost per bit over SPI-NOR
- Significant low cost than parallel NAND

This low-pin-count NAND Flash memory follows the industry-standard serial peripheral interface, and always remains the same pin-out from one density to another. The command sets resemble common SPI-NOR command sets, modified to handle NAND specific functions and added new features. GigaDevice SPI NAND is an easy-to-integrate NAND Flash memory, with specified designed features to ease host management:

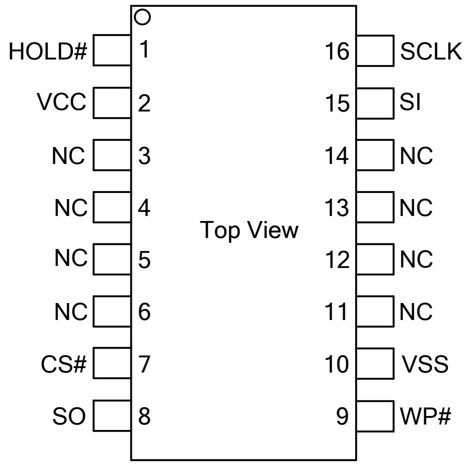
- **User-selectable internal ECC**. ECC code is generated internally during a page program operation. When a page is read to the cache register, the ECC code is detect and correct the errors when necessary. The 64-bytes spare area is available even when internal ECC enabled. The device outputs corrected data and returns an ECC error status.
- **Internal data move or copy back with internal ECC**. The device can be easily refreshed and manage garbage collection task, without need of shift in and out of data.
- **Power on Read with internal ECC**. The device will automatically read first page of fist block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correctly by internal ECC.

It is programmed and read in page-based operations, and erased in block-based operations. Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation. The cache register functions as the buffer memory to enable page and random data READ/WRITE and copy back operations. These devices also use a SPI status register that reports the status of device operation.

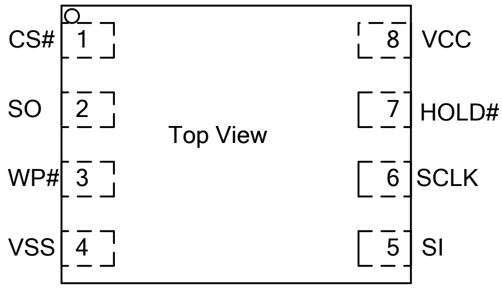
2.1 Product List

Product Number	Density	Voltage	Package Type	Temperature	Page Size
GD5F1GQ4RCYIG	1Gbit	1.7V to 2.0V	WSON8(8*6mm)	-40℃ to 85℃	2Kbyte + 128Byte
GD5F1GQ4RCFIG			SOP16 300mil		
GD5F1GQ4RCZIG			TFBGA24(6*4 Ball Array)		
GD5F1GQ4RC9IG			LGA8(6*8mm)		
GD5F1GQ4UCYIG		2.7V to 3.6V	WSON8(8*6mm)		
GD5F1GQ4UCFIG			SOP16 300mil		
GD5F1GQ4UCZIG			TFBGA24(6*4 Ball Array)		

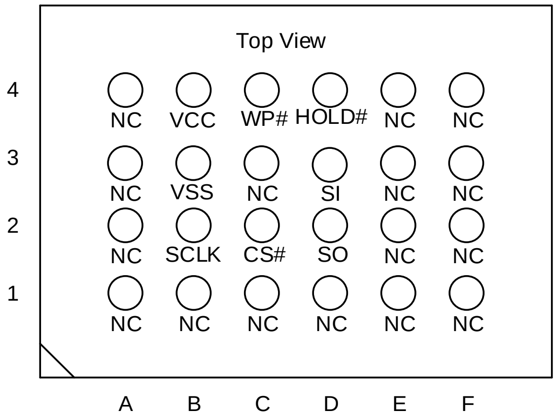
2.2 Connection Diagram



16-LEAD SOP



8-LEAD WSON

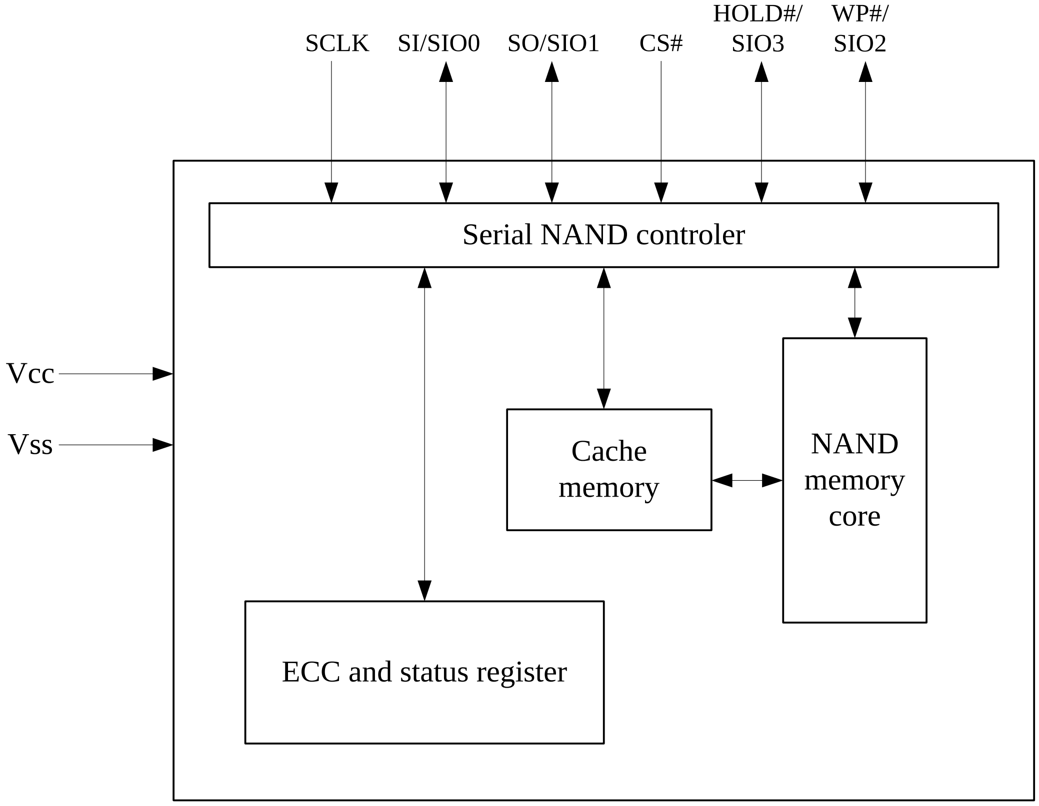


24-BALL TFBGA

2.3 Pin Description

Pin Name	I/O	Description
CS#	**I**	Chip Select input, active low
SO/SIO1	**I/O**	Serial Data Output / Serial Data Input Output 1
WP#/SIO2	**I/O**	Write Protect, active low / Serial Data Input Output 2
VSS	**Ground**	Ground
SI/SIO0	**I/O**	Serial Data Input / Serial Data Input Output 0
SCLK	**I**	Serial Clock input
HOLD#/SIO3	**I/O**	Hold input, active low / Serial Data Input Output3
VCC	**Supply**	Power Supply

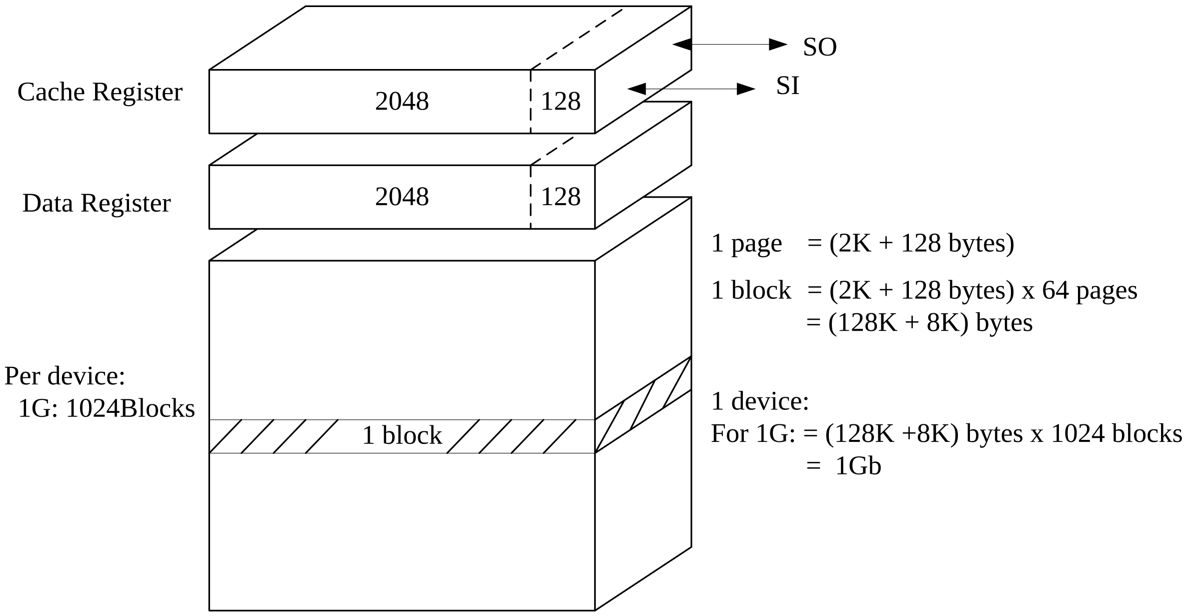
2.4 Block Diagram



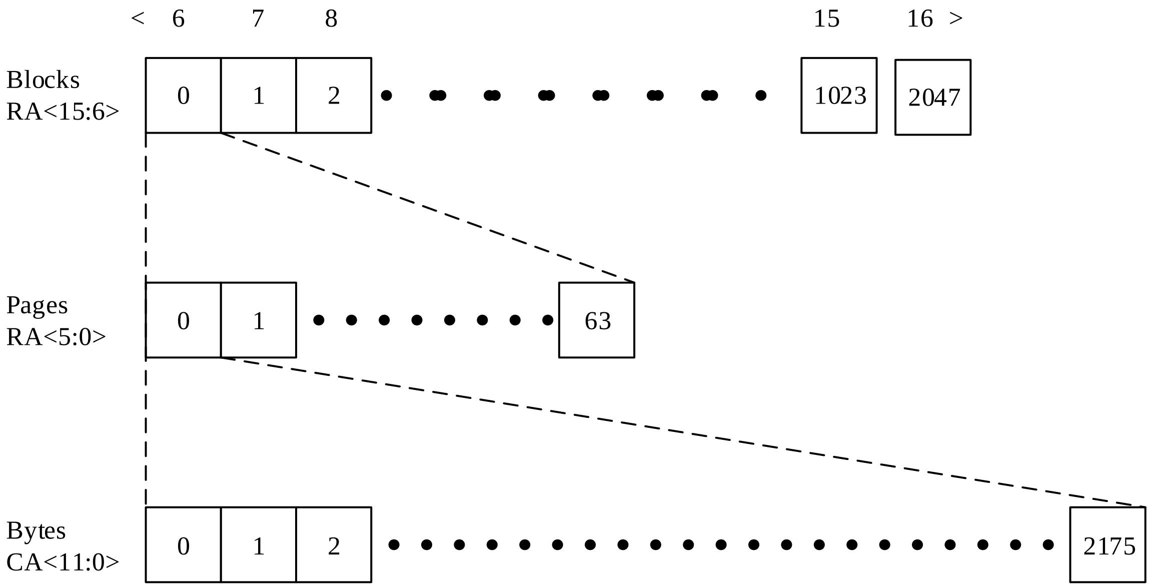
3 ARRAY ORGANIZATION

Each device has	Each block has	Each page has	
1G			
128M+8M	128K+8K	2K+128	bytes
1024 x 64	64	-	pages
1024	-	-	blocks

Figure1. Array Organization



4 MEMORY MAPPING



Note:

1. CA: Column Address. The 12-bit address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2175 are valid. Bytes 2176 through 4095 of each page are “out of bounds,” do not exist in the device, and cannot be addressed.
2. RA: Row Address. RA<5:0> selects a page inside a block, and RA<X:6> selects a block:
   RA<15:6> selects a block for 1G;

5 DEVICE OPERATION

5.1 SPI Modes

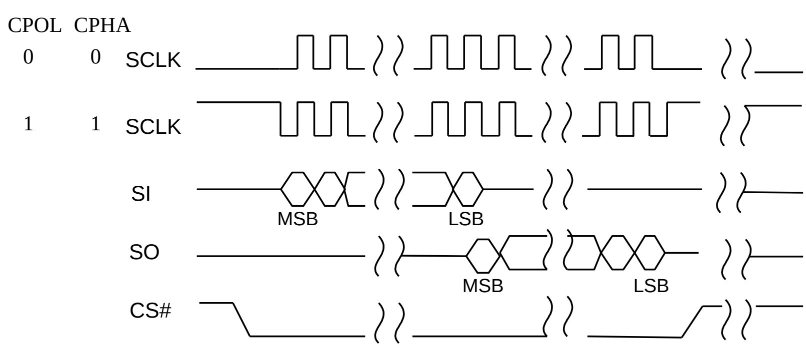
SPI NAND supports two SPI modes:

• CPOL = 0, CPHA = 0 (Mode 0)

• CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK for both modes.All timing diagrams shown in this data sheet are mode 0. See Figure2 for more details.

Figure2. SPI Modes Sequence Diagram



Note: While CS# is HIGH, keep SCLK at VCC or GND (determined by mode 0 or mode 3).

Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

5.2 HOLD Mode

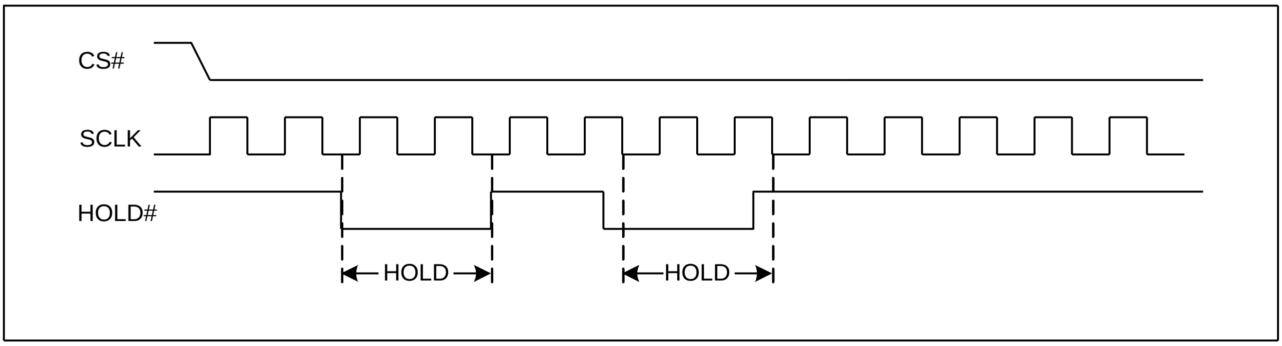
The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don't care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure3. Hold Condition



5.3 Write Protection

SPI NAND provides Hardware Protection Mode besides the Software Mode. Write Protect (WP#) prevents the block lock bits (BP0, BP1, BP2 and INV, CMP) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered.

6 COMMANDS DESCRIPTION

Table1. Commands Set

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	(D7-D0)			Wrap[9]
Set Feature	1FH	A7-A0	(D7-D0)	dummy[1]		
Page Read (to cache)	13H	A23-A16	A15-A8	A7-A0		
Read From Cache	03H	dummy[2]	A15-A8	A7-A 0[8]	(D7-D0)	
Fast Read From Cache	0BH	dummy[2]	A15-A8	A7-A0	dummy[2]	(D7-D0)
Read From Cache x 2	3BH	dummy[2]	A15-A8	A7-A0	dummy[2]	(D7-D0)x2
Read From Cache x 4	6BH	dummy[2]	A15-A8	A7-A0	dummy[2]	(D7-D0)x4
Read From Cache Dual IO	BBH	A15-A0	dummy[3]	(D7-D0)x2		
Read From Cache Quad IO	EBH	A15-A0[4]	(D7-D0)x4			
Read ID[5]	9FH	MID	DID	DID		
Program Load	02H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load x4	32H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load Random Data	84H[7]	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load Random Data x4	C4H/34H[7]	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Block Erase(128K)	D8H	A23-A16	A15-A8	A7-A0		
Reset[6]	FFH					

Notes:

1. The dummy byte can be inputted or not.
2. The x8 clock = dummy<7:0>.
3. The x8 clock = dummy<7:0>, D7-D0.
4. The x8 clock = A15-A0, dummy<7:0>, D7-D0.
5. MID is Manufacture ID (C8h for GigaDevice), DID is Device ID.
6. Reset command:
   - During busy, Reset will reset PAGE READ/PROGRAM/ERASE operation.
   - During idle, Reset will reset status register bits P_FAIL/E_FAIL/ECCS bits.
7. Those commands are only available in Internal Data Move operation.
8. A0 need be 0 for the 03H command.
9. The output would be updated by real-time, until CS# is driven high.

7 WRITE OPERATIONS

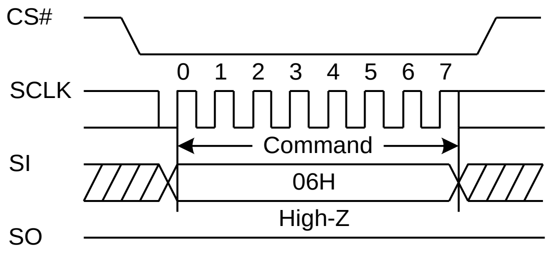
7.1 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to following operations that change the contents of the memory array:

- Page program
- OTP program/OTP protection
- Block erase

The WEL bit can be cleared after a reset command.

Figure4. Write Enable Sequence Diagram

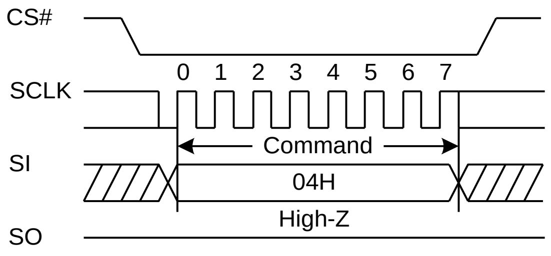


7.2 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is also reset by following condition:

- Page program
- OTP program/OTP protection
- Block erase

Figure5. Write Disable Sequence Diagram



8 FEATURE OPERATIONS

8.1 Get Features (0FH) and Set Features (1FH)

The GET FEATURES (0FH) and SET FEATURES (1FH) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific feature bits (shown in the following table). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06H) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFH) command is issued.

Table2. Features Settings

Register	Addr.	7	6	5	4	3	2	1	0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	ECCS2	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Feature	D0H	Reserved	DS_IO[1]	DS_IO[0]	Reserved	Reserved	Reserved	Reserved	Reserved

Note:If BRWD is enabled and WP# is LOW, then the block lock register cannot be changed.

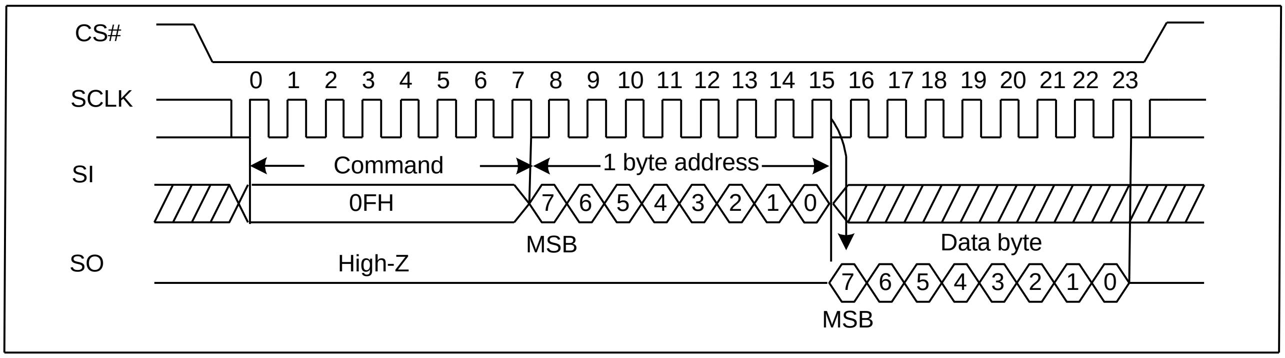
If QE is enabled, the quad IO operations can be executed.

All the reserved bits must be held low when the feature is set.

00h is the default data byte value for Output Driver Register after power-up.

These registers are write/read type, except for Register of Status (C0H) is read only.

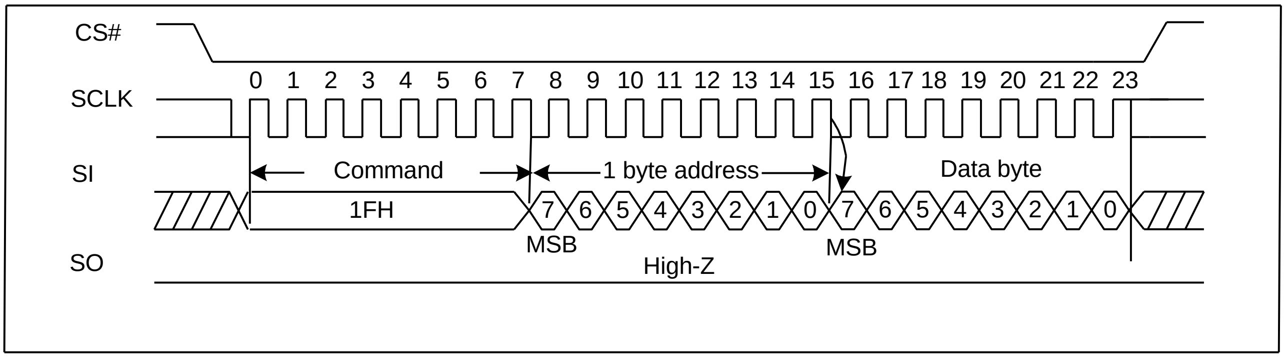
Figure6. Get Features Sequence Diagram



Note: The output would be updated by real-time, until CS# is driven high.

The set features command supports a dummy byte mode after the data byte as well. The features in the feature byte B0H are all volatile except OTP_PRT bit.

Figure7. Set Features Sequence Diagram



9 READ OPERATIONS

9.1 Page Read

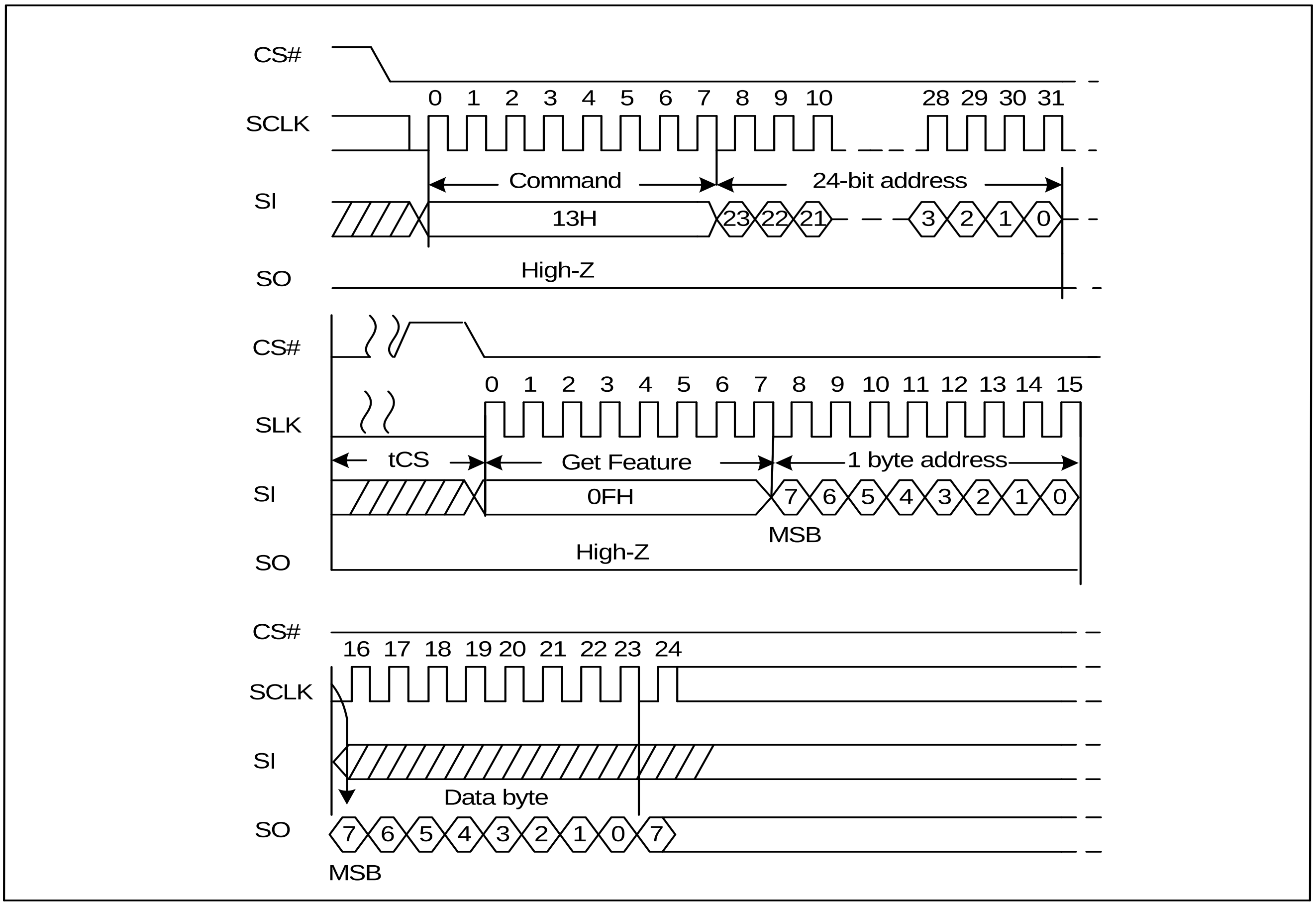
The PAGE READ (13H) command transfers the data from the NAND Flash array to the cache register. The command sequence is as follows:

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read the status)
- 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)/BBH (Read from cache dual IO)/EBH (Read from cache quad IO)

The PAGE READ command requires a 24-bit address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for t_{RD} time. During this time, the GET FEATURE (0FH) command can be issued to monitor the status. Followed the page read operation, the RANDOM DATAREAD (03H/0BH/3BH/6BH/BBH/EBH) command must be issued in order to read out the data from cache. The output data starts at the initial address specified in the command, and will continue until CS# is pulled high to terminate this operation. Refer waveforms to view the entire READ operation.

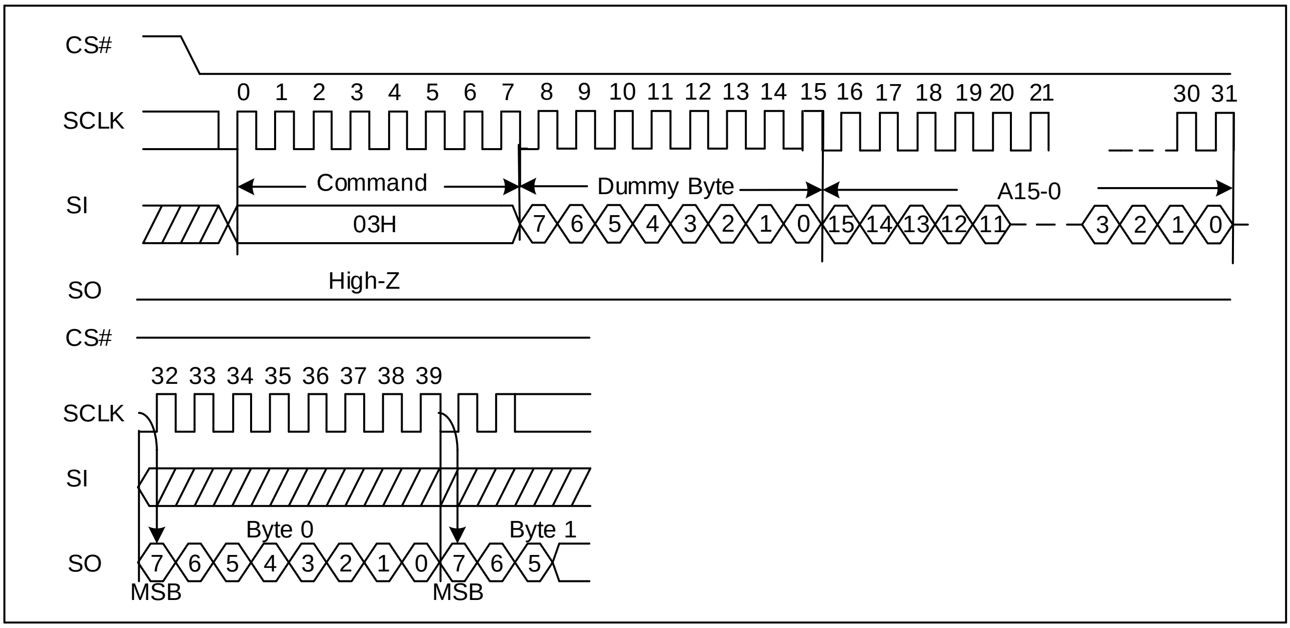
9.2 Page Read to Cache (13H)

Figure8.Page Read to cache Sequence Diagram



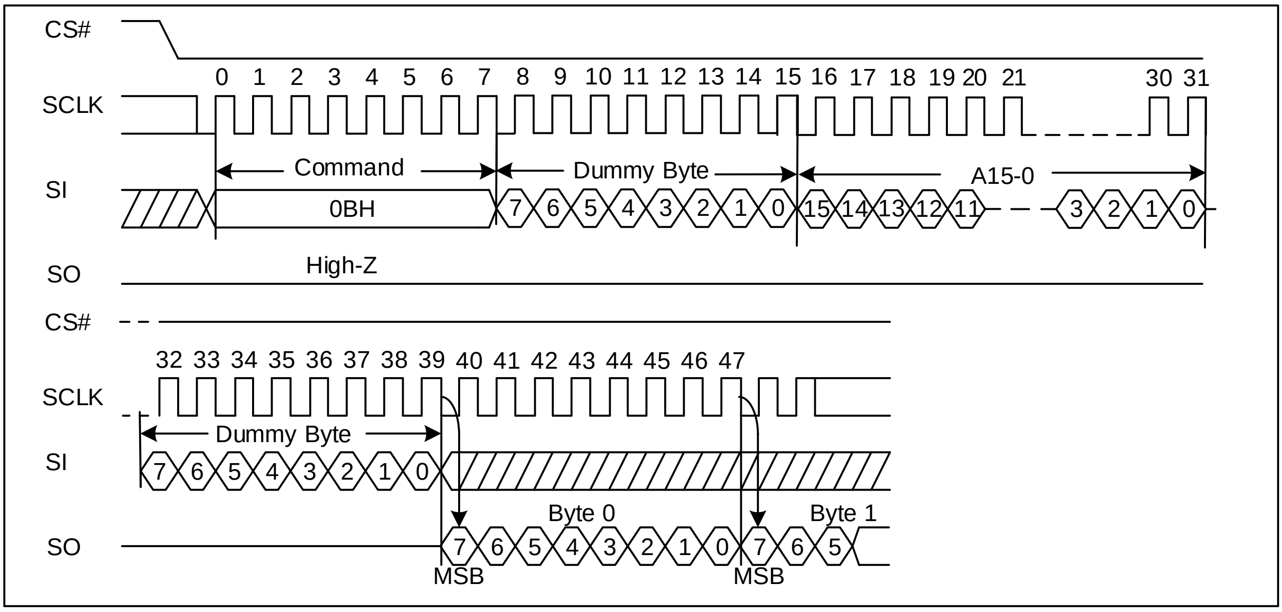
9.3 Read From Cache (03H)

Figure9. Read From Cache Sequence Diagram



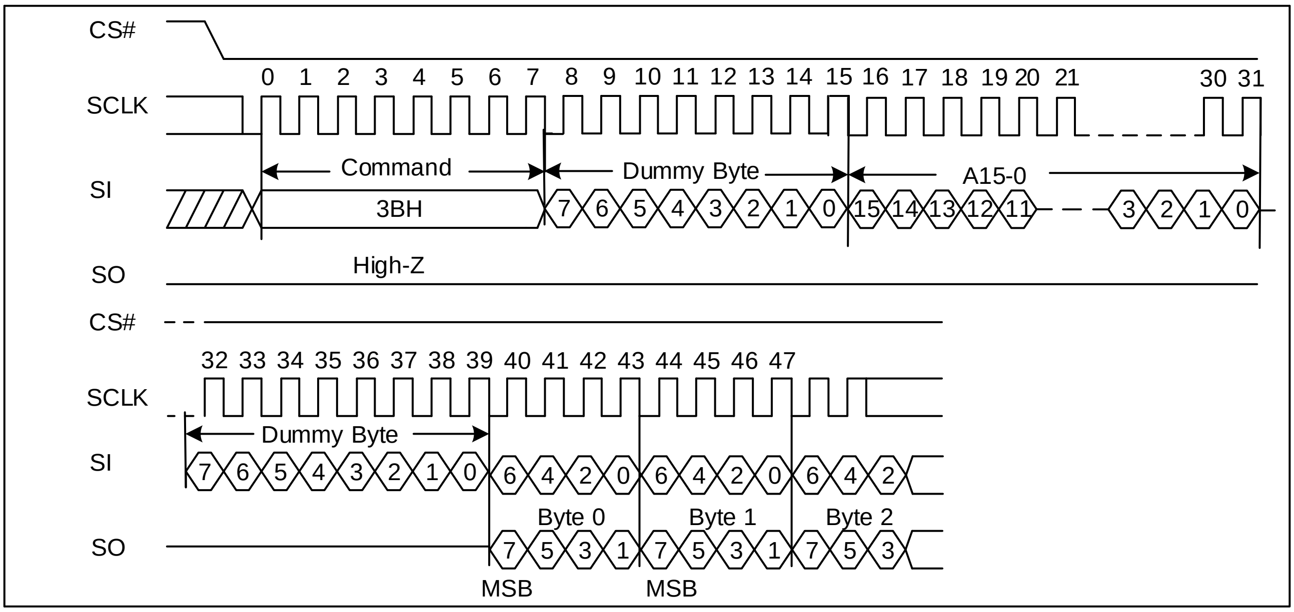
9.4 Fast Read From Cache (0BH)

Figure10. Read From Cache Sequence Diagram



9.5 Read From Cache x2 (3BH)

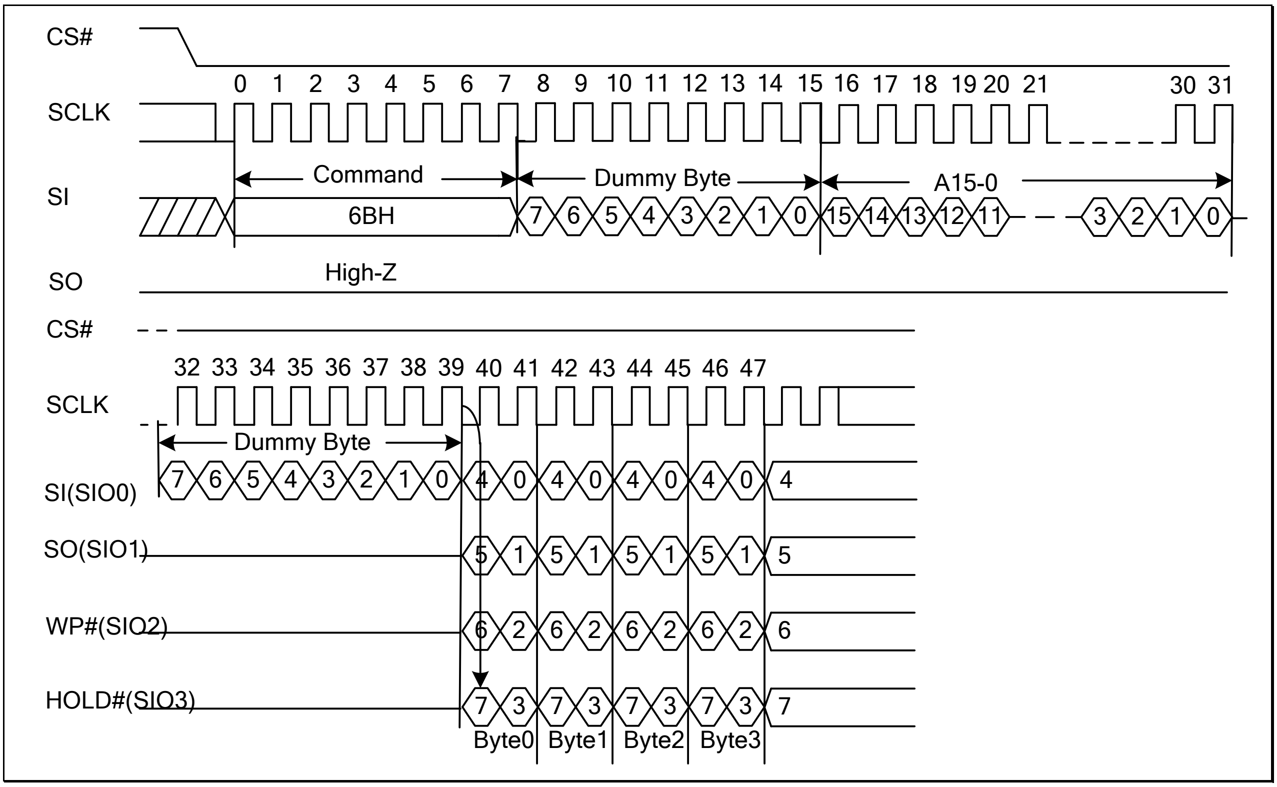
Figure11. Read From Cache x2 Sequence Diagram



9.6 Read From Cache x4 (6BH)

The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache x4 command.

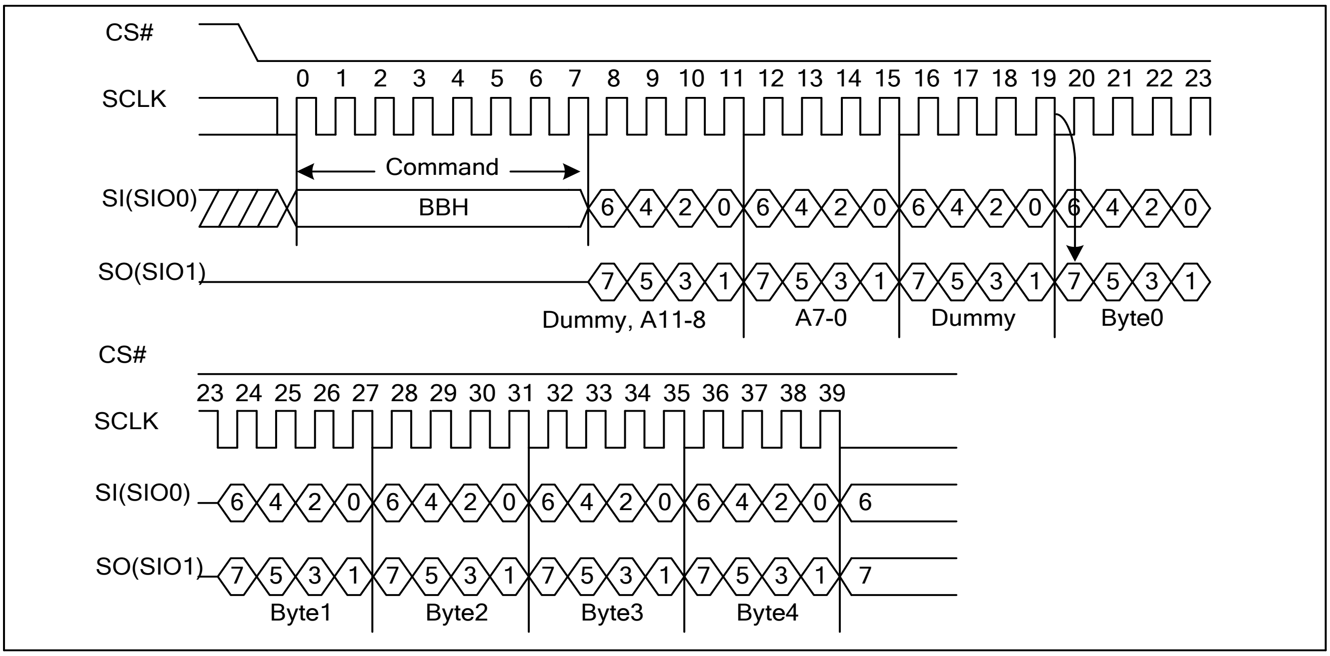
Figure12. Read From Cache x4 Sequence Diagram



9.7 Read From Cache Dual IO (BBH)

The Read from Cache Dual I/O command (BBH) is similar to the Read form Cache x2 command (3BH), followed by a 12bit column address for the starting byte address and a dummy byte by SIO0 and SIO1, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 2-bit per clock cycle from SIO0 and SIO1. The first address byte can be at any location. The address increments automatically to the next higher address after each byte of data shifted out until the end of whole page.

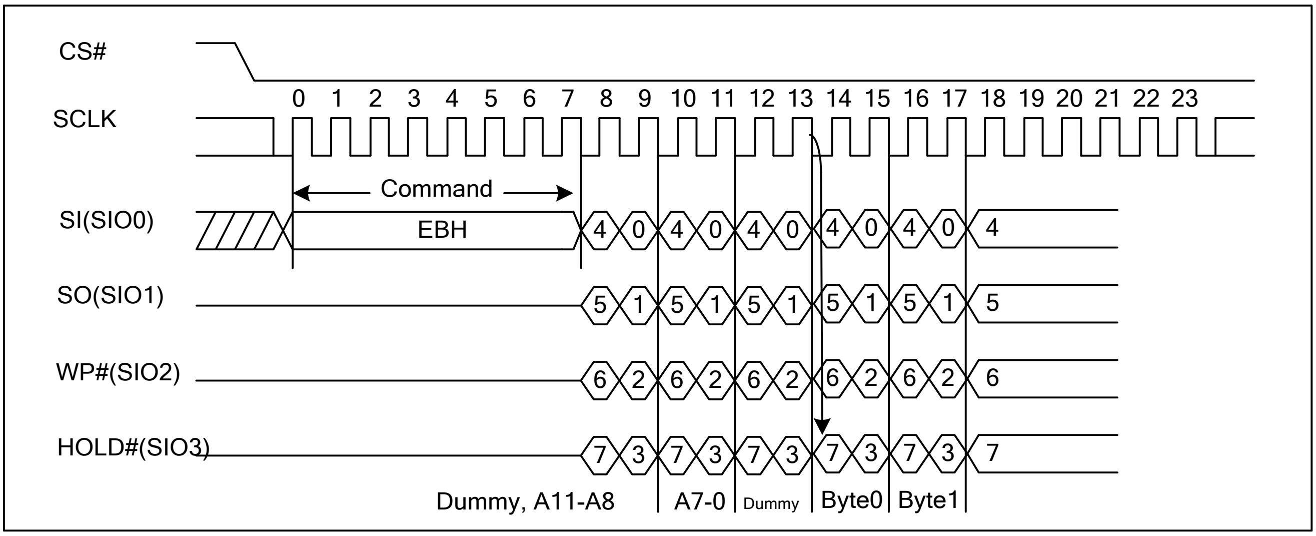
Figure13. Read From Cache Dual IO Sequence Diagram



9.8 Read From Cache Quad IO (EBH)

The Read from Cache Quad IO command is similar to the Read from Cache x4 command, followed a 12-bit column address for the starting byte address and a dummy byte by SIO0, SIO1, SIO3, SIO4, each bit being latched in during the rising edge of SCLK, then the cache contents are shifted out 4-bit per clock cycle from SIO0, SIO1, SIO2, SIO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out until the end of whole page. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the read from cache quad IO command.

Figure14. Read From Cache Quad IO Sequence Diagram



10 Read ID (9FH)

The READ ID command is used to identify the NAND Flash device.

- The READ ID command outputs the Manufacturer ID and the device ID. See Table3 for details.

Figure15. Read ID Sequence Diagram

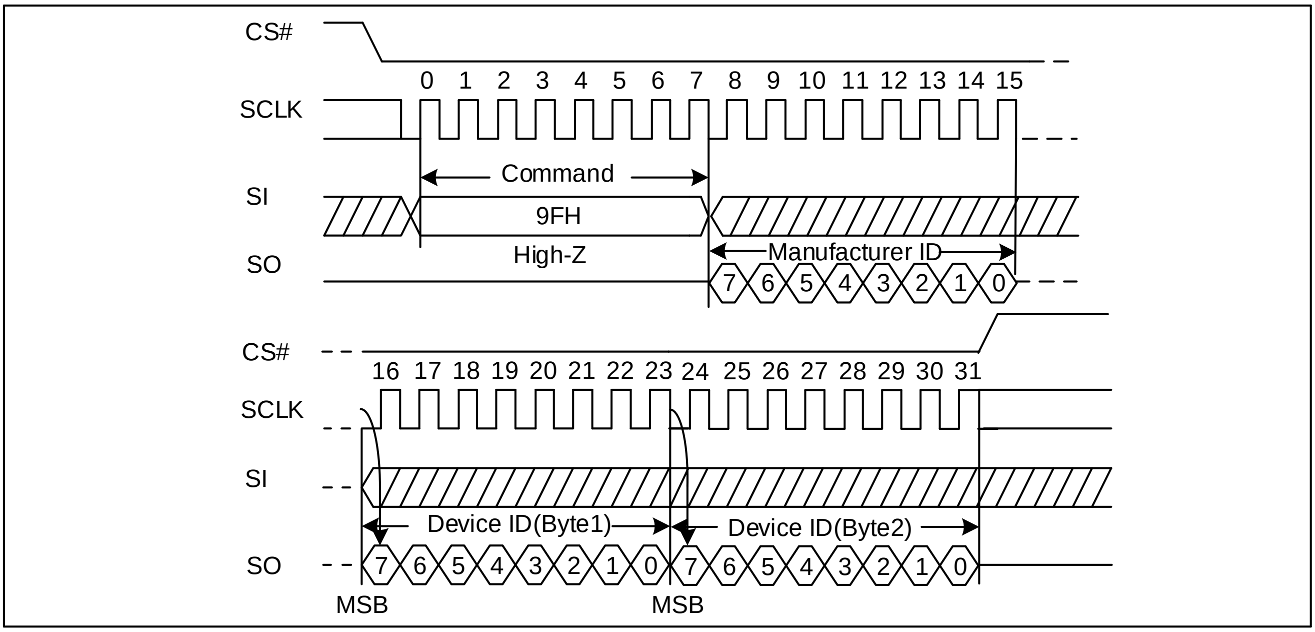


Table3. READ ID Table

ID	Description	Part No	Value	Page Size
Manufacture ID (GigaDevice)	SPI NAND 3.3V	GD5F1GQ4UCxxG	C8h	2Kbyte + 128Byte
	SPI NAND 1.8V	GD5F1GQ4RCxxG		
Device ID (Byte 1)	SPI NAND 1Gbit 3.3V	GD5F1GQ4UCxxG	B1h	
	SPI NAND 1Gbit 1.8V	GD5F1GQ4RCxxG	A1h	
Device ID (Byte 2)	SPI NAND 1Gbit 3.3V	GD5F1GQ4UCxxG	48h	
	SPI NAND 1Gbit 1.8V	GD5F1GQ4RCxxG		

11 PROGRAM OPERATIONS

11.1 Page Program

The PAGE PROGRAM operation sequence programs 1 byte to 2176 bytes of data within a page. The page program sequence is as follows:

- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

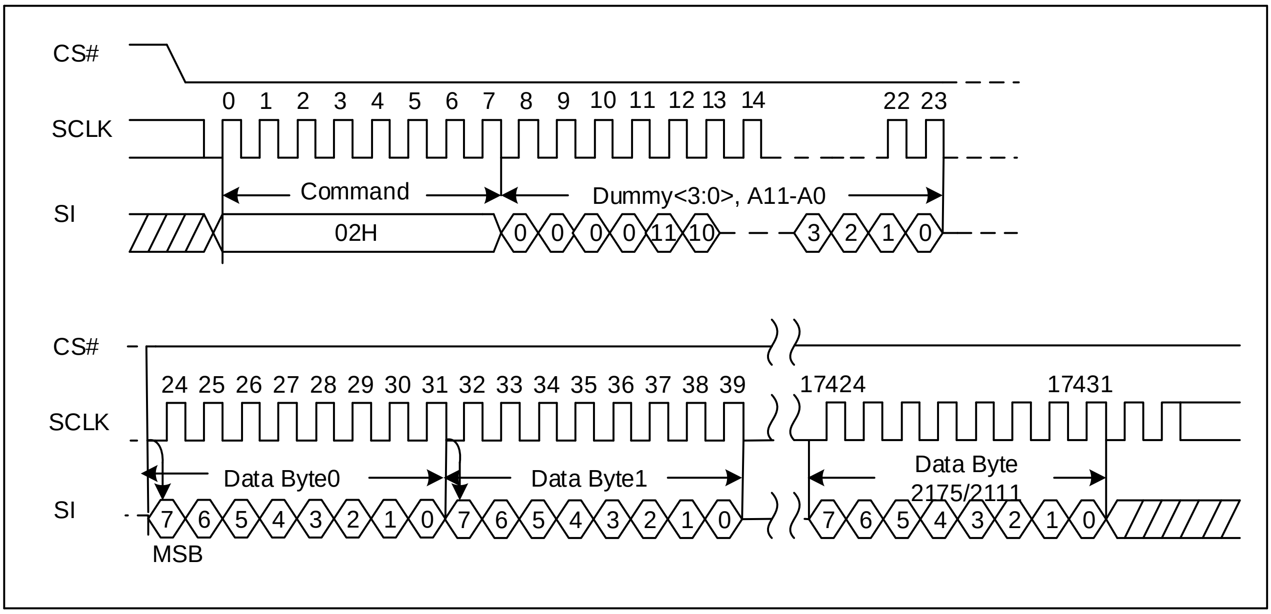
Firstly, a PROGRAM LOAD (02H/32H) command is issued. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits and a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2176 bytes long. If more than 2176bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH. Figure16 shows the PROGRAMLOAD operation. Secondly, prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITEENABLE must be executed in order to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored.

Note:

1. The contents of Cache Register doesn't reset when Program Load (02h) command, Program Random Load (84h) command and RESET (FFh) command.
2. When Program Execute (10h) command was issued just after Program Load (02h) command, SPI-NAND controller outputs 0xFF data to the NAND for the address that data was not loaded by Program Load (02h) command.
3. When Program Execute (10h) command was issued just after Program Load Random Data (84h) command, SPI-NAND controller outputs contents of Cache Register to the NAND.
4. The addressing should be done in sequential order in a block.

11.2 Program Load (PL) (02H)

Figure16. Program Load Sequence Diagram

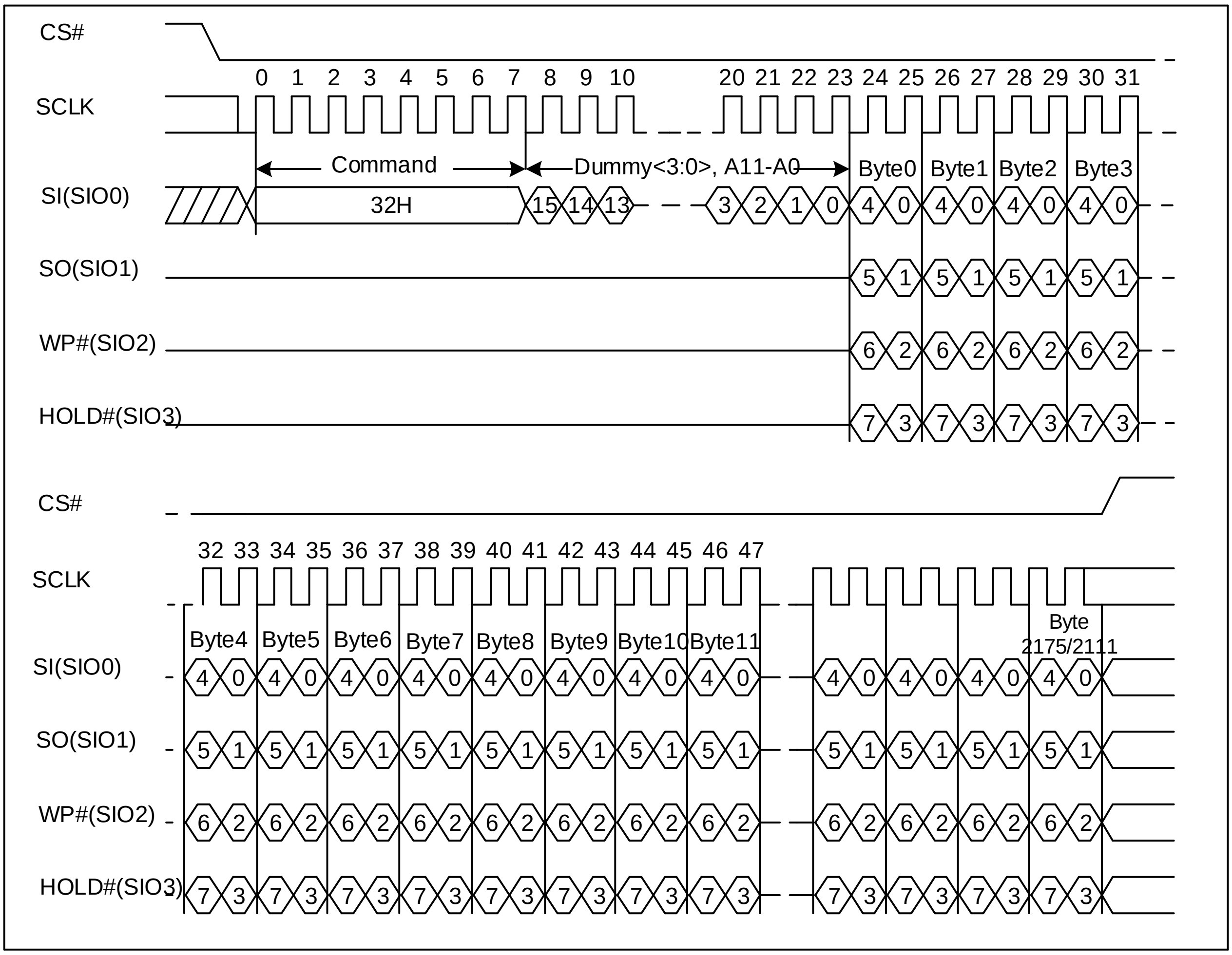


Note: when internal ECC disabled the Data Byte is 2175, when internal ECC enabled the Data Byte is 2111.

11.3 Program Load x4 (PL x4) (32H)

The Program Load x4 command (32H) is similar to the Program Load command (02H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable the program load x4 command.

Figure17. Program Load x4 Sequence Diagram

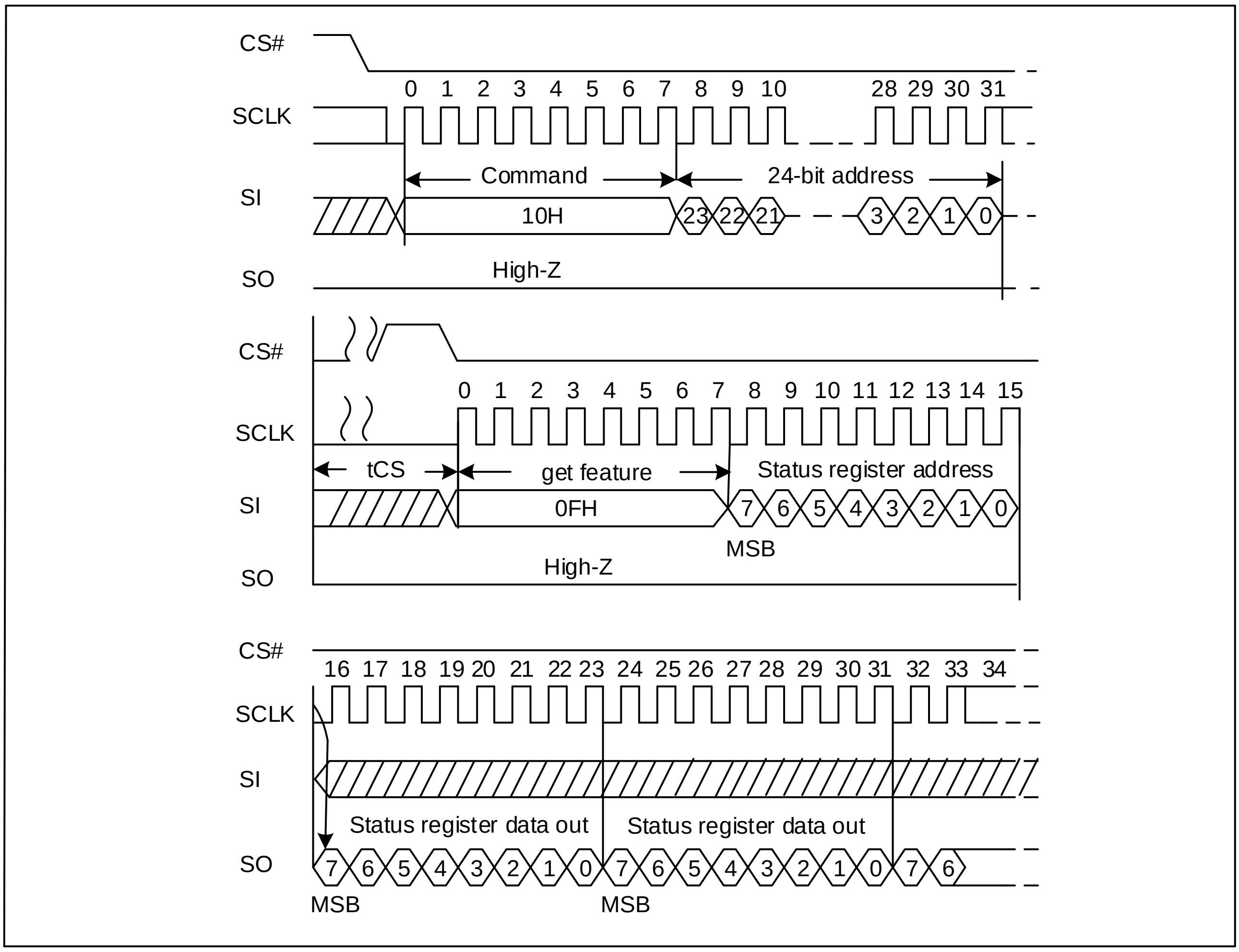


Note: when internal ECC disabled the Byte is 2175, when internal ECC enabled the Byte is 2111.

11.4 Program Execute (PE) (10H)

After the data is loaded, a PROGRAM EXECUTE (10H) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for tPROG time. This operation is shown in Figure18. During this busy time, the status register can be polled to monitor the status of the operation (refer to Status Register). When the operation completes successfully, the next series of data can be loaded with the PROGRAMLOAD command.

Figure18. Program Execute Sequence Diagram



11.5 Internal Data Move

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

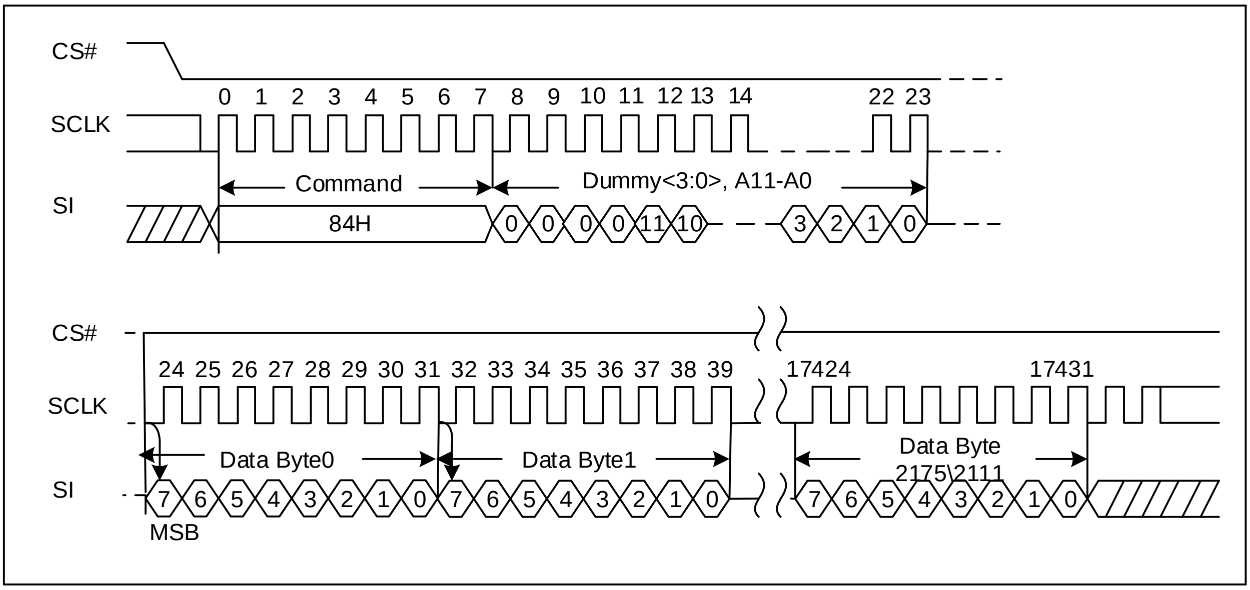
- 13H (PAGE READ to cache)
- Optional 84H/C4H/34H (PROGRAM LOAD RANDOM DATA)
- 06H (WRITE ENABLE)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a PAGE READ (13H) command. The PROGRAM LOAD RANDOM DATA (84H/C4H/34H) command can be issued, if user wants to update bytes of data in the page. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84H/C4H/34H) command must be issued with the new column address. After the data is loaded, the WRITE ENABLE command must be issued, and the PROGRAM EXECUTE (10H) command can be issued to start the programming operation.

11.6 Program Load Random Data (84H)

This command consists of an 8-bit Op code, followed by 4 dummy bits, and a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84H) command must be issued with a new column address, seeFigure19 for details. This command is only available during internal data move sequence.

Figure19. Program Load Random Data Sequence Diagram

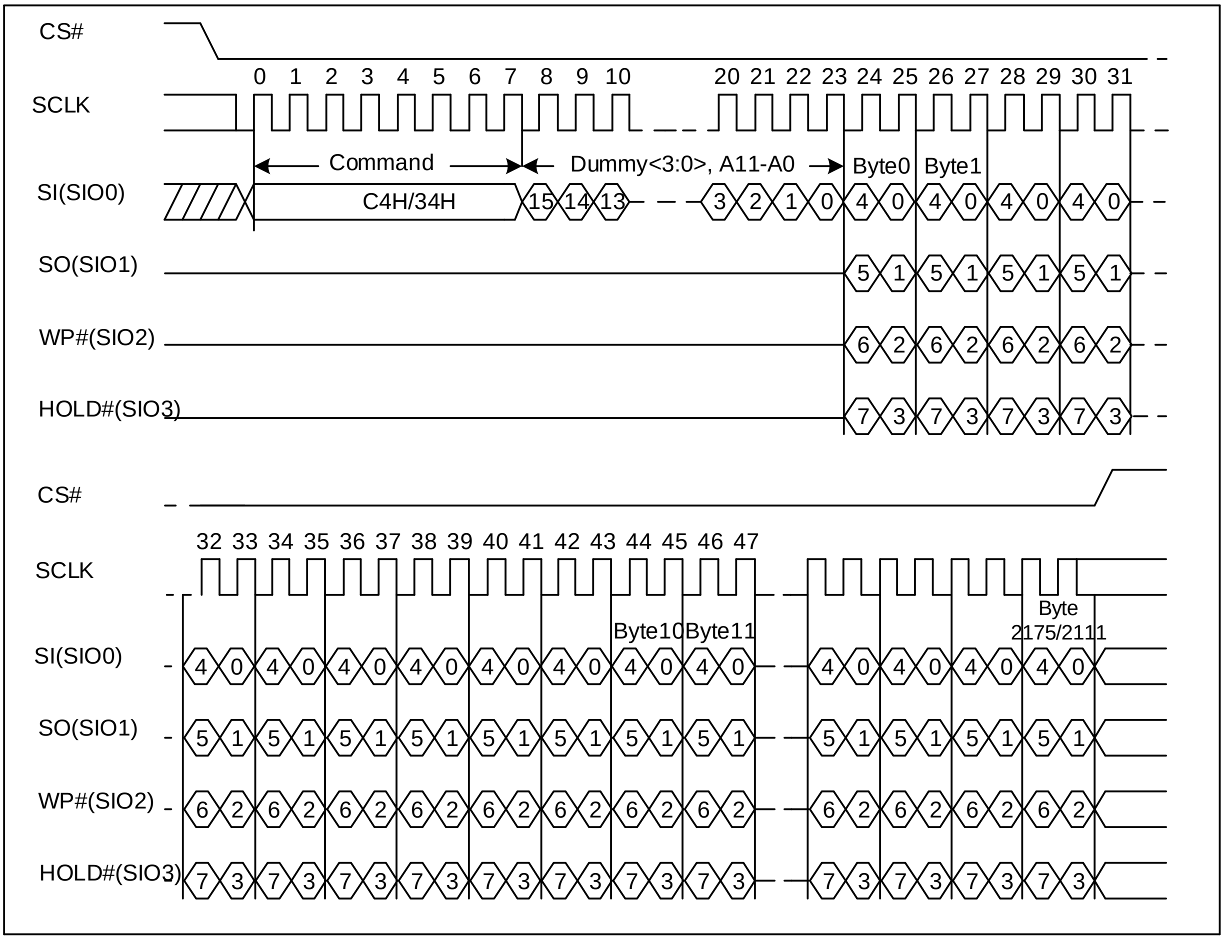


Note: when internal ECC disabled the Data Byte is 2175, when internal ECC enabled the Data Byte is 2111.

11.7 Program Load Random Data x4 (C4H/34H)

The Program Load Random Data x4 command (C4H/34H) is similar to the Program Load Random Data command (84H) but with the capability to input the data bytes by four pins: SIO0, SIO1, SIO2, and SIO3. The command sequence is shown below. The Quad Enable bit (QE) of feature (B0[0]) must be set to enable for the program load random data x4 command. See figure 20 for details. Those two commands are only available during internal data move sequence.

Figure20. Program Load Random Data x4 Sequence Diagram

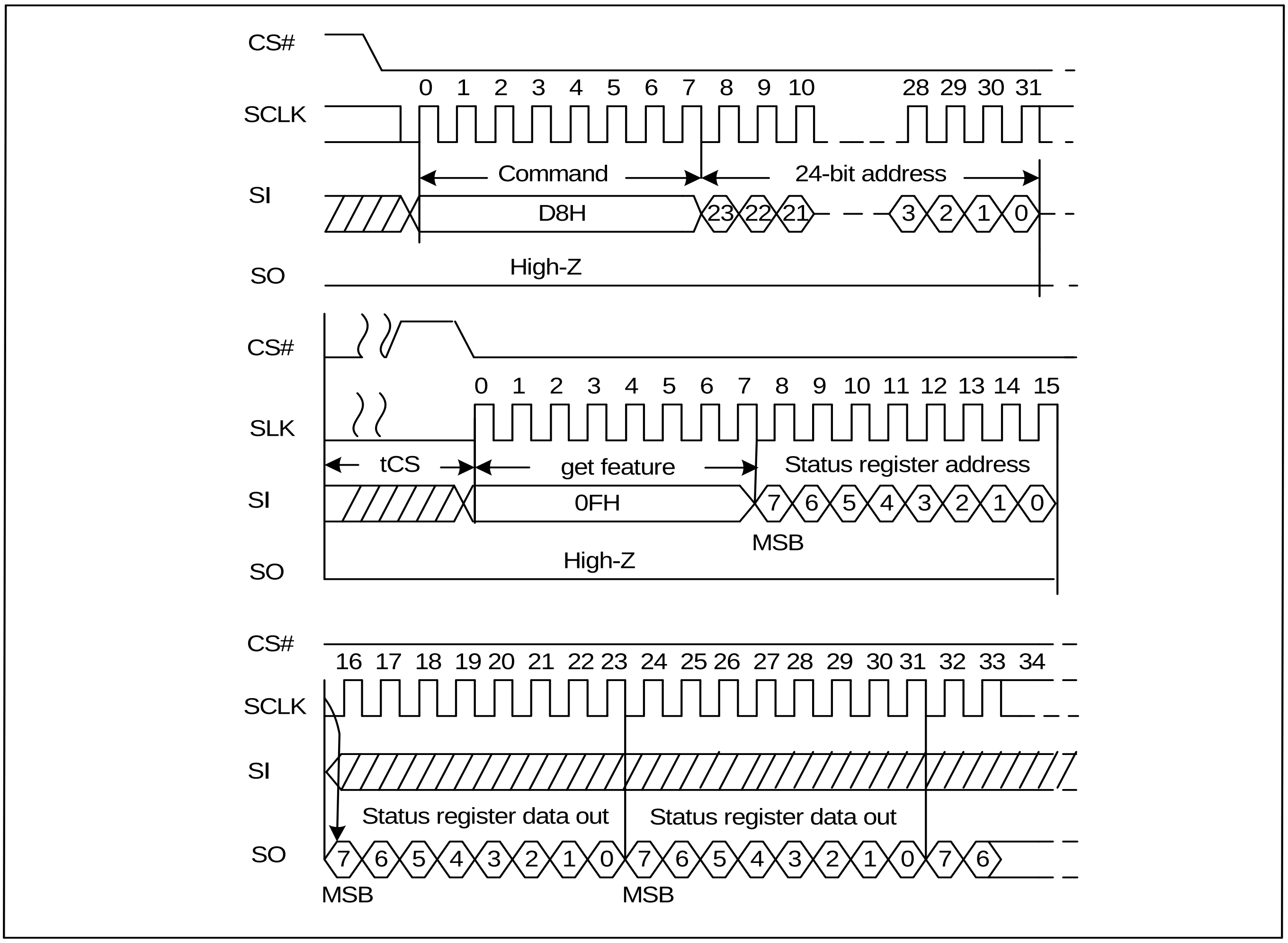


Note: when internal ECC disabled the Data is 2175, when internal ECC enabled the Data is 2111.

12 ERASE OPERATIONS

12.1 Block Erase (D8H)

Figure21. Block Erase Sequence Diagram



The BLOCK ERASE (D8H) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2176 bytes per page (2048 + 128 bytes). Each block is136 Kbytes. The BLOCK ERASE command (D8H) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06H (WRITE ENBALE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITEENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8H) command. This command requires a 24-bit address. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for t_{ERS} time during the BLOCK ERASE operation. The GET FEATURES (0FH) command can be used to monitor the status of the operation.

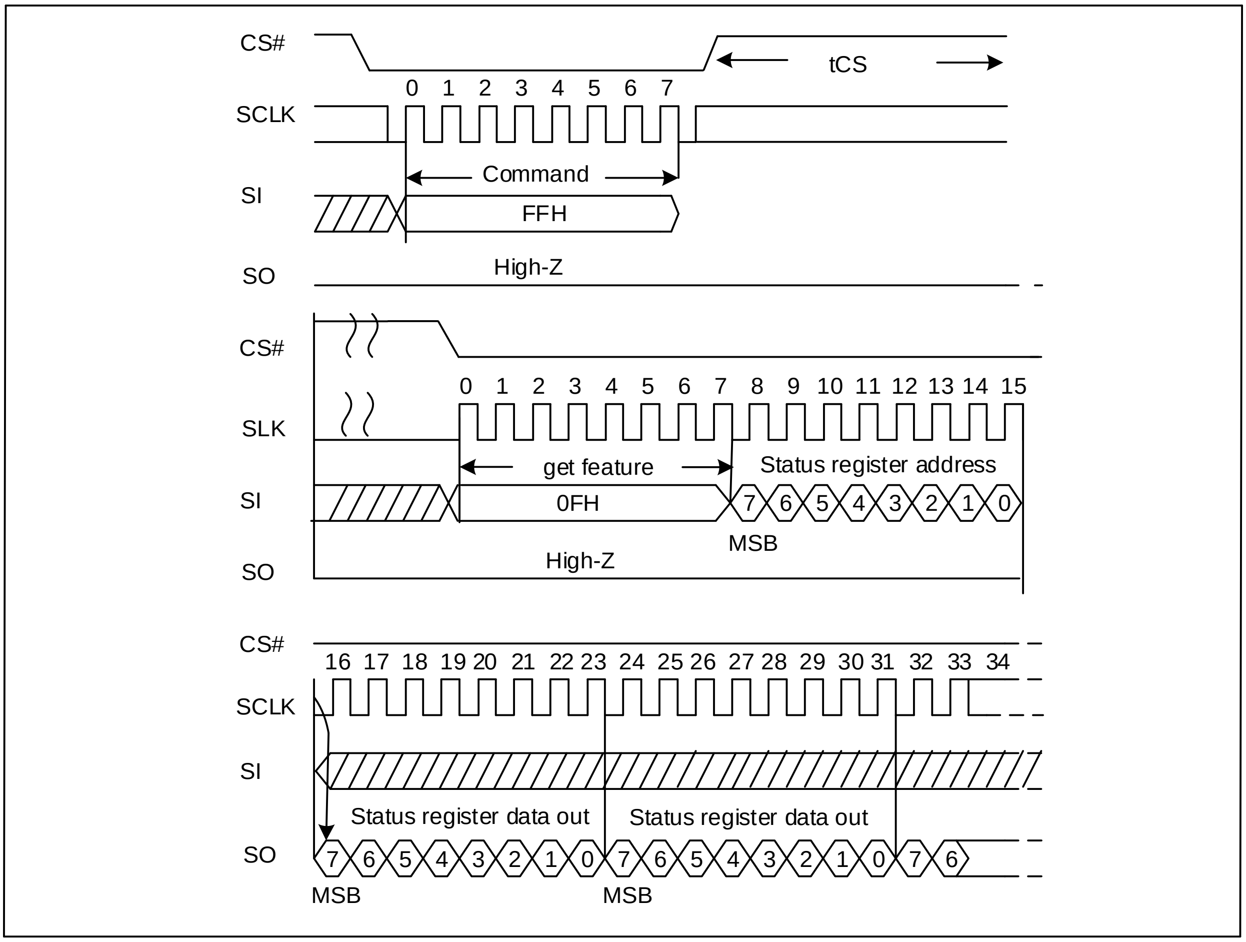
When a block erase operation is in progress, user can issue normal read from cache commands

(03H/0BH/3BH/6BH/BBH/EBH) to read the data in the cache.

13 RESET OPERATIONS

13.1 Reset (FFH)

Figure22. Reset Sequence Diagram



The RESET (FFH) command stops all operations. For example, in case of a program or erase or read operation, the reset command can make the device enter the wait state.

During a cache program or cache read, a reset can also stops the previous operation and the pending operation. The OIP status can be read from 300ns after the reset command is sent.

14 ADVANCED FEATURES

14.1 OTP Region

The serial device offers a protected, One-Time Programmable NAND Flash memory area. 4 full pages (2176 bytes per page) are available on the device. Customers can use the OTP area any way they want, like programming serial numbers, or other data, for permanent storage. When delivered from factory, feature bit OTP_PRT is 0.

To access the OTP feature, the user must set feature bits OTP_EN/OTP_PRT by SET FEATURES command. When the OTP is ready for access, pages 00h–03H can be programmed in sequential order by PROGRAM LOAD (02H) and PROGRAM EXECUTE(10H) commands (when not yet protected), and read out by PAGE READ (13H) command and output data by READ from CACHE(03H/0BH/3BH/6BH/BBH/EBH).

Table4. OTP States

OTP_PRT	OTP_EN	State
x	0	Normal operation
0	1	Access OTP region, read and program data.
1	1	1. When the device power on state OTP_PRT is 0, user can set feature bit OTP_PRT and OTP_EN to 1, then issue PROGRAM EXECUTE (10H) to lock OTP, and after that OTP_PRT will permanently remain 1. 2. When the device power on state OTP_PRT is 1, user can only read the OTP region data.

Note: The OTP space cannot be erased and after it has been protected, it cannot be programmed again, please use this function carefully.

Access to OTP data

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN
- Issue the PAGE PROGRAM (only when OTP_PRT is 0) or PAGE READ command

Protect OTP region

Only when the following steps are completed, the OTP_PRT will be set and users can get this feature out with 0FH command.

- Issue the SET FEATURES command (1FH)
- Set feature bit OTP_EN and OTP_PRT
- 06H (WRITE ENABLE)
- Issue the PROGRAM EXECUTE (10H) command.

14.2 Block Protection

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the “locked” state, i.e., feature bits BP0, BP1and BP2are set to 1, INV, CMP and BRWD are set to 0. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued to alter the state of protection feature bits. When BRWD is set and WP# is LOW, none of the writable protection feature bits can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, status bit OIP remains 0.When an ERASE command is issued to a locked block, the erase failure, 04H, is returned. When a PROGRAM command is issued to a locked block, program failure,08h, is returned.

Table5. Block Lock Register Block Protect Bits

CMP	INV	BP2	BP1	BP0	Protect Row Address	Protect Rows
					1G	
x	x	0	0	0	NONE	None—all unlocked
0	0	0	0	1	FC00h ~ FFFFh	Upper 1/64 locked
0	0	0	1	0	F800h ~ FFFFh	Upper 1/32 locked
0	0	0	1	1	F000h ~ FFFFh	Upper 1/16 locked
0	0	1	0	0	E000h ~ FFFFh	Upper 1/8 locked
0	0	1	0	1	C000h ~ FFFFh	Upper 1/4 locked
0	0	1	1	0	8000h ~ FFFFh	Upper 1/2 locked
x	x	1	1	1	0000h ~ FFFFh	All locked (default)
0	1	0	0	1	0000h ~ 03FFh	Lower 1/64 locked
0	1	0	1	0	0000h ~ 07FFh	Lower 1/32 locked
0	1	0	1	1	0000h ~ 0FFFh	Lower 1/16 locked
0	1	1	0	0	0000h ~ 1FFFh	Lower 1/8 locked
0	1	1	0	1	0000h ~ 3FFFh	Lower 1/4 locked
0	1	1	1	0	0000h ~ 7FFFh	Lower 1/2 locked
1	0	0	0	1	0000h ~ FBFFh	Lower 63/64 locked
1	0	0	1	0	0000h ~ F7FFh	Lower31/32 locked
1	0	0	1	1	0000h ~ EFFFh	Lower 15/16 locked
1	0	1	0	0	0000h ~ DFFFh	Lower7/8 locked
1	0	1	0	1	0000h ~ BFFFh	Lower3/4 locked
1	0	1	1	0	0000h ~ 003Fh	Block0
1	1	0	0	1	0400h ~ FFFFh	Upper 63/64 locked
1	1	0	1	0	0800h ~ FFFFh	Upper31/32 locked
1	1	0	1	1	1000h ~ FFFFh	Upper 15/16 locked
1	1	1	0	0	2000h ~ FFFFh	Upper7/8 locked
1	1	1	0	1	4000h ~ FFFFh	Upper3/4 locked
1	1	1	1	0	0000h ~ 003Fh	Block0

When WP# is not LOW, user can issue bellowscommands to alter the protection states as want.

- Issue SET FEATURES register write (1FH)
- Issue the feature bit address (A0h) and the feature bits combination as the table

14.3 Status Register and Driver Register

The NAND Flash device has a 16-bit status register that software can read during thedevice operation for operation state query. The status register can be read by issuing the GET FEATURES (0FH)command, followed by the feature address C0h (see FEATURE OPERATION). The Output Driver Register can be set and read by issuing the SET FEATURE (0FH) and GET FEATURE command followed by the feature address D0h (see FEATURE OPERATION)..

Table6. Status Register Bit Descriptions

Bit	Bit Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0).
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is executing, indicating the device is busy. When the bit is 0, the interface is in the ready state.
ECCS2~ECCS0	ECC Status	ECCS2~ECCS0 provides ECC status as the following table.

Table7. ECC Status

ECCS2	ECCS1	ECCS0	Description
0	0	0	No bit errors were detected during the previous read algorithm.
0	0	1	Bit errors(<3) were detected and corrected.
0	1	0	Bit errors(=4) were detected and corrected.
0	1	1	Bit errors(=5) were detected and corrected.
1	0	0	Bit errors(=6) were detected and corrected.
1	0	1	Bit errors(=7) were detected and corrected.
1	1	0	Bit errors(=8) were detected and corrected.
1	1	1	Bit errors>8, error exceeded. And cannot be corrected.

Table8. Driver Register Bits Descriptions

DS_S1	DS_S0	Driver Strength
0	0	50%
0	1	25%
1	0	75%
1	1	100%

14.4 Assistant Bad Block Management

As a NAND Flash, the device may have blocks that are invalid when shipped from the factory, and a minimum number of valid blocks (N_{VB})of the total available blocks are specified. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below N_{VB} during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms, which ensure data integrity. Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by programming the Bad Block Mark (00h) to the first spare area location in each bad block. This method is compliant with ONFI Factory Defect Mapping requirements. See the following table I bad-block mark.

System software should initially check the first spare area location for non-FFH data I first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

To simplify the system requirement and guard the data integration, GigaDevice SPI NAND provides assistant Management options as below.

Table9. Bad Block Mark information

Description	Density	Requirement
Minimum number of valid blocks (N_{VB})	1G	1004
Total available blocks per die	1G	1024
First spare area location		Byte 2048
Bad-block mark		00h(use non FFH to check)

14.5 Internal ECC

The serial device offers data corruption protection by offering optional internal ECC.READs and PROGRAMs with internal ECC can be enabled or disabled by setting feature bit ECC_EN. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the “active” state. To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURES command (1FH).
- Set the feature bit ECC_EN as you want:
  1. To enable ECC, Set ECC_EN to 1.
  2. To disable ECC, Clear ECC_EN to 0.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If error bits are detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. The ECC Protection table below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table below.

• ECC can protect according main and spare areas. WRITEs to the ECC area are ignored.

Table10. ECC Protection and Spare Area

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
80Fh	800h	Yes	Spare 0	User meta data 0(1)
81Fh	810h	Yes	Spare 1	User meta data 1
82Fh	820h	Yes	Spare 2	User meta data 2
83Fh	830h	Yes	Spare 3	User meta data 3
87Fh	840h	Yes	Spare Area	Internal ECC parity data

Note1:800H is reserved for initial bad block mark, and please check the initial bad block mark with internal ECC off.

15 POWER ON TIMING

Figure23. Power on Timing Sequence

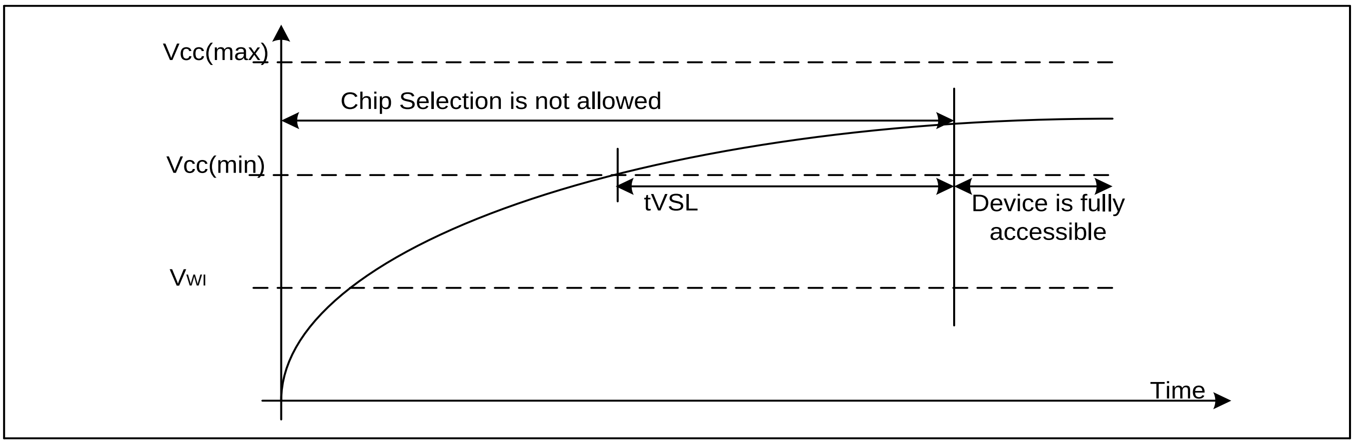


Table11-1. Power-On Timing and Write Inhibit Threshold for 1.8V/3.3V

Symbol	Parameter		Min	Max	Unit
tVSL	VCC(min) To CS# Low		5		ms
VWI	Write Inhibit Voltage	1.8V		1.7	V
		3.3V		2.5	

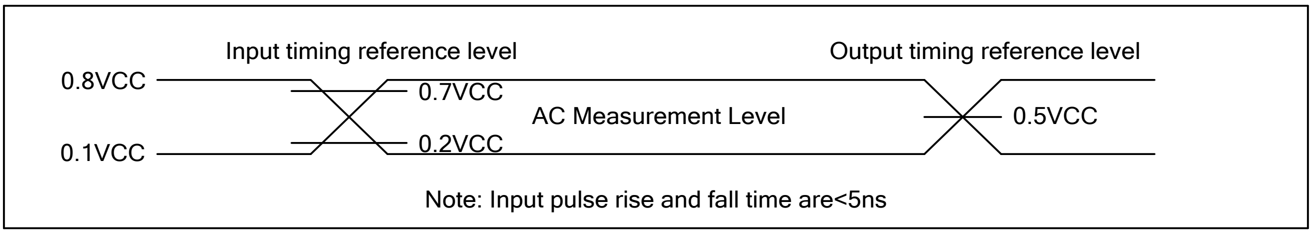
16 ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Applied Input/Output Voltage	-0.6 to 4.0	V
VCC	-0.6 to 4.0	V

17 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
C_L	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.2VCC to 0.7VCC			V	
	Output Timing Reference Voltage	0.5VCC			V	

Figure24. Input Test Waveform and Measurement Level



18 DC CHARACTERISTIC

(T= -40℃~85℃, VCC=1.7~2.0V/2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC, V_{IN}=VCC or VSS			90	μA
I_{CC2}	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 120MHz, Q=Open(*1,*2,*4 I/O)			40	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)			30	mA
I_{CC3}	Operation Current (PP)	CS#=VCC			40	mA
I_{CC4}	Operation Current (BE)	CS#=VCC			40	mA
V_{IL}	Input Low Voltage				0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC			V
V_{OL}	Output Low Voltage	I_{OL} =1.6mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} =-100μA	VCC-0.2			V

19 AC CHARACTERISTICS

(T= -40℃~85℃, VCC=1.7~2.0V/2.7~3.6V, C_L=30pf)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
F_C	Serial Clock Frequency For: all command	DC.		120	MHz
tCH	Serial Clock High Time	4			ns
tCL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL/tCS	CS# High Time	20			ns
tSHQZ	Output Disable Time			20	ns
tCLQX	Output Hold Time	2			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5			ns
tHHCH	Hold# High Setup Time (relative to Clock)	5			ns
tCHHL	Hold# High Hold Time (relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			15	ns
tHHQX	Hold# HighTo Low-Z Output			15	ns
tCLQV	Clock Low To Output Valid			8	ns
tWHSL	WP# Setup Time Before CS# Low	20			ns
tSHWL	WP# Hold Time After CS# High	100			ns

20 PERFORMANCE TIMING

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tRST	CS# High To Next Command After Reset(FFh)			500	us
tRD	Read From Array			80	us
tPROG	Page Programming Time		0.4	0.7	ms
tBERS	Block Erase Time		3	5	ms

Figure25. Serial Input Timing

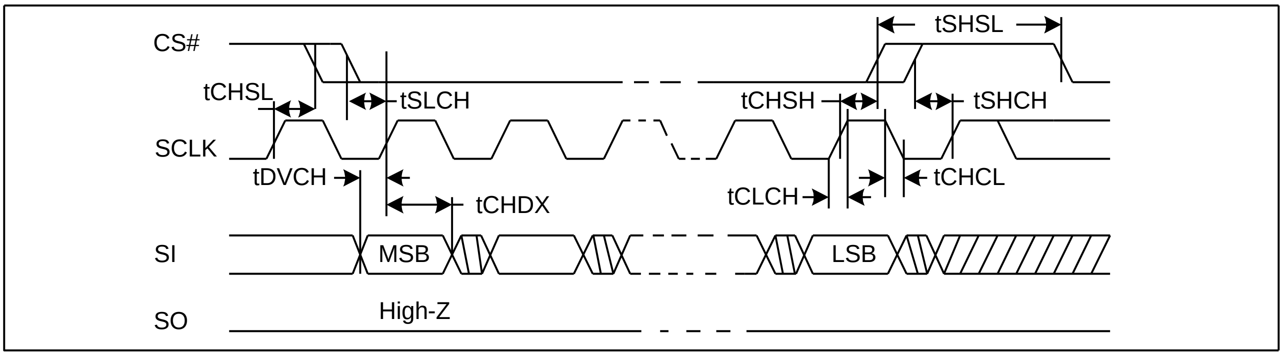


Figure26. Output Timing

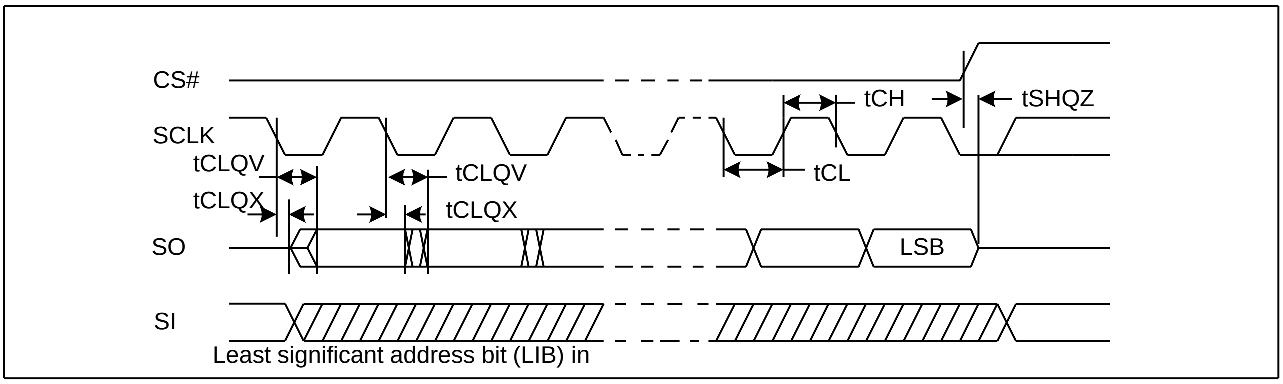


Figure27. Hold Timing

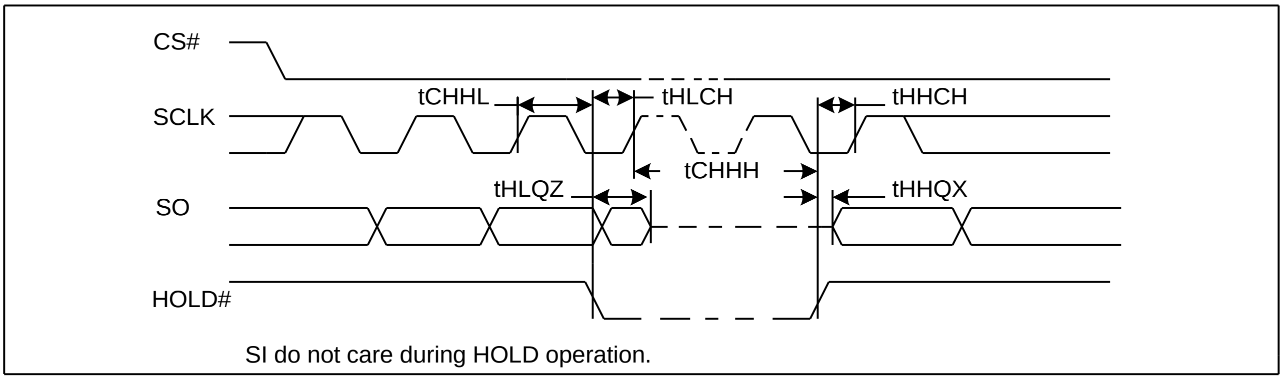
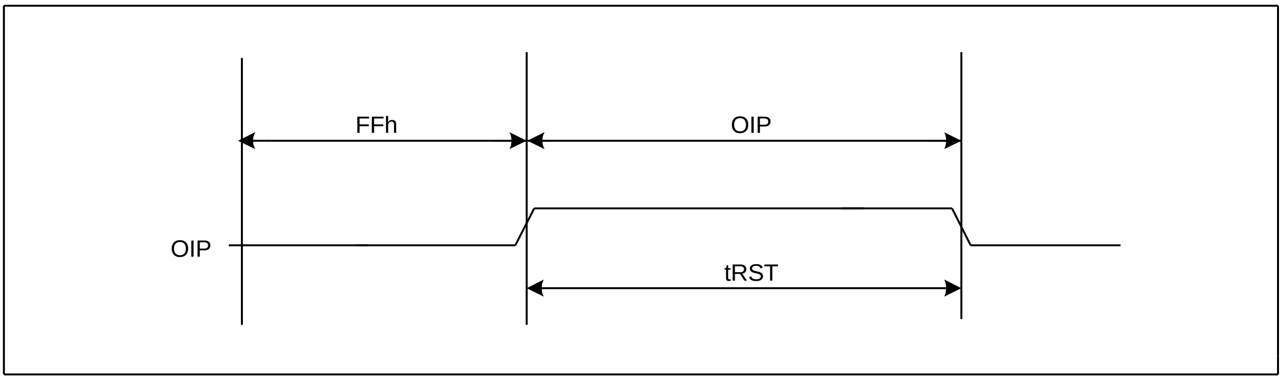


Figure28. Reset Timing



Note: The maximum tRST depends on different operations.

Idle:	maximum tRST = 5us;
Read:	maximum tRST = 5us;
Program:	maximum tRST = 10us;
Erase:	maximum tRST = 500us;

21 ORDERING INFORMATION

GD XX XX XX X X X X X X

GD Prefix

Packing Type
T or No mark: Tube
R: Tape & Reel
Y: Tray

Green Code
G: Pb Free & Halogen Free Green Package
S: Pb Free & Halogen Free Green Package + special function(HW reset +UID/CID+parameter page)

Temperature Range
I: Industrial(-40C to +85C)
J:Industrial(-40 ℃ to +105 ℃)
F: Industrial+[(1)] (-40 ℃ to +85 ℃)

Package Type
Y: WSON8 (6*8mm)
F: SOP16 300mil
Z:TFBGA24(6*4 Ball Array)
9: LGA8 6*8mm

Generation
B: B Version
C: C Version
E: E Version
F: F Version

Voltage
U:3.3V(2.7~3.6V)
R:1.8V(1.7~2.0V)

Interface
Q4: Qua SPI x1/x2/x4

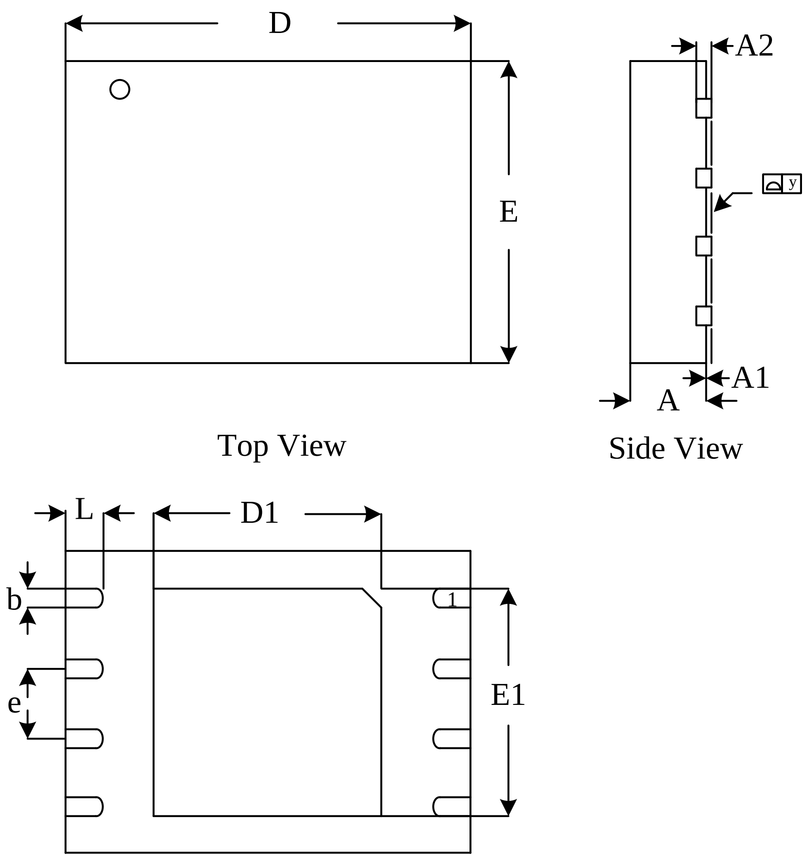
Density
1G: 1Gb 2G: 2Gb
4G: 4Gb 8G: 8Gb

Product Family
5F: SPI NAND Flash

Note: (1) Industrial+: Full Function Test for Automotive application and no AECQ

22 PACKAGE INFORMATION

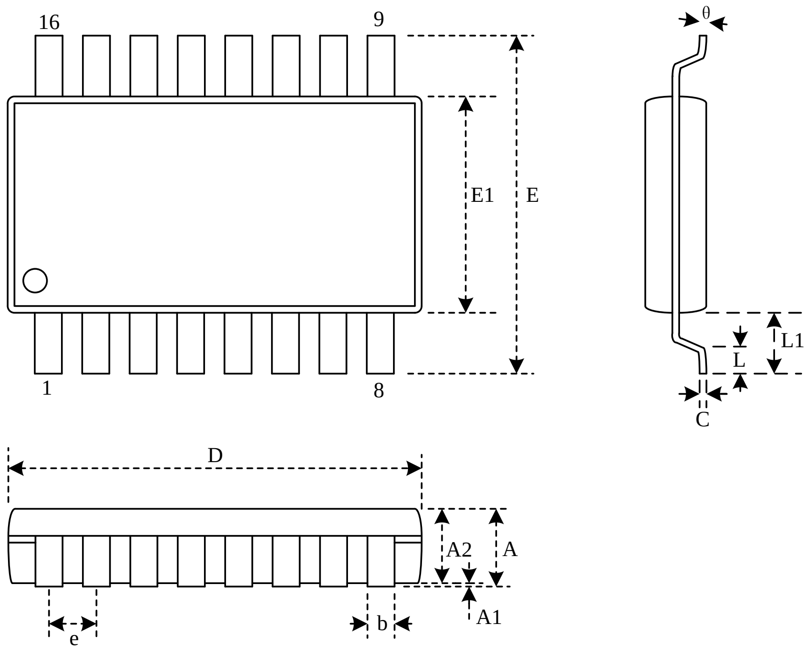
Figure29. WSON8 (8*6mm)



Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.70			0.35	7.95	3.25	5.95	4.15		0.00	0.40
	Nom	0.75		0.20	0.40	8.00	3.40	6.00	4.30	1.27		0.50
	Max	0.80	0.05		0.45	8.05	3.50	6.05	4.40		0.05	0.60
Inch	Min	0.028			0.014	0.313	0.128	0.234	0.163		0.00	0.016
	Nom	0.030		0.008	0.016	0.315	0.134	0.236	0.169	0.05		0.020
	Max	0.032	0.002		0.019	0.317	0.138	0.238	0.173		0.002	0.024

Figure30. SOP16 300MIL

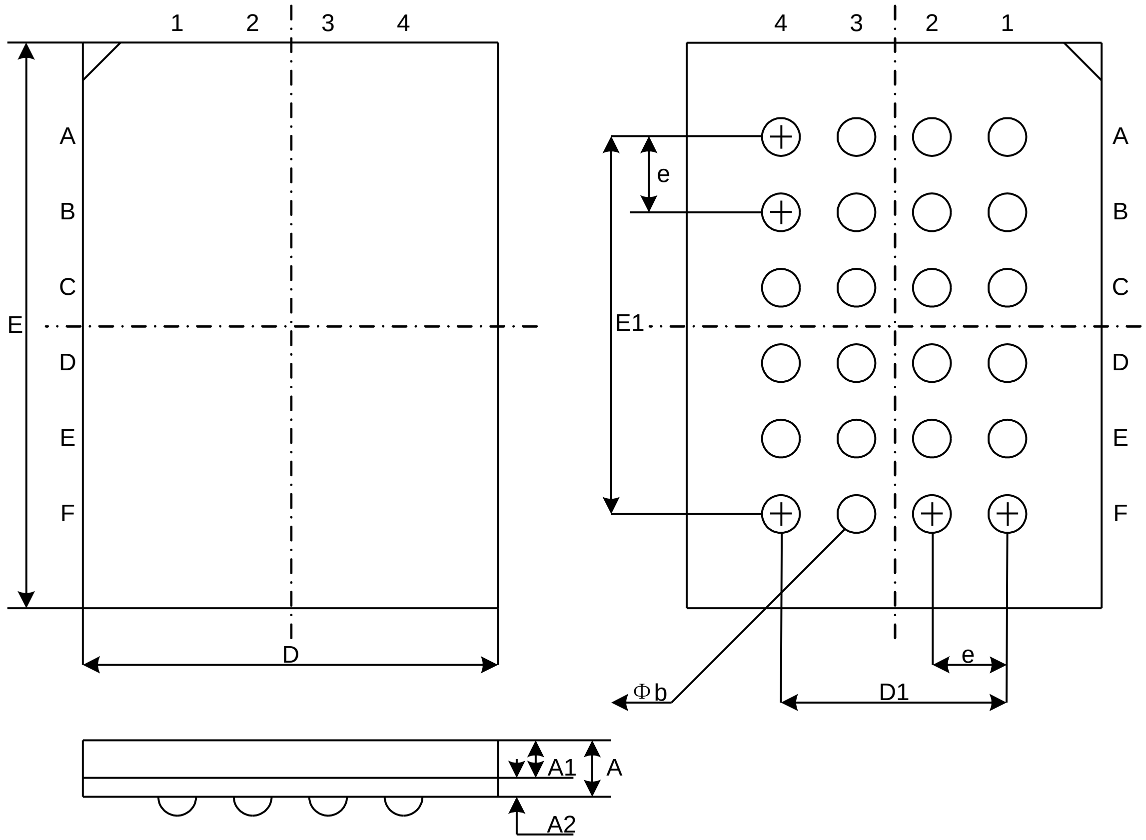


Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0.51	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27	0.84	1.44	0.64	5
	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	0.77	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0.020	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050	0.033	0.057	0.025	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	0.030	8

Note:Both package length and width do not include mold flash.

Figure31. TFBGA-24BALL (6*4 ball array)

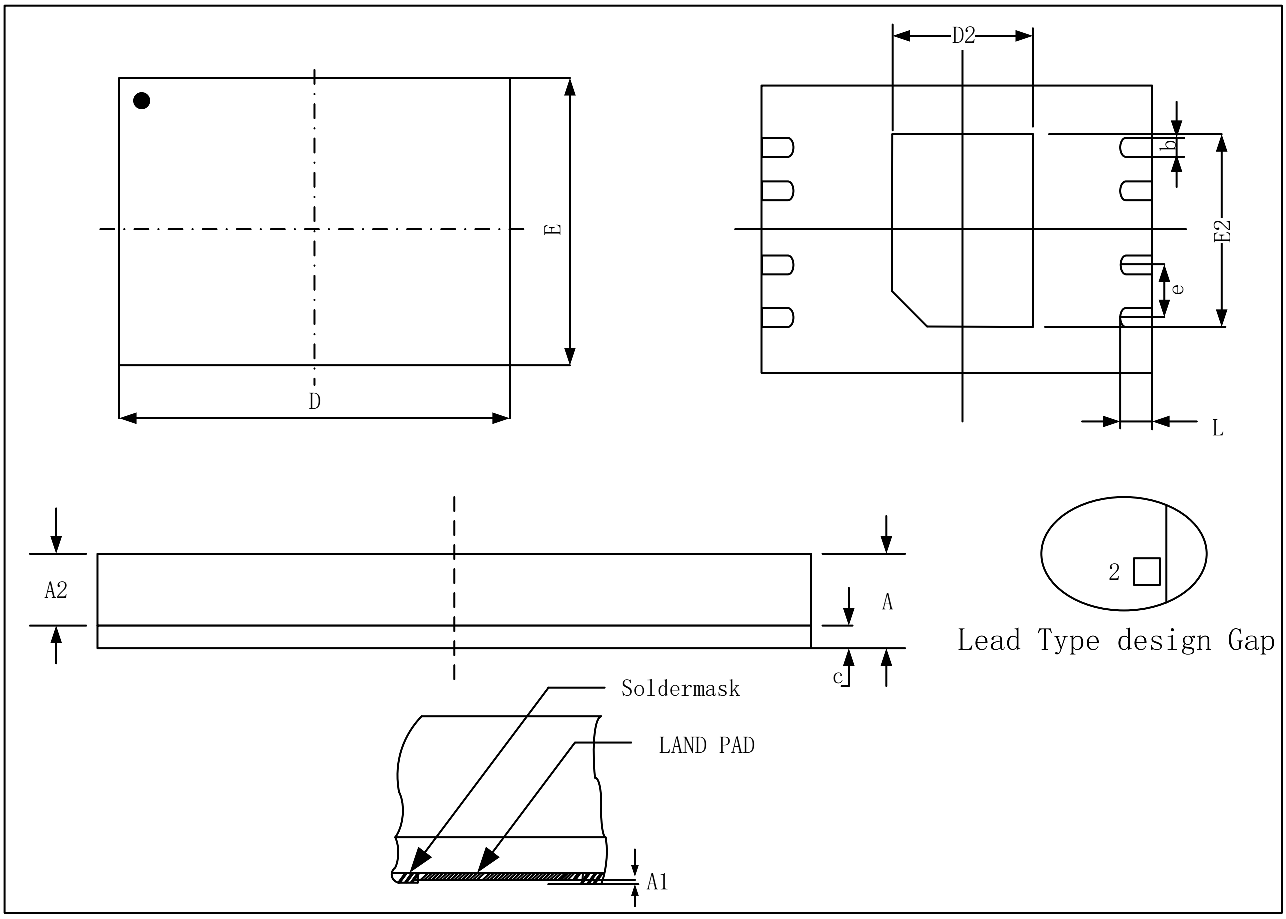


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30	0.85	0.40	6.00	3.00	8.00	5.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010		0.014	0.232		0.311		
	Nom		0.012	0.033	0.016	0.236	0.120	0.315	0.200	0.039
	Max	0.047	0.014		0.018	0.240		0.319		

Note：Both package length and width do not include mold flash.

Figure32. LGA8 GD Type1 (6*8 mm)



Dimensions

Symbol		A	A1	A2	c	b	D	D2	E	E2	e	L
Unit		GD Type1		GD Type1								
mm	Min	0.70	0.02	0.53	0.15	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom				0.18	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80			0.21	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0.001	0.021	0.006	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom				0.007	0.016	0.315	0.134	0.236	0.169		0,020
	Max	0.031			0.008	0.018	0.319	0.138	0.240	0.173		0.022

23 REVISION HISTORY

Version No	Description	Date
1.0	Initial Release Modify DC CHARACTERISTIC, add I_{CC3} and I_{CC4}	2015-3-18
1.1	Modify WSON8 (8*6mm)	2015-6-23
1.2	Add package TFBGA-24BALL (6*4 ball array)	2015-8-12
1.3	Modify ORDERING INFORMATION	2015-10-28
1.4	Add Block0 description	2016-4-1
1.5	Add 24Ball TFBGA package ball define	2016-7-7
1.6	Change power on timing parameter	2016-9-9
1.7	Remove Hardware reset timing at Page39	2016-10-28
1.8	Change tCLQX from 0ns to 2ns	2016-11-14
1.9	Add description at Ch11.1 for Cache register at program	2016-12-14
2.0	Change standby current from 70uA to 90uA Add LGA8 Package POD	2017-4-18
2.1	Update ordering Information	2017-4-20
2.2	Update LGA8 POD size	2017-6-23
2.3	Modify the Number of Figure and Table Modify Package 'R' description	2017-9-1
2.4	Add the Note article 4 of Page Program	Oct.23.2017
2.5	Add the chapter of Valid Part Numbers	Nov.3.2017
2.6	Add the description of 1Gb SLC NAND Flash Delete Valid Part Number of GD5F1GQ4UC9IG	Nov.30.2017
2.7	Modify the Figure of Program Load Sequence Diagram typo Modify the package of LGA8	Dec.11.2017
2.8	Modify the typo of LGA8	Dec.27.2017
2.9	Modify some typo Change Memory Mapping CA from<12:0> to <11:0> Add byte1 and byte2 for two Device ID in Read Sequence Diagram Add page size 2048bytes + 64bytes with ECC enabled Modify figures 16,17,19,20 from Byte 2175 to 2175/2111 and add a note to explain Merge Chapters 2.1 and 21.1 Change the description of protection with WP# Pin	Feb.13.2018
3.0	Improve the Part No in Table3 Modify the Value of Applied Input/ Output Voltage and VCC in Chapter15 Modify the description of LGA8 6*8mm package Update Ordering Information	Jul. 25, 2018

Important Notice