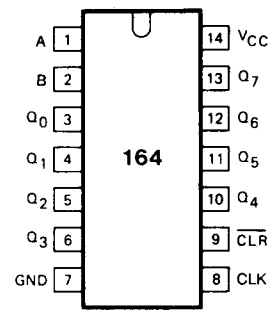
GD54/74HC164, GD54/74HCT164

8 BIT SERIAL-IN/PARALLEL-OUT SHIFT REGISTER

General Description

These devices are identical in pinout to the 54/74LS164. This circuit is an 8-bit, serial-input to parallel-output shift-register. Two serial data inputs are provided so that one input may be used as a data enable. Data at the serial inputs may be changed while the clock, is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register at the rising edge of the clock pulse, where each register is a D-type master/slave flip-flop. An asynchronous clear is provided, which is activated when a low level is present at its input. Clear is independent of the clock and accomplished by a low level at the clear input. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS				OUTPUTS	
	$\overline{CLR}$	CLK	A	B	Q_0	Q_1—Q_7
reset (clear)	L	X	X	X	L	L—L
shift	H	↑	l	l	L	q_0—q_6
	H	↑	l	h	l	q_0—q_0
	H	↑	h	l	L	q_0—q_6
	H	↑	h	h	H	q_0—q_0

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

Logic Diagram

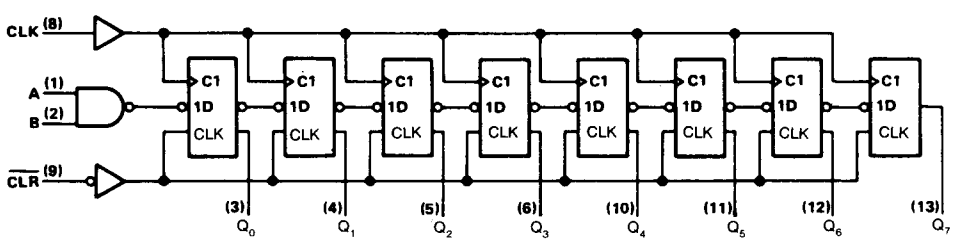


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I < -0.5$ or $V_I > V_{CC}+0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V < V_O < V_{CC}+0.5V$		|25|	mA
I_{CC}	DC V_{CC} or GND current			|50|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC}: GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: GD74 Types	−40	+85	°C
GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f: GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5 V		500	

Typical Clear, Shift, and Clear Sequences

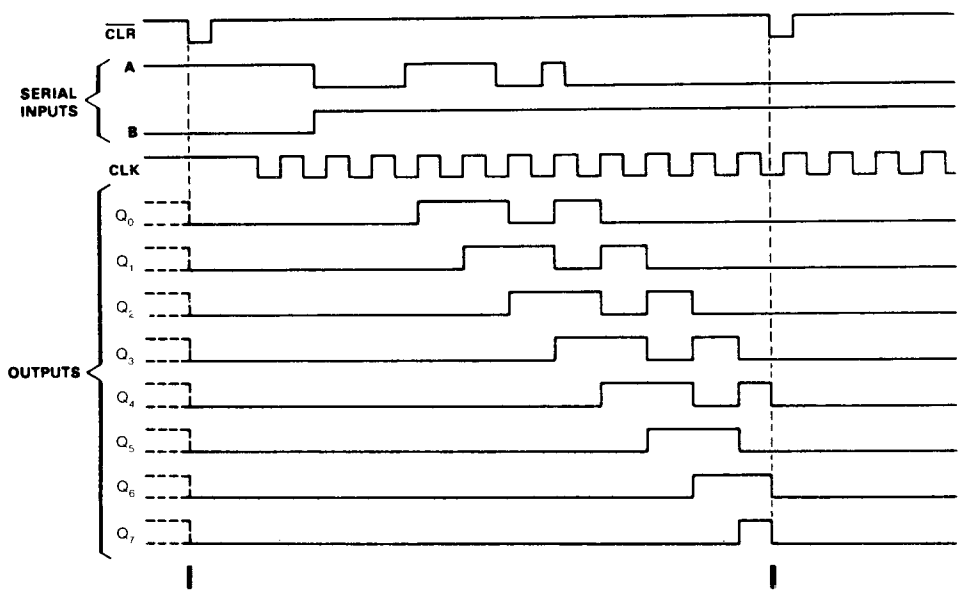


Fig. 2 Typical clear, shift, and clear sequences

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC164		GD54HC164		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			$I_{OH}=-4mA$ $I_{OH}=-5.2mA$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			$I_{OL}=4mA$ $I_{OL}=5.2mA$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT164		GD54HCT164		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5		4.4		4.4		V
			$I_{OH}=-4mA$	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5			0.1		0.1		0.1	V
			$I_{OL}=4mA$	4.5		0.17	0.26		0.33		0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HC164		GD54HC164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{CLR}$ low	2.0	60			75		90		ns
			4.5	12			15		18		
			6.0	10			13		15		
		CLK high or low	2.0	80			100		120		ns
			4.5	16			20		24		
			6.0	14			17		20		
t_{su}	Setup time	A,B to CLK	2.0	60			75		90		ns
			4.5	12			15		18		
			6.0	10			13		15		
t_{rec}	Recovery time	$\overline{CLR}$ to CLK	2.0	60			75		90		ns
			4.5	12			15		18		
			6.0	10			13		15		
t_h	Hold time	A,B to CLK	2.0	5			5		5		ns
			4.5	5			5		5		
			6.0	5			5		5		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC}	$T_A=25°C$			GD54HC164		GD74HC164		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0	6	10		5		42		MHz
		4.5	31	54		25		21		
		6.0	36	62		28		25		
t_{PLH} / t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Q_n	2.0		39	140		215		210	ns
		4.5		14	28		43		42	
		6.0		11	24		37		36	
t_{PLH} / t_{PHL}	Propagation Delay Time CLK to Q_n	2.0		41	170		175		110	ns
		4.5		15	34		35		22	
		6.0		12	29		30		19	
t_{TLH} / t_{THL}	Output Transition Time	2.0		19	75		95		100	ns
		4.5		7	15		19		22	
		6.0		6	13		16		18	

Timing Requirements for HCT : $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT164		GD54HCT164		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{CLR}$ low	4.5	18			23		27		ns
		CLK high or low	4.5	18			23		27		ns
t_{su}	Setup time	A,B to CLK	4.5	16			20		24		ns
t_{rec}	Recovery time	$\overline{CLR}$ to CLK	4.5	16			20		24		ns
t_h	Hold time	A,B to CLK	4.5	5			5		5		ns

AC Characteristics for HCT : $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT164		GD54HCT164		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frquency	4.5	27	55		22		18		MHz
t_{PLH} / t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Q_n	4.5		19	38		48		57	ns
t_{PLH} / t_{PHL}	Propagation Delay Time CLK to Q_n	4.5		17	36		45		54	ns
t_{TLH} / t_{THL}	Output Transition Time	4.5		7	15		19		22	ns

AC Waveforms

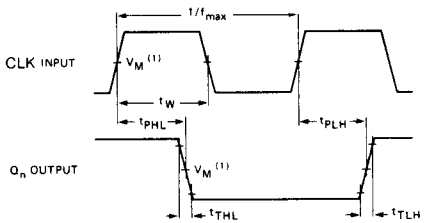


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

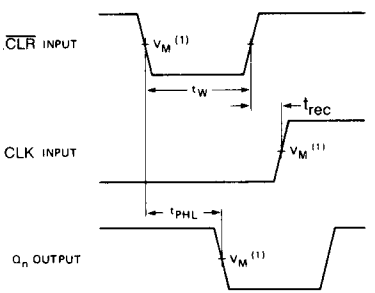


Fig. 4 Waveforms showing the master clear ($\overline{CLR}$) pulse width, the master clear, to output (Q_n) propagation delays and the master clear to clock (CLK) recovery time.

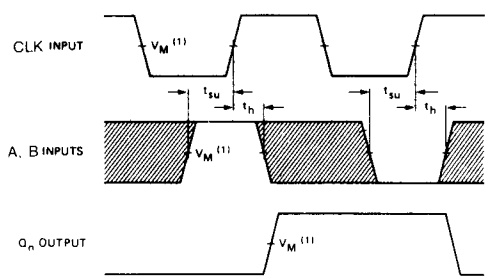


Fig. 5 Waveforms showing the data set-up and hold times for A,B inputs.

Note to AC waveforms

(1) HC : $V_M = 50\%$; $V_I = GND$ to V_{CC}.
HCT : $V_M = 1.3V$; $V_I = GND$ to 3V.