GENERAL SEMICONDUCTOR®

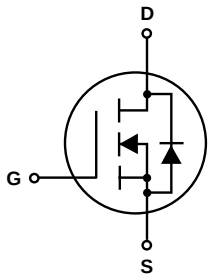
GFD2206

N-Channel Enhancement-Mode MOSFET

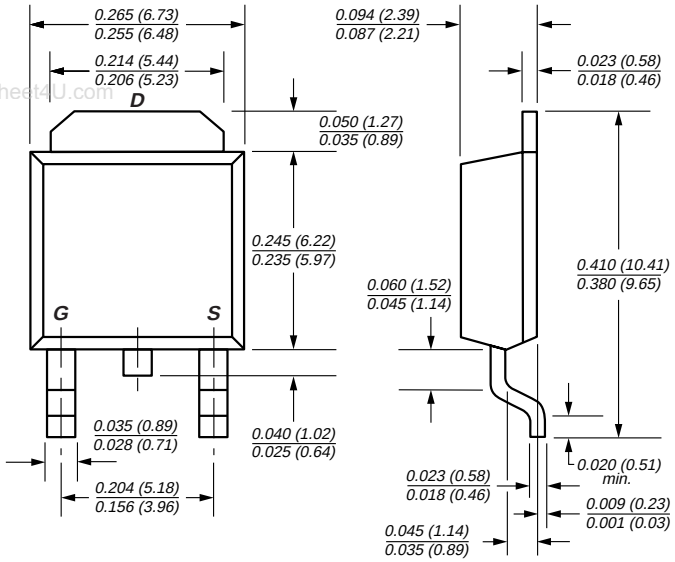
V_{DS} 60V $R_{DS(ON)}$ 22mΩ I_D 42A

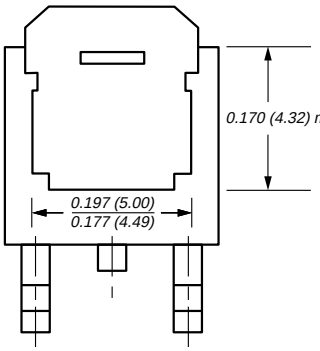
TRENCH GENFET®

New Product

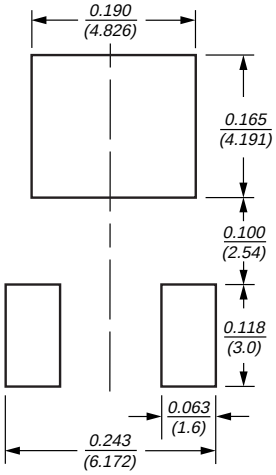


TO-252 (DPAK)





Dimensions in inches and (millimeters)



Mounting Pad Layout

Mechanical Data

Case: JEDEC TO-252 molded plastic body

Terminals: Solder plated, solderable per MIL-STD-750, Method 2026

High temperature soldering guaranteed: 250°C/10 seconds at terminals

Weight: 0.011oz., 0.4g

Features

- Advanced Trench Process Technology
- High Density Cell Design for Ultra Low On-Resistance
- Rugged-Avalanche Energy Rated
- Fast Switching for High Efficiency

Maximum Ratings and Thermal Characteristics (T_C = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current V_{GS} =10V	T_C = 25°C T_C = 100°C	I_D	42 26	A
Pulsed Drain Current[1]		I_{DM}	100	A
Maximum Power Dissipation	T_C = 25°C	P_D	62.5	W
Single Pulse Avalanche Energy[2]		E_{AS}	210	mJ
Avalanche Current[1]		I_{AR}	21	A
Repetitive Avalanche Energy[1]		E_{AR}	11	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C
Junction-to-Case Thermal Resistance		$R_{\theta JC}$	2	°C/W
Junction-to-Ambient Thermal Resistance[3]		$R_{\theta JA}$	40	°C/W

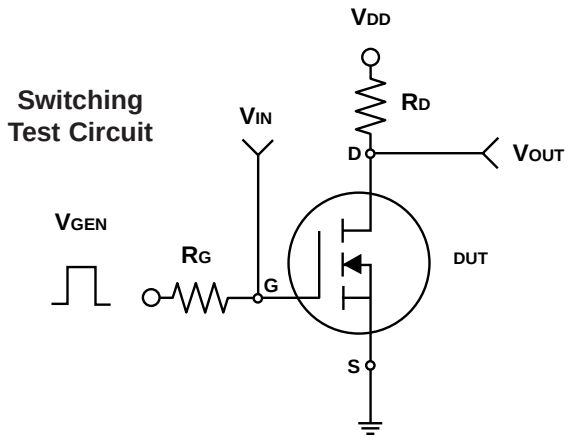
Notes: (1) Repetitive rating; pulse width limited by max. junction temperature
(2) V_{DD} = 30V, starting T_J = 25°C, L = 470μH, R_G = 25Ω, I_{AS} = 21A
(3) Mounted on 1in^2, 2oz. Cu pad on PCB

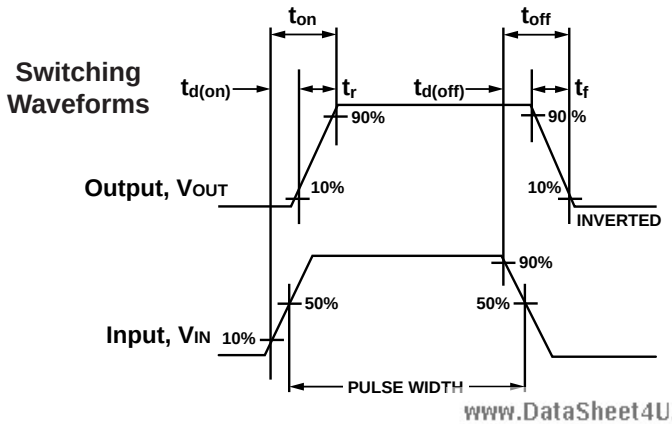
N-Channel Enhancement-Mode MOSFET

Electrical Characteristics (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	60	–	–	V
Drain-Source On-State Resistance(1)	$R_{DS(on)}$	V_{GS} = 10V, I_D = 21A	–	15	22	mΩ
		V_{GS} = 6V, I_D = 20A	–	19	25	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	–	4.0	V
Forward Transconductance(1)	g_{fs}	V_{DS} = 25V, I_D = 21A	–	50	–	S
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V	–	–	1	µA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V	–	–	±100	nA
Dynamic						
Total Gate Charge(1)	Q_g	V_{DS} = 48V, I_D = 21A, V_{GS} = 5V	–	36	50	nC
		V_{DS} = 48V, V_{GS} = 10V, I_D = 21A	–	65	80	
Gate-Source Charge(1)	Q_{gs}		–	15	—	
Gate-Drain ("Miller") Charge(1)	Q_{gd}		–	17	—	
Turn-On Delay Time(1)	$t_{d(on)}$	V_{DD} = 30V, I_D = 21A, R_G = 12Ω, R_D = 1.4Ω, V_{GEN} = 10V	–	20	35	ns
Rise Time(1)	t_r		–	107	160	
Turn-Off Delay Time(1)	$t_{d(off)}$		–	92	120	
Fall Time(1)	t_f		–	56	90	
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz	–	3425	–	pF
Output Capacitance	C_{oss}		–	320	–	
Reverse Transfer Capacitance	C_{rss}		–	162	–	
Source-Drain Diode						
Continuous Source Current	I_S	–	–	–	42	A
Pulsed Source Current	I_{SM}	–	–	–	100	
Diode Forward Voltage(1)	V_{SD}	I_S = 21A, V_{GS} = 0V	–	0.93	1.3	V
Source-Drain Reverse Recovery Time(1)	t_{rr}	I_F = 21A, di/dt = 100A/µs	–	53	–	ns
Source-Drain Reverse Recovery Charge(1)	Q_{rr}		–	92	–	nC

Notes: (1) Pulse width ≤ 300µs; duty cycle ≤ 2%





N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 1 – Output Characteristics

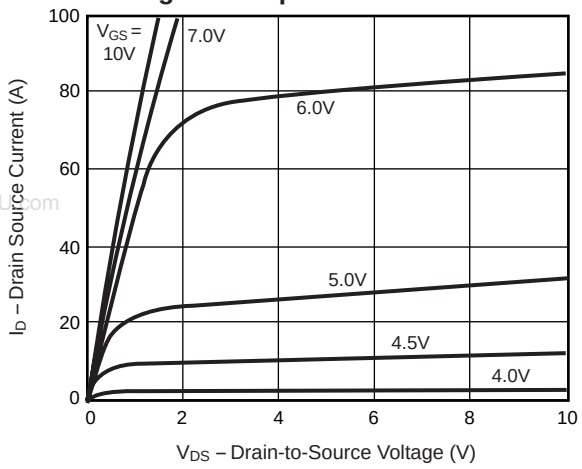


Fig. 2 – Transfer Characteristics

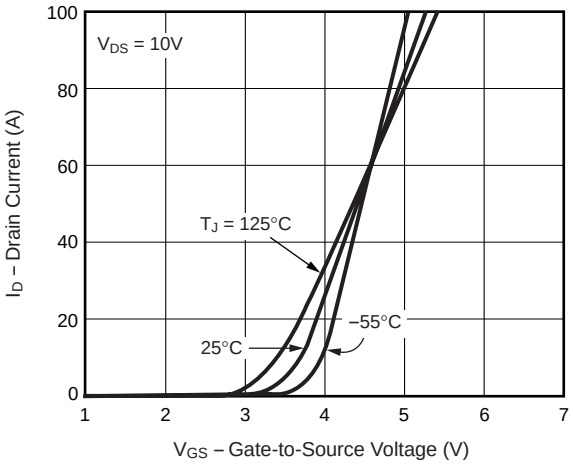


Fig. 3 – On-Resistance vs. Drain Current

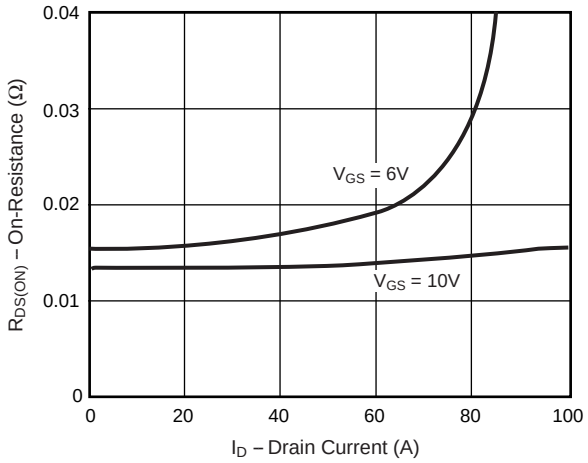


Fig. 4 – Capacitance

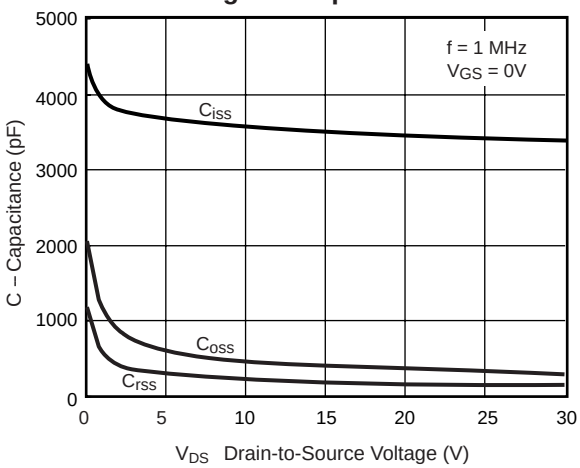


Fig. 5 – Gate Charge

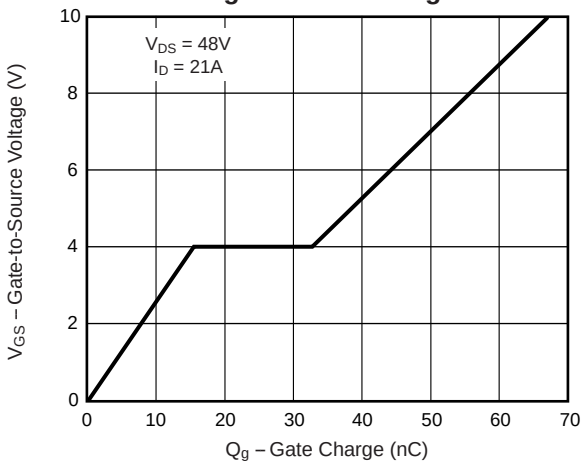
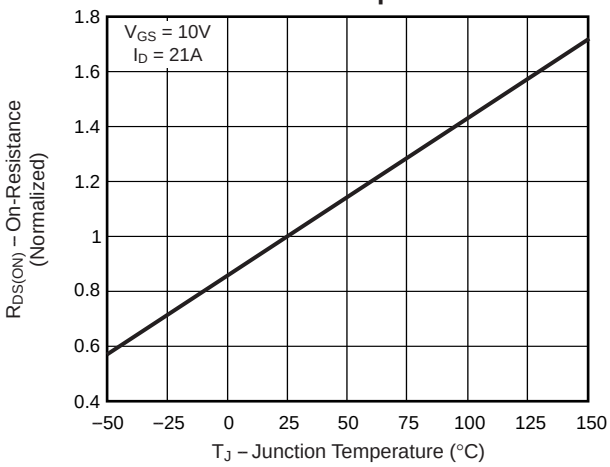


Fig. 6 – On-Resistance vs. Junction Temperature



N-Channel Enhancement-Mode MOSFET

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 7 – Source-Drain Diode Forward Voltage

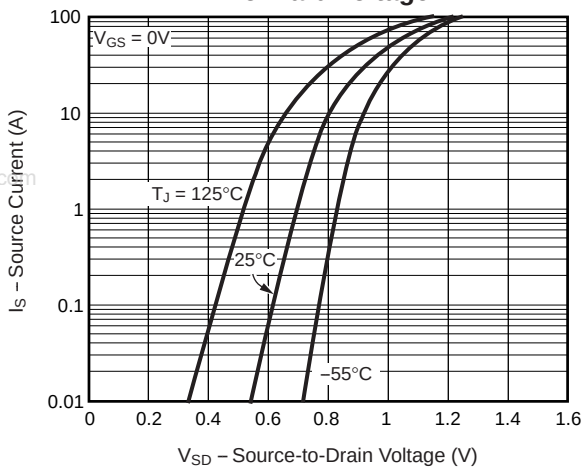


Fig. 8 – On-Resistance vs. Gate-to-Source Voltage

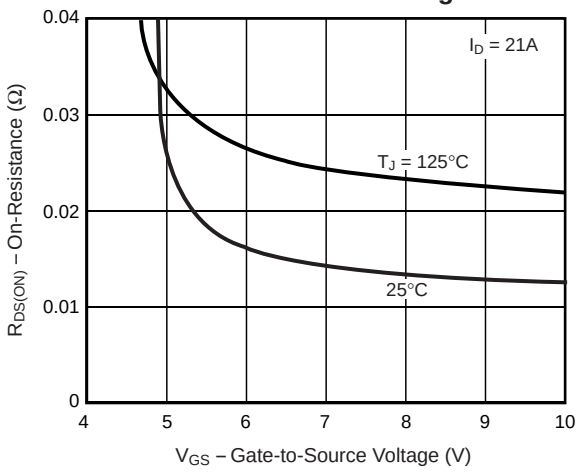


Fig. 9 – Threshold Voltage vs. Temperature

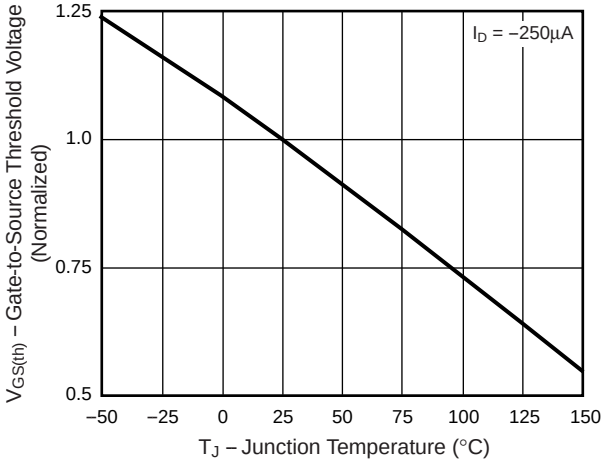


Fig. 10 – Power vs. Pulse Duration

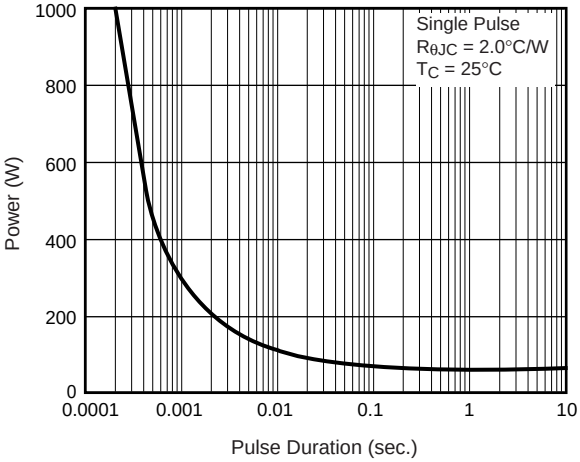


Fig. 11 – Maximum Safe Operating Area

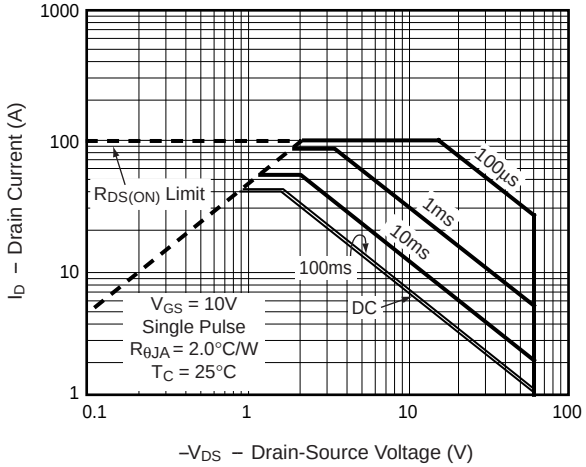


Fig. 12 – Thermal Impedance