GFP5N60

General Description(概述)

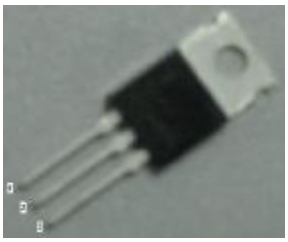
These N-Channel enhancement mode power field effect Transistors are produced using planar stripe, DMOS technology.

GFP5N60是增强型N沟道功率场效应管，采用平面条形DMOS工艺生产制造。

This advanced technology has been especially tailored to minimize on - state resistance , provide superior switching performance,and Withstand high energy pulse in the avalanche and commutaion mode .These devices are well suited for high efficiency switch mode power supply.

GFP5N60具有低导通电阻、优越的开关特性以及抗雪崩击穿能力，适合用于高效开关电源。

TO-220



1.Gate 2.Drain 3.Source

Absolute Maximum ratings（极限参数，除非另有规定，T=25 ℃ ）

Characteristics（参数）	Symbol（符号）	Value(额定值）	Units(单位)
漏源反向击穿电压	BV_{DSS}	600	V
连续漏极电流	I_D	5	A
栅源电压	V_{GS}	± 30	V
雪崩能量	E_{AS}	300	mJ
耗散功率	P_D	120	W
储存温度	T_{STG}	-55 ~150	℃
热阻(结到壳）	$R_{\theta JC}$	1.18	℃/ W
正向压降	V_{SD}	1.4	V

Characteristics 参数名称	Symbol (符号）	Min. (最小值)	Typ. (典型值)	Max. (最大值)	Units (单位)	Test Conditions (测试条件)
开启电压	$V_{GS}(th)$	2.0	-	4.0	V	V_{DS}= V_{GS},I_D=250uA
栅源漏电流	I_{GSS}	-	-	±100	nA	V_{GS}= ±30V, V_{DS}= 0V
漏源漏电流	I_{DSS}	-	-	10	uA	V_{DS}=600V ,V_{GS}= 0V
导通电阻	$R_{DS}(on)$	-	1.6	2.0	Ω	V_{GS}= 10V,I_D=2.5A
跨导	g_{fs}	-	4	-	S	V_{DS}= 50V, I_D=2.5A
输入电容	C_{iss}	-	560	730	pF	V_{GS}= 0V, V_{DS}= 25V F=1.0MHz
输出电容	C_{oss}	-	80	100		
传输电容	C_{rss}	-	9	12		
导通延迟时间	$td_{(on)}$	-	13	35	ns	V_{DD}= 300V, I_D= 5A R_G=25 Ω
上升时间	t_r	-	45	100		
下降延迟时间	$td_{(off)}$	-	35	80		
下降时间	t_f	-	40	90		
栅极存储电荷	Q_g	-	16	20	nC	V_{DS}= 480V, V_{GS}= 10V I_D=5A
栅源电荷	Q_{gs}	-	3.5	-		
栅漏电荷	Q_{gd}	-	7.8	-		

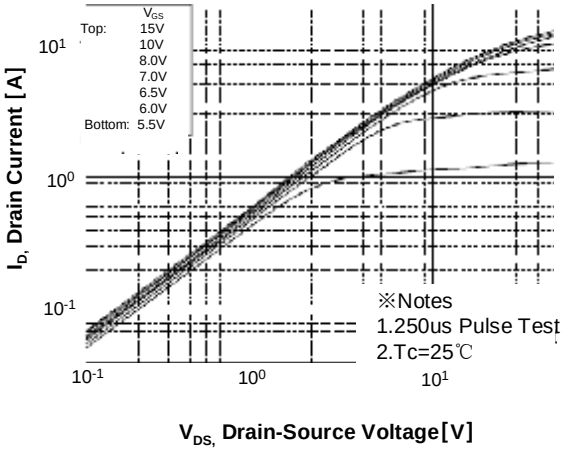


Figure 1.On-Region Characteristics

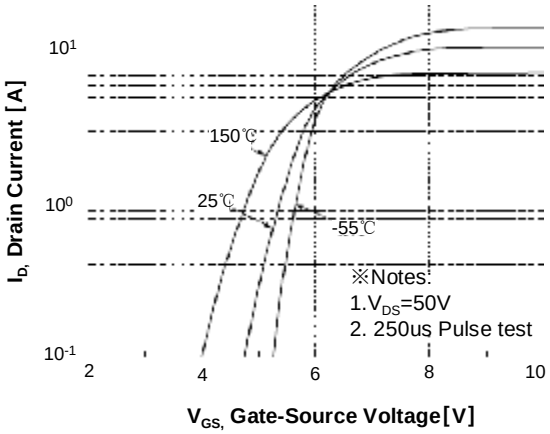


Figure 2.Transfet Characteristics

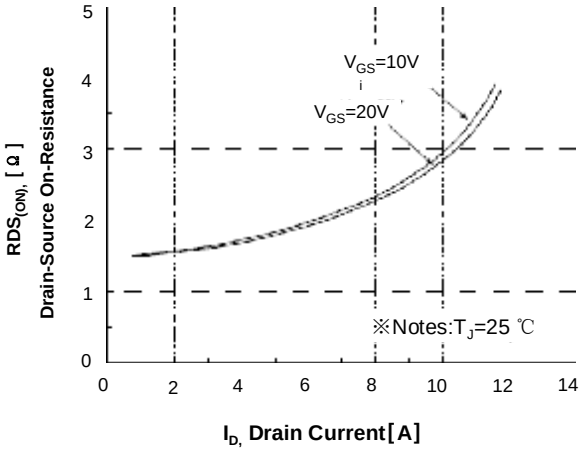


Figure 3.On-Resistance Variation vs. Drain Current and Gate Voltage

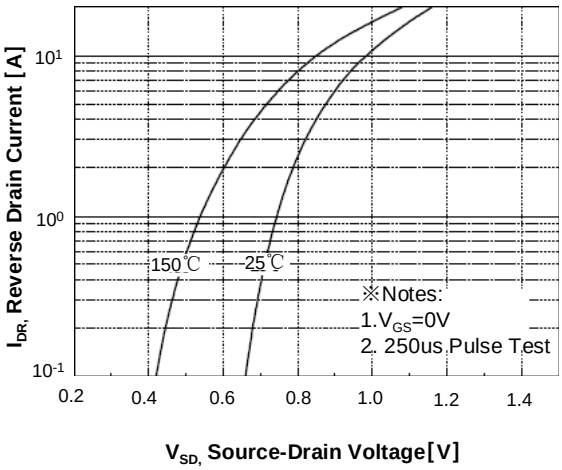


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

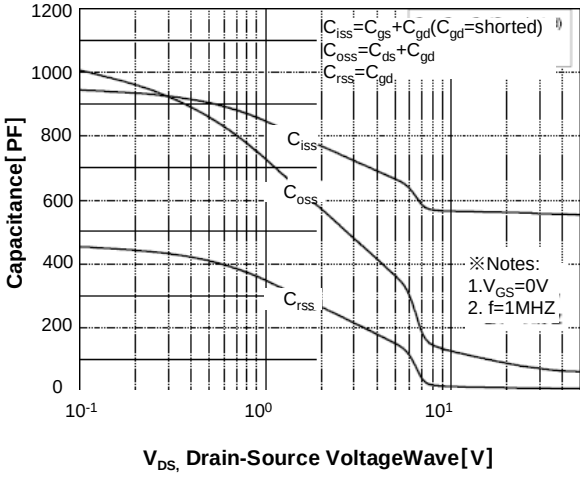


Figure 5.Capacitance Characteristics

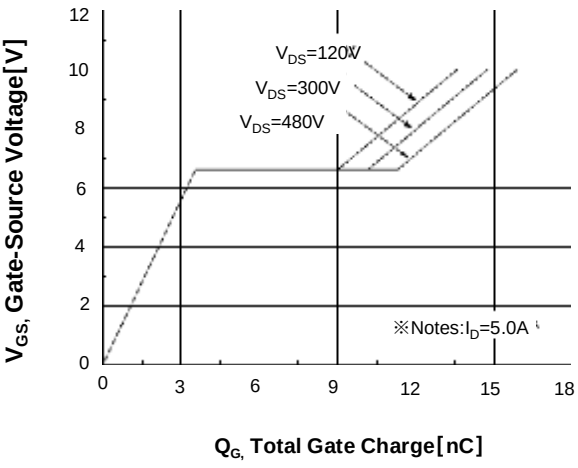


Figure 6. Gate Charge Characteristics

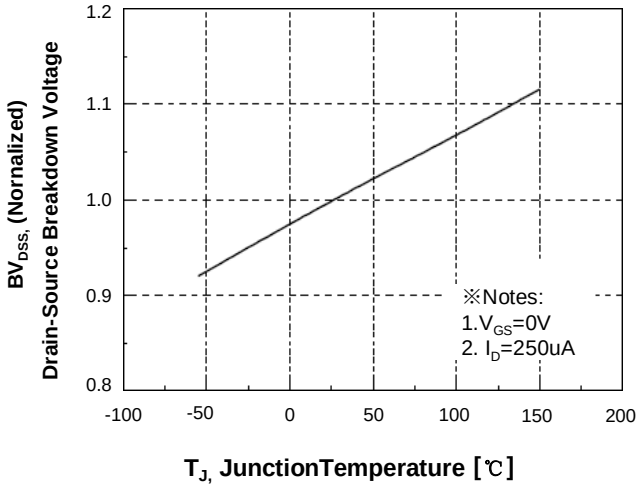


Figure 7. Breakdown Voltage Variation vs.Temperature

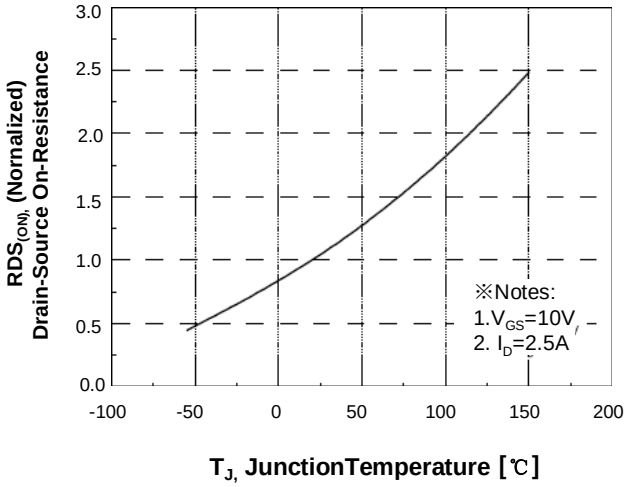


Figure 8. On-Resistance Variation vs.Temperature

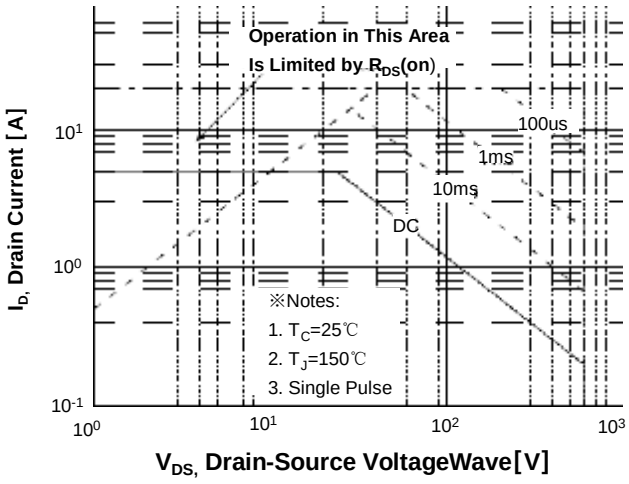


Figure 9. Maximum Safe Operating Area

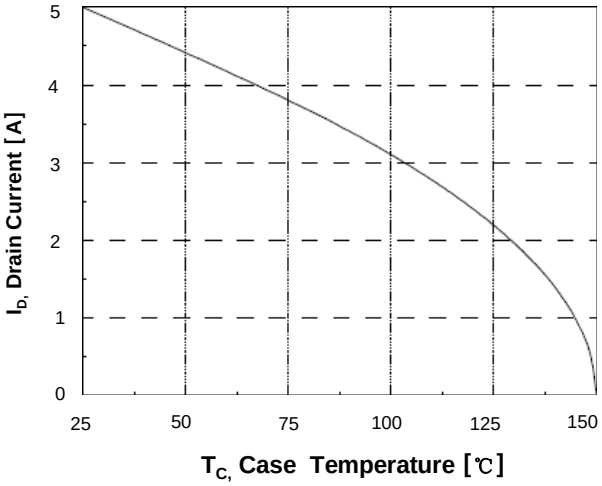


Figure 10. Maximum Drain Current vs. Case Temperature

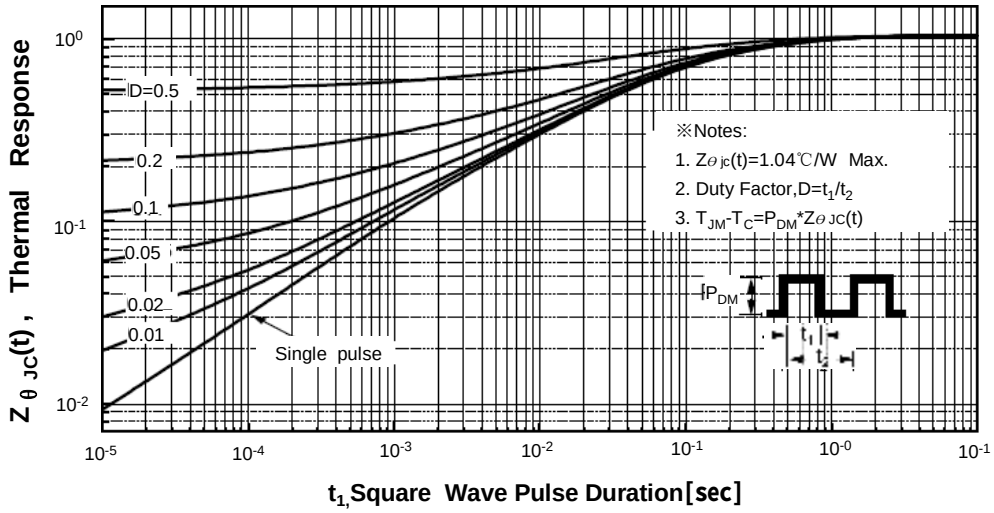


Figure 11. Transient Thermal Response Curve

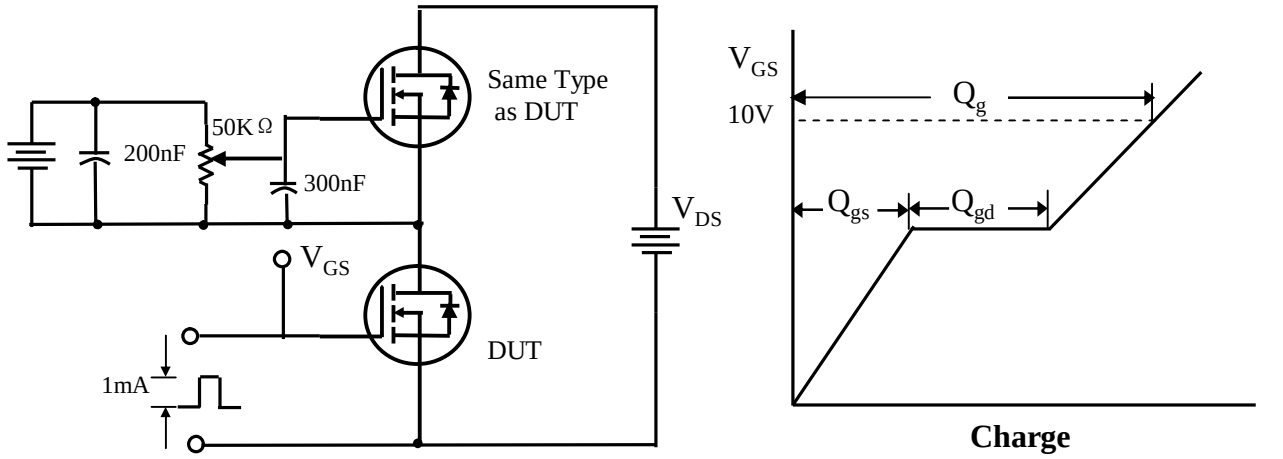


Fig 12. Gate Charge test Circuit & Waveforms

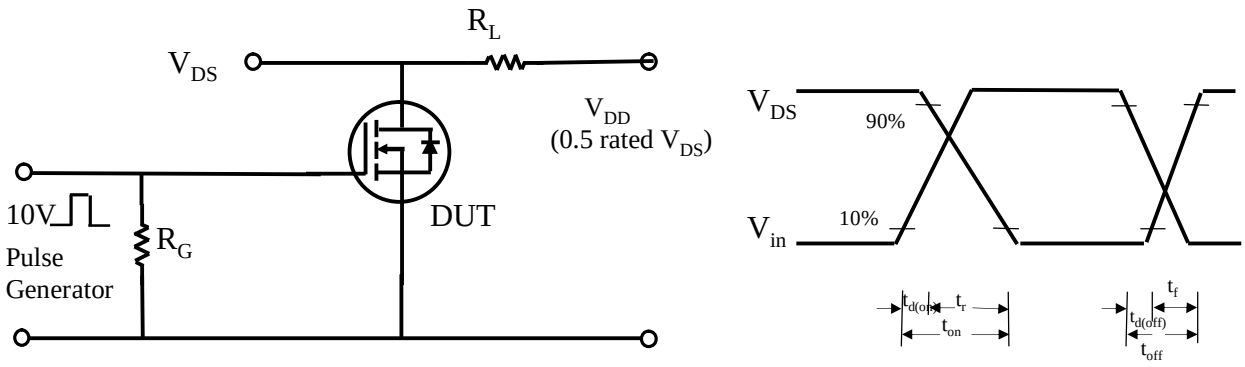


Fig 13. Switching test Circuit & Waveforms

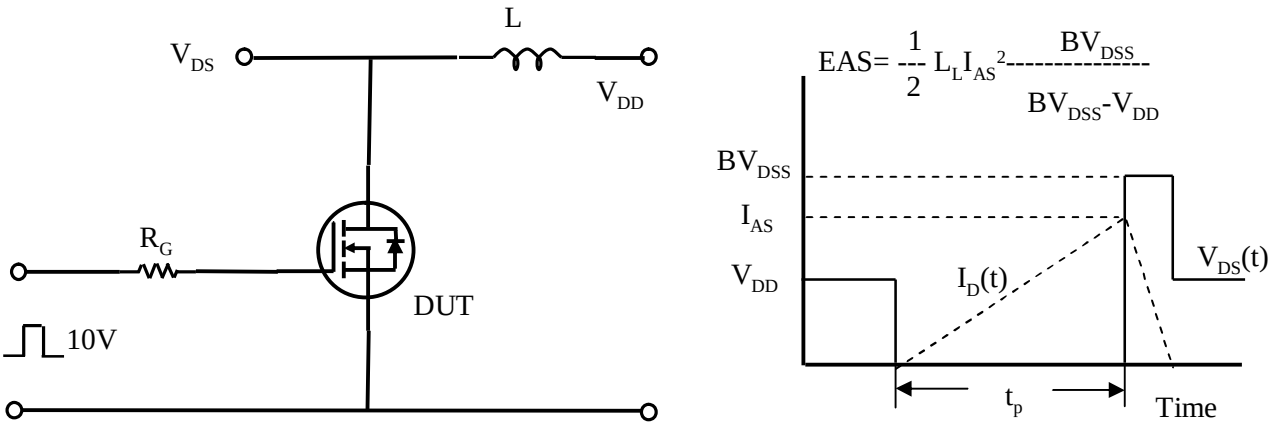


Fig 14. Unclamped Inductive Switching test Circuit & Waveforms

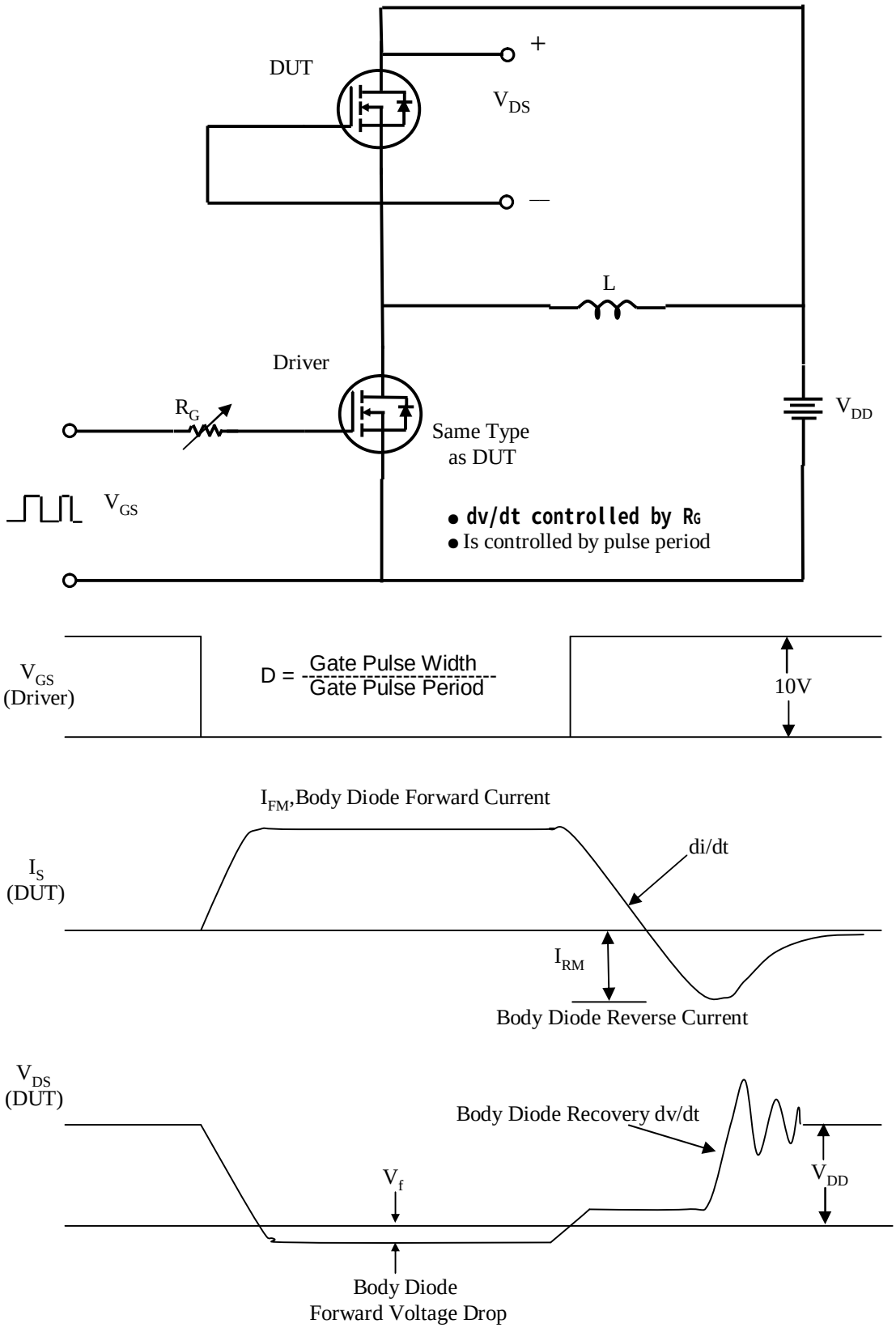


Fig 15. Peak Diode Recovery dv/dt test Circuit & Waveforms