

# GFP8N60

## General Description(概述)

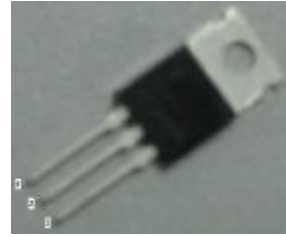
These N-Channel enhancement mode power field effect Transistors are produced using planar stripe, DMOS technology.

GFP8N60是增强型N沟道功率场效应管，采用平面条形DMOS工艺生产制造。

This advanced technology has been especially tailored to minimize on - state resistance , provide superior switching performance, and Withstand high energy pulse in the avalanche and commutaion mode .These devices are well suited for high efficiency switch mode power supply, electronic lamp ballasts based on half bridge topology.

GFP8N60具有低导通电阻、优越的开关特性以及抗雪崩击穿能力，适合用于高效开关电源、电子镇流器等。

TO-220



1.Gate 2.Drain 3.Source

## Absolute Maximum ratings (极限参数，除非另有规定，T=25 °C)

Characteristics (参数)	Symbol (符号)	Value(额定值)	Units(单位)
漏源反向击穿电压	$V_{DSS}$	600	V
连续漏极电流	$I_D$	7.5	A
栅源电压	$V_{GS}$	$\pm 30$	V
雪崩能量	$E_{AS}$	230	mJ
耗散功率	$P_D$	147	W
储存温度	$T_{STG}$	-55 ~150	°C
热阻(结到壳)	$R_{\theta JC}$	0.85	°C/W
正向压降	$V_{SD}$	1.4	V

Characteristics 参数名称	Symbol (符号)	Min. (最小值)	Typ. (典型值)	Max. (最大值)	Units (单位)	Test Conditions (测试条件)
开启电压	$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
栅源漏电流	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 30V, V_{DS} = 0V$
漏源漏电流	$I_{DSS}$	-	-	10	$\mu A$	$V_{DS} = 600V, V_{GS} = 0V$
导通电阻	$R_{DS(on)}$	-	1.0	1.2	$\Omega$	$V_{GS} = 10V, I_D = 3.75A$
跨导	$g_{fs}$	-	8.7	-	S	$V_{DS} = 40V, I_D = 3.75A$
输入电容	$C_{iss}$	-	965	1255	pF	$V_{GS} = 0V, V_{DS} = 25V$ $F = 1.0MHz$
输出电容	$C_{oss}$	-	105	135		
传输电容	$C_{rss}$	-	12	16		
导通延迟时间	$t_{d(on)}$	-	16.5	45	ns	$V_{DD} = 300V, I_D = 7.5A$ $R_G = 25 \Omega$
上升时间	$t_r$	-	60.5	130		
下降延迟时间	$t_{d(off)}$	-	81	170		
下降时间	$t_f$	-	64.5	140		
栅极存储电荷	$Q_g$	-	28	36	nC	$V_{DS} = 480V, V_{GS} = 10V$ $I_D = 7.5A$
栅源电荷	$Q_{gs}$	-	4.5	-		
栅漏电荷	$Q_{gd}$	-	12	-		

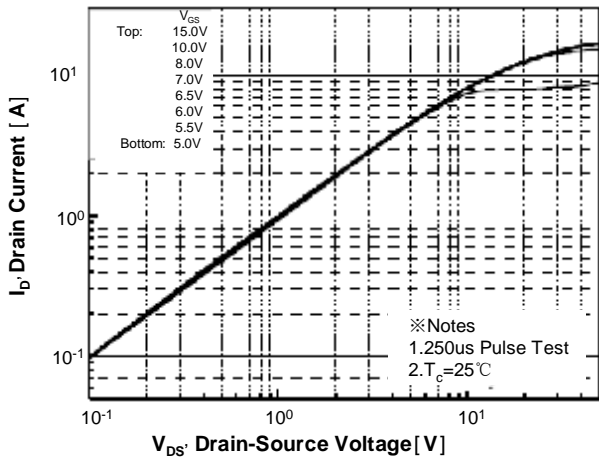


Figure 1. On-Region Characteristics

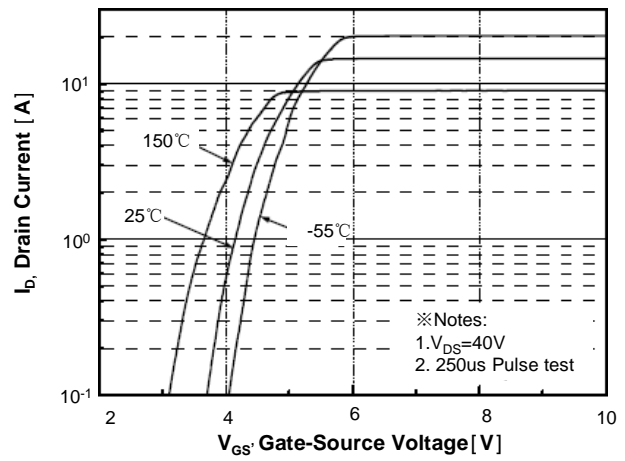


Figure 2. Transfet Characteristics

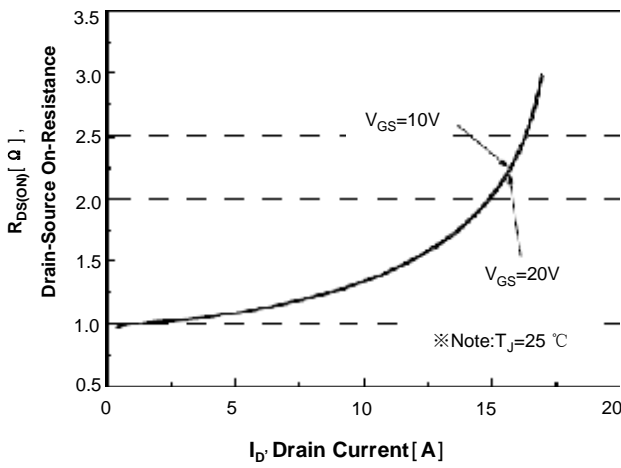


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

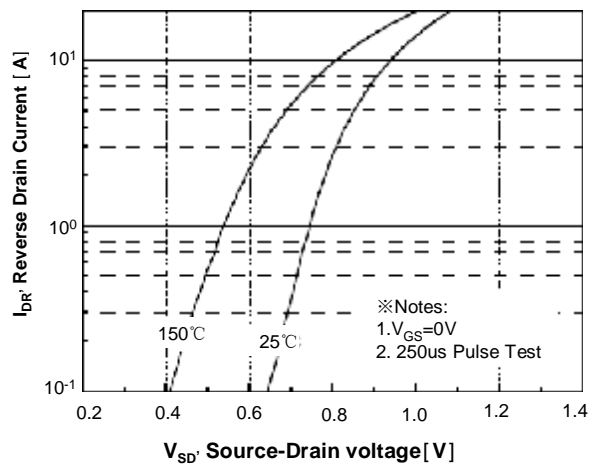


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

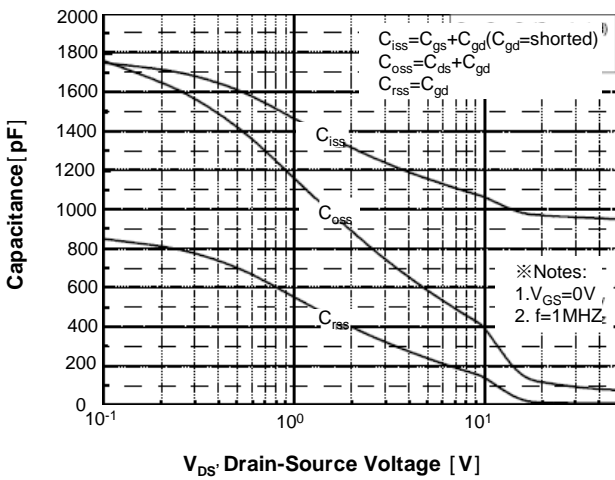


Figure 5. Capacitance Characteristics

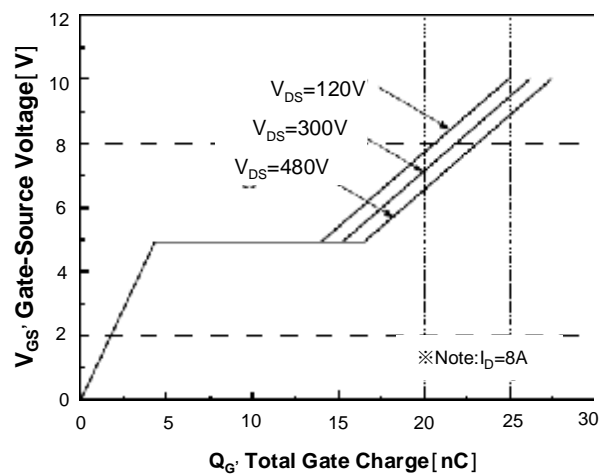


Figure 6. Gate Charge Characteristics

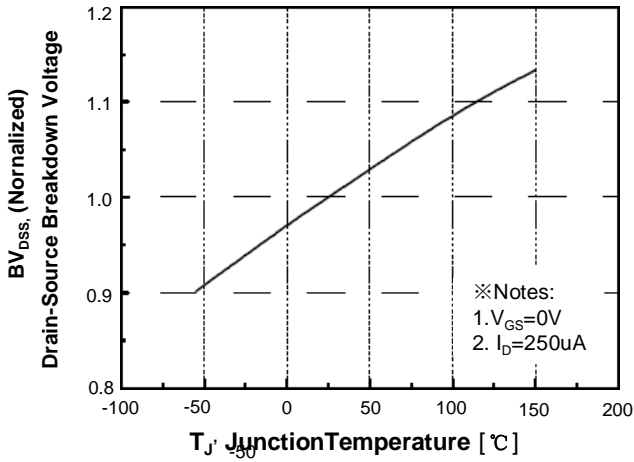


Figure 7. Breakdown Voltage Variation vs Temperature

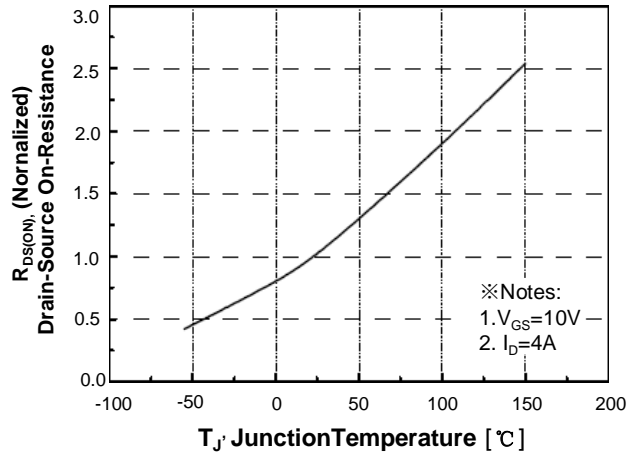


Figure 8. On-Resistance Variation vs Temperature

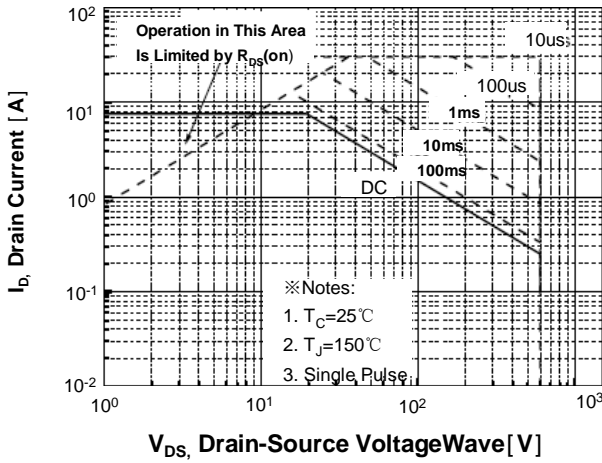


Figure 9. Maximum Safe Operating Area

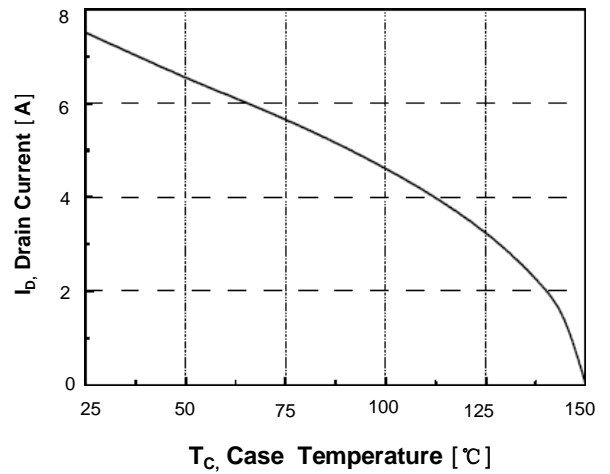


Figure 10. Maximum Drain Current vs. Case Temperature

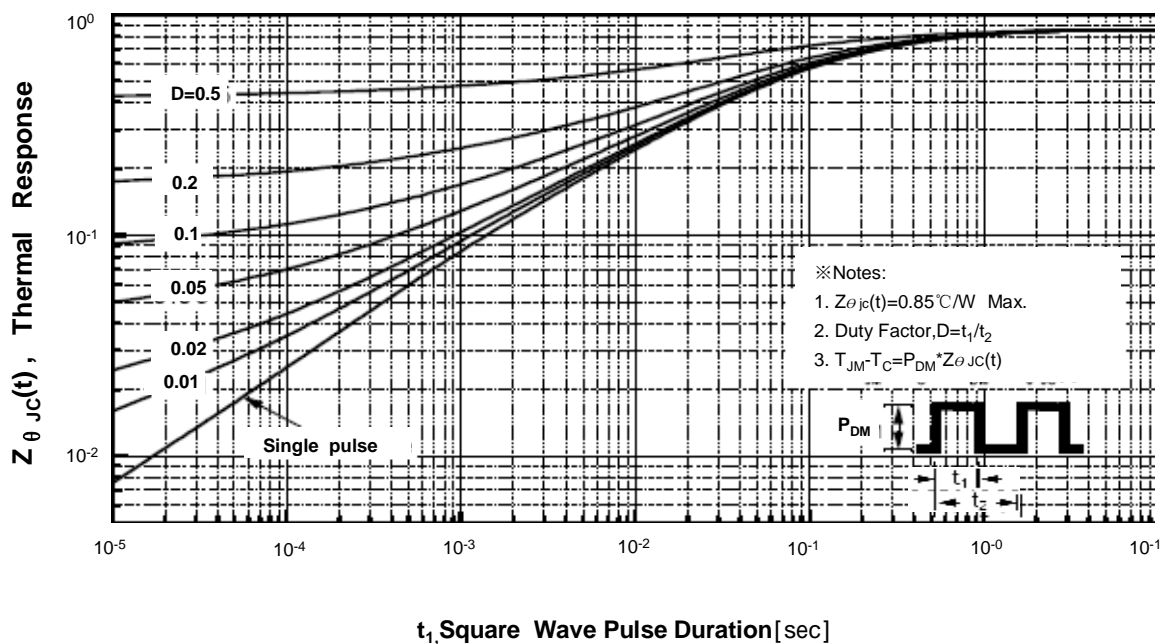
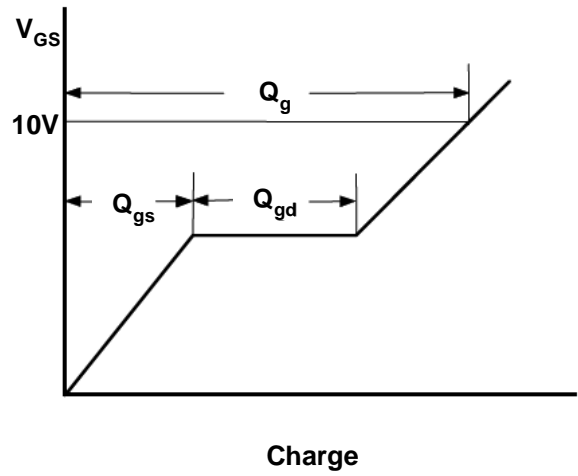
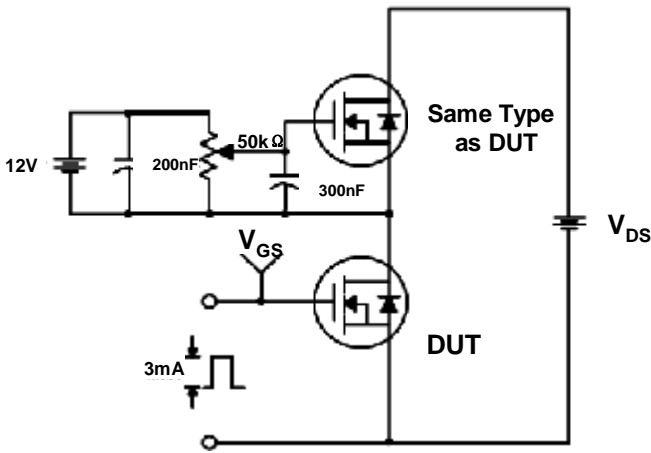
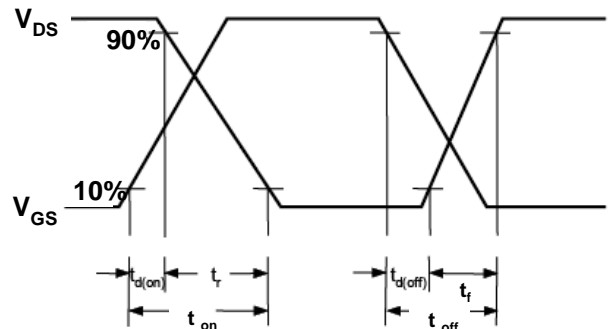
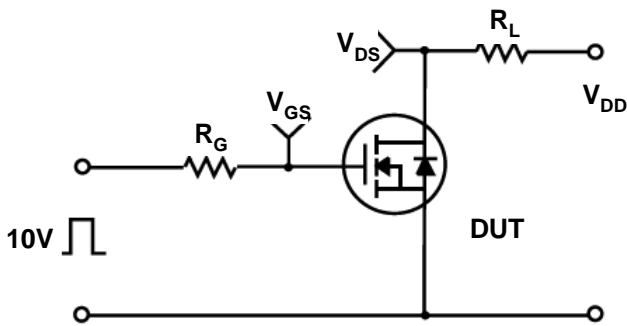


Figure 11. Transient Thermal Response Curve

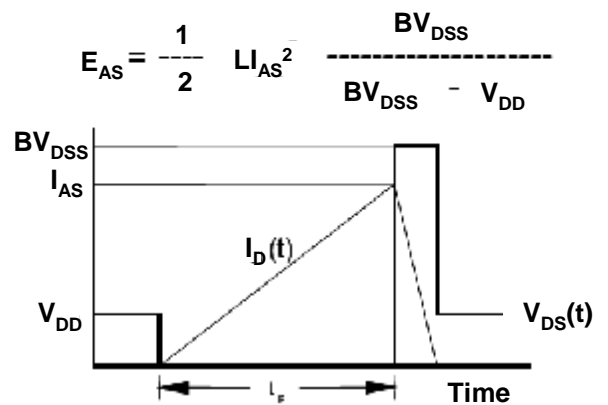
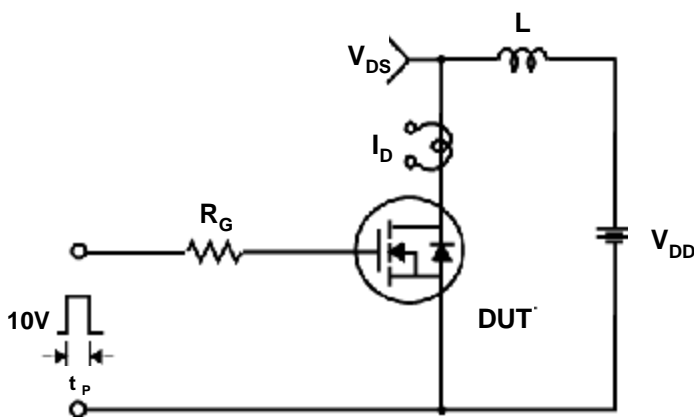
## Gate Charge Test Circuit & Waveform



## Resistive Switching Test Circuit & Waveforms



## Unclamped Inductive Switching Test Circuit & Waveforms



# Peak Diode Recovery dv/dt Test Circuit & Waveforms

