

GJ60L02**N-CHANNEL ENHANCEMENT MODE POWER MOSFET**

BV _{DSS}	25V
R _{DS(ON)}	13mΩ
I _D	50A

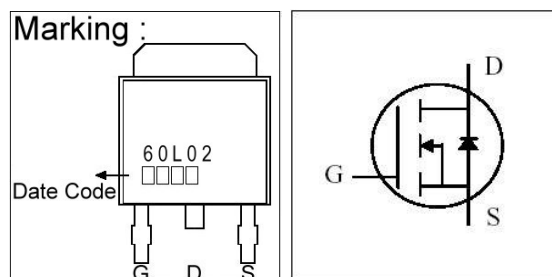
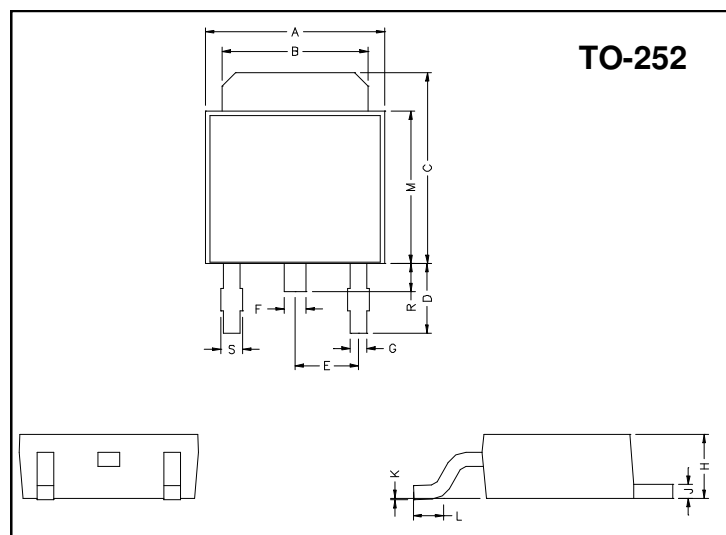
Description

The GJ60L02 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-252 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

Features

- *Simple Drive Requirement
- *Low Gate Charge
- *Fast Switching

Package Dimensions

REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.40	6.80	G	0.50	0.70
B	5.20	5.50	H	2.20	2.40
C	6.80	7.20	J	0.45	0.55
D	2.40	3.00	K	0	0.15
E	2.30 REF.		L	0.90	1.50
F	0.70	0.90	M	5.40	5.80
S	0.60	0.90	R	0.80	1.20

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V _{DS}	25	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current, V _{GS} @10V	I _D @T _C =25°C	50	A
Continuous Drain Current, V _{GS} @10V	I _D @T _C =100°C	32	A
Pulsed Drain Current ¹	I _{DM}	180	A
Total Power Dissipation	P _D @T _C =25°C	62.5	W
Linear Derating Factor		0.5	W/°C
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55 ~ +150	°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-case Max.	R _{thj-c}	2.0	°C/W
Thermal Resistance Junction-ambient Max.	R _{thj-a}	110	°C/W

Electrical Characteristics (T_j = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	25	-	-	V	V _{GS} =0, I _D =250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	0.037	-	V/°C	Reference to 25°C, I _D =1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	30	-	S	V _{DS} =10V, I _D =25A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =25V, V _{GS} =0
Drain-Source Leakage Current(T _j =150°C)		-	-	25	uA	V _{DS} =20V, V _{GS} =0
Static Drain-Source On-Resistance	R _{DS(ON)}	-	-	13	mΩ	V _{GS} =10V, I _D =25A
		-	-	26		V _{GS} =4.5V, I _D =20A
Total Gate Charge ²	Q _g	-	21	-	nC	I _D =25A V _{DS} =20V V _{GS} =5V
Gate-Source Charge	Q _{gs}	-	2.8	-		
Gate-Drain ("Miller") Change	Q _{gd}	-	16	-		
Turn-on Delay Time ²	T _{d(on)}	-	8	-	ns	V _{DS} =15V I _D =20A V _{GS} =10V R _G =3.3Ω R _D =0.75Ω
Rise Time	T _r	-	75	-		
Turn-off Delay Time	T _{d(off)}	-	22	-		
Fall Time	T _f	-	20	-		
Input Capacitance	C _{iss}	-	605	-	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
Output Capacitance	C _{oss}	-	415	-		
Reverse Transfer Capacitance	C _{rss}	-	195	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.26	V	I _S =50A, V _{GS} =0V, T _j =25°C
Continuous Source Current (Body Diode)	I _S	-	-	50	A	V _D =V _G =0V, V _S =1.26V
Pulsed Source Current (Body Diode) ¹	I _{SM}	-	-	180	A	

Drain-Source Avalanche Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Single Pulse Avalanche Energy ²	E _{AS}	-	-	61	mJ	V _{DD} =25V, I _D =35A, L=100uH
Avalanche Current	I _{AR}	-	-	35	A	V _{GS} =10V,

Notes: 1. Pulse width limited by safe operating area.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

Characteristics Curve

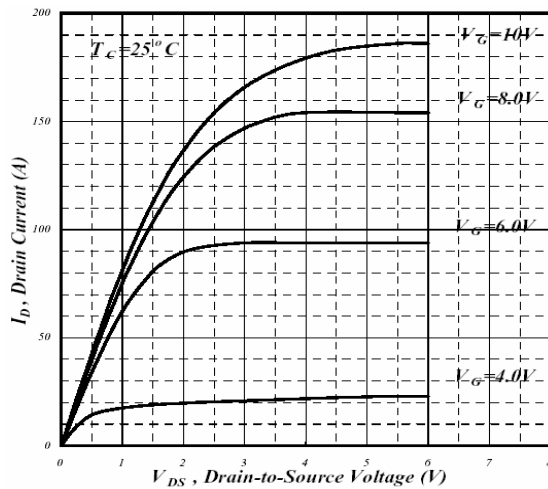


Fig 1. Typical Output Characteristics

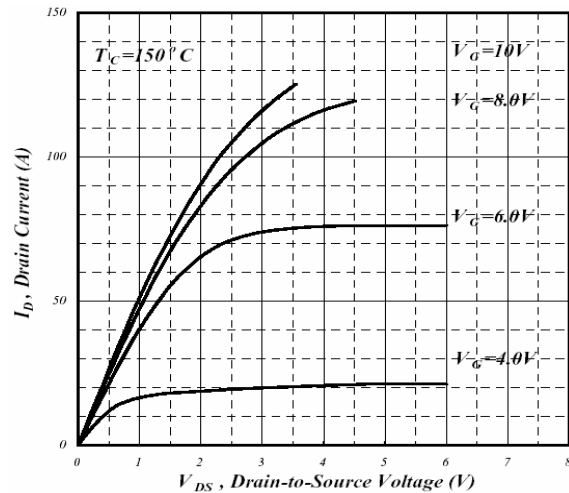


Fig 2. Typical Output Characteristics

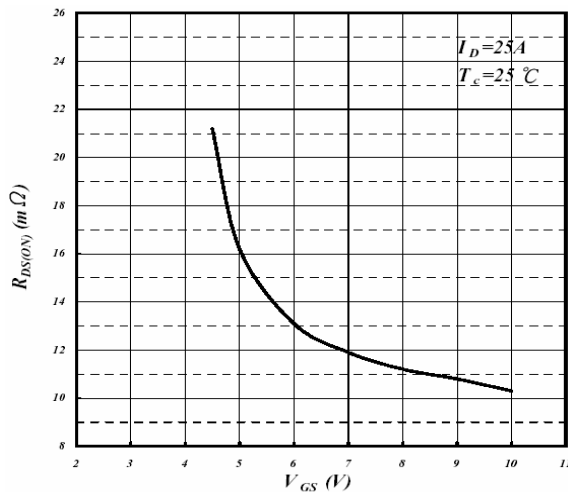


Fig 3. On-Resistance v.s. Gate Voltage

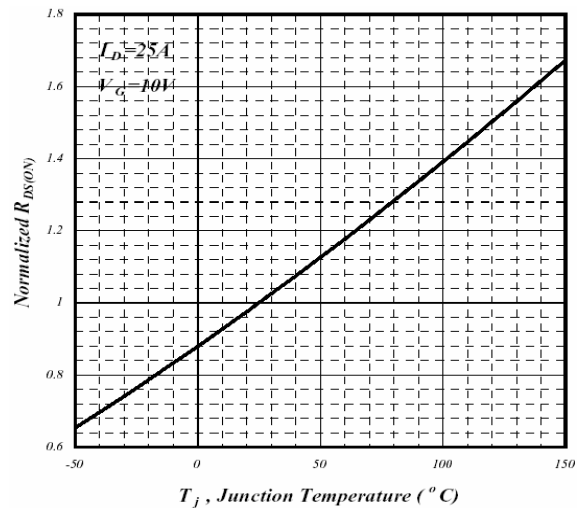


Fig 4. Normalized On-Resistance v.s. Junction Temperature

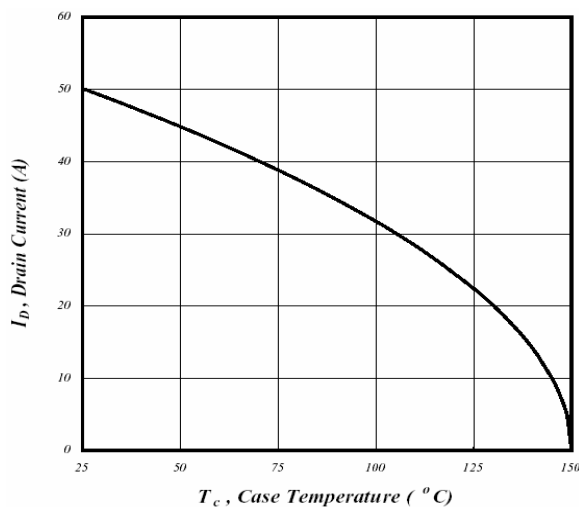


Fig 5. Maximum Drain Current v.s. Case Temperature

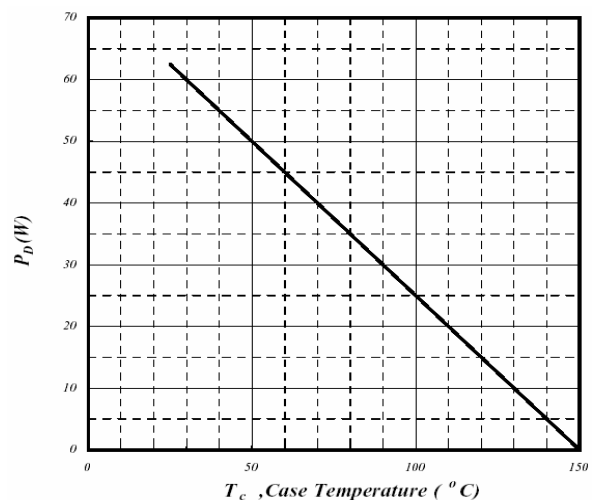


Fig 6. Type Power Dissipation

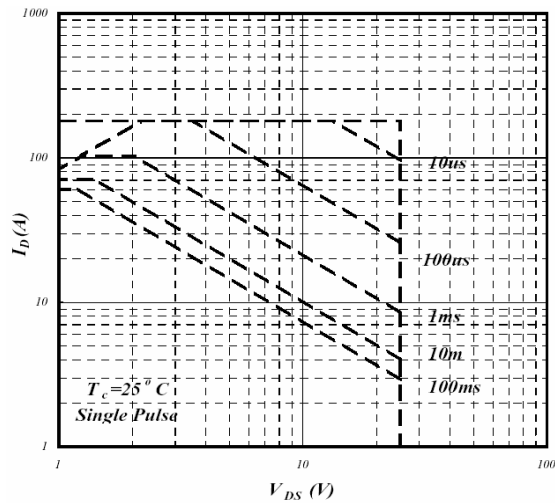


Fig 7. Maximum Safe Operating Area

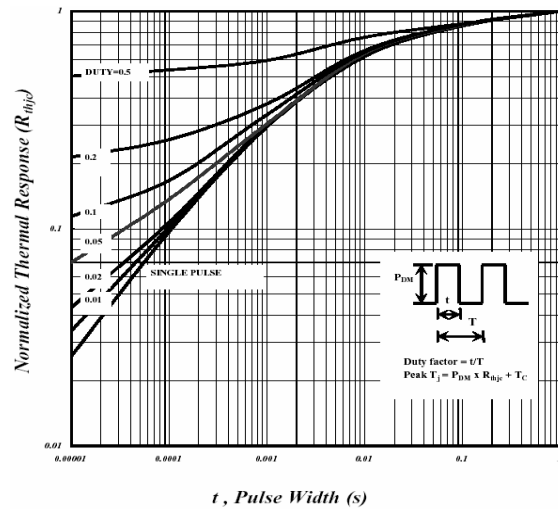


Fig 8. Effective Transient Thermal Impedance

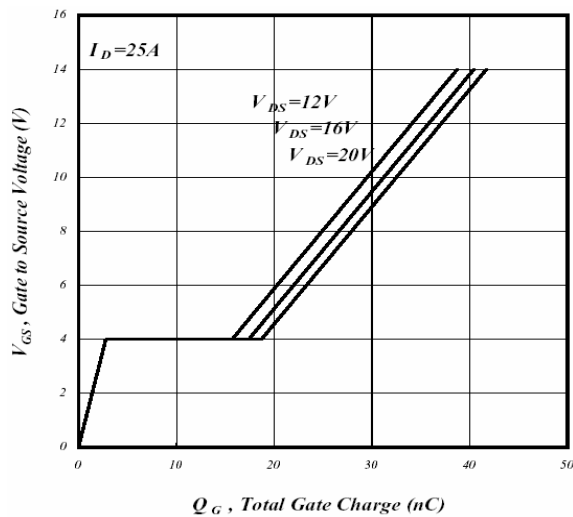


Fig 9. Gate Charge Characteristics

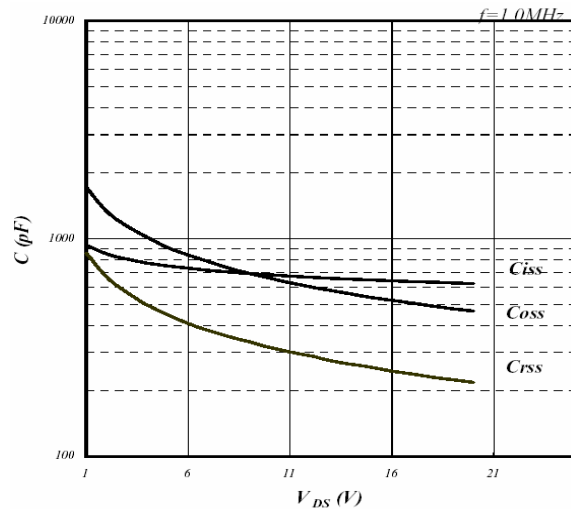


Fig 10. Typical Capacitance Characteristics

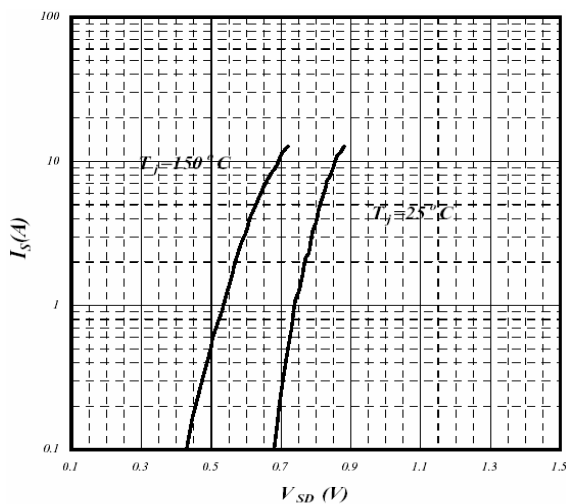


Fig 11. Forward Characteristics of Reverse Diode

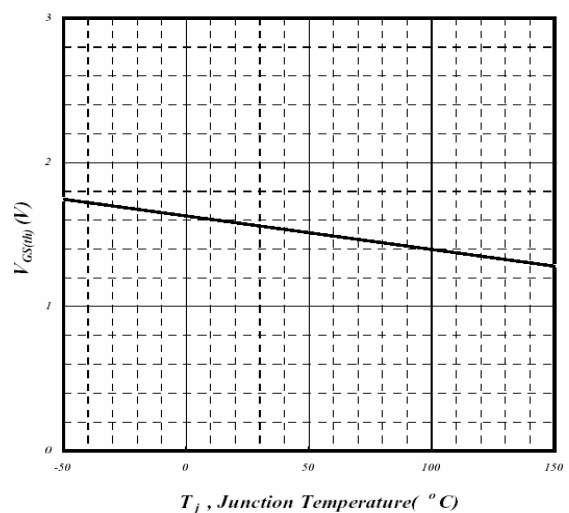


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

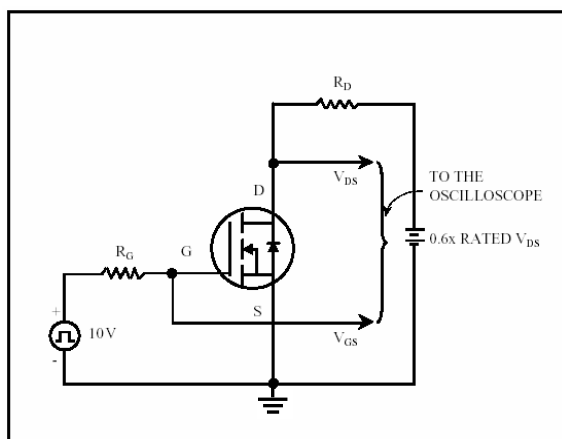


Fig 13. Switching Time Circuit

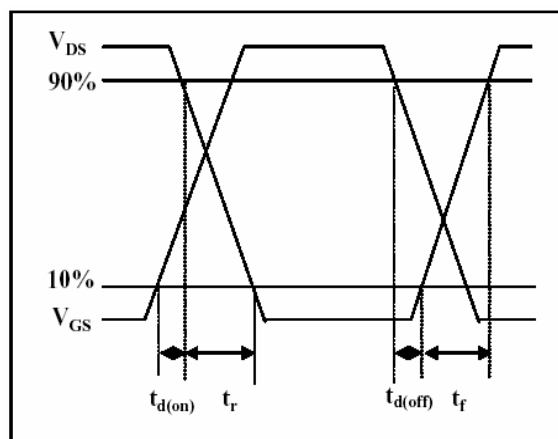


Fig 14. Switching Time Waveform

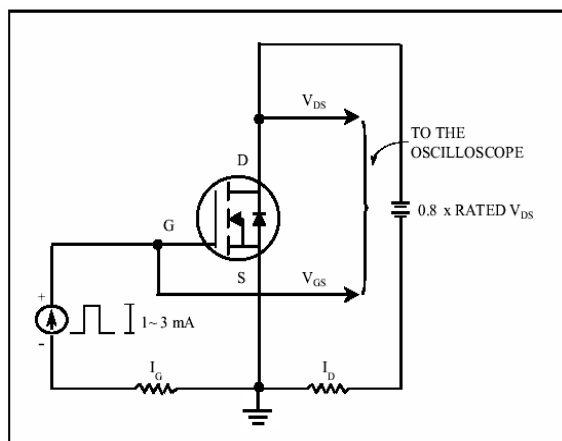


Fig 15. Gate Charge Circuit

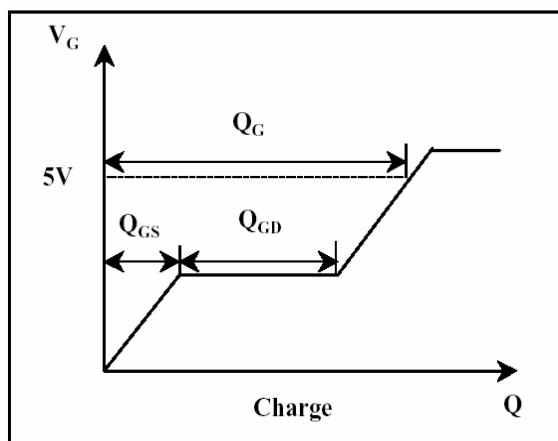


Fig 16. Gate Charge Waveform

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